RCA Integrated Circuits

This DATABOOK contains complete technical information on the full line of RCA monolithic integrated circuits: linear types, MOS field-effect (MOS/FET) types, COS/MOS digital types, memory types, microprocessor types, and high-reliability types.

General operating considerations for RCA integrated circuits and a listing of symbols and special terms used in the data are given in the following pages. The book is then divided into six major sections, one for each of the various types of devices. General information such as dimensional outlines and ordering information is included in an Appendix at the back of the book. The Appendix also includes abstracts of relevant RCA Application Notes. The final pages contain a complete index to individual type numbers.

To facilitate type selection, comprehensive product selection charts are included at the beginning of each major section. In many cases, industry cross-reference or replacement guides are also included. Data pages for individual devices are then included as nearly as possible in alpha-numerical sequence of type numbers. Because some devices are grouped together to show similarity of function and/or data, individual type numbers may be out of sequence. If you don't find the type number you're looking for where you expect it to be, check the index to devices.

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Operating Considerations

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

MOUNTING

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the

inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alchols are isopropanol, methanol, and special denatured alcohols, such as SDA1; SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trade Mark: Emerson and Cumming, Inc.

COS/MOS INTEGRATED CIRCUITS

Handing

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to V_{SS} or V_{DD}. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to V_{SS} or V_{DD} can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size,

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Terms and Symbols

A	closed-loop voltage gain
A_{AF}	audio amplifier gain
A_{DIFF}	differential voltage gain
ACC	automatic chroma control
AFC	automatic frequency control
AFT	automatic fine tuning
AGC	automatic gain control
AMR	am rejection
A_{OL}	open-loop voltage gain
A_V	amplifier voltage gain
b_{fs}	small-signal, common-source, forward transfer susceptance (imaginary part of corresponding admittance; see y_{fs})
b_{is}	small-signal, common-source, input susceptance (imaginary part of corresponding admittance; see y_{is})
b_{os}	small-signal, common-source, output susceptance (imaginary part of corresponding admittance, see y_{os})
b_{rs}	small-signal, common-source, reverse transfer susceptance (imaginary part of corresponding admittance, see y_{rs})
BW	bandwidth (unity gain)
BW_{OL}	open-loop bandwidth
C_{AD}	address capacitance
C_{BI}	base-to-substrate capacitance
C_{CB}	collector-to-base capacitance
C_{CE}	chip-enable capacitance
C_{CS}	chip-select capacitance
C_{DI}	data input capacitance
C_{DO}	data output capacitance
C_{EB}	emitter-to-base capacitance
C_{EXT}	external capacitance
C_{FB}	feedback capacitance
C_I	input capacitance
C_{ios}	small-signal output capacitance
C_{is}	small-signal input capacitance
C_{iss}	small-signal, common-source short-circuit input capacitance
C_{I-O}	input-to-output capacitance; data in/out capacitance
CMMR	common-mode rejection ratio
C_O	output capacitance
C_{os}	feedthrough capacitance
C_{oss}	small-signal, common-source short-circuit output capacitance
C_{QP}	charge-pump capacitance
C_{rss}	small-signal, common-source short-circuit, reverse transfer capacitance
C_{WE}	read/write input capacitance
e_i	input sensitivity
E_N	I/F noise voltage
e_N	low-frequency noise voltage; equivalent short-circuit input noise voltage ($\mu V\sqrt{Hz}$)
$e_{N(total)}$	wideband noise voltage referenced to input
e_{O1}/e_{O2}	channel separation
E_{ON}	broadband output noise voltage
f_{CL}	clock input frequency
f_{max}	maximum operating frequency
f_p	charge-pump input-pulse frequency
f_t	unity-gain crossover frequency; gain-bandwidth product
f_ϕ	input-pulse frequency
G_p	power gain
G_m	forward transconductance (large-signal)
h_{FE}	static forward-current transfer ratio (beta)
h_{fe}	small-signal forward-current transfer ratio
I^+	dc supply current
I^-	dc supply current
I_A	amplifier supply current
I_{ABC}	amplifier bias current
I_{AGC}	AGC source current
I_B	base current
I_C	collector current
I_{CBO}	collector cutoff current
I_{CEO}	collector cutoff current
$I_{CE(OFF)}$	output leakage current
I_{CSH}	chip-select input current - high level
I_{CSL}	chip-select input current - low level
I_D	drain current
$I_{D(ON)}$	dc on-state drain current
I_{DARK}	dark current
I_{DF}	diode forward current
$I_D{}^N$	output drive current, n-channel (sink); the output drive current flowing into the output terminal at a specified output voltage level.
$I_D{}^P$	output drive current, p-channel (source); the output drive current flowing out of the output terminal at a specified output voltage level.
I_{DDO}	supply current for drain supply voltage (V_{DD})
I_{DS}	zero-gate (bias) drain current (dual-gate types)
I_{DSS}	zero-gate (bias) drain current (single-gate types)
I_F	forward current
I_G	channel (input) gate lead current
I_{GR}	channel (input) gate reverse current
I_{GS}	gate terminal current (single-gate types)
I_{G1S}	gate-No.1 terminal current dual-gate types
I_{G2S}	gate-No. 2 terminal current dual-gate types
I_{GSSF}	gate-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G1SSF}	gate-No.1 source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSF}	gate-No. 2-to-source forward leakage current, all other terminals shorted to source (dual-gate types).
I_{GSSR}	gate-to-source reverse leakage current, all other terminals shorted to source (single-gate types).
I_{G1SSR}	gate-No. 1-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{G2SSR}	gate-No.2-to-source reverse leakage current, all other terminals shorted to source (dual-gate types).
I_{GT}	gate trigger current; gate terminal current
I_I	input current
I_{IB}	input bias current
I_{IBC}	internal bias current
I_{IH}	input leakage current, high level; the current flowing into an input when the input is set at the high logic state.
I_{IL}	input leakage current, low level; the current flowing into an input when the input is set at the low logic state.
I_{IO}	input offset current
αI_{IO}	average temperature coefficient of input offset current
$\Delta I_{IO}/\Delta T$	temperature coefficient of input offset current (drift)
I_{LIM}	short-circuit limiting current
I_{MTR}	current-mirror transfer ratio
I_N	I/F noise current
i_N	equivalent open-circuit noise current ($pA/\sqrt{Hz}$)
I_O	output current
$I_{O(DIFF)}$	differential output current (sink)
I_{OO}	output offset current
I_{OL}	output leakage current, low level; the current flowing out of a three-state device when the device is the off state and the output is forced to a low level.
I_{OM}	peak output current
$\lvert I_{OM}\rvert$	magnitude of peak output current
$I_{OM}{}^+$	maximum output current (source)
$I_{OM}{}^-$	maximum output current (sink)
I_p	photo current
$I_{p\text{-}p}$	peak-to-peak output current
I_Q	total quiescent current
I_{QPL}	charge-pump input current
I_R	dc reverse (leakage) current
I_{REFO}	supply current for reference supply voltage
I_S	strobe load current
I_{SR}	strobe reverse current
I_{SSO}	supply current for source voltage (V_{SS})
I_{SXO}	supply current for supply voltage
I_{TH}	threshold current
I_{TOTAL}	total supply current
k_N	normalized factor ($k_N = k/k_r$)
MAG	maximum available power gain
MUG	maximum useable power gain (unneutralized)
NF	noise factor
P_O	power output
P_D	device dissipation
P_{SRR}	power supply rejection ratio
$r_{ds(off)}$	small-signal drain-to-source off-state resistance
$r_{ds(on)}$	static drain-to-source on-state resistance
R_{GS}	gate leakage-current resistance
R_O	output resistance
R_o	low-frequency output resis+
r_o	small-signal output resis+
r_{oss}	small-signal, short-cir common-source o resistance

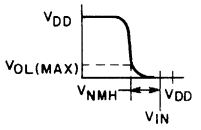
Terms and Symbols (cont'd)

R_OOFF	data output off resistance
R_I	differential input resistance
r_i	small-signal input resistance
r_{iss}	small-signal, short-circuit, common-source input resistance
R_i	low-frequency input resistance
R_{ON}	ON resistance; the ON-state resistance of an analog switch at specified input and load conditions.
$\triangle R_{ON}$	△ON resistance; the difference in ON-state resistance between any 2 analog switches at specified input and load conditions.
S/N	signal-to-noise ratio
SR	slew rate
T_A	ambient temperature
t_{AA}, t_{ADA}	access time from address
t_{AC}	access time from chip select
t_{AH}, t_{ADH}	address hold time
t_{AM}	output active from MRD
t_{AS}, t_{ADS}	address setup time
t_{CE}	chip-enable active time
$t_{\overline{CE}}$	chip-enable non-active time
t_{CEA}	address time from chip enable
$t_{\overline{CS}}$	chip-select setup time
$t_{\overline{CSV}}$	chip-select valid time
t_d	delay time
t_{DOA}	data-out active time
t_{DOH}	data-out hold time
t_{DH}, t_{D1H}	data-in hold time, data hold time
t_{DS}, t_{D1S}	data-in setup time, data setup time
t_{D1W}	data width effective time
t_{DR}	differential recovery time
t_f	fall time
$t_{f\phi}$	input-pulse rise time
t_{fCE}	chip select input fall time
t_{fCL}	clock fall time
t_H	data hold time; data-to-clock hold time; clock-to-write enable hold time
THD	total harmonic distortion
t_{off}	turn-off time
t_{on}	turn-on time
t_{PDH}	previous data hold time
t_{PHL}	propagation delay time (high-to-low-level)
t_{PLH}	propagation delay time (low-to-high-level)
t_{PHZ}	3-state propagation delay (output high-to-high impedance)
t_{PZH}	3-state propagation delay (high impedance-to-ouput high)
t_{PLZ}	3-state propagation delay (output low-to-high impedance)
t_{PZL}	3-state propagation delay (high impedance-to-output low)
t_r	rise time
t_{RA}	read access time
t_{RC}	read cycle time
t_{RCE}	chip-slect input rise time
t_{RCL}	clock rise time
$t_{R\phi}$	input-pulse rise time
t_{RDH}	read hold time
t_{RDW}	read width effective time
t_{RFC}	refresh cycle time
t_{RFR}	refresh period time
t_{rr}	reverse recovery time
t_{RWC}	read/modify/write cycle time
t_S	setup time
t_{STG}	storage time
t_{THL}	transition time (high-to-low level)
t_{TLH}	transition time (low-to-high level)
t_W	pulse width
t_{WC}	write cycle time
t_{WRH}	write hold time
t_{WRW}	write width time
t_{WRS}	write setup time
t_{WW}	write pulse width
V^+	DC positive supply voltage
V^-	DC negative supply voltage
V_{ABC}	amplifier bias voltage
V_{BB}	substrate voltage
V_{BE}	base-to-emitter voltage
$V_{BE(sat)}$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage
$V_{(BR)CES}$	collector-to-emitter breakdown voltage
$V_{(BR)DI}$	dc breakdown voltage between diode and substrate
$V_{(BR)R}$	dc reverse breakdown voltage
$V_{(BR)EBO}$	emitter-to-base breakdown voltage
$V_{(BR)GSSF}$	dc gate-to-source forward breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G1SSF}$	dc gate-No.1-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)G2SSF}$	dc gate No.2-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)GSSR}$	dc gate-to-source reverse breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G2SSR}$	dc gate-No.2-to-source reverse breakdown voltage, all other terminals shorted to source (dual-gate types)
V_{CBO}	collector-to-base voltage
V_{CC}	drain supply voltage used as a second positive supply voltage. It is $\leqslant V_{DD}$ and referenced to V_{SS}
V_{CEL}	chip-enable input voltage, low level
V_{CEH}	chip-enable input voltage, high level
VCO	voltage controlled oscillator
V_{CEO}	collector-to-emitter voltage
$V_{CEO(sus)}$	collector-to-emitter sustaining voltage
V_{CIO}	collector-to-substrate voltage
V_{CP}	charge pump voltage
V_{CSL}	chip-select voltage, low level
V_{CSH}	chip-select voltage, high level
V_{DD}	drain supply voltage (the most positive supply voltage; always referenced to ground)
V_{DG}	drain-to-gate voltage (single-gate types)
V_{DG1}	drain-to-gate-No.1 voltage (dual-gate types)
V_{DG2}	drain-to-gate-No.2 voltage (single-gate types)
V_{DIO}	diode-to-substrate voltage
V_{DR}	diode reverse voltage
V_{DS}	drain-to-source voltage
V_{EE}	source voltage (the most negative supply voltage in a 3-supply voltage system)
V_F	dc forward voltage
$\triangle V_F/\triangle T$	temperature coefficient of forward voltage drop
V_{GH}	channel gate input voltage, high level
V_{GL}	channel gate input voltage, low level
V_{GS}	gate-to-source voltage
$V_{GS(TH)}$	gate-to-source threshold voltage
$V_{GS(Off)}$	gate-to-source cutoff voltage (single-gate types)
V_{G1S}	gate-No.1-to-source voltage (dual-gate type)
$V_{G1S(Off)}$	gate-No.1-to-source cutoff voltage (dual-gate types)
V_{G2S}	gate-No.2-to-source voltage (dual-gate types)
$V_{G2S(off)}$	gate-No.2-to-source cutoff voltage (dual-gate types)
V_I	input voltage
$V_{I(Lim)}$	input limiting voltage
V_{ICR}	common-mode input voltage range
V_{IL}	input-voltage, low level
V_{IH}	input-voltage, high level
V_{IO}	input offset voltage
$\lvert V_{IO}\rvert$	magnitude of input offset voltage
$\triangle V_{IO}/\triangle T$	temperature coefficient of magnitude of input offset voltage
$\triangle V_{IO}/\triangle T$	temperature coefficient of input offset voltage drift
$\triangle V_{IO}/\triangle V^+$	positive input-offset-voltage sensitivity
$\triangle V_{IO}/\triangle V^-$	negative input-offset-voltage sensitivity
αV_{IO}	average temperature coefficient of input-offset voltage
$V_{i(Lim)}$	input limiting voltage (knee)
V_{knee}	protective diode knee voltage (protected gate types)
V_N	output noise voltage
V_{NL}	noise voltage, inputs low; the low-level dc input noise voltage. It is specified for the full range of voltage above V_{SS} for which the output logic does not change state.
V_{NH}	noise voltage, inputs high; the high level dc input noise voltage. It is specified for the full range of voltage below V_{DD} for which the output logic level does not change state.

Terms and Symbols (cont'd)

V_{NM} noise margin; the noise voltage that may be added between any output and input in a COS/MOS logic system.

V_{NML} noise margin, inputs low; the noise voltage that may be added between any output and input in the low-logic state so that the resulting voltage ($V_{OH\ min}$) will be within the noise margin specifications.



V_{DD}	V_{NMH}	$V_{OL(MAX)}$
5	1	0.5
10	1	1
15	1	1.5

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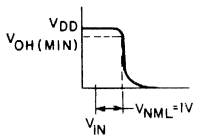
V_{NMH} noise margin, inputs high; the noise voltage that may be added between any input and output in the high logic state so that the resulting output voltage ($V_{OL\ max}$) will be within the noise margin specifications shown below



V_{DD}	V_{NML}	$V_{OH(MIN)}$
5	1	4.5
10	1	9
15	1	13.5

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V_O output voltage

$\Delta V_O/\Delta V^-$ dc supply voltage sensitivity

$\Delta V_O/\Delta V^+$ dc supply voltage sensitivity

$V_{O(rms)}$ open-loop output voltage swing

ΔV_O output voltage temperature coefficient

$V_{Op\text{-}p}$ output voltage swing

$V_{O(af)}$ recovered af voltage

V_{OL} output voltage, low level; the voltage level at an output when the input logic conditions have been set to establish logic LOW output.

V_{OO} output offset voltage

V_{OH} output voltage, high level; the voltage level at an output when the input logic conditions have been set to establish a logic HIGH output.

V_{OM}^+ maximum output voltage

V_{OM}^- maximum output voltage

V_{QP} charge pump voltage

V_{QPL} charge pump input voltage, low level

V_{QPH} charge-pump input voltage, high level

V_{REF} reference voltage

V_{REG} regulated supply voltage

V_{RR} supply voltage rejection ratio

V_{TH} input threshold voltage

V_Z zener voltage

Y_{fs} magnitude of small-signal, common-source, short-circuit forward transfer admittance (transadmittance)

Y_{is} small-signal, common-source, short-circuit, input-admittance (conductance, real part of admittance; susceptance, imaginary part of admittance)

Y_{os} small-signal, common-source, short-circuit, output admittance

$|Y_{rs}|$ magnitude of small-signal, common-source, short-circuit, reverse transadmittance

$\angle Y_{rs}$ phase angle of small-signal, common-source, short-circuit, reverse transadmittance

$(-)_{rs}$ angle of reverse transadmittance, common-source circuit

Z_1 input impedance

Z_O output impedance

Z_Z zener impedance

ϕ phase angle

ϕ phase margin

η efficiency

ϕL open-loop phase lag

Linear Integrated Circuits

Operational Amplifiers

		Micropower							High-Current							General-Purpose																							
																Single Unit																							
																Low Noise																					COS/MOS Output, MOS/FET Input			Bipolar Output, MOS/FET Input		
		Single OTA●		Triple OTA ●			Single OP AMP																																		
		CA3080	CA3080A	CA3060A	CA3060B	CA3060	CA3078A	CA3078	CA3033	CA3033A	CA3047	CA3047A	CA3094	CA3094A	CA3094B	CA6741	CA6078A▲	CA101	CA101A	CA201	CA201A	CA301A	CA107	CA207	CA307	CA741C	CA741	CA748C	CA748	CA3130	CA3130A	CA3130B	CA3140	CA3140A	CA3140B			
	Page No.	200	200	166	166	166	196	196	123	123	123	123	231	231	231	316	316	20	20	20	20	20	24	24	24	50	50	50	50	280	280	280	295	295	295			
Applications	Sample and Hold												■	■	■															■	■	■	■	■	■			
	Switching	■	■	■	■	■							■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Schmitt Trigger	■	■	■	■	■			■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Multivibrator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Modulator	■	■	■	■	■	■	■					■	■	■		■																					
	Mixer	■	■	■	■	■	■	■					■	■	■		■																					
	Detector	■	■	■	■	■	■	■					■	■	■		■																					
	Comparator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	DC Amplifier	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Timer						■	■					■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Wideband Large Signal																																■	■	■			
Features	Multiple Unit			■	■	■																																
	AGC Capability	■	■	■	■	■							■	■	■																							
	Balanced Input	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Short-Circuit Protection	■	■	■	■	■	■	■								■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■			
	Internal Frequency Compensation															■							■	■	■	■	■						■	■	■			
	Offset Adjustment						■	■	■	■	■	■					■	■	■	■	■	■						■	■	■	■	■	■	■	■	■			
	Negative V_{ICR} near V^-	■	■	■	■	■	■	■					■	■	■		■													■	■	■	■	■	■			
	Low Power Supply Current (<1 mA)	■	■	■	■	■	■	■					■	■	■		■																					
	Ultra-Low I_{IB}	■	■	■	■	■	■	■					■	■	■		■													■	■	■	■	■	■			
	Very Low V_{IO} & I_{IO}																																					
	TYPE DESIGNATION SUFFIX LETTER (See Note 1)																																					
Package	Flat Pack Ceramic																																					
	Dual In-Line Ceramic (DIC)			D	D	D			■	■																												
	Hermetic Gold CHIP (DIP)																	G		G	G	G	G	G	G	G	G	G	G									
	Dual In-Line Plastic (DIP)	E*				E					■	■	E*	E*							E*			E*	E*	E*	E*	E*									
	TO-5 Style Straight Lead	■	■				T	T					T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T	T			
	TO-5 Style Dual-In-Line (DIL-CAN)	S	S				S	S					S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S			
	Frit Seal Dual-In-Line Ceramic																																					
	Beam Lead																										L											
	Chip	H				H		H	H				H								H			H	H		H											
	Gold Chip																				GH			GH	GH		GH											

Note 1: The indicated suffix letter identifies the package for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

● Operational Transconductance Amplifier ▲ Micropower Type * 8-lead DIP (MINI-DIP) package.

Operational Amplifiers

		General-Purpose								Wideband														Precision					
		Multiple Unit																											
		Dual					Quad																						
		CA747C	CA747	CA1458	CA1558	CA3401	CA124	CA224	CA324	CA3008	CA3008A	CA3010	CA3010A	CA3015	CA3015A	CA3016	CA3016A	CA3029	CA3029A	CA3030	CA3030A	CA3037	CA3037A	CA3038	CA3038A	CA3100	CA108	CA108A	CA208	CA208A	CA308	CA308A
	Page No.	50	50	50	50	307	34	34	34	89	89	89	89	89	89	89	89	89	89	89	89	89	89	89	89	257	27	27	27	27	27	27
Applications	Switching	■	■	■	■	■	■	■	■																		■	■	■	■	■	■
	Schmitt Trigger	■	■	■	■	■	■	■	■																		■	■	■	■	■	■
	Multivibrator	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Modulator																															
	Mixer																															
	Detector																															
	Comparator	■	■	■	■	■	■	■	■																	■	■	■	■	■	■	■
	DC Amplifier	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Timer																										■	■	■	■	■	■
	Wideband Large Signal																									■						
Features	Multiple Unit	■	■	■	■	■	■	■	■																							
	AGC Capability																															
	Balanced Input	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■
	Short-Circuit Protection	■	■	■	■	■	■	■	■																		■	■	■	■	■	■
	Internal Frequency Compensation	■	■	■	■	■	■	■	■																		■	■	■	■	■	■
	Offset Adjustment	■	■							■	■	■	■	■	■	■	■	■	■	■	■	■	■	■								
	Negative V_{ICR} near V^-					■	■	■	■																							
	Low Power Supply Current (<1 mA)																									■	■	■	■	■	■	■
	Ultra-Low I_{IB}																									■	■	■	■	■	■	■
	Very Low V_{IO} & I_{IO}																											■		■		■
	TYPE DESIGNATION SUFFIX LETTER (See Note 1)																															
Package	Flat Pack Ceramic									■	■					■	■															
	Dual In-Line Ceramic (DIC)																					■	■	■	■							
	Hermetic Gold CHIP (DIP)	G	G	G	G	G	G	G	G																							
	Dual In-Line Plastic (DIP)	E	E	E*	E*	E	E	E	E									■	■	■	■											
	TO-5 Style Straight Lead	T	T	T	T							■	■	■	■											T	T	T	T	T	T	T
	TO-5 Style Dual In-Line (DIL-CAN)			S	S																					S	S	S	S	S	S	S
	Frit Seal Dual In-Line Ceramic																															
	Beam Lead													L																		
	Chip	H		H		H			H					H												H						
	Gold Chip	GH		GH					GH																							

NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

* 8-lead DIP (MINI-DIP)

Arrays

		Transistor Arrays								Amplifier Arrays					
		Differentially Connected Pair Plus Three Individual					Super β Diff. Amp. Plus 3 n-p-n Trans.	1 n-p-n & 1 p-n-p/n-p-n transistors, 1 zener diode, 1 PUT* 1 SCR▲ (Thyristor)	COS/MOS Array 3 n-channel & 3 p-channel transistors	High-Freq. n-p-n	Dual Independent (Differential)				Three Ampl.	Four Ampl.
		CA3045	CA3046	CA3086	CA3146A	CA3146	CA3095	CA3097	CA3600	CA3127	CA3026	CA3049	CA3102	CA3054	CA3035	CA3048
	Page No.	145	145	213	260	260	235	244	309	276	114	151	151	114	127	148
Applications	Comparator							■	■							
	Detector	■	■	■	■	■	■			■	■	■	■	■		
	Differential Amplifier	■	■	■			■		■	■	■	■	■			
	Limiter			■					■							
	Mixer			■			■		■	■		■	■			■
	Modulator			■						■		■	■			
	Multivibrator			■			■		■	■		■	■			■
	Oscillator			■			■	■	■	■		■	■			
	Schmitt Trigger			■						■						
	Sense Amplifier			■						■		■	■			
	Switching			■				■	■	■		■	■			
	Thyristor & SCR Control			■				■	■							
	Timer							■	■							
	VHF							■		■						
	Regulator							■								
Features	High Input Resistance								■							
	Balanced Input	■	■	■	■	■	■			■		■	■			
	Balanced Output	■	■	■	■	■	■			■		■	■			
	Low Noise						■		■						■	■
	AGC Capability						■			■		■	■			
	Multiple Unit	■	■	■	■	■	■		■	■		■	■	■	■	■
	Wide Band	■	■	■	■	■	■			■		■	■		■	
Package	TYPE DESIGNATION SUFFIX LETTER (SEE NOTE 1)															
	Flat Pack Ceramic															
	Dual In-Line Ceramic	■														
	Dual In-Line Plastic		■	■	E	E	E	E	E	E			E	■		■
	TO-5 Style Straight Lead										■	■			■	
	TO-5 Style Formed Lead														VI	
	Frit Seal Dual-In-Line Ceramic	F	F	F												
	Chip	H				H	H	H			H	H	H	H	H	H
	Beam-Lead	L										L		L		

* Programmable Unijunction Transistor ▲ Silicon Controlled Rectifier

Arrays

		Diode Arrays			Transistor Arrays																			
					General-Purpose										2 Transistors 2 Zener Diodes, 1 Diode	Dual Darlington Connected			Darlington Connected Pair Plus Two Individual			
		Quad Plus Two	Individual	5-Pair	n-p-n							p-n-p	p-n-p & n-p-n											
		CA3019	CA3039	CA3141	CA3081	CA3082	CA3083	CA3183A	CA3183	CA3724	CA3725	CA3084	CA3096	CA3096A	CA3093	CA3036	CA3050	CA3051	CA3018	CA3018A	CA3118A	CA3118
	Page No.	105	129	298	203	203	205	260	260	314	314	207	240	240	228	128	155	155	102	102	260	260
Applications	Comparator						■	■	■						■							
	Detector	■	■	■			■	■	■				■	■			■	■	■	■	■	■
	Differential Amplifier						■	■	■			■	■	■	■		■	■	■	■	■	■
	Limiter	■	■	■			■	■	■			■							■	■	■	■
	Mixer	■	■	■			■	■	■			■							■	■	■	■
	Modulator	■	■	■			■	■	■			■							■	■	■	■
	Multivibrator	■	■	■			■	■	■			■							■	■	■	■
	Oscillator				■	■	■	■	■			■							■	■	■	■
	Schmitt Trigger						■	■	■	■	■											
	Sense Amplifier						■	■	■				■	■								
	Switching	■	■	■	■	■	■	■	■	■	■	■										
	Thyristor & SCR Control				■	■	■	■	■	■	■		■	■	■				■	■	■	■
	Timer																					
	VHF																					
	Regulator														■							
	Core Memory Driver (High Speed)									■	■											
	High Current Driver									■	■											
Features	High Input Resistance																					
	Balanced Input						■	■	■			■	■	■		■	■	■	■	■	■	■
	Balanced Output						■	■	■			■				■	■	■	■	■	■	■
	Low Noise												■	■		■						
	AGC Capability																		■	■	■	■
	Multiple Unit															■	■	■	■	■	■	■
	Wide Band																		■	■	■	■
Package	TYPE DESIGNATION SUFFIX LETTER (See Note 1)																					
	Flat Pack Ceramic																					
	Dual In-Line Ceramic																■					
	Hermetic Gold CHIP (DIP)									G	G											
	Dual In-Line Plastic				■	■	■	E	E			■	E	E	E			■				
	TO-5 Style Straight Lead	■	■													■			■	■	T	T
	TO-5 Style Formed Lead																					
	Frit Seal Dual-In-Line Ceramic				F	F	F															
	Chip	H	H		H	H	H		H			H	H		H				H			H
	Gold Chip									GH	GH											
	Beam-Lead		L				L					L							L			

NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

Broadband (Video) and Differential Amplifiers, and AM/FM Communications Circuits

		Broadband (Video) Amplifiers								Differential Amplifiers													AM/FM Communications Circuits									
		CA3002	CA1352	CA3020	CA3020A	CA3021	CA3022	CA3023	CA3040†	CA3000	CA3001●	CA3004	CA3005	CA3006	CA3007	CA3026	CA3028A	CA3028B	CA3049	CA3050	CA3051	CA3053	CA3054	CA3102E	CA3011	CA3012	CA3013	CA3014	CA3043	CA3075	CA3076	CA3088	CA3089	CA2111A	CA3123
	Page No.	79	64	107	107	111	111	111	131	74	76	81	84	84	87	114	118	118	151	155	155	118	114	265	97	97	99	99	140	192	194	215	217	72	271
Applications	Voltage Regulator									■	■	■	■	■		■	■	■	■					■											
	Comparator																																		
	Comparator – High Current Output																																		
	Control – Relays, Heaters, LED's Lamps, etc.																																		
	Detector	■										■	■	■		■			■	■	■		■	■			■	■	■	■		■	■	■	
	Differential Amplifier	■	■	■	■				■	■	■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	
	Limiter			■	■	■	■	■				■	■	■			■	■	■			■		■	■	■	■	■	■	■	■		■	■	
	Mixer	■		■	■				■	■	■	■	■	■		■			■	■	■		■	■										■
	Modulator	■							■	■	■	■	■	■		■	■	■	■	■	■	■	■	■											
	Multivibrator									■	■					■				■	■		■												
	Oscillator			■	■					■							■	■	■			■		■											■
	Schmitt Trigger	■							■	■	■					■	■	■	■	■	■	■	■	■											
	Sense Amplifier	■							■	■	■					■	■	■	■	■	■	■	■	■	■	■									
	Switching			■	■											■	■	■	■	■	■	■		■											
	Thyristor & SCR Control																																		
	Freq. Doubler, Mult., Divide, Sq. Root, Squarer																																		
	Display Decoder-Driver																																		
	Timer																																		
Features	Balanced Input	■		■	■				■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■	■	■	■	■	■		■	■	
	Balanced Output			■	■				■	■	■	■	■	■	■	■	■	■	■	■	■		■	■	■	■									
	Low Noise (1/f)																																		
	Regulated Power Supply			■	■																								■	■	■	■	■	■	■
	Class B Output			■	■																														
	AGC Capability	■	■			■	■	■	■	■	■	■	■	■			■	■				■										■	■		■
	Multiple Unit															■			■	■	■		■	■											
	Wide Band	■	■	■				■	■		■	■	■	■		■	■	■	■				■	■	■	■	■	■	■	■	■		■	■	
	Micropower					■																													
	Decimal Pt. Output																																		
	Ripple Blanking																																		
Package	Type Designation Suffix Letter (See Note 1)																																		
	Flat Pack (FP)																																		
	Dual-In-Line Ceramic (DIC)																			■															
	Dual-In-Line Plastic (DIP)		E																		■		■	E						■‡		E	E	E,Q	E
	TO-5	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	T			■			■	■	■	■	■		■				
	Chip	H		H				H		H	H		H			H	H		H				H	H		H			H	H	H				
	Beam Lead																L		L				L												
	Frit Seal																F	F				F								F					
	TO-5 Style Dual-In-Line (DIL-CAN)																S	S				S													

NOTE 1: The indicated suffix letter identifies the package type for the device type number having a suffix letter; a black square is shown for a type number with no suffix letter.

- ● CA3001 is also useful as a Broadband (Video) Amplifier.
- † CA3040 is also useful as a Differential Amplifier.
- ‡ In quad-in-line package (Q)

Power-Control and Voltage-Regulator Circuits, Analog Multiplier, and Computer-Interface Circuits

		Power Control													Voltage Regulators			Analog Multiplier	Computer Interface Circuits					General Purpose							
		Thyristor Control				Power Control Switch/ Ampl.			Programmable Comparator		Timers		Photo Det.						Sense Ampl.	Decoder Drivers				Voltage Comparator							
																								Single			Quad.				
		CA3058	CA3059	CA3079	CA3097	CA3094A	CA3094B	CA3094	CA3098	CA3099	CA555	CA555C	CA3062	CA3085	CA3085A	CA3085B	CA3091	CA1541	CD2500E	CD2501E	CD2502E	CD2503E	CA111	CA211	CA311	CA139	CA139A	CA239	CA239A	CA339	CA339A
	Page No.	161	161	161	244	231	231	231	250	254	42	42	172	210	210	210	222	69	318	318	318	318	30	30	30	37	37	37	37	37	37
Applications	Voltage Regulator					■	■	■						■	■	■															
	Comparator	■	■	■	■	■	■	■	■	■													■	■	■	■	■	■	■	■	■
	Comparator – High Current Output	■	■	■		■	■	■	■	■				■	■	■															
	Control – Relays, Heaters, LED's, Lamps, Etc.	■	■	■	■	■	■	■	■	■																					
	Detector	■	■	■									■				■														
	Differential Amplifier	■	■	■		■	■	■	■	■																					
	Limiter																														
	Mixer					■	■	■									■														
	Modulator					■	■	■	■	■	■	■					■														
	Multivibrator				■	■	■	■	■	■			■										■	■	■	■	■	■	■	■	■
	Oscillator	■	■	■	■	■	■	■	■	■	■	■																			
	Schmitt Trigger				■	■	■	■	■	■													■	■	■	■	■	■	■	■	■
	Sense Amplifier																	Sense Amplifier													
	Switching	■	■	■		■	■	■	■	■				■																	
	Thyristor & SCR Control	■	■	■	■	■	■	■	■	■				■	■	■															
	Freq. Doubler, Mult., Divide, Sq. Root, Squarer																■														
	Display Decoder-Driver																		■	■	■	■									
	Timer	■	■	■	■	■	■	■	■	■	■	■																			
Features	Balanced Input					■	■	■	■	■													■	■	■	■	■	■	■	■	■
	Balanced Output												■																		
	Low Noise (1/f)					■	■	■						■	■	■															
	Regulated Power Supply	■	■	■						■																					
	Class B Output																														
	AGC Capability					■	■	■																							
	Multiple Unit																									■	■	■	■	■	■
	Wide Band																														
	Micropower					■	■	■	■	■																					
	Decimal Pt. Output																		■		■										
	Ripple Blanking																			■		■									
		Type Designation Suffix Letter (See Note 1)																													
Package	Flat Pack (FP)																														
	Dual-In-Line Ceramic (DIC)	■															D	D													
	Hermetic Gold CHIP (DIP)										G	G											G	G	G	G	G	G	G	G	G
	Dual-In-Line Plastic (DIP)		■	■	E			E	E	E	E*			E*					E	E	E	E			E*	E	E	E	E	E	E
	TO-5					T	T	T	T		T		■	■	■	■							T	T	T						
	Chip		H		H			H	H	H	H			H			H	H							H					H	
	Gold Chip											GH													GH					GH	
	Beam Lead													L																	
	Frit Seal																														
	TO-5 Style Dual-In-Line (DIL-CAN)					S	S	S	S		S			S	S								S	S	S						

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* 8-lead DIP (MINI-DIP) package.

Consumer Circuits

TV Receiver Circuits

		Remote Control	Automatic Fine-Tuning(AFT)			IF Systems: Sound					IF Systems: Pix			Chroma Systems: 2 Package										3 Package				Luminance Processor	"Jungle" Circuit		Horizontal Systems	
		CA3035	CA3044	CA3064	CA3139	CA3134	CA3041	CA3042	CA3065	CA2111A	CA270A,B,C	CA3068	CA1352	CA3066	CA3067	CA3070	CA3121	CA3067	CA3126	CA1398	CA3125	CA3128	CA3137	CA3070	CA3071	CA3072	CA3170	CA3143	CA3120	CA3142	CA920A	CA3147
	Page No.	127	142	175	292	288	134	137	177	72	39	183	64	180	180	185	269	180	274	67	273	279	290	185	185	185	304	300	265	265	59	302
Circuit Functions	Audio Driver						■	■	■																							
	Audio Preamplifier	■					■	■	■	■																						
	ACC													■		■	■		■	■		■	■	■	■		■					
	AFC/AFT		■	■	■						■																					
	AFPC															■			■			■		■			■					
	AGC										■	■	■																■	■		
	Chroma Amplifier													■			■		■	■		■	■		■							
	Chroma Demodulator														■		■	■			■		■			■						
	Chroma Processor:													■		■	■		■	■				■	■		■					
	PAL Systems																					■										
	Luminance Processor																											■				
	Converter																															
	Detector		■	■	■	■		■	■	■	■					■							■	■			■					
	Video Amplifier										■	■									■		■		■			■	■	■		
	Sync Processor																												■	■	■	
	IF Amplifier		■	■	■	■	■	■	■	■		■	■																			
	Limiter		■			■	■	■	■	■																						
	Oscillator													■		■		■	■	■		■	■	■			■					
	Audio Power Amplifier					■																										
	Tint Control														■	■				■			■	■			■					
	Hor. Oscillator																														■	■
	Hor. Driver																														■	■
	Noise Gate																														■	■
	Vert. Sync. Output																															■
Package	TYPE DESIGNATION SUFFIX LETTER (See Note 1))																															
	Dual-In-Line Plastic			E	E	E,EM				E			E			■	E			E	E		E	■	■	■	E	E	E	E	E	E
	Quad In-Line Plastic				Q	QM	■	■	■	Q	W	■		■	■			■	Q			Q										
	TO-5 Standard Lead	■	■																													
	TO-5 Formed Lead	VI	VI	■																												

Note 1: Where a code letter is shown (E, EM, Q, T, VI), add the code letter as a suffix to the type number to identify the package (and lead configuration) option. A black square indicates no suffix code is added to the type number for that package option.

QM = Quad-in-line plastic with heat sink
EM = Dual-in-line plastic with heat sink
W = Modified Quad-in-line plastic

Consumer Circuits

		Audio Circuits						Multiplex Decoders			AM Rcvr. Ckts.		FM Receiver Circuits							
		Pre-Amp.		Drivers		Power Amplifiers							FM IF Subsystems					FM IF Gain Blocks		
		CA3036	CA3052	CA3094	CA3094A,B	CA810	CA3131, CA3132	CA758	CA1310	CA3090A	CA3088	CA3123	CA2111A	CA3089	CA3075	CA3043	CA3013, CA3014	CA3011	CA3012	CA3076
	Page No.	128	158	231	231	57	287	54	61	220	215	271	72	217	192	140	99	97	97	194
Circuit Functions	Audio Driver			■	■			Stereo Multiplex Decoder												
	Audio Preamplifier	■	■	■	■						■			■	■	■	■			
	ACC																			
	AFC/AFT													■						
	AFPC																			
	AGC			■	■						■			■						
	Chroma Amplifier																			
	Chroma Demodulator																			
	Chroma Signal Processor																			
	Converter										■	■								
	Detector										■		■	■	■	■	■			
	Video Amplifier																	■	■	■
	Sync Processor																			
	IF Amplifier										■	■	■	■	■	■	■	■	■	■
	Limiter												■	■	■	■	■	■	■	■
	Oscillator											■								
	Audio Power Amplifier					■	■													
	Tint Control																			
Package	TYPE DESIGNATION SUFFIX LETTER (See Note 1)																			
	Dual-In-Line Plastic		■				EM	E	E		E	E	E	E						
	Quad-In-Line Plastic					Q,QM				Q			Q		■					
	TO-5 Standard Lead	■		T	T											■	■	■	■	■
	TO-5 Formed Lead																			

Note:1: Where a code letter is shown (E, EM, Q, T, V1), add the code letter as a suffix to the type number to identify the package (and lead configuration) option. A black square indicates no suffix code is added to the type number for that package option.

QM = Quad-in-line plastic with heat sink

EM = Dual-in-line plastic with heat sink

Linear IC Replacement Guide

Advanced Micro Devices Type No.	RCA Direct Replacement
AM101AT	CA101AT
AM101T	CA101T
AM201T	CA201T
AM301AT	CA301AT
AM307T	CA307T
AM741CT	CA741CT
AM741T	CA741T
AM747CT	CA747CT
AM747T	CA747T
AM748CT	CA748CT
AM748T	CA748T

Analog Devices Type No.	RCA Direct Replacement
AD101AH	CA101AT
AD201H	CA201T
AD301AH	CA301AT
AD741	CA741T
AD741C	CA741CT

Fairchild Semiconductor Type No.	RCA Direct Replacement
LM101AD	CA101AG
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM108AH	CA108AT
LM108H	CA108T
LM111H	CA111T
LM139D	CA139G
LM201AD	CA201AG
LM201AH	CA201AT
LM201H	CA201T
LM207H	CA207T
LM208AH	CA208AT
LM208H	CA208T
LM301AD	CA301AG
LM301AH	CA301AT
LM301AN	CA301AG CA301AE
LM307H	CA307T
LM307N	CA307G CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
LM339D	CA339G
LM339N	CA339G CA339E
μA723HC	CA723CT
μA723HM	CA723T
741DC	CA741CG● CA741CE●
741DM	CA741G● CA741E●
741HC	CA741CT
741HM	CA741T
741TC	CA741CG CA741CE
747DC	CA747CG CA747CE

Fairchild Semiconductor Type No.	RCA Direct Replacement
747DM	CA747G CA747E
747HC	CA747CT
747HM	CA747T
748DC	CA748CG*
748DM	CA748CG*
748HC	CA748CT
748HM	CA748T
748TC	CA748CG CA748CE
μA758	CA758E
MC1458P1	CA1458G
MC3401P	CA3401G
FPQ3724P	CA3724G
FPQ3725P	CA3725G
U5B7748312	CA748T
U5B7748393	CA748CT
U5R7723312	CA723T
U5R7723393	CA723CT
U6A7723393	CA723CE
U9T7558393	CA1458G

Intersil Type No.	RCA Direct Replacement
ICL-101-TY	CA101T
ICL-101A-TY	CA101AT
ICL-108-TY	CA108T
ICL-108A-TY	CA108AT
ICL-201-TY	CA201T
ICL-201A-TY	CA201AT
ICL-208-TY	CA208T
ICL-208A-TY	CA208AT
ICL-301A-PA	CA301AG● CA301AE●
ICL-301A-TY	CA301AT
ICL-308-TY	CA308T
ICL-308A-TY	CA308AT
ICL-723-TZ	CA723T
ICL-723C-TZ	CA723CT
ICL-741-TY	CA741T
ICL-741C-TY	CA741CT
ICL-741-LNC	CA741CG CA741CE
ICL-748-TY	CA748T
ICL-748C-TY	CA748CT
ICL-8741-PA	CA741G CA741E
ICL-8741C-PA	CA741CG CA741CE
ICL-8748-PA	CA748G CA748E
ICL-8748C-PA	CA748CG● CA748CE●

Motorola Semiconductor Type No.	RCA Direct Replacement
MLM101AG	CA101AT
MLM107G	CA107T
MLM111G	CA111T
MLM201AG	CA201AT
MLM207G	CA207T
MLM211G	CA211T

Motorola Semiconductor Type No.	RCA Direct Replacement
MC1310P	CA1310E
MC1311P	CA758E
MC1352P	CA1352E
MC1357P	CA2111AE
MC1398P	CA1398E
MC1441L	CA1541D
MC1458G	CA1458T
MC1458C1	CA1458G
MC1458CP1	CA1458G CA1458E
MC1541L	CA1541D
MC1558G	CA1558T
MC1558L	CA1558G
MC1723CG	CA723CT
MC1723CH	CA723CH
MC1723G	CA723T
MC1741G	CA741T
MC1741CG	CA741CT
MC1741CL	CA741CG
MC1741CP1	CA741CG CA741CE
MC1741L	CA741G
MC1741P2	CA741E●
MC1741CP2	CA741CE●
MC1747CL	CA747CG
MC1747CP2	CA747CG
MC1747L	CA747G
MC1748G	CA748T
MC1748CG	CA748CT
MC1748CP1	CA748CG
MC3302P	CA339AE
MC3401P	CA3401E
MPQ3724P	CA3724G
MPQ3725P	CA3725G

National Semiconductor Type No.	RCA Direct Replacement
LM101AD	CA101AG●
LM101AH	CA101AT
LM101H	CA101T
LM107D	CA107G●
LM107H	CA107T
LM108AH	CA108AT
LM108H	CA108T
LM111H	CA111T
LM124D	CA124G
LM139AD	CA139AG
LM139D	CA139G
LM201AH	CA201AT
LM201AD	CA201AG●
LM201H	CA201T
LM207D	CA207G●
LM207H	CA207T
LM208AH	CA208AT
LM208H	CA208T
LM211H	CA211T
LM224D	CA224G
LM239AD	CA239AG
LM239D	CA239G
LM301AH	CA301AT
LM301AN	CA301AG CA301AE
LM307D	CA307G●

National Semiconductor Type No.	RCA Direct Replacement
LM307H	CA307T
LM307N	CA307G CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
LM324D	CA324G
LM324N	CA324G CA324E
LM339AD	CA339AG
LM339AN	CA339AG CA339AE
LM339D	CA339G
LM339N	CA339G CA339E
LM723CH	CA723CT
LM723H	CA723T
LM741CD	CA741CG●
LM741CH	CA741CT
LM741CN	CA741CG● CA741CE●
LM741D	CA741G
LM741H	CA741T
LM747CD	CA747CG■
LM747CH	CA747CT
LM747CN	CA747CG■ CA747CE■
LM747D	CA747G
LM747H	CA747T
LM748H	CA748T
LM748CH	CA748CT
LM748CN	CA748CG CA748CE
LM1310N	CA1310E
LM1458H	CA1458T
LM1458N	CA1458G CA1458E
LM1558H	CA1558T
LM1800N	CA758E
LM2111	CA2111AE
LM2901N	CA339G
DH3724CD	CA3724G
DH3724CN	CA3724G
DH3725CD	CA3725G
DH3725CN	CA3725G
LM3900N	CA3401G*

Precision Monolithic Type No.	RCA Direct Replacement
SSS108AJ	CA108AT
SSS108J	CA108T
SSS208AJ	CA208AT
SSS208J	CA208T
SSS308AJ	CA308AT
SSS308J	CA308T

Raytheon Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM108AH	CA108AT

Linear IC Replacement Guide (Con't)

Raytheon Type No.	RCA Direct Replacement
LM108H	CA108T
LM111H	CA111T
LM201AH	CA201AT
LM201H	CA201T
LM207H	CA207T
LM211H	CA211T
LM301AH	CA301AT
LM301AN	CA301AG CA301AE
LM307H	CA307T
LM307N	CA307G CA307E
LM308AH	CA308AT
LM308H	CA308T
LM311H	CA311T
RC723T	CA723CT
RM723T	CA723T
RC741DN	CA741CG● CA741CE●
RC741TE	CA741CT
RM741TE	CA741T
RC748DN	CA748CG CA748CE
RC748TE	CA748CT
RM748TE	CA748T
RC1458DN	CA1458G CA1458E
RC14587	CA1458T
SP3724QD	CA3724G
SP3725QD	CA3725G
RM4558TE	CA1558T

Silicon General Type No.	RCA Direct Replacement
SG101AT	CA101AT
SG101M	CA101S
SG101T	CA101T
SG107T	CA107T
SG108AT	CA108AT
SG108T	CA108T
SG111T	CA111T
SG201AT	CA201AT
SG201T	CA201T
SG207T	CA207T
SG208AT	CA208AT
SG208T	CA208T
SG211T	CA211T
SG301AM	CA301AG● CA301AE●
SG301AT	CA301AT
SG307M	CA307G● CA307E●
SG307T	CA307T
SG308AT	CA308AT
SG308T	CA308T
SG311T	CA311T
SG339AN	CA339AG CA339AE
SG339N	CA339G CA339E
SG723CT	CA723CT
SG723T	CA723T
SG741CM	CA741CG CA741CE

Silicon General Type No.	RCA Direct Replacement
SG741CT	CA741CT
SG741M	CA741G● CA741E●
SG741T	CA741T
SG747CT	CA747CT
SG747T	CA747T
SG748CM	CA748CG● CA748CE●
SG748CT	CA748CT
SG748M	CA748G CA748E
SG748T	CA748T
SG1458M	CA1458G CA1458E

Signetics Type No.	RCA Direct Replacement
LM101AH	CA101AT
LM101H	CA101T
LM107H	CA107T
LM201AH	CA201AT
LM201H	CA201T
LM301AH	CA301AT
LM301AN$_1$	CA301AG CA301AE
LM307H	CA307T
LM307N	CA307G CA307E
μA723CL	CA723CT
μA723L	CA723T
N5558T	CA1458T
N5558V	CA1458G CA1458E
N5741T	CA741CT
N5741V	CA741CG● CA741CE●
N5747A	CA747CG■ CA747CE■
N5748T	CA748CT
N5748V	CA748CG CA748CE
S5558T	CA1558T
S5741T	CA741T
S5748T	CA748T

Solitron Type No.	RCA Direct Replacement
UC4741	CA741T
UC4741C	CA741CT

Sprague Type No.	RCA Direct Replacement
ULN2111A	CA2111AE
ULN2125A	CA3120E
ULN2269A	CA3121E
ULN2741D	CA741T
ULN2747A	CA747CG■ CA747CE■
ULS2741D	CA741CT
ULX2210	CA1310E
ULX2244	CA758E

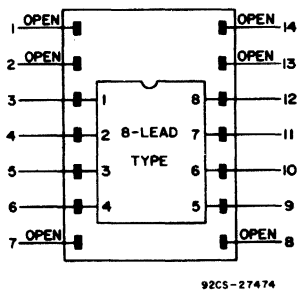
Texas Instruments Type No.	RCA Direct Replacement
SN52101AJ	CA101AG●
SN52101AJA	CA101AG●
SN52101AJP	CA101AG
SN52101AL	CA101AT
SN52101AN	CA101AG●
SN52101AP	CA101AG
SN52101L	CA101T
SN52107JA	CA107G●
SN52107JP	CA107G
SN52107L	CA107T
SN52107N	CA107G●
SN52107P	CA107G
SN52108L	CA108T
SN52108AL	CA108AT
SN52558L	CA1558T
SN52558JP	CA1558G CA1558G
SN52558P	CA1558S CA1558E
SN52741J	CA741G●
SN52741JA	CA741G●
SN52741JP	CA741G
SN52741L	CA741T
SN52741N	CA741G● CA741G
SN52741P	CA741S CA741E
SN52747J	CA747G
SN52747JA	CA747G
SN52747L	CA747T
SN52747N	CA747G
SN52748L	CA748T
SN52748J	CA748G●
SN52748JA	CA748G●
SN52748JP	CA748G
SN52748N	CA748G● CA748G
SN52748P	CA748S● CA748E●
SN72301AJ	CA301AG●
SN72301AJA	CA301AG●
SN72301AJP	CA301AG
SN72301AL	CA301AT
SN72301AN	CA301AG● CA301AG
SN72301AP	CA301AE
SN72307JA	CA307G●
SN72307JP	CA307G
SN72307L	CA307T
SN72307N	CA307G● CA307G
SN72307P	CA307S CA307E
SN72308AL	CA308AT
SN72308L	CA308T
SN72558JP	CA1458G
SN72558L	CA1458T
SN72558P	CA1458G CA1458E
SN72741J	CA741CG
SN72741JA	CA741CG●
SN72741JP	CA741CG
SN72741L	CA741CT
SN72741N	CA741CG●

Texas Instruments Type No.	RCA Direct Replacement
SN72741P	CA741CG CA741CE●
SN72747	CA747CT
SN72747J	CA747CG
SN72747JA	CA747CG
SN72747N	CA747CG
SN72748J	CA748CG●
SN72748JA	CA748CG●
SN72748JP	CA748CG
SN72748L	CA748CG
SN72748N	CA748CG●
SN72748P	CA748CG CA748CE
SN76115N	CA1310E
SN76116N	CA758E
SN76650N	CA1352E

*Can be selected to replace LM3900N

■Terminals 9 and 13 must be externally

●Can be substituted for the correspondi 14-lead dual-in-line type by inserting d vice into 14-pin socket (or board) so th terminal No. 1 of the 8-lead RCA type coincides with socket (or board) termi No. 3 of the 14-lead type to be replace



14-Lead Terminal Arrangement For Type to be Replaced

Note:
RCA types in TO-5 packages are also su plied with dual-in-line formed leads ("D CAN" package) and are designated with suffix letter (S). These types are both pi and electrical direct replacements for th corresponding 8-lead "Mini-Dip" dual-ir line types.

CA101, CA201, CA301 Types

Operational Amplifiers

For Commercial, Industrial, and Military Applications

RCA-CA101, CA101A, CA201, CA201A, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

Types CA101A and CA201A have all the desirable features and characteristics of the CA101 and CA201, respectively, plus superior input-offset characteristics, and improved noise performance.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

"G" Suffix Types—Hermetic Gold-CHIP Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

Features:

- **Short-circuit protection and latch-free operation**
- **Unity-gain phase compensation with a single 30-pF capacitor**
- **Replacement for industry types 101, 101A, 201, 201A, 301A**

Applications:

- **Long-interval integrator**
- **Timers**
- **Sample and hold circuits**
- **Summing amplifiers**
- **Multivibrators**
- **Comparators**
- **Instrumentation**
- **AC/DC converters**
- **Inverting amplifiers**
- **Sine- & square-wave generators**
- **Capacitance multipliers & simulated inductors**

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals):		
CA101, CA101A, CA201, CA201A	44	V
CA301A	36	V
DC INPUT VOLTAGE	±15	V
(For supply voltage less than ± 15 V, the Input Voltage rating is equal to the DC Supply Voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION	Indefinite*	
DEVICE DISSIPATION:		
Up to $T_A = 75^oC$	500	mW
Above $T_A = 75^oC$	derate linearly at 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating –		
CA101, CA101A	−55 to +125	°C
CA201A	−25 to +85	°C
CA201, CA301A	0 to +70	°C
Storage (All types)	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

* At $T_A \leq 70^oC$ and $T_C \leq 125^oC$ (CA101);
$T_A \leq 75^oC$ and $T_C \leq 125^oC$ (CA101A, CA201A);
$T_A \leq 55^oC$ and $T_C \leq 70^oC$ (CA201, CA301A).

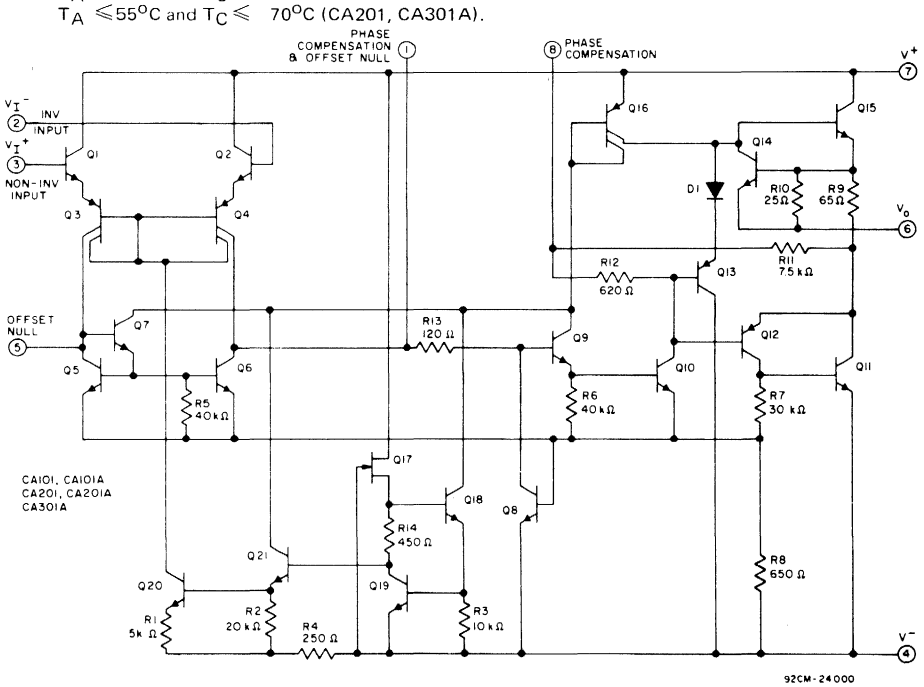
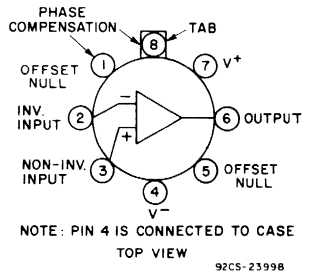
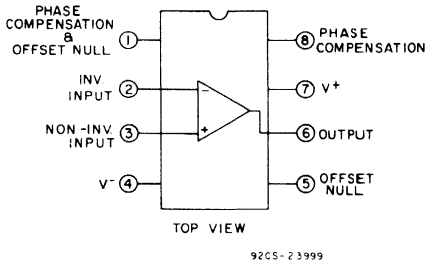


Fig.1 – Schematic diagram.



a – TO-5 style package for all types

T-Suffix
S-Suffix



b – Plastic package for CA301A

G-Suffix
E-Suffix

Fig.2 – Functional diagrams.

CA101, CA201, CA301 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 5 to 15 V		LIMITS CA101 Min.	CA101 Typ.	CA101 Max.	CA201 Min.	CA201 Typ.	CA201 Max.	UNITS	LIMITS CA101A CA201A Min.	CA101A CA201A Typ.	CA101A CA201A Max.	CA301A Min.	CA301A Typ.	CA301A Max.	UNITS
Input Offset Voltage V_{IO}	T_A=25°C	$R_S \leq 10k\Omega$	–	1	5	–	2	7.5	mV	–	–	–	–	–	–	mV
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		–	0.7	2	–	2	7.5	
		$R_S \leq 10k\Omega$	–	–	6	–	–	10		–	–	–	–	–	–	
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}		$R_S \leq 10k\Omega$	–	6	–	–	10	–	μV/°C	–	–	–	–	–	–	μV/°C
		$R_S \leq 50\Omega$	–	3	–	–	6	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	3	15	–	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	−55°C to +25°C		–	–	–	–	–	–	nA/°C	–	0.02	0.2	–	–	–	nA/°C
	0°C to +25°C		–	–	–	–	–	–		–	–	–	–	0.02	0.6	
	+25°C to +70°C		–	–	–	–	–	–		–	–	–	–	0.01	0.3	
	+25°C to +125°C		–	–	–	–	–	–		–	0.01	0.1	–	–	–	
Input Offset Current I_{IO}	T_A=0°C		–	–	–	–	150	750	nA	–	–	–	–	–	–	nA
	T_A=25°C		–	40	200	–	100	500		–	1.5	10	–	3	50	
	T_A=70°C		–	–	–	–	50	400		–	–	–	–	–	–	
	T_A=125°C		–	10	200	–	–	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	–	20	–	–	70	
	T_A=−55°C		–	100	500	–	–	–		–	–	–	–	–	–	
Input Bias Current I_{IB}	T_A=−55°C		–	0.28	1.5	–	–	–	μA	–	–	–	–	–	–	μA
	T_A=0°C		–	–	–	–	0.32	2		–	–	–	–	–	–	
	T_A=25°C		–	0.12	0.5	–	0.25	1.5		–	0.03	0.075	–	0.07	0.25	
			–	–	–	–	–	–		–	–	0.1	–	–	0.3	
Supply Current $I^{\pm}$	T_A=25°C	$V^{\pm}$=15V	–	–	–	–	–	–	mA	–	–	–	–	1.8	3	mA
		$V^{\pm}$=20V	–	1.8	3	–	1.8	3		–	1.8	3	–	–	–	
	T_A=125°C	$V^{\pm}$=20V	–	1.2	2.5	–	–	–		–	1.2	2.5	–	–	–	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V^{\pm}$=15V, V_O=±10V	$R_L \geq 2k\Omega$	50	160	–	20	150	–	V/mV	50	160	–	25	160	–	V/mV
	$V^{\pm}$=15V, V_O=±10V	$R_L \geq 2k\Omega$	25	–	–	15	–	–		25	–	–	15	–	–	
Input Resistance R_I	T_A=25°C		0.3	0.8	–	0.1	0.4	–	MΩ	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing V_{OPP}	$V^{\pm}$=15V	R_L=10kΩ	±12	±14	–	±12	±14	–	V	±12	±14	–	±12	±14	–	V
	$V^{\pm}$=15V	R_L=2kΩ	±10	±13	–	±10	±13	–		±10	±13	–	±10	±13	–	
Common-Mode Input-Voltage Range V_{ICR}	$V^{\pm}$=15V		±12	–	–	±12	–	–	V	–	–	–	±12	–	–	V
	$V^{\pm}$=20V		–	–	–	–	–	–		±15	–	–	–	–	–	
Common-Mode Rejection Ratio CMRR		$R_S \leq 10k\Omega$	70	90	–	65	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	
Supply-Voltage Rejection Ratio PSRR		$R_S \leq 10k\Omega$	70	90	–	70	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	

▲ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified: CA101, CA101A: −55 to +125°C; CA201A: −25 to +85°C; CA201, CA301A: 0 to 70°C

	CA101	CA201	CA101A	CA201A	CA301A	
Max. V_{IO} (T_A = 25°C)	5	7.5	2	2	7.5	mV
Max. I_{IO} (T_A = 25°C)	200	500	10	10	50	nA
Min. A_{OL} (T_A = 25°C)	50	20	50	50	25	V/mV
T_A Range (Operating)	−55 to +125	0 to +70	−55 to +125	−25 to +85	0 to +70	°C
Slew Rate (Summing ampl.)	–	–	10	10	10	V/μs

CA101, CA201, CA301 Types

TYPICAL STATIC CHARACTERISTICS

Type CA101

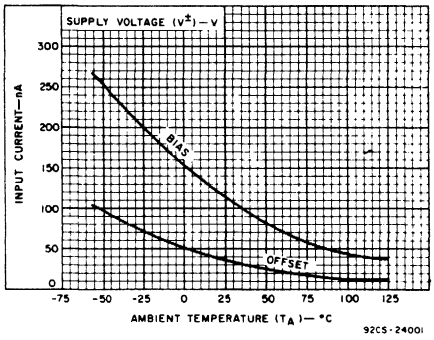


Fig.3 – Input current (I_{IO}, I_{IB}) vs. temperature.

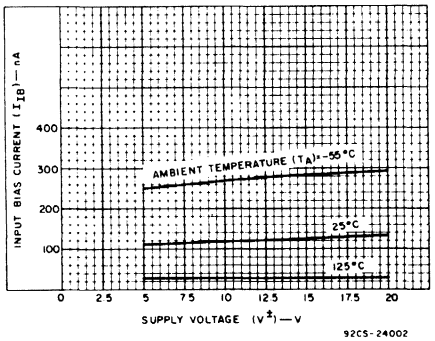


Fig.4 – Input bias current vs. supply voltage.

Types CA101, CA101A, and CA201A

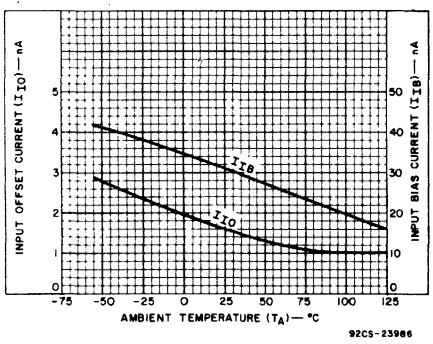


Fig. 5 – Input current (I_{IO}, I_{IB}) vs. temperature (CA101A and CA201A only).

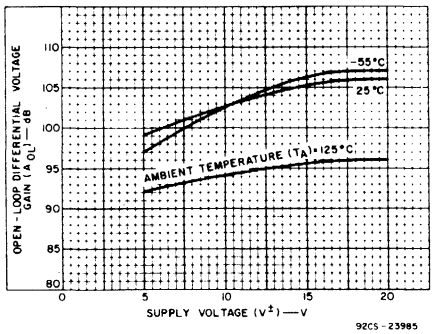


Fig.6 – Voltage gain vs. supply voltage.

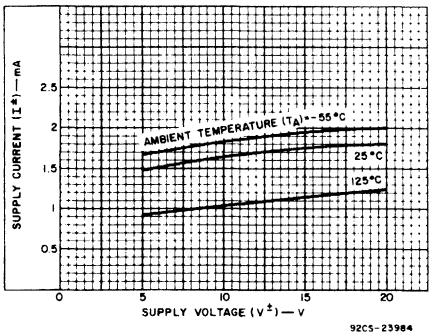


Fig.7 – Supply characteristics.

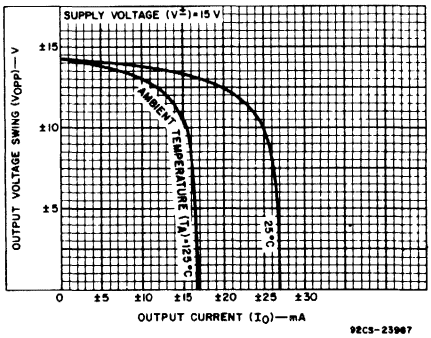


Fig.8 – Output characteristics.

Type CA301A

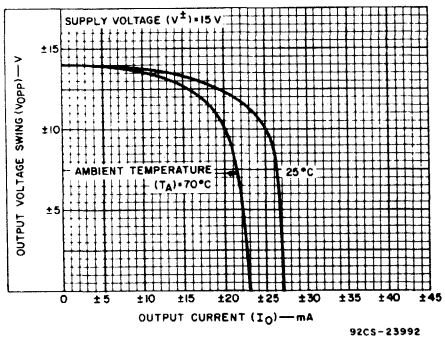


Fig. 9 – Output characteristics.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA101A AND CA201A

Single-Pole Compensation

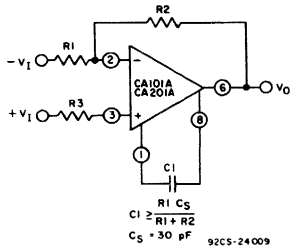


Fig. 10 – Test circuit employing single-pole compensation.

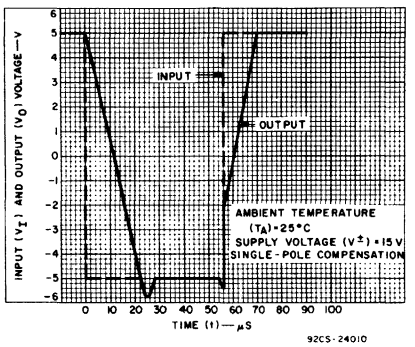


Fig. 11 – Voltage follower (V_I, V_O) pulse response.

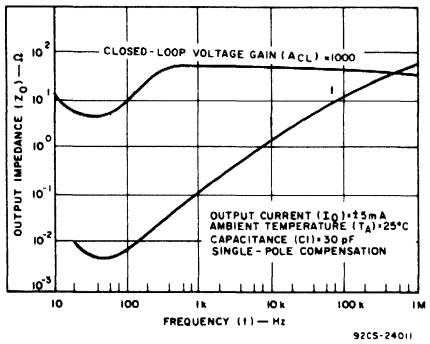


Fig. 12 – Closed-loop output impedance vs. frequency.

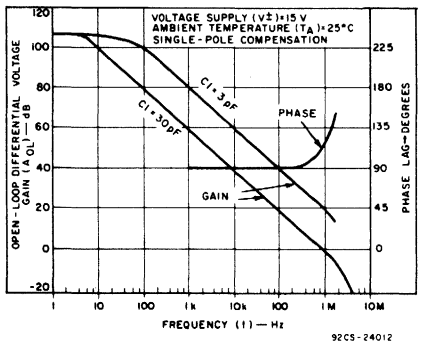


Fig. 13 – Voltage gain and phase lag vs. frequency.

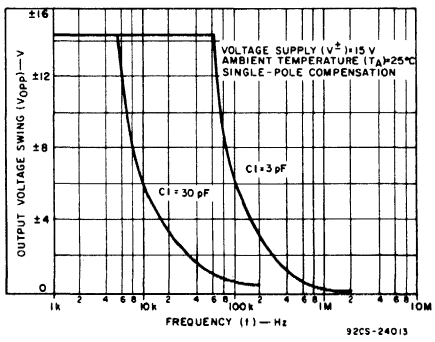


Fig. 14 – Output voltage swing vs. frequency.

CA101, CA201, CA301 Types

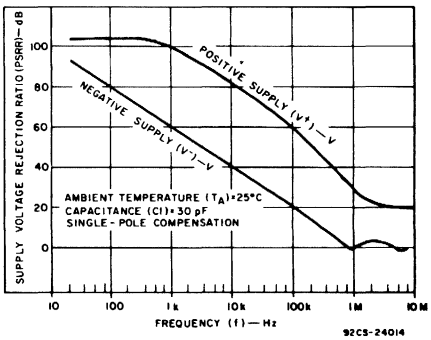


Fig. 15 — Supply voltage rejection ratio vs. frequency.

Two-Pole Compensation

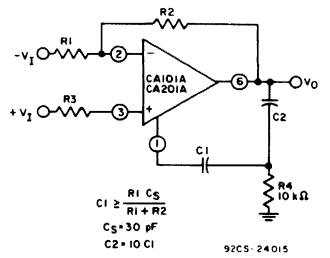


Fig. 16 — Test circuit employing two-pole compensation.

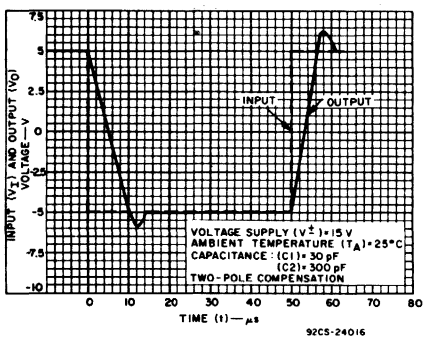


Fig. 17 — Voltage follower pulse response.

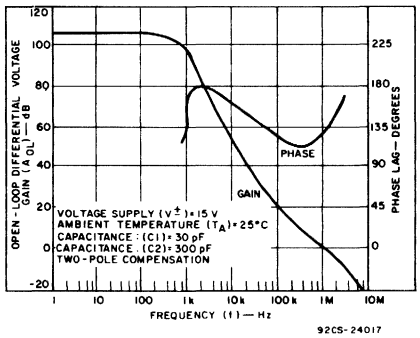


Fig. 18 — Voltage gain and phase lag vs. frequency.

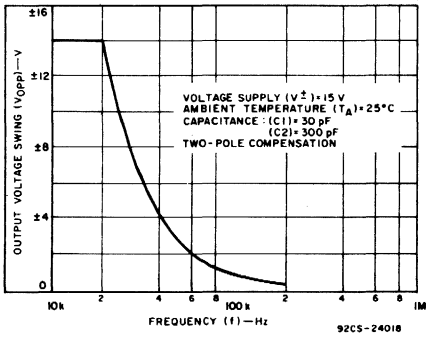


Fig. 19 — Output voltage swing vs. frequency.

Feed-Forward Compensation

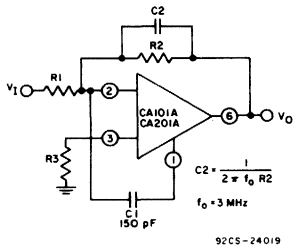


Fig. 20 — Test circuit employing feedforward compensation.

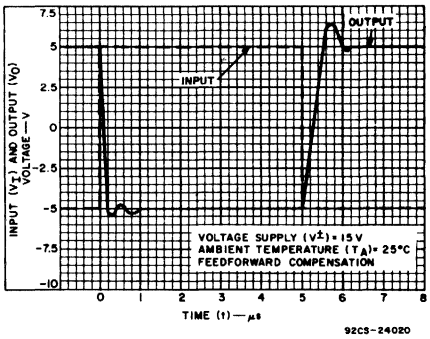


Fig. 21 — Inverter pulse response.

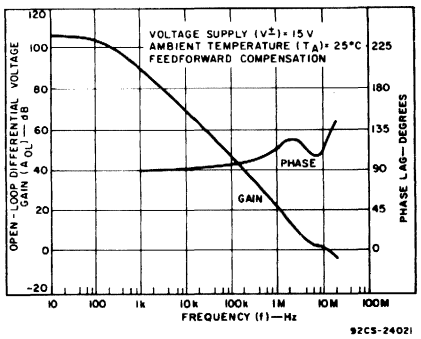


Fig. 22 — Voltage gain and phase lag vs. frequency.

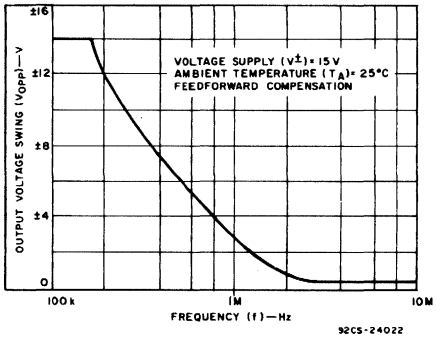


Fig. 23 — Output voltage swing vs. frequency.

CA101A AND CA201A

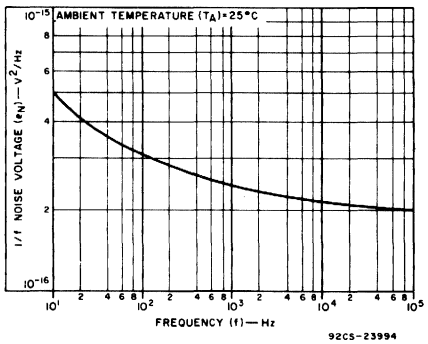


Fig. 24 — I/f noise voltage vs. frequency.

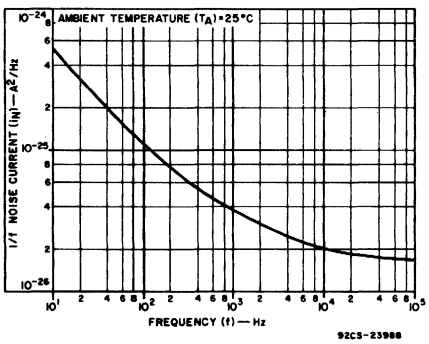


Fig. 25 — I/f noise current vs. frequency.

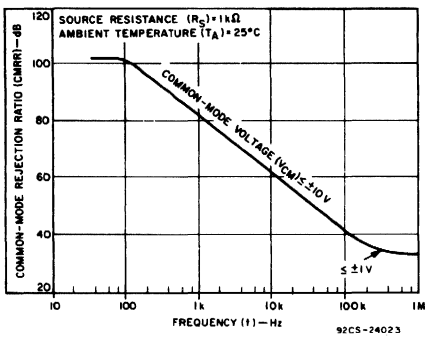


Fig. 26 — Common-mode rejection ratio vs. frequency.

CA107, CA207, CA307 Types
Operational Amplifiers

For Military, Industrial, and Commercial Applications

RCA-CA107, CA207, CA307 are general-purpose operational amplifiers intended for use in military, industrial, and commercial applications. A 30-pF on-chip capacitor provides internal frequency compensation. Low input current over temperature range (100 nA max.) for the CA107 and CA207 make these types especially well suited for applications such as long interval timers and sample-and-hold circuits.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA307 is also available in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

The CA107, CA207, and CA307 are direct replacements for industry types 107, 207, and 307 in packages with similar terminal arrangements.

Type \ Feature	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C	Package (Suffix)
CA107	3	20	100	−55 to +125	G, S, T
CA207	3	20	100	−25 to +85*	G, S, T
CA307	10	70	300	0 to +70▲	G, E, S, T

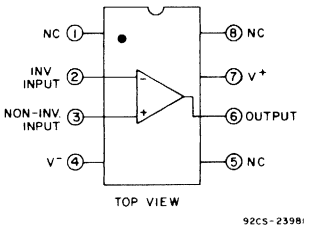
*Types CA207G, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temp. range of −25 to +85°C.

▲Types CA307G, E, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temp. range of 0 to 70°C.

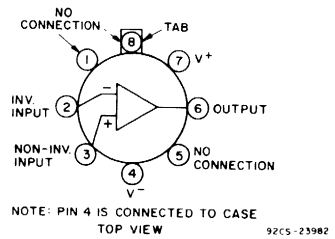
"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

Applications:

- **Long-interval integrators**
- **Timers**
- **Sample-and-hold circuits**
- **Summing amplifiers**
- **Multivibrators**



Functional diagram for plastic package.



Functional diagram for TO-5 style packages.

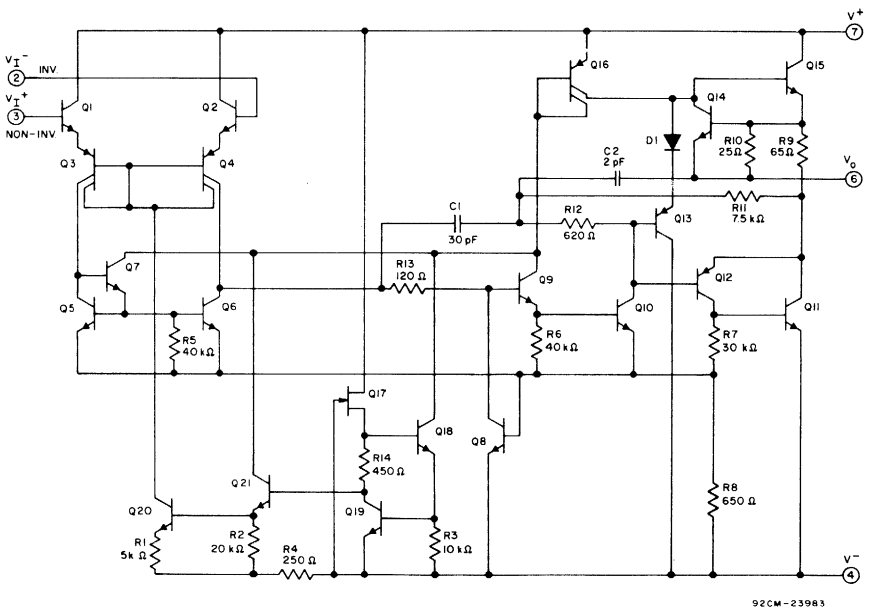


Fig. 1 — Schematic diagram of CA107, CA207, and CA307.

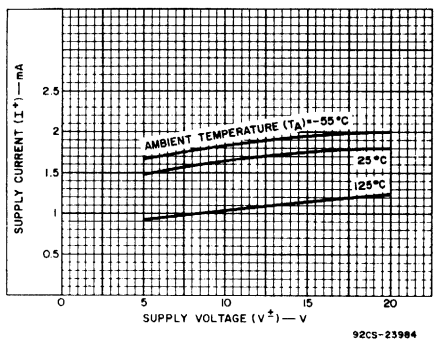


Fig. 2 — Supply current vs. supply voltage.

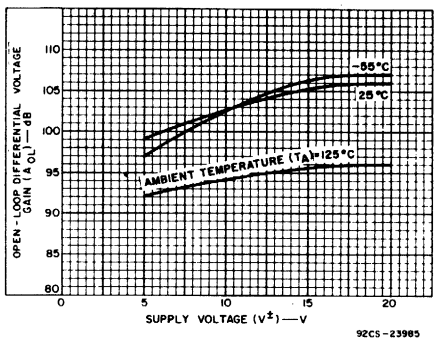


Fig. 3 — Open-loop differential voltage gain vs. supply voltage.

CA107, CA207, CA307 Types

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^\circ C$:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals):		
CA107, CA207	44	V
CA307	36	V
DC INPUT VOLTAGE	±15	V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)		
DIFFERENTIAL INPUT VOLTAGE	±30	V
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite	
DEVICE DISSIPATION UP TO $T_A = 70^\circ C$	500	mW
Above $T_A = 70^\circ C$ Derate linearly at	6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating – CA107	−55°C to +125°C	
CA207	−25°C to +85°C▲	
CA307	0°C to +70°C†	
Storage – All Types	−65°C to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C	

*For type CA307 continuous short circuit is allowed for Case Temperature to +70°C and ambient temperature to +55°C.

▲Types CA207G, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of −25 to +85°C.

†Types CA307G, E, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

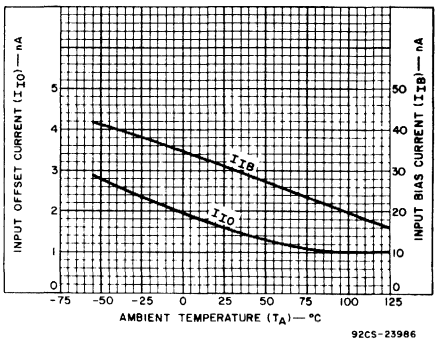


Fig. 4 – Input offset and input bias currents vs. ambient temperature.

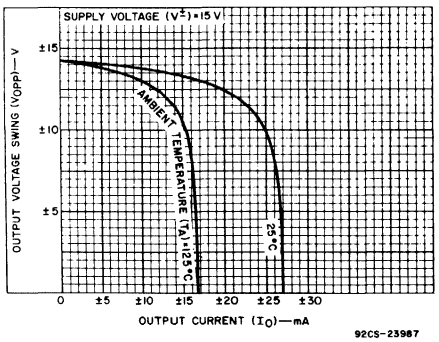


Fig. 5 – Output voltage swing vs. output current.

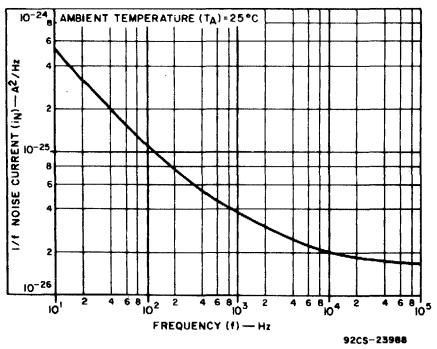


Fig. 6 – 1/f noise current vs. frequency.

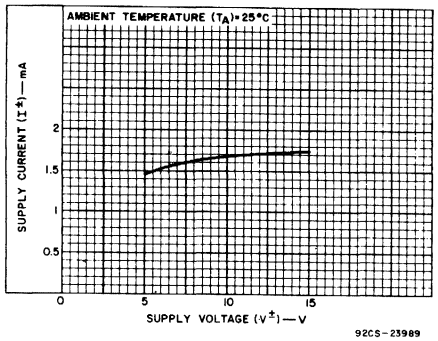


Fig. 7 – Supply current vs. supply voltage.

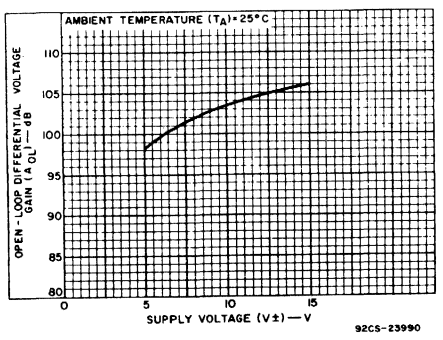


Fig. 8 – Open-loop differential voltage gain vs. supply voltage.

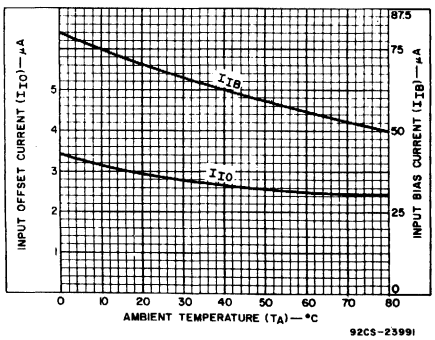


Fig. 9 – Input offset and input bias current vs. ambient temperature.

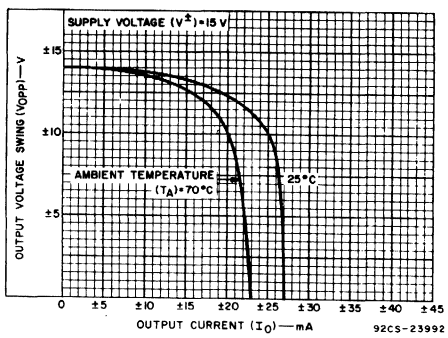


Fig. 10 – Output voltage swing vs. output current.

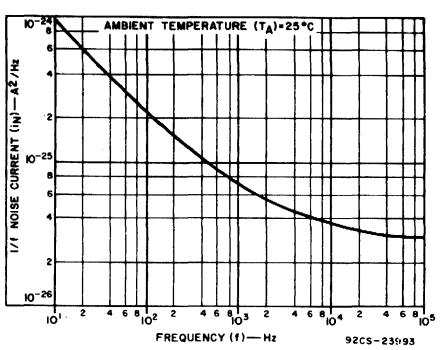


Fig. 11 – 1/f noise current vs. frequency.

CA107, CA207, CA307 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS▲ Supply Voltage (V±) = 5 V to 15 V (CA307) 5 V to 20 V (CA107,CA207)	LIMITS						UNITS
		CA107 CA207			CA307			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	T_A = 25°C, $R_S \leq 50\,k\Omega$	–	0.7	2	–	2	7.5	mV
	$R_S \leq 50\,k\Omega$	–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage, αV_{IO}		–	3	15	–	6	30	μV/°C
Input Offset Current, I_{IO}		–	–	20	–	–	70	nA
	T_A = 25°C	–	1.5	10	–	3	50	
Average Temperature Coefficient of Input Offset Current, αI_{IO}	See Note 1	–	0.01	0.1	–	0.01	0.3	nA/°C
	See Note 2	–	0.02	0.2	–	0.02	0.6	
Input Bias Current, I_{IB}		–	–	100	–	–	300	nA
	T_A = 25°C	–	30	75	–	70	250	
Supply Current, $I^{\pm}$	T_A = +125°C, $V^{\pm}$ = 20 V	–	1.2	2.5	–	–	–	mA
	T_A = 25°C, $V^{\pm}$ = 20 V, (CA307 $V^{\pm}$ = 15 V)	–	1.8	3	–	1.8	3	
Open-Loop Differential Voltage Gain, A_{OL}	$V^{\pm}$ = 15 V, V_O = ±10 V, $R_L \geq 2\,k\Omega$	25	–	–	15	–	–	V/mV
	$V^{\pm}$ = 15 V, V_O = ±10 V $R_L \geq 2\,k\Omega$, T_A = 25°C	50	160	–	25	160	–	
Input Resistance, R_I	T_A = 25°C	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing, V_{OPP}	$V^{\pm}$ = 15 V, R_L = 10 kΩ	±12	±14	–	±12	±14	–	V
	$V^{\pm}$ = 15 V, R_L = 2 kΩ	±10	±13	–	±10	±13	–	
Input Voltage Range, V_{ICR}	$V^{\pm}$ = 20 V, (CA307 $V^{\pm}$ = 15 V)	±15	–	–	±12	–	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 50\,k\Omega$	80	96	–	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq 50\,k\Omega$	80	96	–	70	96	–	dB

Note 1: For CA107, +25, to +125°C; For CA207, +25 to +85°C: For CA307, +25 to 70°C.

Note 2: For CA107, −55 to +25°C; For CA207, −25 to +25°C: For CA307, 0 to +25°C.

▲ Characteristics applicable over operating temperature range as shown below unless otherwise specified.

CA107 – T_A = −55 to +125°C

CA207 – T_A = −25 to +85°C

CA307 – T_A = 0 to 70°C

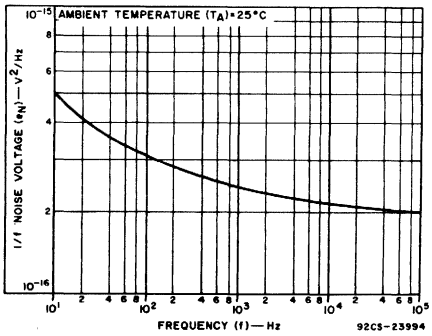


Fig. 12 – 1/f noise voltage vs. frequency.

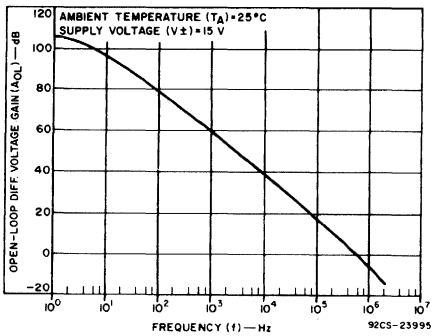


Fig. 13 – Open-loop differential voltage gain vs. frequency.

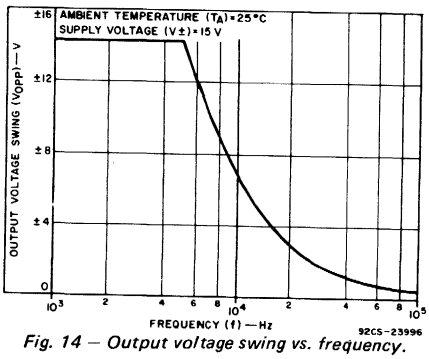


Fig. 14 – Output voltage swing vs. frequency.

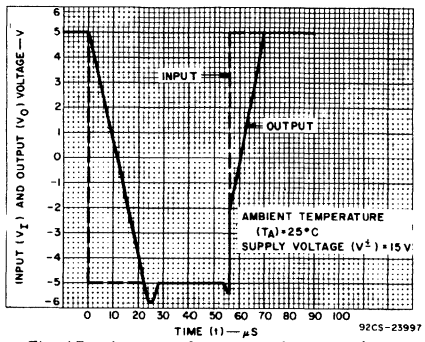


Fig. 15 – Input and output voltage vs. time.

CA108, CA208, CA308 Types

Precision Operational Amplifiers

For Military, Industrial, and Commercial Applications

Applications:

- Instrumentation
- Summing amplifier
- Comparator
- Multivibrators
- Band-pass filters
- Sample and hold

RCA-CA108T, CA108AT, CA108S, CA108AS, CA208T, CA208AT, CA208S, CA208AS, CA308T, CA308AT, CA308S, and CA308AS are uncompensated precision operational amplifiers using super-beta transistors and feature very low offset parameters, high input impedance, and defined drift rates with temperature change.

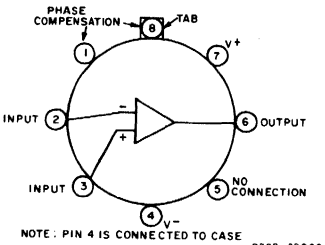
In addition to low drift, these super-beta op-amps have input currents sufficiently low to insure low drift, even when using high source resistances, e.g., 10 megohms.

These devices have sufficient supply rejection to operate from unregulated power supplies within a range of ±2 V to ±20 V, and the input bias current is specifically controlled for use in sample-and-hold applications.

The "A" versions have all the desirable features and characteristics of their prototypes plus exceptionally low input offset voltage characteristics. The CA108, CA108A, CA208, CA208A, CA308, and CA308A are direct replacements for industry types 108,108A,208,208A,308,308A, and they are supplied in either standard 8-lead TO-5 packages or in 8-lead TO-5 packages with dual-in-line formed leads ("DIL-CAN").

Features:

- Maximum input bias current – 2 nA for CA108 & CA208 series
  7 nA for CA308 series
- Maximum input offset current – 0.2 nA for CA108 & CA208 series
  1 nA for CA308 series
- Supply current of only 300 μA, even in saturation
- Maximum input offset voltage of 0.5 mV for "A" suffix types



TOP VIEW

FUNCTIONAL DIAGRAM

ELECTRICAL CHARACTERISTICS, MAXIMUM VALUES AT T_A = 25°C	CA108T CA108S	CA108AT CA108AS	CA208T CA208S	CA208AT CA208AS	CA308T CA308S	CA308AT CA308AS
Input Offset Voltage (V_{IO})	2 mV	0.5 mV	2 mV	0.5 mV	7.5 mV	0.5 mV
Input Offset Current (I_{IO})	0.2 nA				1 nA	
Input Bias Current (I_{IB})	2 nA			7 nA		
Average Temperature Coefficient of Input Offset Voltage ($\Delta V_{IO}/\Delta T$)	15 μV/°C	5 μV/°C	15 μV/°C	5 μV/°C	30 μV/°C	5 μV/°C
Ambient Operating-Temperature Range	–55 to +125°C		–25 to +85°C		0 to +70°C	

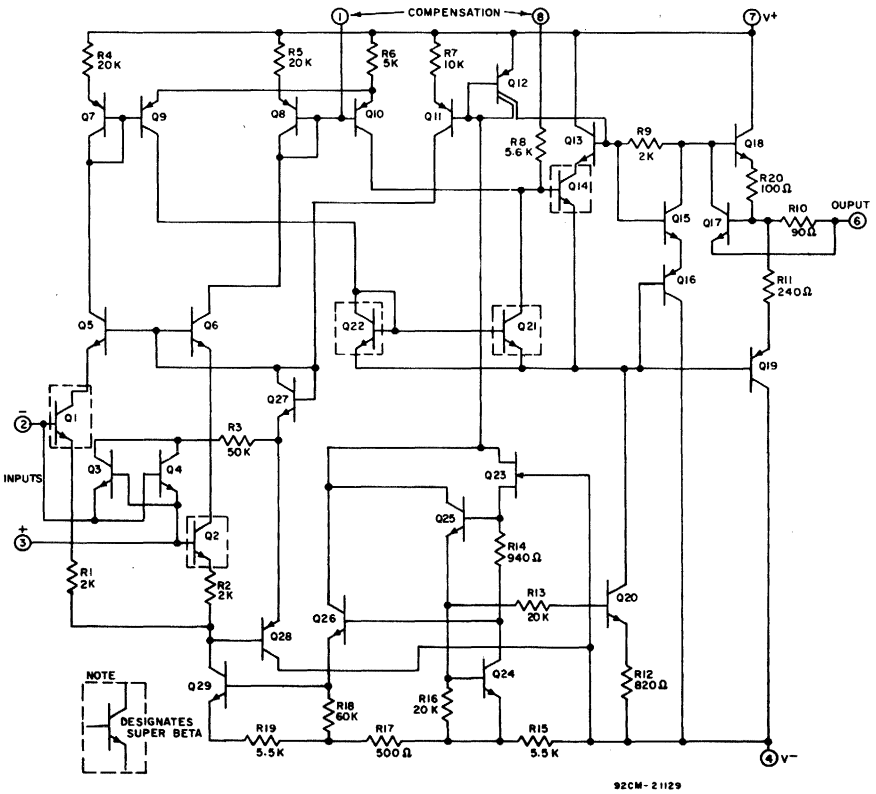


Fig. 1 – Schematic diagram.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DC Supply Voltage (Between V^+ and V^- Terminals):
- CA108, CA108A, CA208, CA208A . . . . . 40 V
- CA308, CA308A . . . . . 36 V

DC Input Voltage . . . . . ±15 V
(For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage)

Differential Input Current . . . . . ±10 mA

Output Short-Circuit Duration . . . . . Indefinite

Device Dissipation . . . . . 500 mW

Ambient Temperature Range:
- Operating – CA108, CA108A . . . . . –55°C to +125°C
- CA208, CA208A . . . . . –25°C to +85°C
- CA308, CA308A . . . . . 0°C to +70°C
- Storage – All Types . . . . . –65°C to +150°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +300 °C

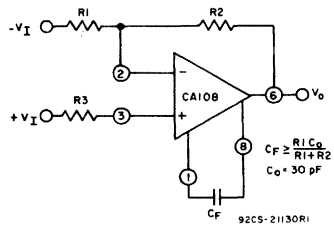


Fig. 2–Standard frequency-compensation.

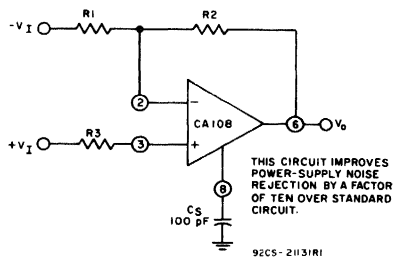


Fig. 3–Alternate frequency-compensation.

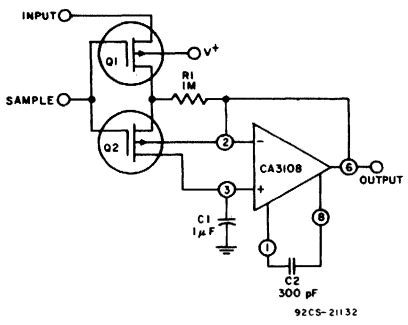


Fig. 4 – Sample-and-hold circuit.

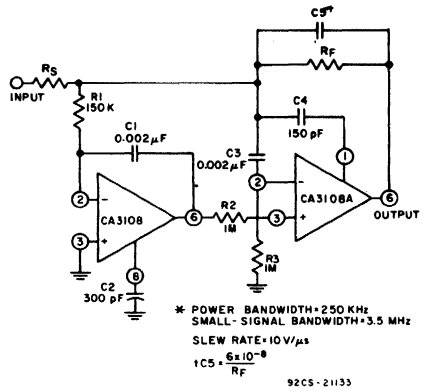


Fig. 5 – Fast summing amplifier circuit.*

CA108, CA208, CA308 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS FIG. No.	TEST CONDITIONS Supply Voltage (V) = ±5 V to ±15 V	LIMITS CA108 CA208 Min.	CA108 CA208 Typ.	CA108 CA208 Max.	CA108A CA208A Min.	CA108A CA208A Typ.	CA108A CA208A Max.	CA308 Min.	CA308 Typ.	CA308 Max.	CA308A Min.	CA308A Typ.	CA308A Max.	UNITS
Input Offset Voltage	V_{IO}	6,7	T_A = 25°C	–	0.7	2	–	0.3	0.5	–	2	7.5	–	0.3	0.5	mV
			Note 1	–	–	3	–	–	1	–	–	10	–	–	0.73	
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$		Note 1	–	3	15	–	1	5	–	6	30	–	1	5	µV/°C
Input Offset Current	I_{IO}	8,9	Note 1	–	–	0.4	–	–	0.4	–	–	1.5	–	–	1.5	nA
			T_A = 25°C	–	0.05	0.2	–	0.05	0.2	–	0.2	1	–	0.2	1	
Average Temperature Coefficient of Input Offset Current	$\frac{\Delta I_{IO}}{\Delta T}$		Note 1	–	0.5	2.5	–	0.5	2.5	–	2	10	–	2	10	pA/°C
Input Bias Current	I_{IB}	10, 11	Note 1	–	–	3	–	–	3	–	–	10	–	–	10	nA
			T_A = 25°C	–	0.8	2	–	0.8	2	–	1.5	7	–	1.5	7	
Supply Current	I_Q	12, 13	T_A = +125°C	–	0.15	0.4	–	0.15	0.4	–	–	–	–	–	–	mA
			T_A = 25°C	–	0.3	0.6	–	0.3	0.6	–	0.3	0.8	–	0.3	0.8	
Large-Signal Voltage Gain	A_V	2,14 15	V = ±15 V, T_A = 25°C V_O = ±10 V, $R_L \geq 10$ kΩ	50	300	–	80	300	–	25	300	–	80	300	–	V/mV
			V = ±15 V, V_O = ±10 V $R_L \geq 10$ kΩ, Note 1	25	–	–	40	–	–	15	–	–	60	–	–	
Input Resistance	R_I		T_A = 25°C	30	70	–	30	70	–	10	40	–	10	40	–	MΩ
Output Voltage	V_O	16, 17	V = ±15 V, R_L = 10 kΩ, Note 1	±13	±14	–	±13	±14	–	±13	±14	–	±13	±14	–	V
Input Voltage Range	V_I		V = ±15 V, Note 1	±13.5	–	–	±13.5	–	–	±14	–	–	±14	–	–	
Common-Mode Rejection Ratio	CMRR		Note 1	85	100	–	96	110	–	80	100	–	96	110	–	dB
Supply-Voltage Rejection Ratio	V_{RR}		Note 1	80	96	–	96	110	–	80	96	–	96	110	–	

Note 1: Ambient Temperature (T_A) over applicable operating temperature range as shown below unless otherwise specified.

CA108 CA108A	CA208 CA208A	CA308 CA308A
−55 to +125°C	−25 to +85°C	0 to +70°C

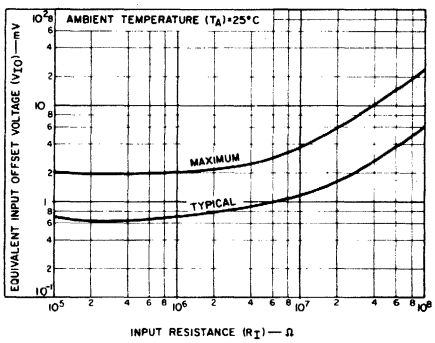


Fig. 6 – Input offset error for CA108, CA108A, CA208, and CA208A.

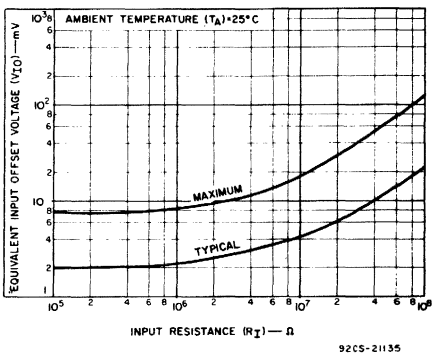


Fig. 7 – Input offset error for CA308 and CA308A.

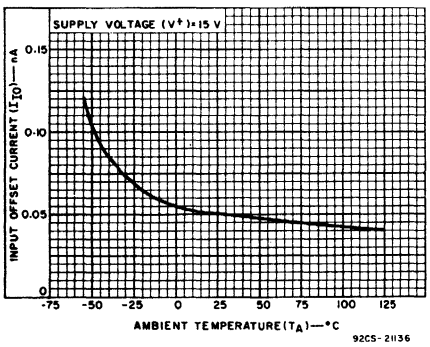


Fig. 8 – Input offset current vs. temperature for CA108, CA108A, CA208, and CA208A.

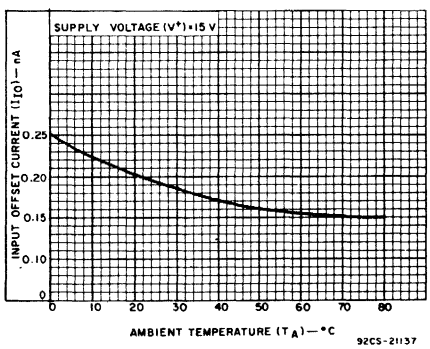


Fig. 9 – Input offset current vs. temperature for CA308 and CA308A.

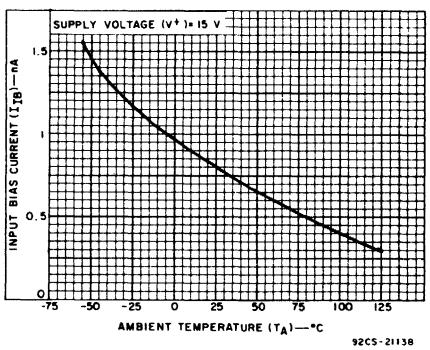


Fig. 10 – Input bias current vs. temperature for CA108, CA108A, CA208, and CA208A.

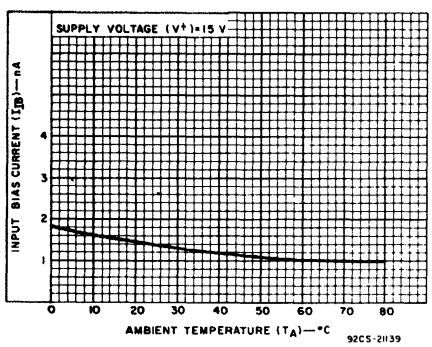


Fig. 11 – Input bias current vs. temperature for CA308 and CA308A.

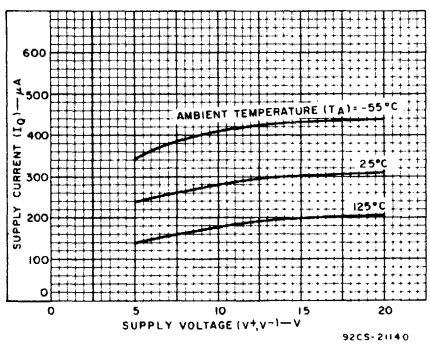


Fig. 12 – Supply current vs. supply voltage for CA108, CA108A, CA208, and CA208A.

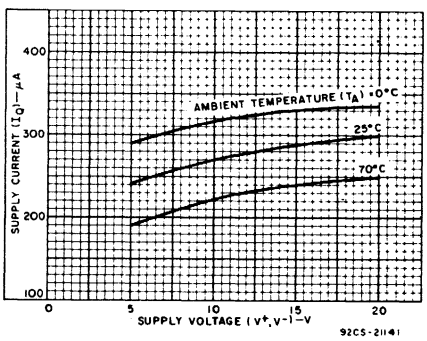


Fig. 13 – Supply current vs. supply voltage for CA308 CA308A.

CA108, CA208, CA308 Types

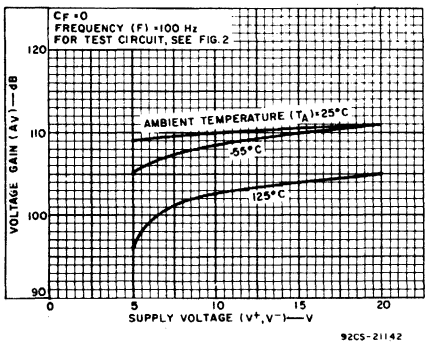


Fig. 14 – Voltage gain vs. supply voltage for CA108, CA108A, CA208, and CA208A.

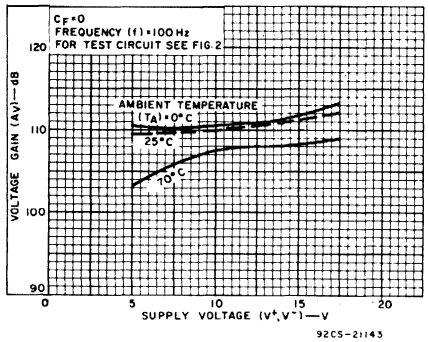


Fig. 15 – Voltage gain vs. supply voltage for CA308 and CA308A.

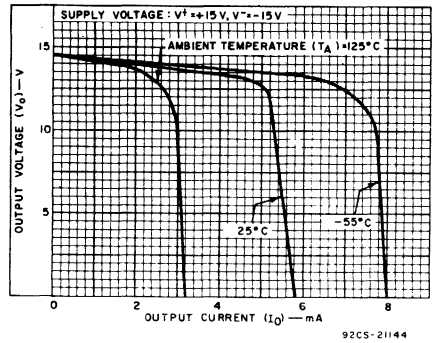


Fig. 16 – Output voltage vs. output current for CA108, CA108A, CA208, and CA208A.

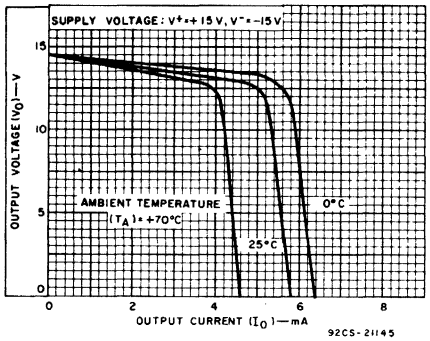


Fig. 17 – Output voltage vs. output current for CA308 and CA308A.

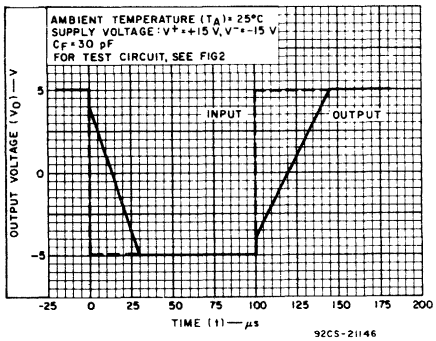


Fig. 18 – Voltage-follower pulse response for all types.

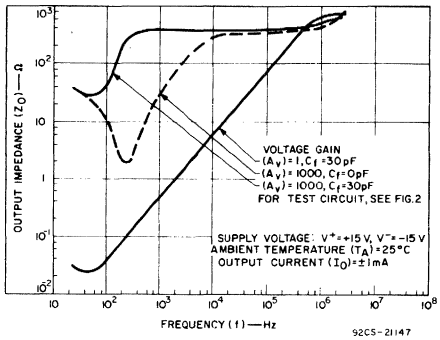


Fig. 19 – Closed-loop output impedance for all types.

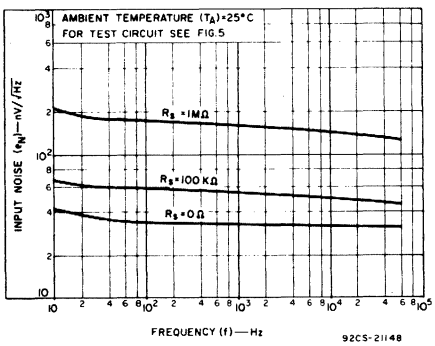


Fig. 20 – Input noise voltage for all types.

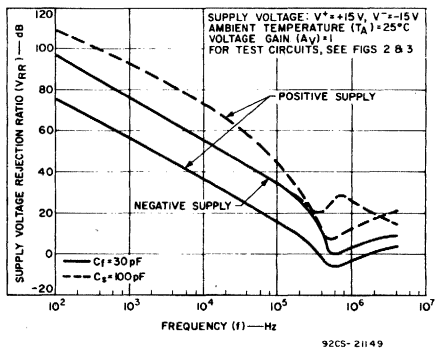


Fig. 21 – Power-supply rejection for all types.

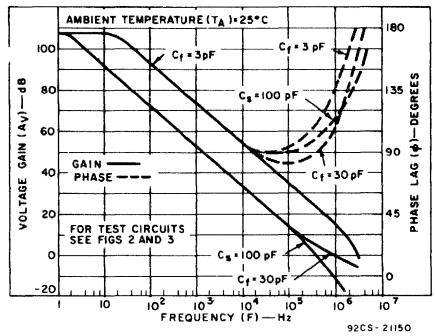


Fig. 22 – Open-loop frequency response for all types.

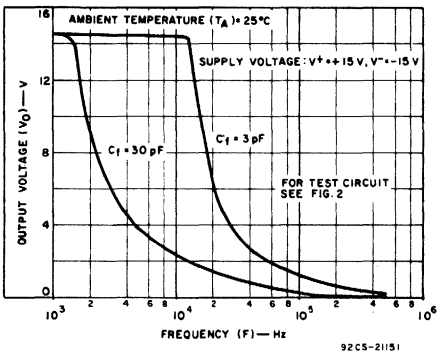


Fig. 23 – Large-signal frequency response for all types.

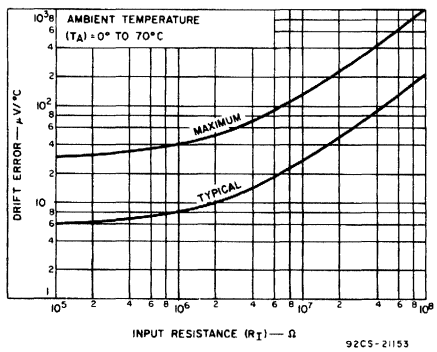


Fig. 24 – Drift error vs. input resistance for CA108, CA108A, CA208, and CA208A.

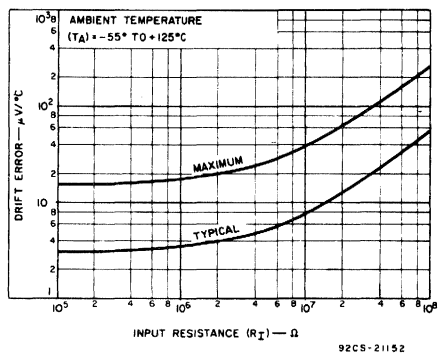


Fig. 25 – Drift error vs. input resistance for CA308 and CA308A.

CA111, CA211, CA311 Types

Voltage Comparators

For Commercial and Industrial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types—Standard Dual-In-Line Plastic Package

"T" and "S" Suffix Types—TO-5 Style Package

Applications

- **Multivibrators**
- **Positive and negative peak detectors**
- **Crystal oscillators**
- **Zero-crossing detectors**
- **Solenoid, relay, and lamp drivers**

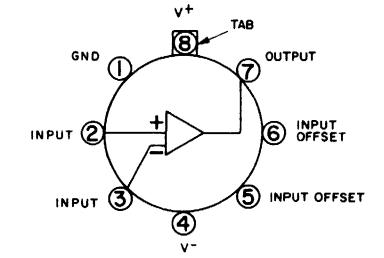
Features

- **Single- or dual-supply operation**
- **Power consumption — 135 mW at ±15 V**
- **Strobe capability**
- **Low input-offset current:**
  CA111, CA211 — 4 nA(typ.)
  CA311 — 6 nA(typ.)
- **Differential input-voltage range — ±30 V**
- **Directly interchangeable with National Semiconductor LM111, LM211, and LM311 Series types**

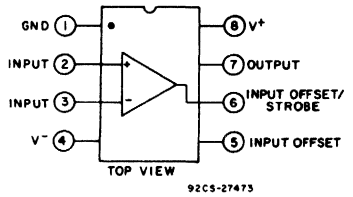
The RCA-CA111, CA211, and CA311 are monolithic voltage comparators that operate from dual supplies up to ±15 V, or from single supplies down to 5 V. This single-supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition, they can drive lamps or relays, and switch voltages up to 50 V (CA311, 40 V) at currents as high as 50 mA.

The inputs and the outputs of the CA111, CA211, and CA311 can be isolated from system ground, allowing the output to drive loads referred to ground, V^+, or V^-.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA311 is also available in the 8-lead dual-in-line plastic package ("MINI-DIP",E suffix), and in chip form (H suffix).



Functional diagram for TO-5 style package.



Functional diagram for plastic package.

Type \ Feature	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C	Package (Suffix)
CA111	3	10	100	−55 to +125	G,S,T
CA211	3	10	100	−25 to +85▲	G,S,T
CA311	7.5	50	250	0 to +70 †	G,E,S,T

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals) . . . . . 36 V
DC INPUT VOLTAGE* . . . . . ±15 V
DIFFERENTIAL INPUT VOLTAGE . . . . . ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}):
  CA111, CA211 . . . . . 50 V
  CA311 . . . . . 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) . . . . . 30 V
OUTPUT SHORT-CIRCUIT DURATION . . . . . 10 s
DEVICE DISSIPATION:
  Up to $T_A = 25°C$ . . . . . 500 mW
  Above $T_A = 25°C$ . . . . . derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating:
    CA111 . . . . . −55 to +125°C
    CA211 . . . . . −25 to +85°C▲
    CA311 . . . . . 0 to +70°C†
  Storage, all types . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
  from case for 10 seconds max. . . . . +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

▲ Types CA211G,S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of −25 to +85°C.

† Types CA311G,E,S and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

CA111, CA211, CA311 Types

TYPICAL CHARACTERISTICS – ALL TYPES

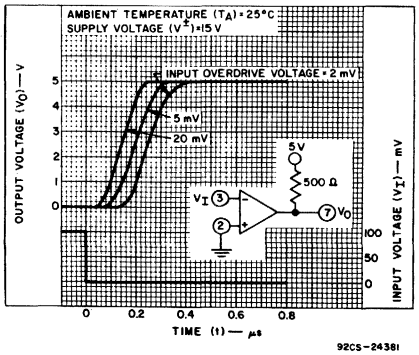


Fig. 1 – Response time for various input overdrive voltages–positive input.

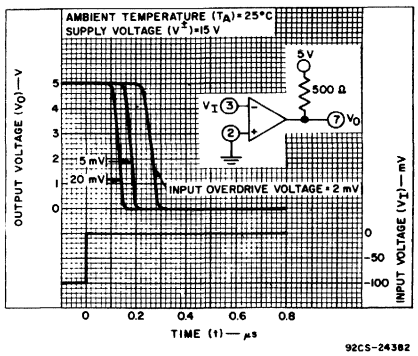


Fig. 2 – Response time for various input overdrive voltages–negative input.

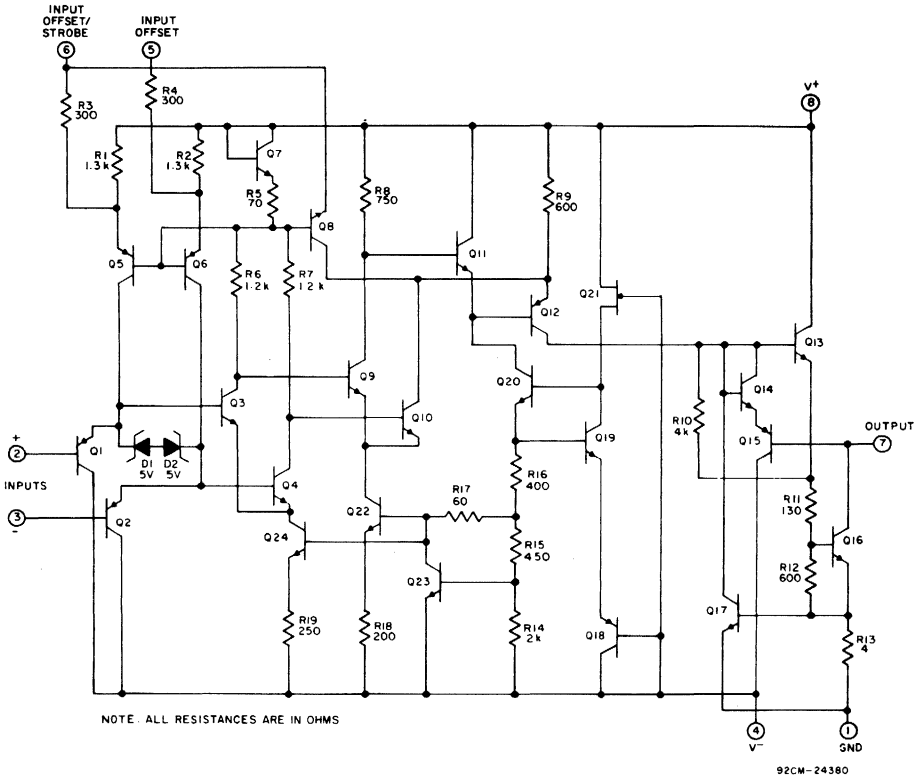


Fig. 3 – Schematic diagram for CA111, CA211, and CA311.

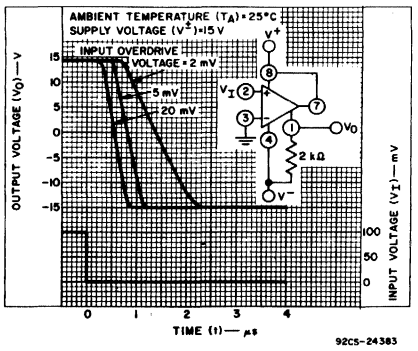


Fig. 4 – Response time for various input overdrive voltages–positive input.

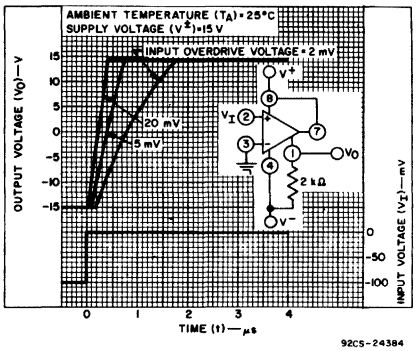


Fig. 5 – Response time for various input overdrive voltages–negative input.

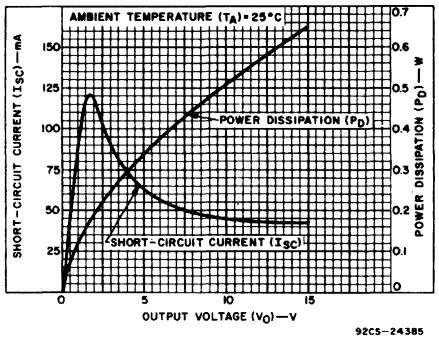


Fig. 6 – Output limiting characteristics.

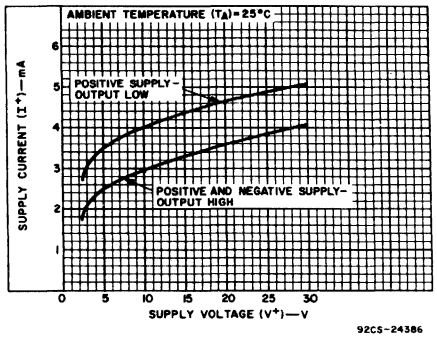


Fig. 7 – Supply current vs. supply voltage.

TYPICAL CHARACTERISTCS –CA111, CA211

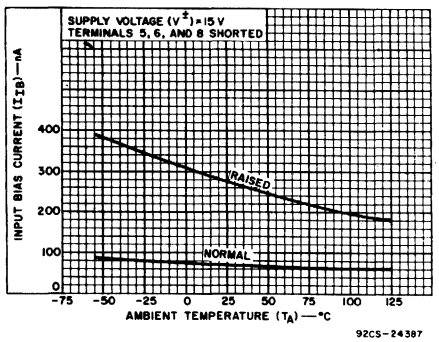


Fig. 8 – Input bias current vs. ambient temperature.

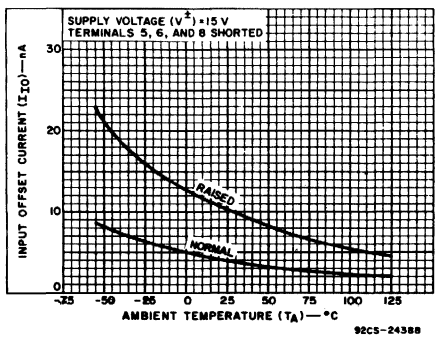


Fig. 9 – Input offset current vs. ambient temperature.

CA111, CA211, CA311 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS: SUPPLY VOLTAGE ($V^{\pm}$) = 15 V UNLESS OTHERWISE SPECIFIED		LIMITS: CA111 CA211 TYP.	CA111 CA211 MAX.	CA311 TYP.	CA311 MAX.	UNITS
Input Offset Voltage, V_{IO}	$R_s \leq 5\ k\Omega$, Note 2	T_A=25°C	0.7	3	2	7.5	mV
		Note 1	–	4	–	10	
Saturation Voltage	V_I = –5 mV, I_O = 50 mA (For CA311, $V_I \leq$ –10 mV)	T_A=25°C	0.75	1.5	–	–	V
	$V^+ \geq$4.5 V, V^-=0, $V_I \leq$ –6 mV, $I_{SINK} \leq$ 8 mA (For CA311, $V_I \leq$ –10 mV)	Note 1	0.23	0.4	–	–	
Input Voltage Range, V_{IPP}		Note 1	±14	–	±14	–	V
Input Offset Current, I_{IO}	Note 2	T_A = 25°C	4	10	6	50	nA
		Note 1	–	20	–	70	
Input Bias Current, I_{IB}	Note 2	T_A=25°C	60	100	100	250	nA
		Note 1	–	150	–	300	
Positive Supply Current, I^+		T_A = 25°C	5.1	6	5.1	7.5	mA
Negative Supply Current, I^-		T_A=25°C	4.1	5	4.1	5	mA
Output Leakage Current	$V_I \geq$5 mV, V_O = 35 V (For CA311, $V_I \geq$ –10 mV)	T_A=25°C	0.2	10	–	–	nA
		Note 1	0.1	0.5	–	–	μA
Strobe On Current		T_A=25°C	3	–	3	–	mA
Voltage Gain, A		T_A=25°C	200	–	200	–	V/mV
Response Time	100 mV Input Step with 5 mV overdrive voltage	T_A=25°C	200	–	200	–	ns

Note 1: Ambient temperature (T_A) over applicable operating temperature range as shown below.

CA111	CA211	CA311
–55 to +125°C	–25 to +85°C	0 to +70°C

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1-mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ±15 V dual supply.

TYPICAL CHARACTERISTICS – CA111, CA211 (CONT'D)

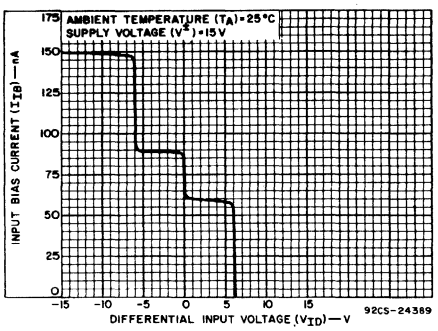


Fig. 10 – Input characteristcs.

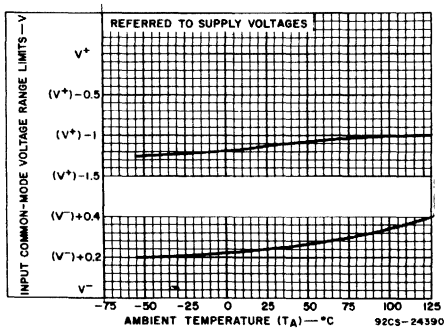


Fig. 11 – Common-mode voltage range limits vs. ambient temperature.

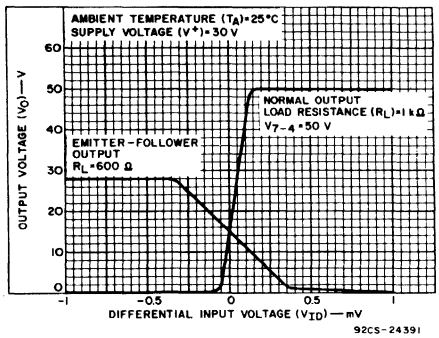


Fig. 12 – Transfer function.

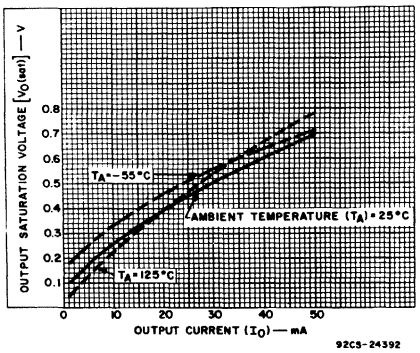


Fig. 13 – Output saturation voltage vs. output current.

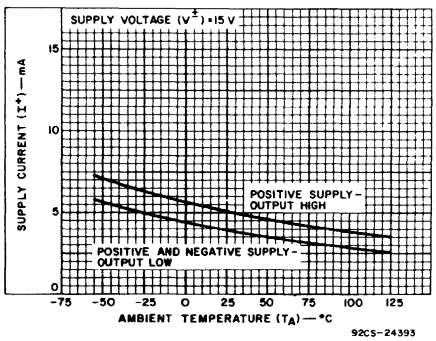


Fig. 14 – Supply current vs. ambient temperature.

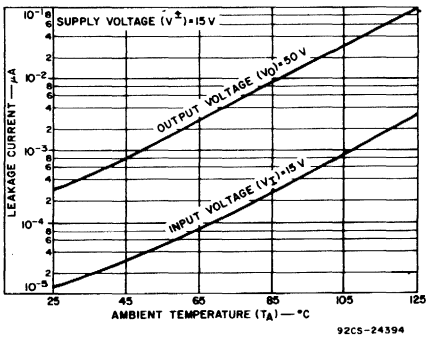


Fig. 15 – Input and output leakage current vs. ambient temperature.

CA111, CA211, CA311 Types

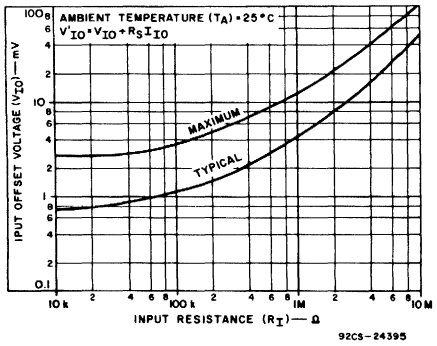


Fig. 16 – Offset error.

TYPICAL CHARACTERISTICS – CA311

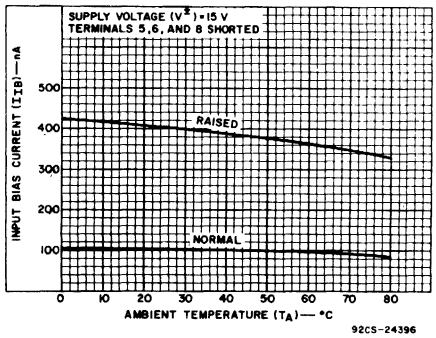


Fig. 17 – Input bias current vs. ambient temperature.

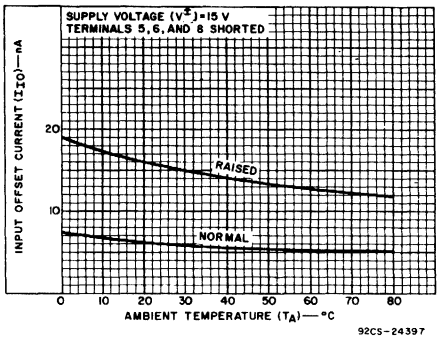


Fig. 18 – Input offset current vs. ambient temperature.

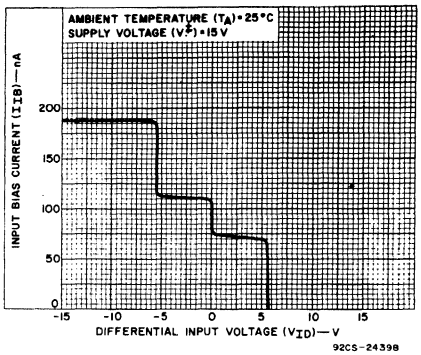


Fig. 19 – Input characteristics.

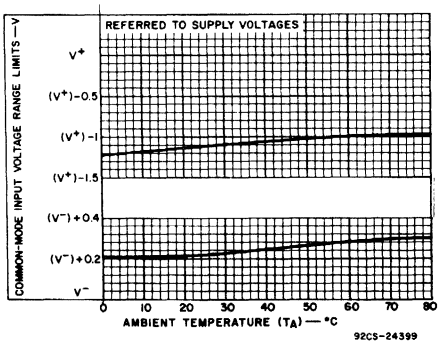


Fig. 20. – Common-mode voltage range limits vs. ambient temperature.

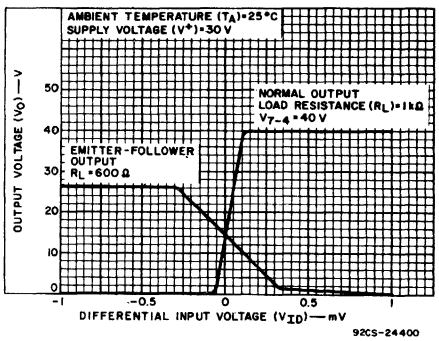


Fig. 21 – Transfer function.

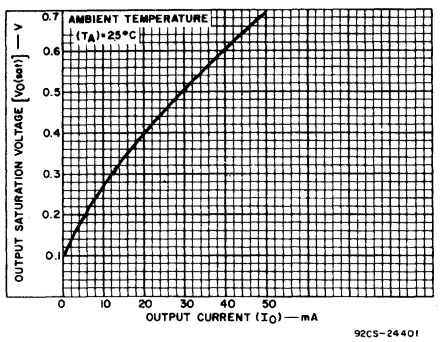


Fig. 22 – Output saturation voltage vs. output current.

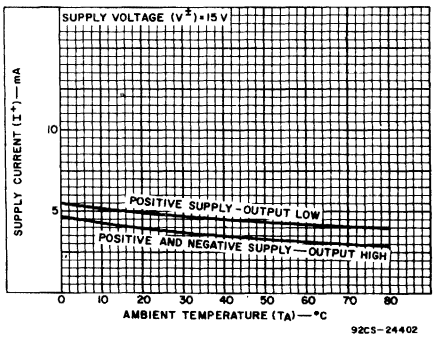


Fig. 23 – Supply current vs. ambient temperature.

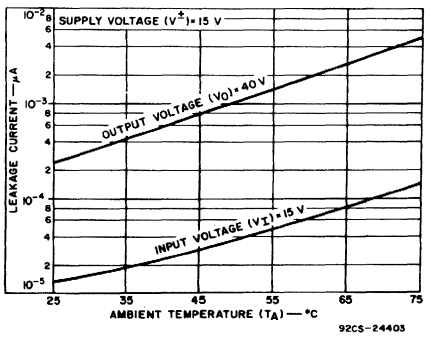


Fig. 24 – Input and output leakage current vs. ambient temperature.

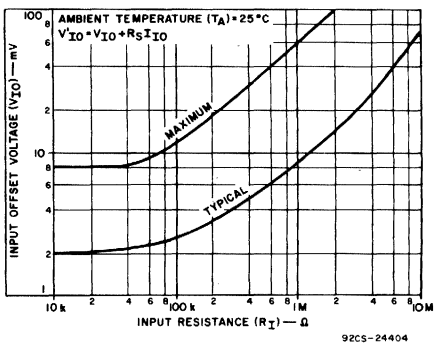


Fig. 25 – Offset error.

CA124, CA224, CA324 Types

Quad Operational Amplifiers

For Commercial, Industrial, and Military Applications

"E" Suffix Types: Standard Dual-In-Line Plastic Package
"G" Suffix Types: Hermetic Gold-Chip Dual-In-Line Plastic Package

The RCA-CA124, -CA224, and -CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specifically to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to $V^+ - 1.5$ V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix), or in a hermetic gold-chip 14-lead dual-in-line plastic package (G suffix) to provide true hermetic performance. The CA324 is also available in chip form (H suffix), and as a hermetic gold-chip (HG suffix).

Features:

- **Operation from single or dual supplies**
- **Unity-gain bandwidth . . . . . 1 MHz (typ.)**
- **DC voltage gain . . . . . 100 dB (typ.)**
- **Input bias current . . . . . 45 nA (typ.)**
- **Input offset voltage . . . . . 2 mV (typ.)**
- **Input offset current . . . . . 5 nA (typ.) for CA224, CA324**
  3 nA (typ.) for CA124
- **Replacement for industry types 124, 224, 324**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

Applications

- **Summing amplifiers**
- **Multivibrators**
- **Oscillators**
- **Transducer amplifiers**
- **DC gain blocks**

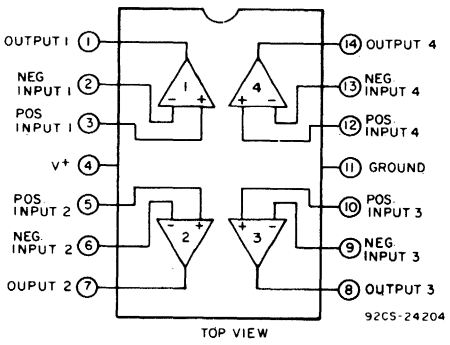


Fig. 1 – Functional diagram.

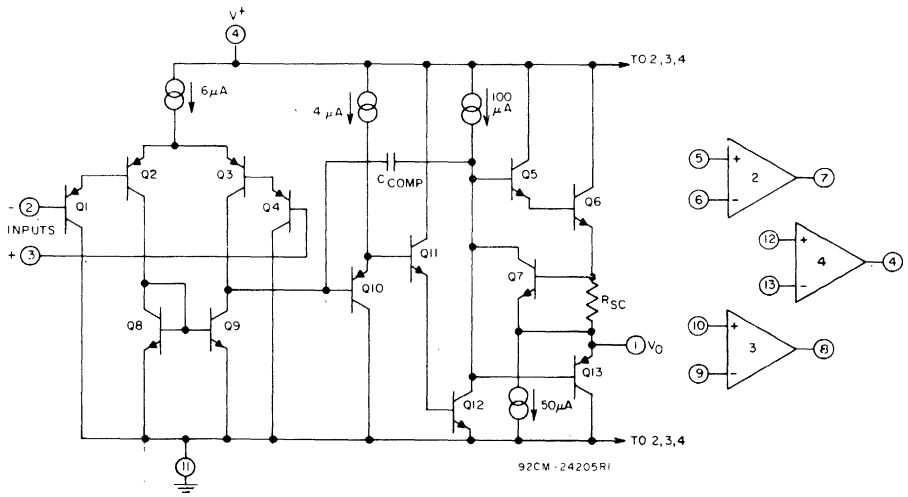


Fig. 2—Schematic diagram—one of four operational amplifiers.

CA124, CA224, CA324 Types

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA124 LIMITS			CA224, CA324 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	Min.	Typ.	Max.	
	T_A = 25°C							
Input Offset Voltage, V_{IO}	Note 3	–	2	5	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	V^+–1.5	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	–	–120	–	dB
		T_A = –55 to +125°C			T_A = -40 to +85°C (CA224), T_A = 0 to 70°C (CA324)			
Input Offset Voltage, V_{IO}	Note 3	–	–	7	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	–	–	500	nA
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.8	2	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	26	–	–	V
	R_L=10 kΩ	27	28	–	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

CA124, CA224, CA324 Types

TYPICAL CHARACTERISTICS CURVES

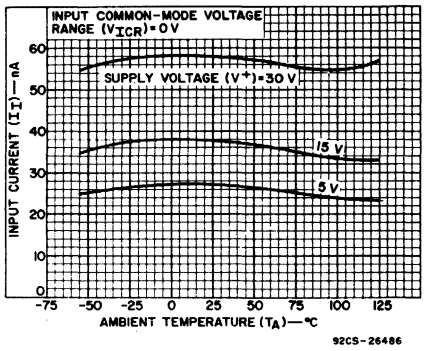


Fig. 3—Input current vs. ambient temperature.

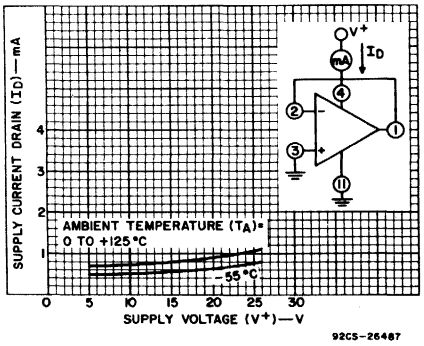


Fig. 4—Supply current drain vs. supply voltage.

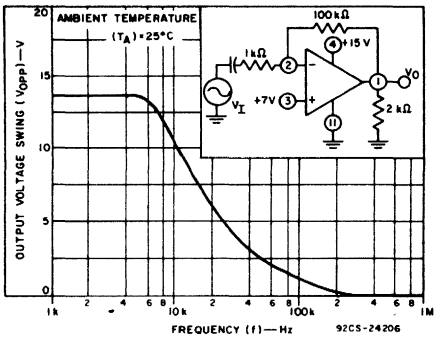


Fig. 5—Large-signal frequency response.

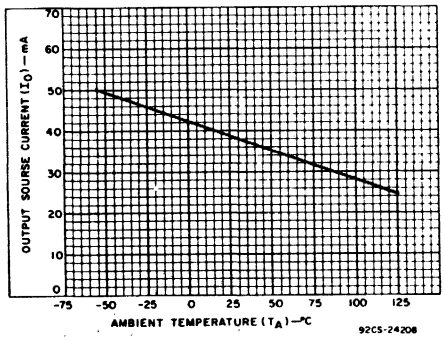


Fig. 6—Output current vs. ambient temperature.

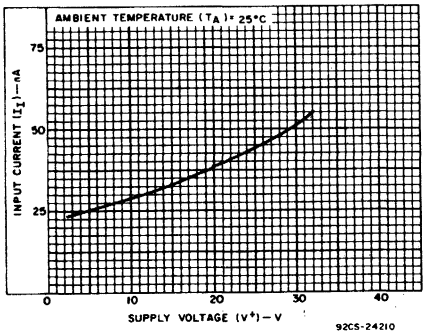


Fig. 7—Input current vs. supply voltage.

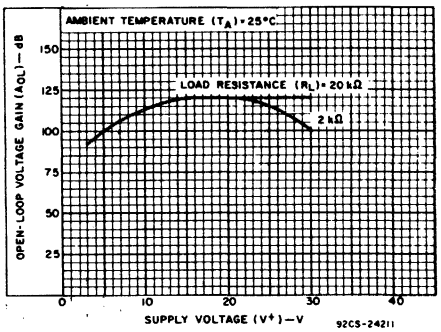


Fig. 8—Voltage gain vs. supply voltage.

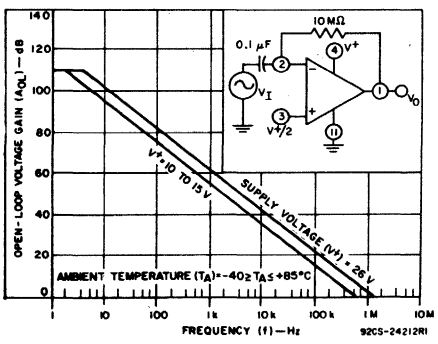


Fig. 9—Open-loop frequency response.

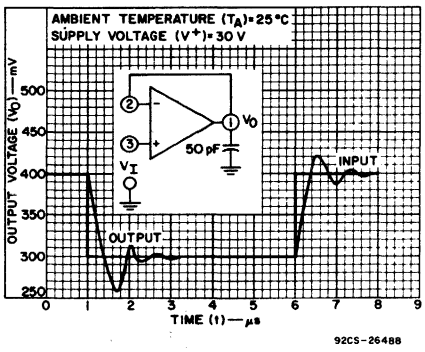


Fig. 10—Voltage follower pulse response (small signal).

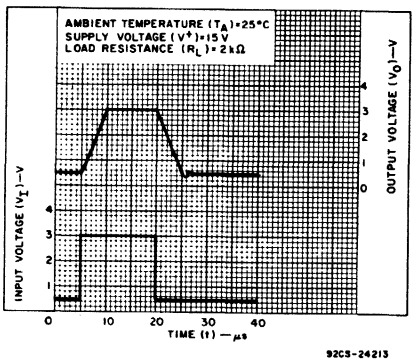


Fig. 11—Voltage follower pulse response.

CA139, CA239, CA339 Types
Quad Voltage Comparators

For Industrial, Commercial, and Military Applications

The RCA-CA139, -CA239, -CA339, -CA139A, -CA239A, and -CA339A types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input-offset-voltage characteristic. These devices are supplied in a 14-lead dual-in-line plastic package (E suffix), or in a 14-lead dual-in-line plastic package with a hermetic chip (G suffix), to provide true hermetic performance. The CA339 is also available in chip form (H suffix), and as a hermetic chip (HG suffix).

"E" Suffix Types: Standard Dual-In-Line Plastic Package
"G" Suffix Types: Hermetic Gold-Chip Dual-In-Line Plastic Package

Features:

- **Operation from single or dual supplies**
- **Common-mode input-voltage range to ground**
- **Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS**
- **Differential input-voltage range equal to the supply voltage**
- **Maximum input-offset voltage (V_{IO}):**
  CA139A, CA239A, CA339A – 2 mV
  CA139, CA239, CA339 – 5 mV
- **Replacement for industry types 139, 239 339, 139A, 239A, and 339A**

Applications:

- **Square-wave generators**
- **Time-delay generators**
- **Pulse generators**
- **Multivibrators**
- **High-voltage digital logic gates**
- **A/D converters**
- **MOS clock timers**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	–0.3 V to +36 V
INPUT CURRENT ($V_I < -0.3$ V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲ (Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–55 to +125°C
Storage	–65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

* Inputs must not go more negative than –0.3 V.

▲Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.

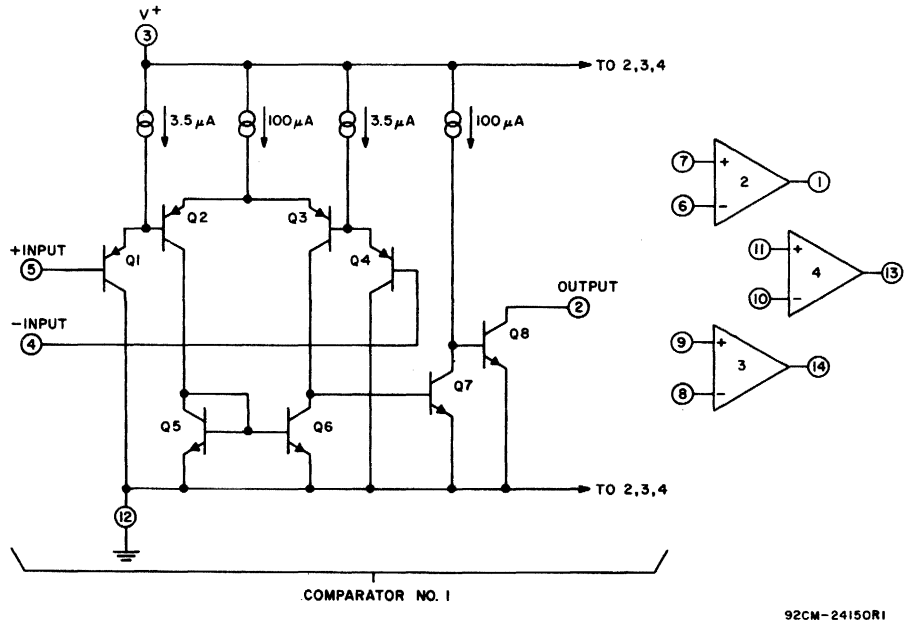


Fig. 1 –Schematic diagram.

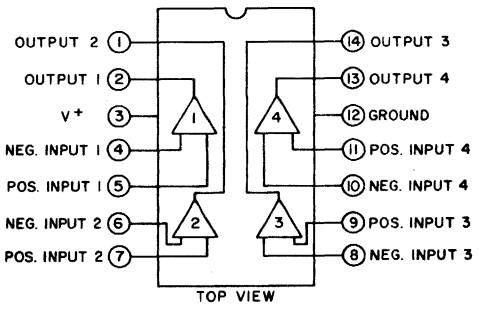


Fig. 2 –Functional diagram.

TYPICAL CHARACTERISTICS

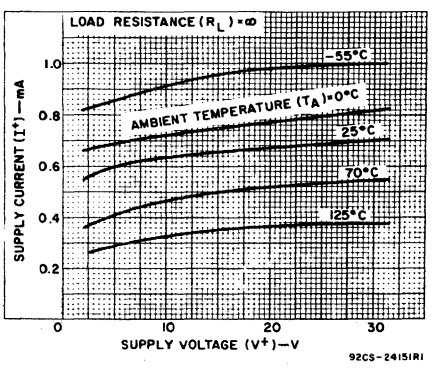


Fig. 3–Supply current vs. supply voltage.

CA139, CA239, CA339 Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V^+ = 5$ V, Unless otherwise indicated		LIMITS CA139 Min.	CA139 Typ.	CA139 Max.	CA139A Min.	CA139A Typ.	CA139A Max.	UNITS
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, R_S = 0	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	V_I^- = 1 V, V_I^+ = 0 V, I_{SINK} ≤ 4 mA	25°C	–	250	500	–	250	500	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO}) CA139, CA139A	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
CA239, CA239A CA339, CA339A			–	5	50	–	5	50	
CA139, CA139A		Note 1	–	–	100	–	–	100	
CA239, CA239A CA339, CA339A			–	–	150	–	–	150	
Input Bias Current (I_{IB}) CA139, CA139A	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
CA239, CA239A CA339, CA339A			–	25	250	–	25	250	
CA139, CA139A		Note 1	–	–	300	–	–	300	
CA239, CA239A CA339, CA339A			–	–	400	–	–	400	
Supply Current (I^+)	R_L = ∞ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	V_I^+ ≥1 V, V_I^- = 0, V_O = 5 V	25°C	–	0.1	–	–	0.1	–	nA
	V_I^+ ≥1 V, V_I^- = 0, V_O = 30 V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	V_I^- ≥1 V, V_I^+ = 0, V_O ≤+1.5 V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	R_L ≥15 kΩ, V^+=15 V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139, CA139A (−55 to +125°C) | CA239, CA239A (−25 to +85°C) | CA339, CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) − 1.5 V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS (Cont'd)

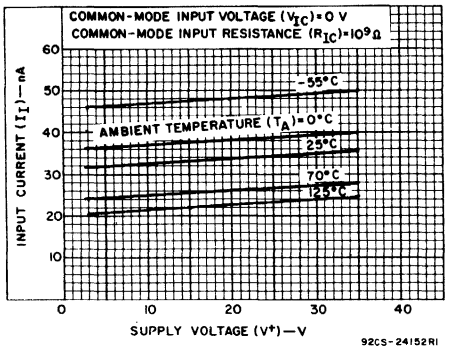


Fig. 4—Input current vs. supply voltage.

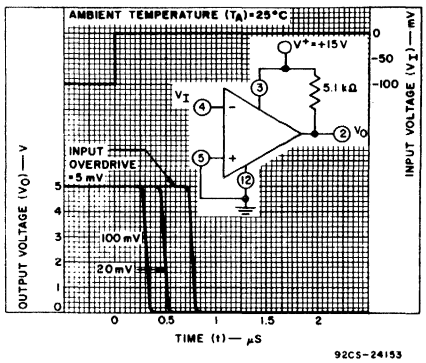


Fig. 5—Response time for various input overdrives—negative transition.

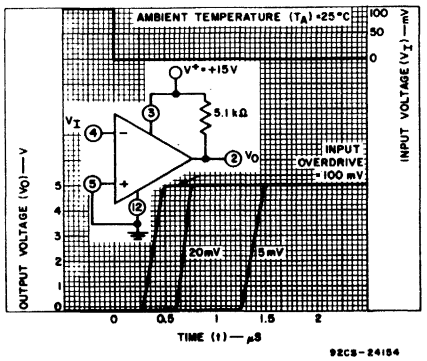


Fig. 6—Response time for various input overdrives—positive transition.

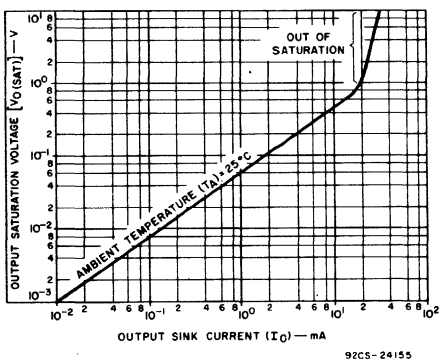


Fig. 7—Output saturation voltage vs. output sink current.

CA270 Types

TV Synchronous Demodulators

For Color and Black-and White TV Systems

The RCA-CA270AW, CA270BW, and CA-270CW are integrated circuits which perform the functions of synchronous detection of the TV if, video amplification and buffering, and noise inversion on dual-polarity waveforms. These devices also offer agc and afc facilities for use with n-p-n transistor if amplifiers and tuners. Both positive and negative polarities of video output are available. This feature provides great flexibility by permitting the designer to use either output for deriving the video and sound channels.

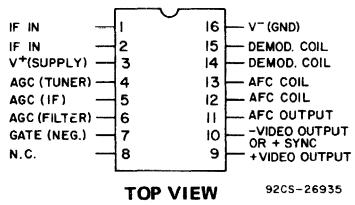
The RCA-CA270 series is pin-compatible and electrically similar to the industry series TCA270, but incorporates several improved features. In particular, improved white noise inversion and sync inversion systems force overshoots in the video waveform to be returned to accurately defined potentials. This design effectively removes dependence on both the degree of overshoot and temperature variations. In addition, reduced current consumption assures lower over-all power dissipation, thereby improving reliability.

The three types are electrically identical in most parameters. The CA270B has the most stringent limits on white level, video inversion, and afc dc offset. The CA270C has the least stringent limits on white level and video inversion, and no afc limits.

The CA270 series is supplied in a 16-lead staggered quad-in-line plastic package ("W" suffix).

Features:

- **Synchronous detector with single tuned coil**
- **Provides rf and if agc (forward)**
- **Tuner afc available with single quadrature coil**
- **Dual-polarity noise inverters**
- **Video amplifier**
- **Positive- and negative-polarity buffered video**
- **Differential if input**
- **Optional use of gating pulse**
- **Low-voltage, single-polarity power supply**



Terminal assignment.

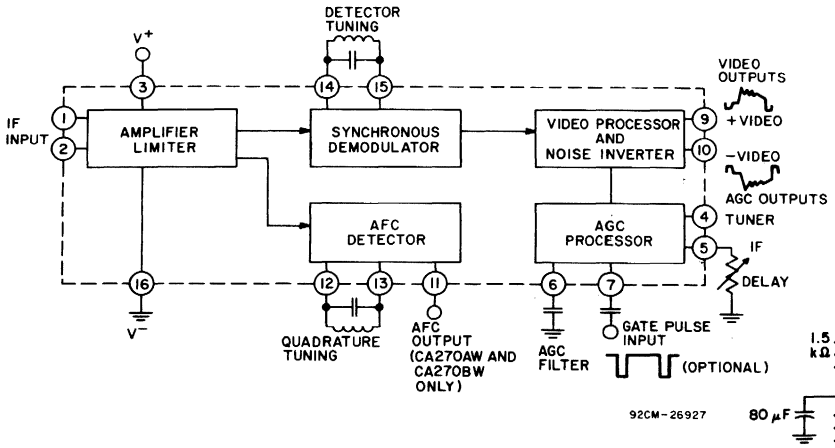


Fig. 1—Functional block diagram of CA270AW, CA270BW, and CA270CW TV synchronous demodulator.

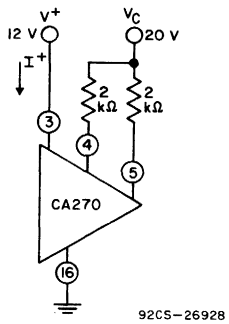


Fig. 2—Supply-current test circuit.

MAXIMUM RATINGS,
Absolute-Maximum Values at T_A=25°C:

DC SUPPLY VOLTAGE (Between Terminals 3 and 16 for 10 s max., with current limited to 100 mA) ..... 18 V

DEVICE DISSIPATION:
Up to T_A = 55°C ..... 750 mW
Above T_A = 55°C ... derate linearly 7.9 mW/°C

OPERATING TEMPERATURE RANGE ..... −40 to +55°C

STORAGE TEMPERATURE RANGE .....−65 to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

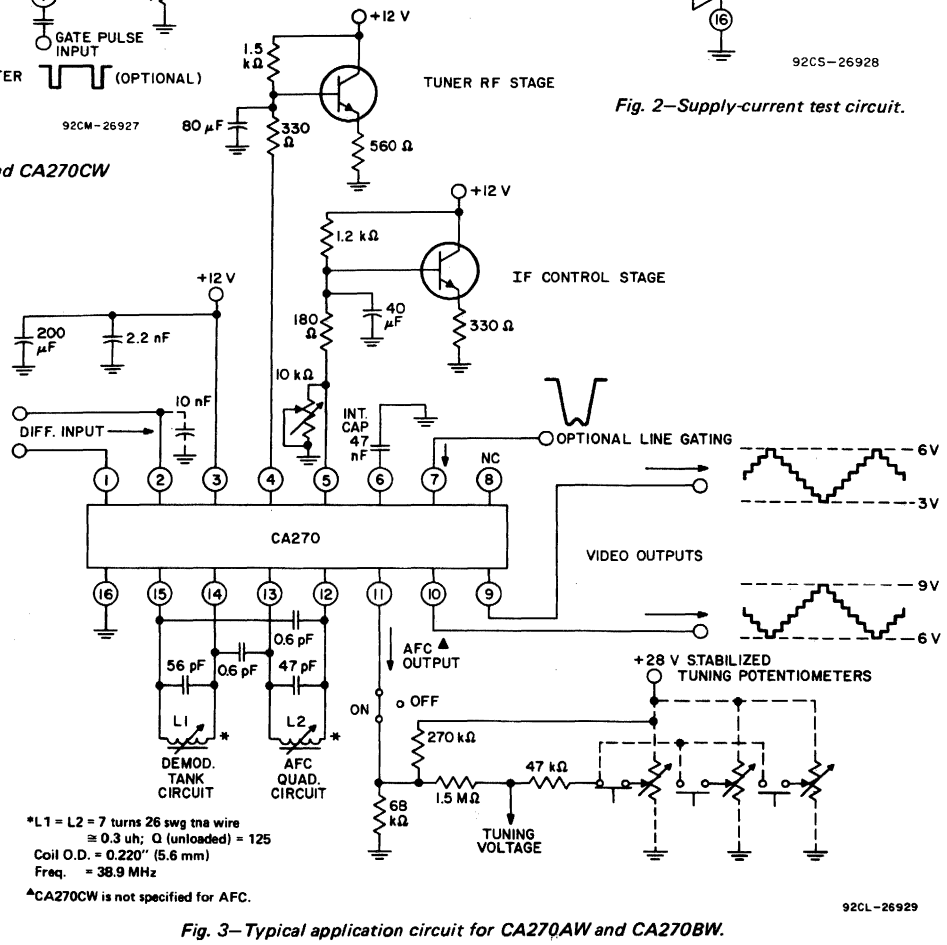


Fig. 3—Typical application circuit for CA270AW and CA270BW.

CA270 Types

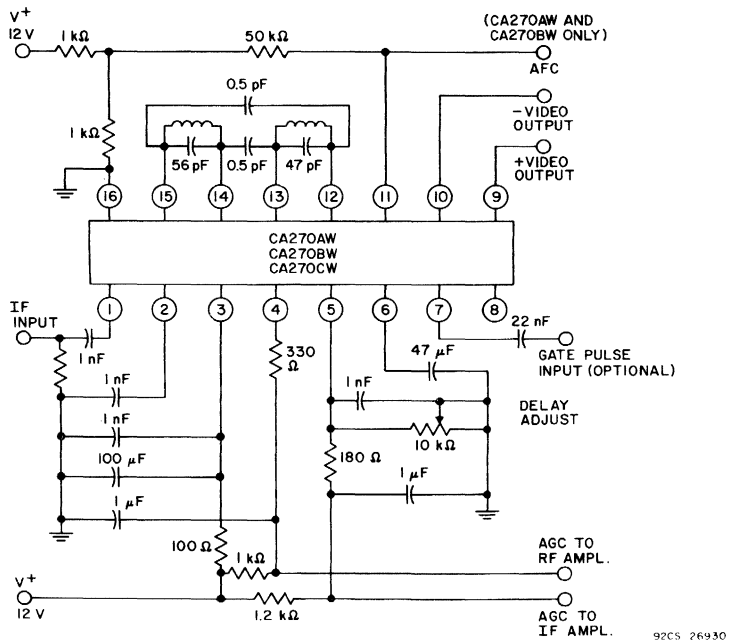


Fig. 4—Test circuit for CA270AW, CA270BW, and CA270CW.

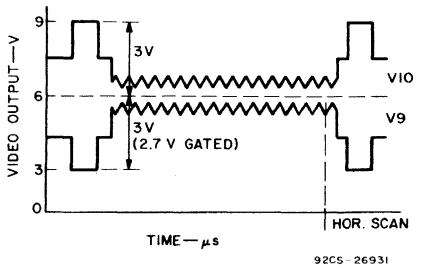


Fig. 5—Typical waveforms for video outputs.

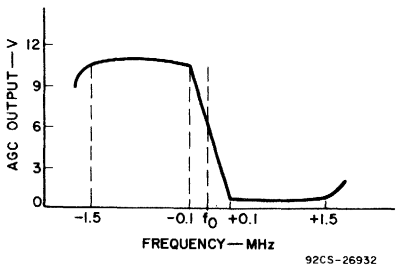


Fig. 6—Typical AFC characteristic.

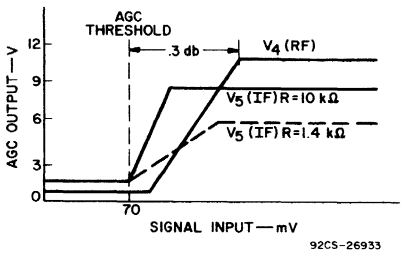


Fig. 7—Typical AGC characteristics.

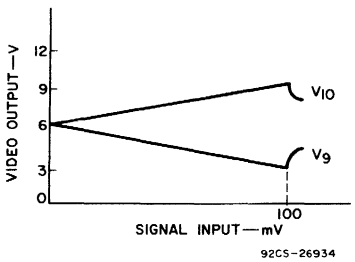


Fig. 8—Typical transfer characteristics.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 12 V, and Referenced to Test Circuit (Fig. 4).

CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage, V^+	V^+=12 V		10.2	12	13.8	V
Supply Current, I^+ (See Fig. 2)	V^+=12 V		22	40	56	mA
Video Characteristics: DC Output Voltage, Term.9 (See Fig. 5)	Zero Signal	CA270AW CA270BW CA270CW	5.7 5.8 5.5	6 6 6	6.3 6.2 6.5	V
DC Output Voltage, Term.10 (See Fig. 5)	Zero Signal	CA270AW CA270BW CA270CW	5.6 5.7 5.5	6 6 6	6.4 6.3 6.5	V
Sync Tip Output Voltage, Term.9	Output=AGC threshold (non-gated)		–	3	–	V
AC Input Voltage, Terms.1,2	Input for output= AGC threshold		50	70	100	mV
Input Res.,Term.1			–	3.3	–	KΩ
Input Res., Term.2			–	3.3	–	KΩ
Video Bandwidth, Term.9	At output = –3 dB		–	5	–	MHz
Differential Gain	See Note 1		–	–	10	%
Differential Phase	See Note 1		–	–	10	deg
Intermod. Products: Beat Freq.,1.6 MHz Beat Freq.,2.8 MHz	See Note 1 (95% sat. blue colour bar)		– –	– –	–60 –67	dB dB
Rejection at Carrier Freq., Terms.9,10,11	F=Video Carrier;V_{IN} for Term.9(dc)=3.7V		–40	–	–	dB
Rejection,Twice Carrier Freq.,Terms.9,10,11	F=2X Video Carrier; V_{IN} for Term.9(dc) =3.7 V		–40	–	–	dB
AGC Characteristics: Sat.Voltage, Term.4	Zero Sig.; I_4 = 10 mA		–	–	0.3	V
Sat. Voltage, Term.5	Zero Sig.; I_5 = 10 mA		0.7	–	1.2	V

CA270 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 12 V, (Cont'd) and Referenced to Test Circuit (Fig. 4).

CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Breakdown Voltage, Terms. 4,5	I_4 or I_5=1 mA (sink)		14	–	–	V
Control Current, Terms. 4,5			10	–	–	mA
Current Ratio I_4/I_5	I_5 = 1 mA		6	–	–	
Input Signal Increase with resp. to AGC Threshold (See Fig.7)	AGC from threshold to max.		–	–	0.5	dB
AGC Gating Pulse Input, Term. 7 (optional)	Pulse voltage=$V^+$to 0; See Note 2		2	–	V^+	V
Input Res.,Term.7			–	1.8	–	KΩ
AFC Characteristics: (See Fig. 6) Output Voltage, Term. 11	f = f_o ± 0.2 MHz	CA270AW CA270BW CA270CW	10 10 –	– – –	– – –	V_{p-p}
Output Voltage, Term. 11	f = f_o ± 1.2 MHz	CA270AW CA270BW CA270CW	10 10 –	– – –	– – –	V_{p-p}
DC Offset Voltage, Term. 11	Zero Sig.; measured across R_L = 50 KΩ to +6 V	CA270AW CA270BW CA270CW	–1.7 –1 –	– – –	1.7 1 –	V
Noise Inverter Characteristics: Inversion Threshold, Term. 9	Positive noise pulses		–	6.6	–	V
Inversion Threshold, Term. 9	Negative noise pulses		–	2.2	–	V
Noise Inversion Sensitivity,Term. 9	Signal inversion threshold for complete inversion		–	10	–	mV
Video Inversion Characteristics: Video Inversion, Term. 9 (at low carrier levels)	Carrier increase from 0 to 5 mV (appx.8% carrier)	CA270AW CA270BW CA270CW	– – –	– – –	0.2 0.1 0.3	V

Note 1: CCIR modulation system, peak white = 10% carrier.
Note 2: Maximum pulse amplitude must never exceed the supply voltage (V^+).

APPLICATIONS

The diagram shown in Fig. 3 is typical of the type of circuit used in a practical application of the CA270 series devices.

Video Detector

The if input signal may be applied push-pull to terminals 1 and 2, or single-ended to either terminal 1 as shown, or to terminal 2. These input terminals are internally biased.

The detector tank circuit can be tuned by applying a 50 mV cw signal of video if frequency to the input and adjusting the inductor L1 for maximum differential output between terminals 9 and 10. The input signal is then reduced to 25 mV and L1 is readjusted for maximum output.

AFC Detector

The afc quadrature tank circuit should be tuned only after the detector adjustment has been made. Using the same input signal, inductor L2 should be adjusted for 6 V dc output at terminal 11. The 0.5-pF quadrature phase-shift coupling capacitors can affect symmetry and actual values will depend on the layout used. When L1 and L2 are properly tuned, the output swing at terminal 11 will be 10 volts minimum for frequencies of ±0.2 MHz to ±1.2 MHz about the if carrier frequency.

AGC Detector

The agc threshold, corresponding to sync tip level, is approximately 3 volts at terminal 9. Full agc potential will be developed if the input signal increases by 0.5 dB maximum with respect to the threshold value. The agc control at terminal 4 is intended for tuner control. The agc control at terminal 5 is for forward agc control of n-p-n transistors in the if amplifier. When sinking 10 mA, the zero-signal agc voltage at terminal 4 is 0.3 volt maximum; at terminal 5, it is 1.2 volts maximum.

The design of the device is such that the sink current at terminal 4 is a minimum of 6 times that at terminal 5. The rf agc sink current begins to decrease when the if sink current is about one-sixth of that required to saturate the rf agc output at terminal 4. The rf agc delay may be adjusted by means of a variable resistor between terminal 5 and ground. This adjustment modifies the if system gain, thus affecting the rf delay threshold. At maximum gain the current into terminal 5 is large compared to the current in the variable resistor and adjustment is ineffective. As the signal increases and rf agc is applied, the terminal 5 sink current approaches zero and the if agc is determined by the value of the variable resistor.

A horizontal gating pulse may be applied to terminal 7 to gate the agc detector. The agc threshold (sync tip) decreases approximately 0.3 volt at terminal 9 when gating is used. The gating pulses must be negative-going with a recommended minimum amplitude of 3 volts. They may be ac or dc coupled, but the maximum peak value must not exceed the dc supply voltage at terminal 3. If dc coupling is used, the potential during flyback should be less than 0.5 volt and during scan, greater than 1.5 volts.

Noise Inverter

Noise pulses in excess of 6.6 volts at terminal 9, which would result in "white spots", are processed in the device by inverting and clamping them to near black level (approx. 3.6 V). Noise pulses at levels of less than 2.2 volts at terminal 9 which would result in sync noise interference, are inverted and returned to black level.

Complete inversion occurs for signals 10 mV above the inversion threshold.

CA555, CA555C Types

Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in hermetic IC Gold-CHIP 8-lead dual-in-line plastic packages (G Suffix), standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacements for industry types in packages with similar terminal arrangements e.g.SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . .	18	V
DEVICE DISSIPATION:		
Up to T_A = 55°C	600	mW
Above T_A = 55°C Derate linearly	5	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating		
CA555	−55 to +125	°C
CA555C	0 to 70	°C▲
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. . . .	+265	°C

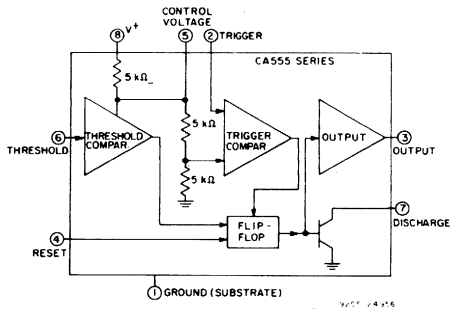


Fig. 1 – Functional diagram of the CA555 series.

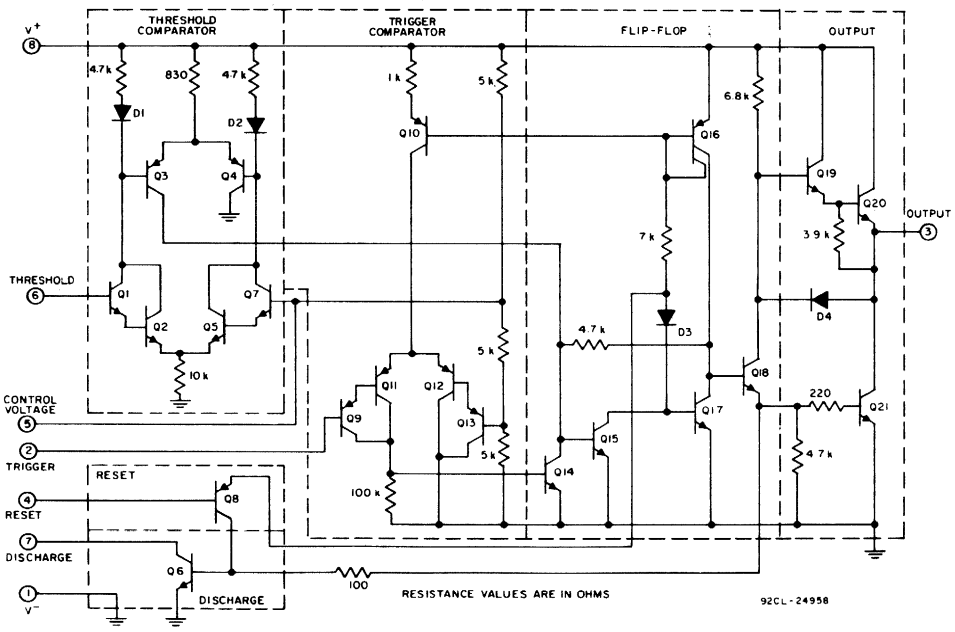


Fig. 2 – Schematic diagram of the CA555 and CA555C.

▲The CA555E, S, J, and T can be operated over the temperature range of −55°C to +125°C although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

CA555G, CA555CG:

Hermetic Gold-CHIP 8-Lead Dual-In-Line Plastic Package (MINI-DIP)

CA555T, CA555CT:

Standard 8-Lead TO-5 Style Package

CA555S, CA555CS:

Standard 8-Lead TO-5 Style Package With Formed Leads (DIL-CAN)

CA555E, CA555CE:

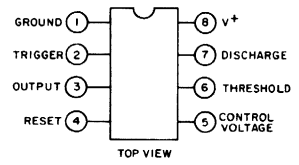
8-Lead Dual-In-Line Plastic Package (MINI-DIP)

Features:

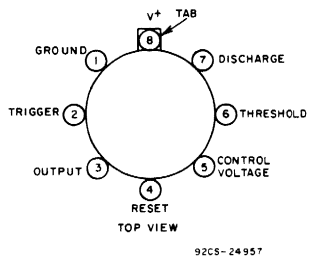
- **Accurate timing from microseconds through hours**
- **Astable and monostable operation**
- **Adjustable duty cycle**
- **Output capable of sourcing or sinking up to 200 mA**
- **Output capable of driving TTL devices**
- **Normally ON and OFF outputs**
- **High-temperature stability −0.005%/°C**
- **Directly interchangeable with SE555, NE555, MC1555, and MC1455**

Applications:

- **Precision timing**
- **Sequential timing**
- **Time-delay generation**
- **Pulse generation**
- **Pulse-width and position modulation**
- **Pulse detector**



a. MINI-DIP plastic package TO-5 style package with formed leads



b. TO-5 style package

Fig. 3 – Terminal assignment diagrams.

CA555, CA555C Types

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	(2/3)V^+	–	–	(2/3)V^+	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	V
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	R_1, R_2 = 1 to 100 kΩ, C = 0.1 μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/°C
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

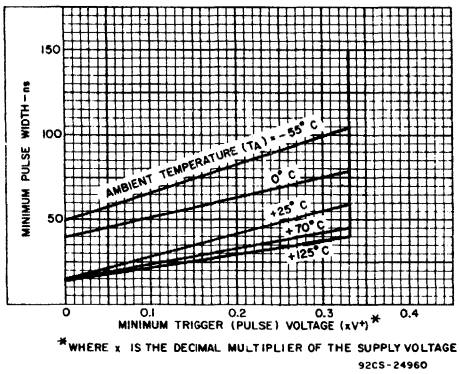


Fig. 4 – Minimum pulse width vs. minimum trigger voltage.

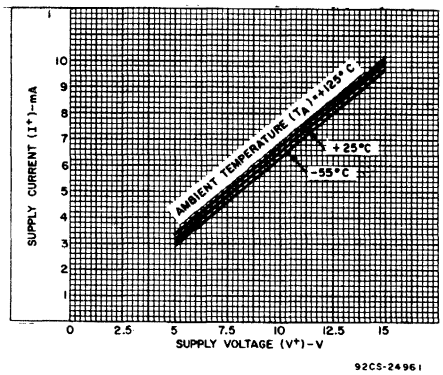


Fig. 5 – Supply current vs. supply voltage.

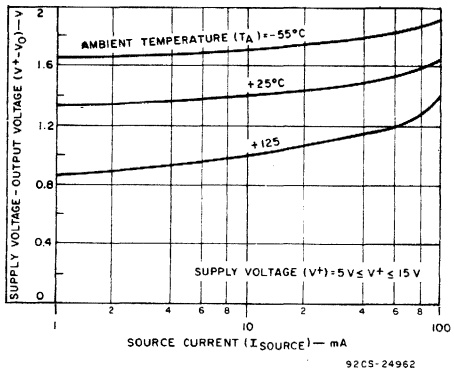


Fig. 6 – Output voltage drop (high state) vs. source current.

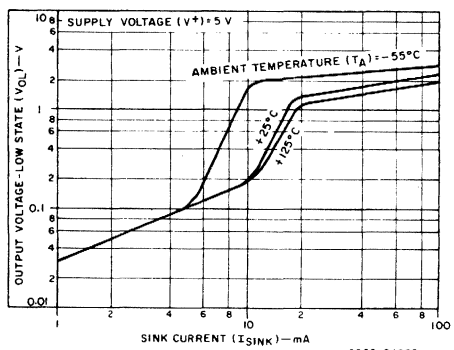


Fig.7 – Output voltage-low state vs. sink current at $V^+ = 5$ V.

CA555, CA555C Types

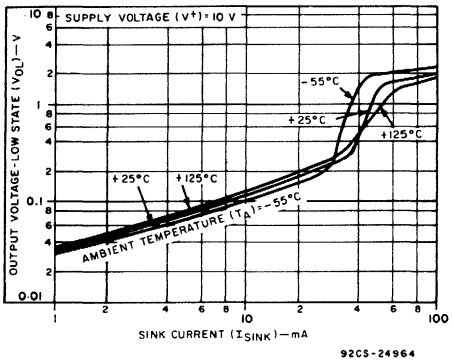


Fig.8 — Output voltage-low state vs. sink current at $V^+ = 10$ V.

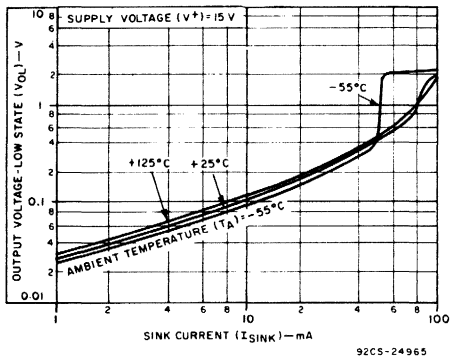


Fig.9 — Output voltage-low state vs. sink current at $V^+ = 15$ V.

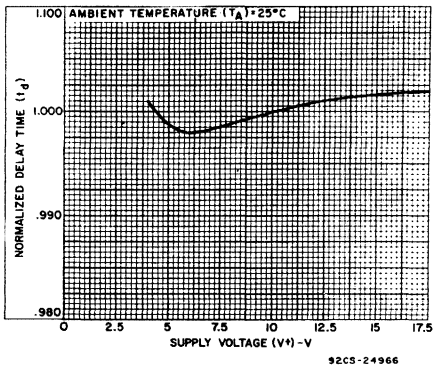


Fig.10 — Delay time vs. supply voltage.

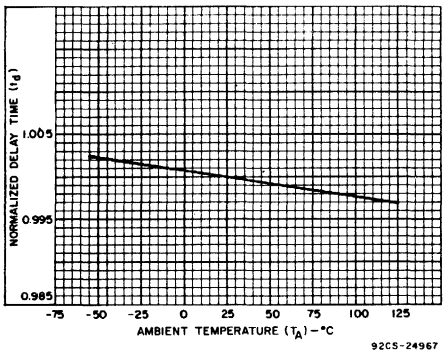


Fig.11 — Delay time vs. temperature.

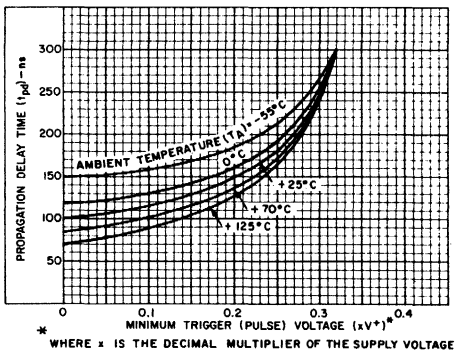


Fig.12 — Propagation delay time vs. trigger voltage.

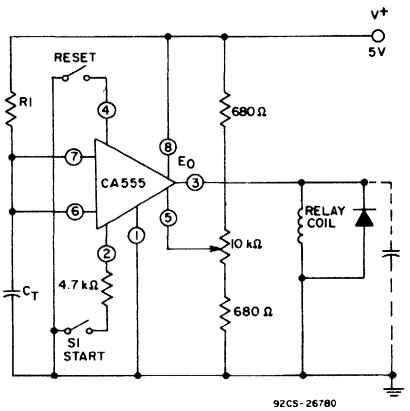


Fig.13 — Reset timer (monostable operation).

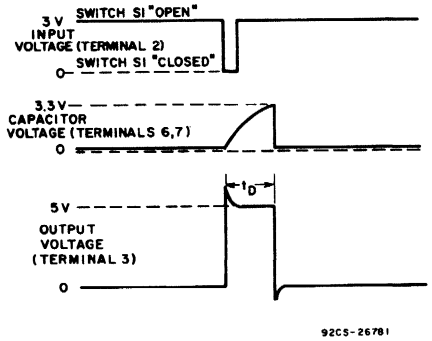


Fig.14 — Typical waveforms for reset timer.

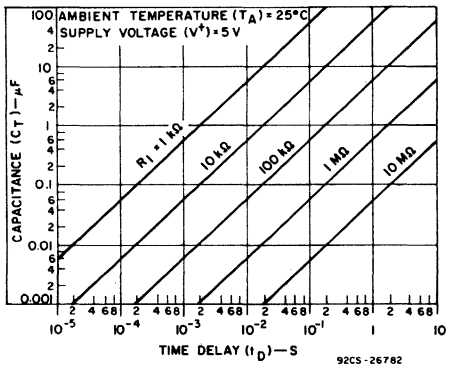


Fig.15 — Time delay vs. resistance and capacitance.

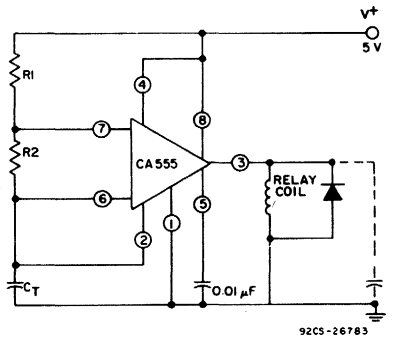


Fig.16 — Repeat cycle timer (astable operation).

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;

$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

where $t_1 = 0.693(R_1 + R_2)\,C_T$

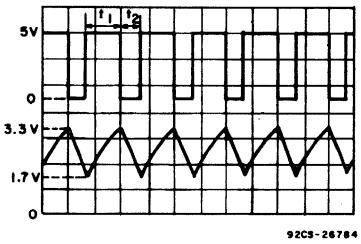
and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.

CA555, CA555C Types



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig. 17 – Typical waveforms for repeat cycle timer.

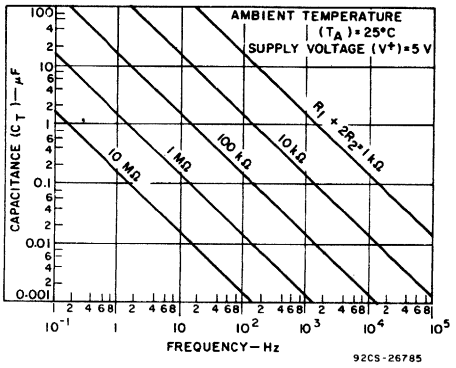


Fig. 18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

CA723 Types

Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Output Currents up to 150 mA Without External Pass Transistors

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style ceramic package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of −55°C to +125°C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE: Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:

Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT Derate linearly	6.3	mW/°C
CA723E, CA723CE Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering): At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

Features:

- Up to 150 mA output current
- Positive and negative voltage regulation
- Regulation in excess of 10A with suitable pass transistors
- Input and output short-circuit protection
- Load and line regulation: 0.03%
- Direct replacement for 723 and 723C industry types
- Adjustable output voltage: 2 to 37 V

Applications:

- Series and shunt voltage regulator
- Floating regulator
- Switching voltage regulator
- High-current voltage regulator
- Temperature controller

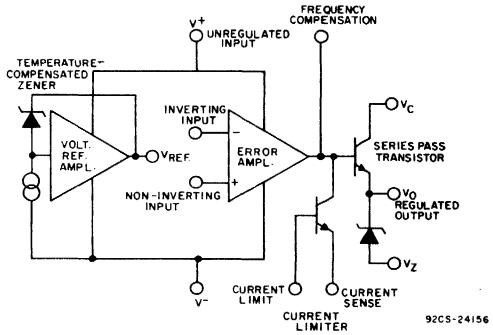


Fig. 1 – Functional diagram of the CA723 and CA723C.

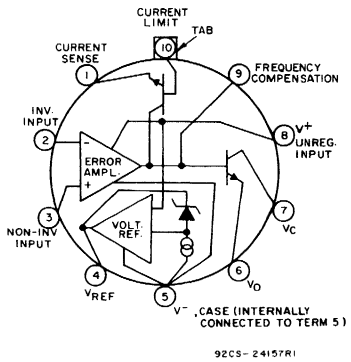


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

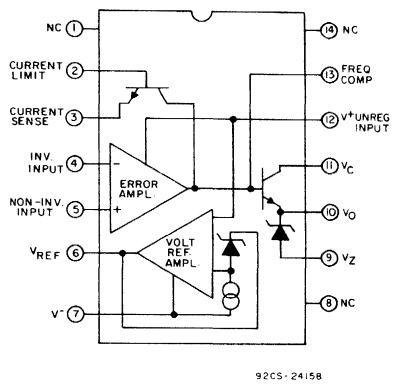


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

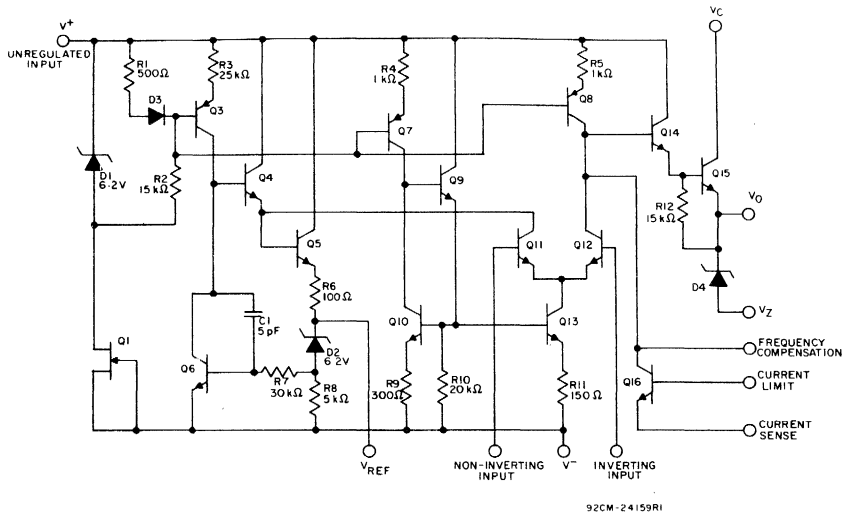


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

CA723 Types

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance R_1R_2 R_1+R_2 at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I-V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = O to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, $\triangle V_O$	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

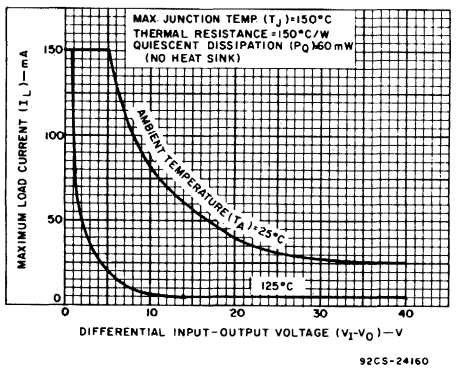


Fig. 5 – Max. load current vs differential input-output voltage.

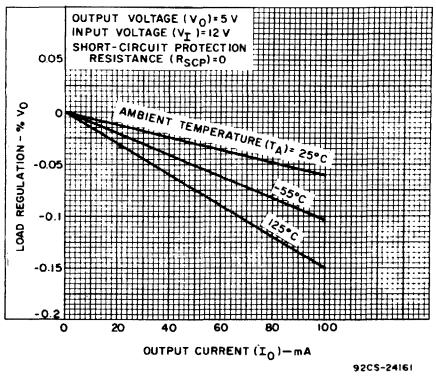


Fig. 6 – Load regulation without current limiting.

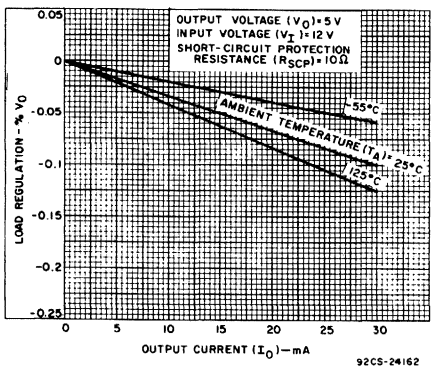


Fig. 7 – Load regulation with current limiting.

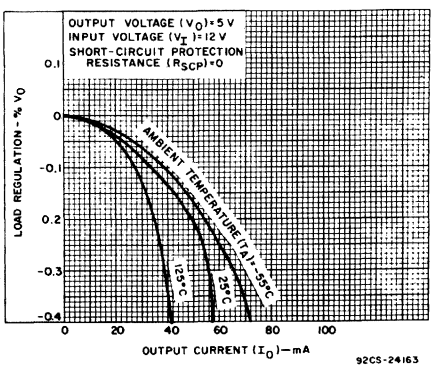


Fig. 8 – Load regulation with current limiting.

CA723 Types

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

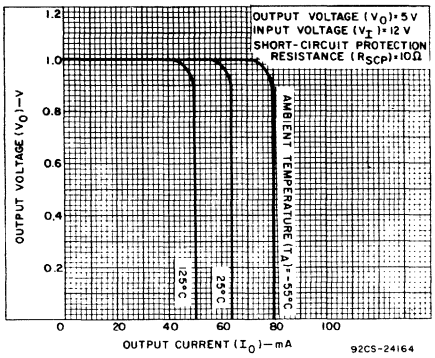


Fig. 9 — Current limiting characteristics.

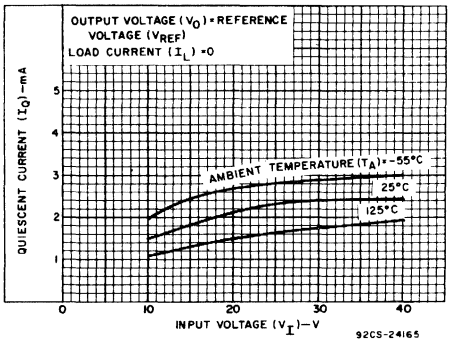


Fig. 10 — Quiescent current vs. input voltage.

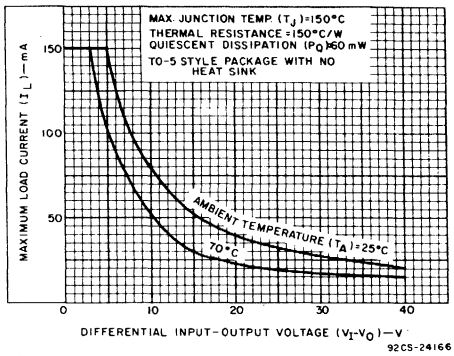


Fig. 11 — Max. load current vs differential input-output voltage CA723CT.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

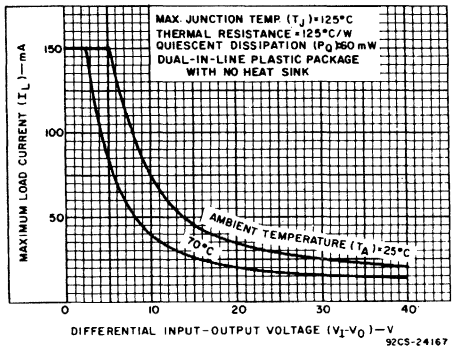


Fig. 12 — Max. load current vs differential input-output voltage for CA723CE.

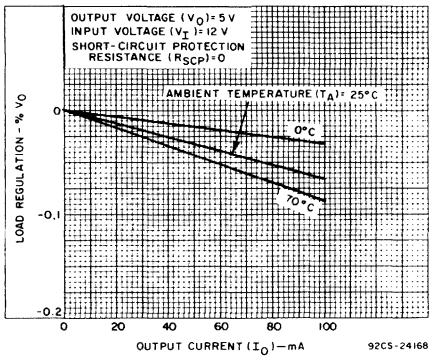


Fig. 13 — Load regulation without current limiting.

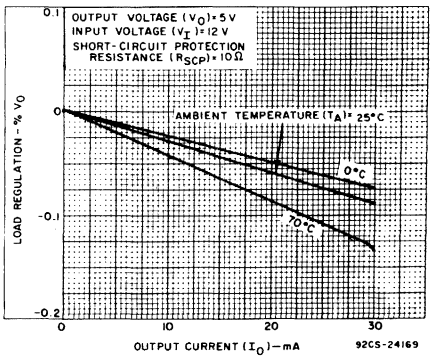


Fig. 14 — Load regulation with current limiting.

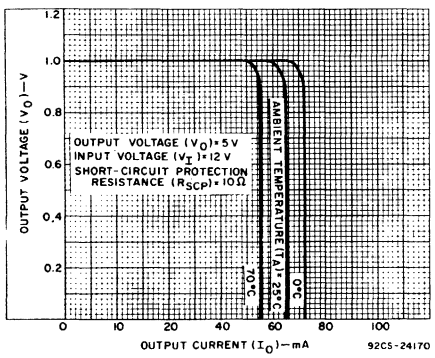


Fig. 15 — Current limiting characteristics.

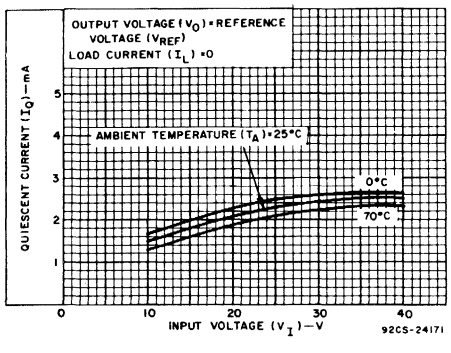


Fig. 16 — Quiescent current vs. input voltage.

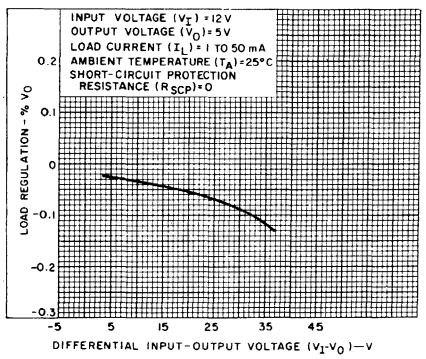


Fig. 17 — Load regulation vs. differential input-output voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

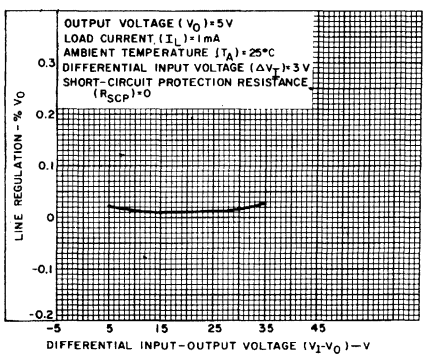


Fig. 18 — Line regulation vs. differential input-output voltage.

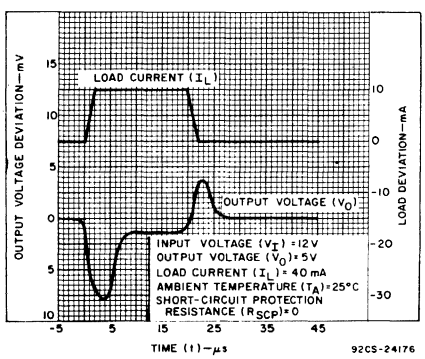


Fig. 19 — Line transient response.

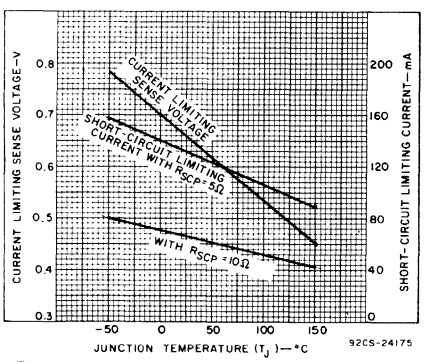


Fig. 20 — Current limiting characteristics vs. junction temperature.

CA723 Types

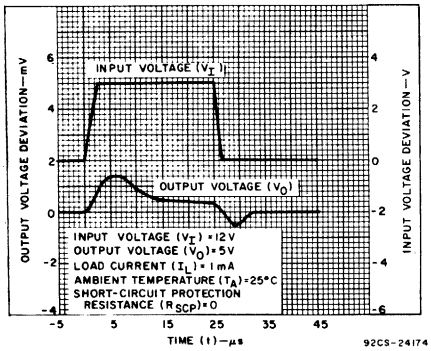


Fig. 21 — Load transient response.

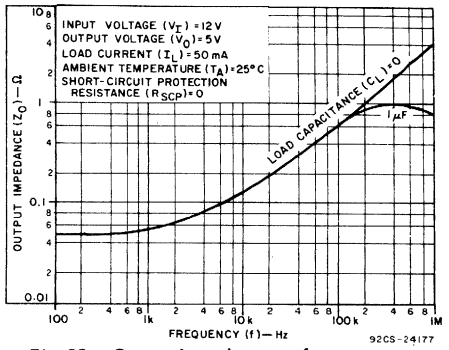
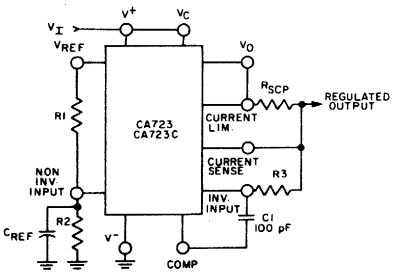


Fig. 22 — Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

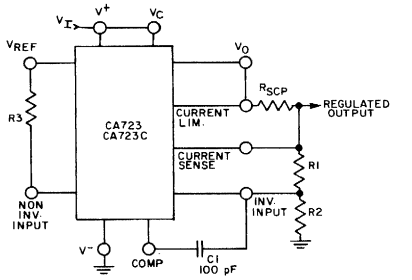


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

Fig. 23 — Low-voltage regulator circuit (V_O = 2 to 7 volts).



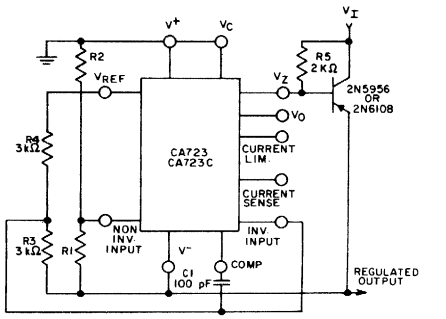
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	4.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

Fig. 24 — High-voltage regulator circuit (V_O = 7 to 37 volts).

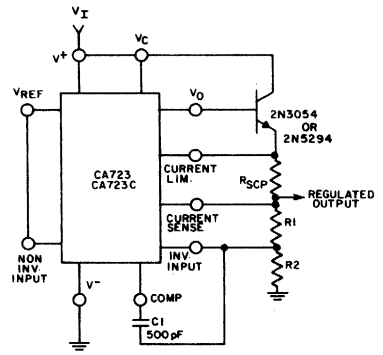


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA)	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

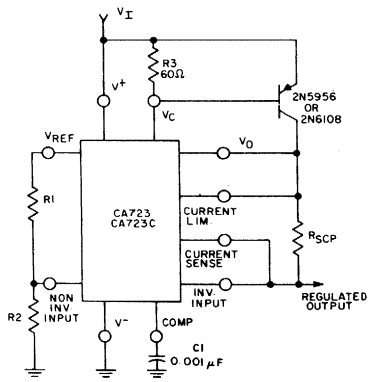
Fig. 25 — Negative-voltage regulator circuit.



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

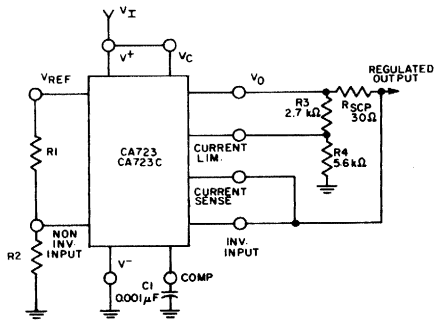
Fig. 26 — Positive-voltage-regulator circuit (with external n-p-n pass transistor).



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 1 A)	5 mV

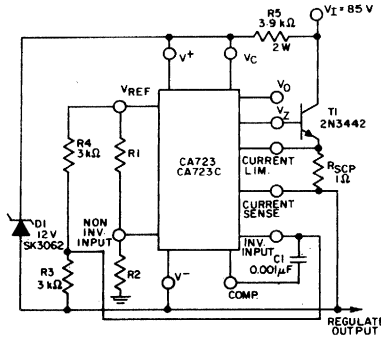
Fig. 27 — Positive voltage-regulator circuit (with external p-n-p pass transistor).



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 10 mA)	1 mV
SHORT-CIRCUIT CURRENT	20 mA

Fig. 28 — Foldback current-limiting circuit.



Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50 V
LINE REGULATION (ΔV_I = 20 V)	15 mV
LOAD REGULATION (ΔI_L = 50 mA)	20 mV

Fig. 29 — Positive-floating regulator circuit.

CA741, CA747, CA748, CA1458, CA1558 Types

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commercial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747CG, CA747E, CA747G (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

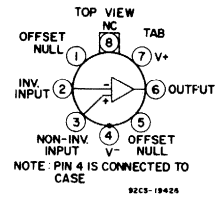
RCA's manufacturing process makes it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

Features:

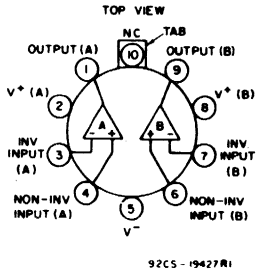
- **Input bias current (all types): 500 nA max.**
- **Input offset current (all types): 200 nA max.**

Applications:

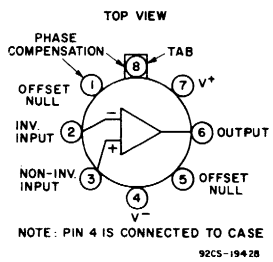
- **Comparator**
- **DC amplifier**
- **Integrator or differentiator**
- **Multivibrator**
- **Narrow-band or band-pass filter**
- **Summing amplifier**



1a.—CA741CS, CA741CT, CA741S, & CA741T with internal phase compensation.



1b.—CA747CT and CA747T with internal phase compensation.



1c.—CA748CS, CA748CT, CA748S, and CA748T with external phase compensation.

Fig. 1 — Functional diagrams.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC Supply Voltage (between V^+ and V^- terminals):	
CA741C, CA747C▲, CA748C, CA1458▲	36 V
CA741, CA747▲, CA748, CA1558▲	44 V
Differential Input Voltage	±30 V
DC Input Voltage*	±15 V
Output Short-Circuit Duration	Indefinite
Device Dissipation:	
Up to 70°C (CA741C, CA748C)	500 mW
Up to 75°C (CA741, CA748)	500 mW
Up to 30°C (CA747)	800 mW
Up to 25°C (CA747C)	800 mW
Up to 30°C (CA1558)	680 mW
Up to 25°C (CA1458)	680 mW
For Temperatures Indicated Above	Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE, CA747CG)	±0.5 V
Ambient Temperature Range:	
Operating – CA741, CA747E, CA748, CA1558	−55 to +125 °C
CA741C, CA747C, CA748C, CA1458	0 to +70 °C†
Storage	−65 to +150 °C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265 °C

* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

CA741, CA747, CA748, CA1458, CA1558 Types

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

Type No.	PACKAGE TYPE AND SUFFIX LETTER										FIG. No.
	TO-5 STYLE			PLASTIC		Gold-CHIP PLASTIC		CHIP	Gold-CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L	8L	14L				
CA1458	T		S	E		G		H	GH		1d, 1h
CA1558	T		S	E		G					1d, 1h
CA741C	T		S	E		G		H	GH		1a, 1e
CA741	T		S	E		G				L	1a, 1e
CA747C		T			E		G	H	GH		1b, 1f
CA747		T			E		G				1b, 1f
CA748C	T		S	E		G		H	GH		1c, 1g
CA748	T		S	E		G					1c, 1g

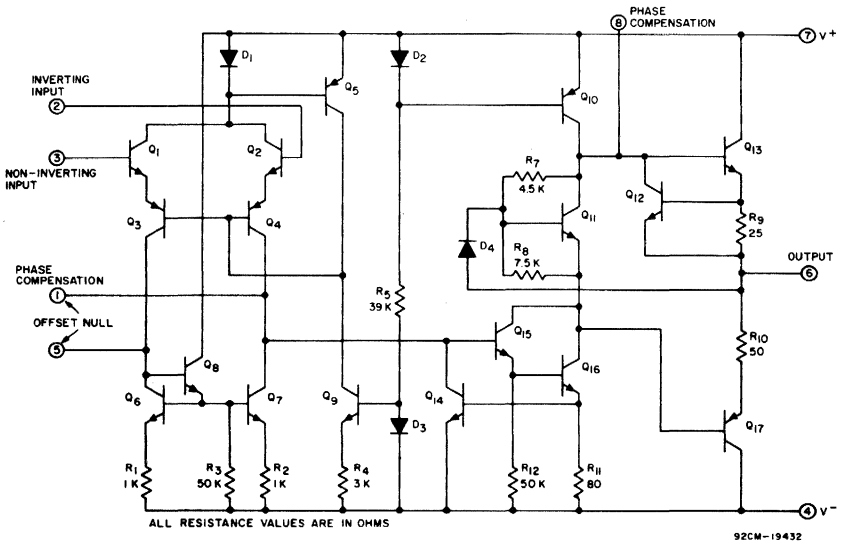
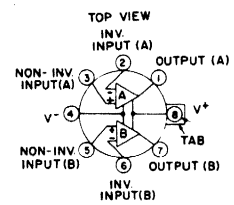
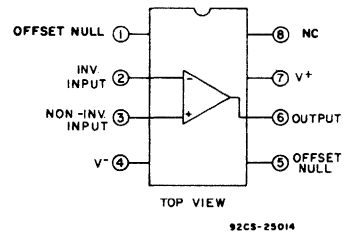


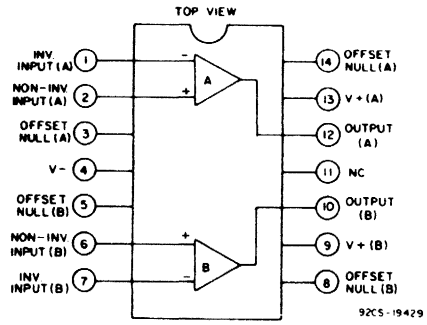
Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.



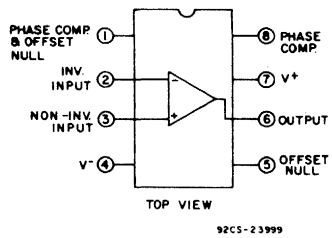
1d.—CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



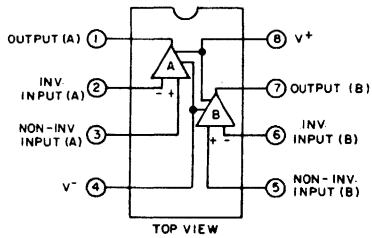
1e.—CA741CE,CA741CG,CA741E, and CA741G with internal phase compensation.



1f.—CA747CE,CA747CG,CA747E, and CA747G with internal phase compensation.



1g.—CA748CE,CA748CG,CA748E, and CA748G with external phase compensation.



1h.—CA1458E,CA1458G,CA1558E, and CA1558G with internal phase compensation.

Fig. 1 — Functional Diagrams (Cont'd)

CA741, CA747, CA748, CA1458, CA1558 Types

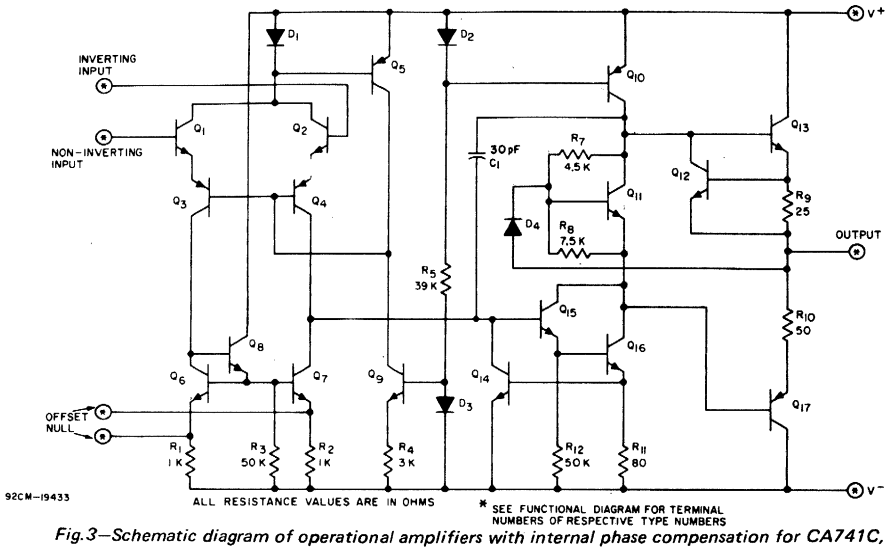


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

ELECTRICAL CHARACTERISTICS

For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

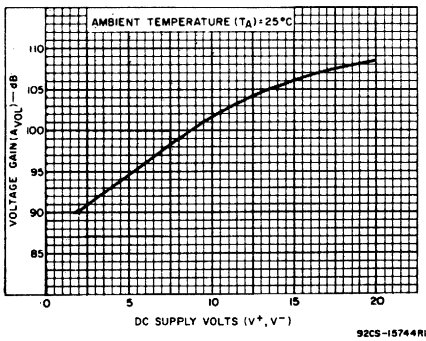


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

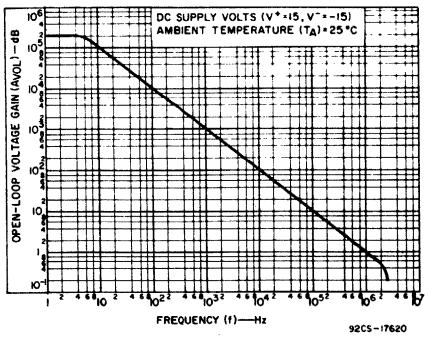


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

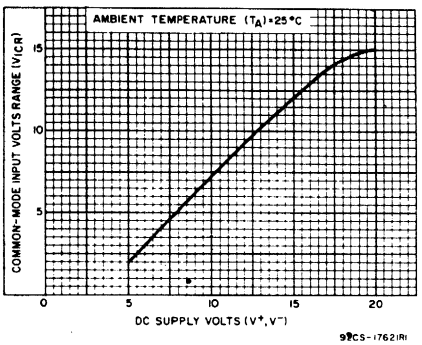


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

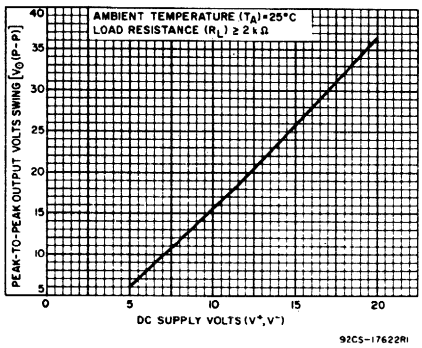


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

CA741, CA747, CA748, CA1458, CA1558 Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	25 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

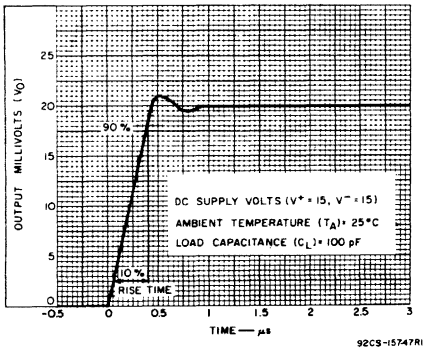


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

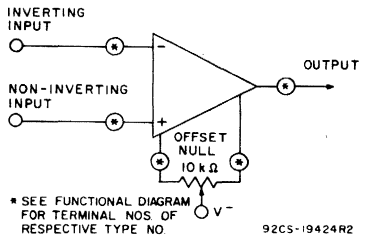


Fig.9—Voltage-offset null circuit for CA741C, CA741, CA747CE, CA747CG, CA747E, and CA747G.

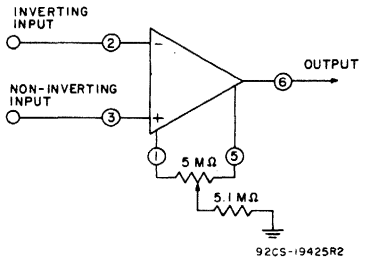


Fig.10—Voltage-offset null circuit for CA748C and CA748.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm = \pm 15$ V	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain $V_I = 20$ mV $R_L = 2\,k\Omega$ $C_L \leq 100$ pF	0.3	μs
Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq 2\,k\Omega$	0.5	V/μs
Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

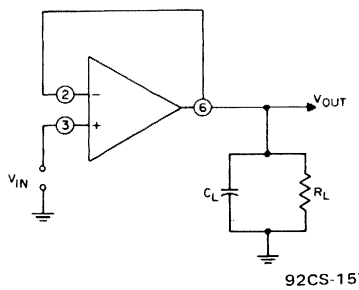


Fig.11—Transient response test circuit for all types.

CA758E

RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- **Low distortion (THD): 0.4% (typ.)**
- **Excellent SCA rejection: 70 dB typ.**
- **RC oscillator**
- **High-audio-channel separation: 45 dB**
- **Power supply range: 10 to 16 V dc**
- **Requires only one adjustment for complete alignment**
- **Low-impedance outputs**
- **Stereo indicator lamp drive: 150 mA typ.**

RCA-CA758E is a monolithic silicon integrated circuit RC phase-lock loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA758E is pin compatible and electrically equivalent to industry types μA758, MC1311P, LM1800, and ULX2244.

The CA758E decodes the multiplexed stereo input signal into left and right channel audio output signals. The decoder also suppresses SCA (storecast) transmissions when present in the composite stereo signal.

The decoder uses a minimum of external components, and requires one adjustment (oscillator frequency) for complete alignment. In addition, the CA758E provides automatic mono-stereo mode switching and energizes a stereo indicator lamp.

The CA758E is supplied in a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC Supply Voltage	+18 V
DC Supply Voltage (for ≤ a 15-second period)	+22 V
DC Voltage at Term. 7 (Lamp Driver Circuit with Lamp "OFF")	+22 V
Device Dissipation:	
Up to $T_A = 70^oC$	730 mW
Above $T_A = 70^oC$ derate linearly	9.1 mW/°C
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

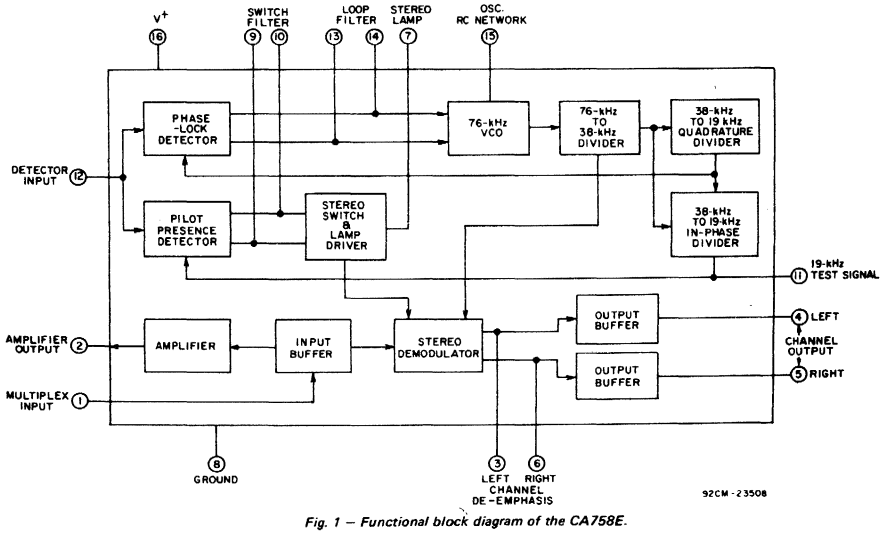


Fig. 1 – Functional block diagram of the CA758E.

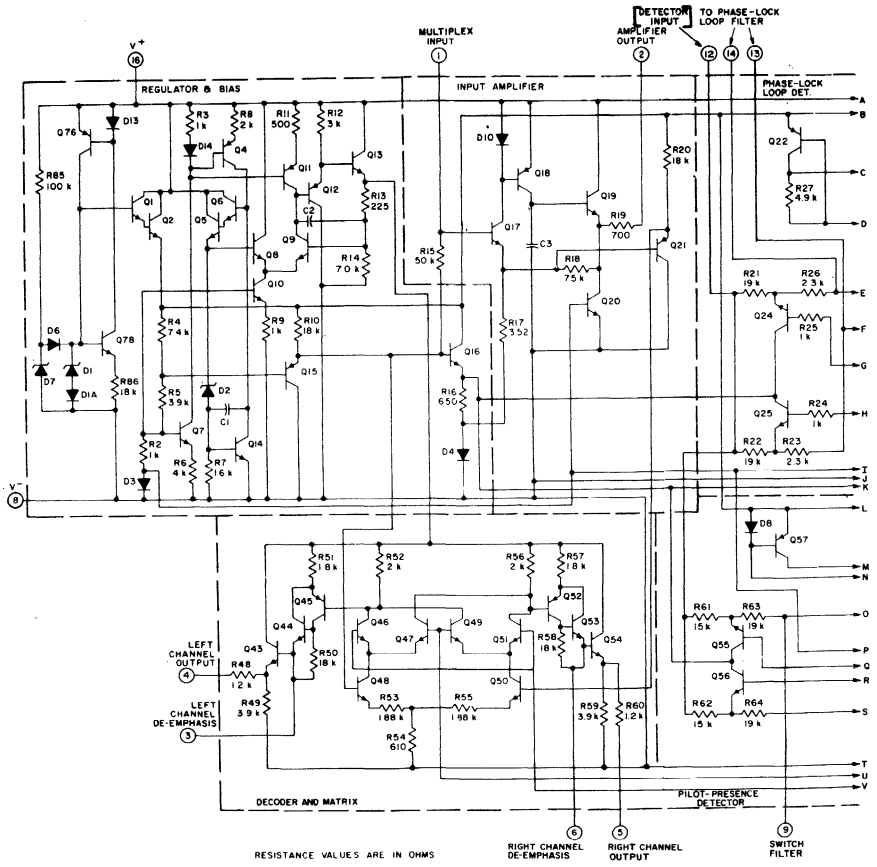


Fig. 2 – Schematic diagram of the CA758E.

CA758E

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig 7 unless otherwise specified) $V^+ = 12\ V, T_A = 25^oC$ Multiplex Input Signal (L=R, pilot "OFF") = 300 mV RMS 19-kHz Pilot Level = 30 mV RMS f (modulation) = 400 Hz or 1 kHz	• LIMITS Min.	Typ.	Max.	UNITS
Static Characteristics					
Total Current	Lamp "OFF"	–	26	35	mA
Maximum Available Lamp Current		75	150	–	mA
DC Voltage at Term. 7 (Lamp Driver)	I (Lamp) = 50 mA	–	1.3	1.8	V
DC Voltage Shift at either Term. 4 or 5 (Output)	Stereo-to-Mono Operation	–	30	150	mV
Dynamic Characteristics					
Power Supply Ripple Rejection	For a 200-Hz, 200-mV RMS Signal	35	45	–	dB
Input Resistance		20	35	–	kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation (Stereo)	At f = 100 Hz	–	40	–	dB
	f = 400 Hz	30	45	–	dB
	f = 10 kHz	–	45	–	dB
Channel Balance (Monaural)		–	0.3	1.5	dB
Voltage Gain	At f = 1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level:					
19-kHz Input	Lamp "ON"	–	15	20	mV RMS
19-kHz Input	Lamp "OFF"	2.0	7.0	–	mV RMS
Hysteresis	Lamp "OFF"	3.0	7.0	–	dB
Capture Range (Deviation from 76-kHz Center Frequency)		±2.0	±4.0	±6.0	%
Total Harmonic Distortion	Multiplex Input Signal = 600 mV RMS (Pilot "OFF")	–	0.4	1.0	%
19-kHz Rejection		25	35	–	dB
38-kHz Rejection		25	45	–	dB
SCA (Storecast) Rejection	Measured Composite Signal: 80% Stereo, 10% Pilot, 10% SCA	–	70	–	dB
Voltage-Controlled Oscillator (VCO) Tuning Resistance	Total Resistance (Term. 15 to 8) required to set f_{REF} = 19 kHz ± 10 Hz (Term. 11)	21.0	23.3	25.5	kΩ
Voltage-Controlled Oscillator Frequency Drift	$0^o \leq T_A \leq 25^oC$	–	+0.1	±2	%
	$25^o \leq T_A \leq 70^oC$	–	−0.4	±2	%

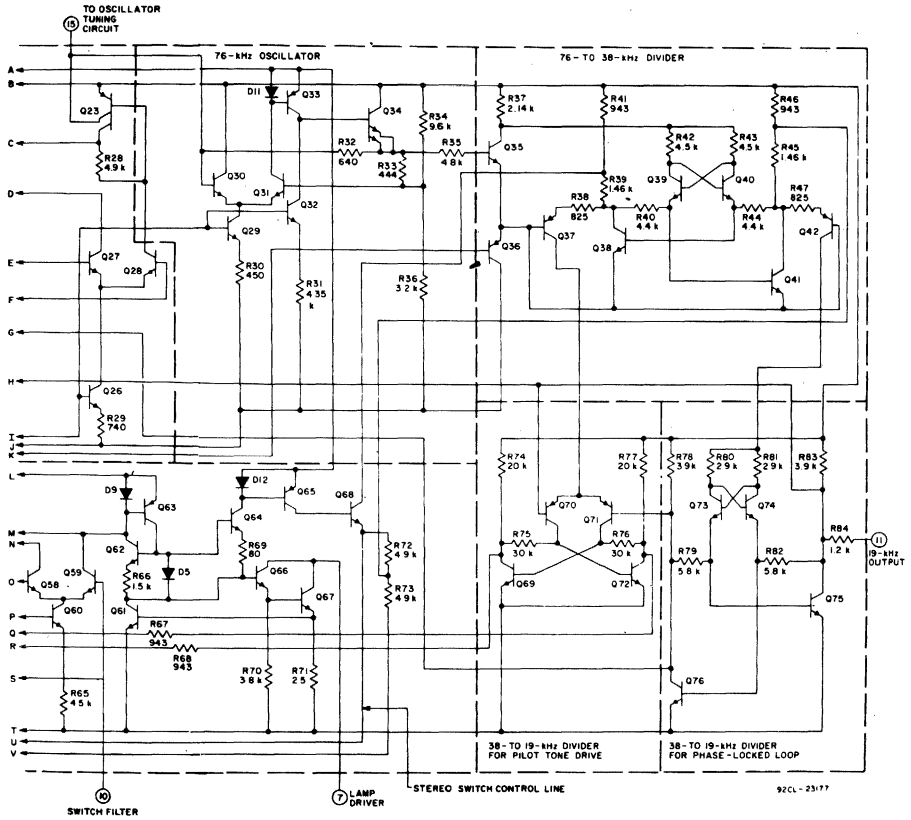


Fig.2 – Schematic diagram of the CA758E (Cont'd).

TYPICAL PERFORMANCE CHARACTERISTICS

(Referenced to Fig. 7)

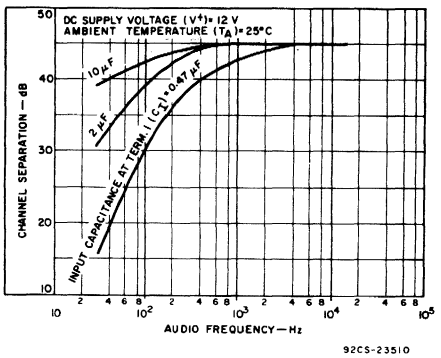


Fig.3 — Channel separation vs. audio frequency.

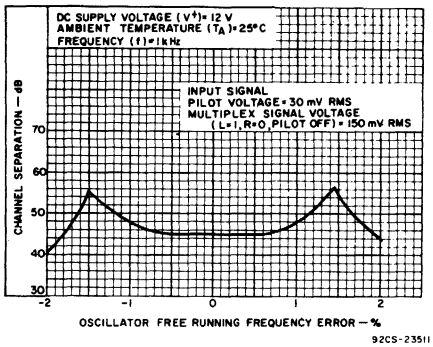


Fig.4 — Channel separation vs. oscillator free running frequency error.

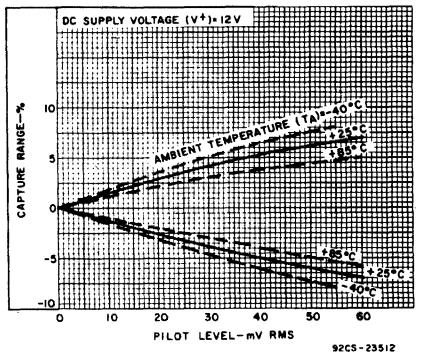


Fig.5 — Capture range vs. pilot level.

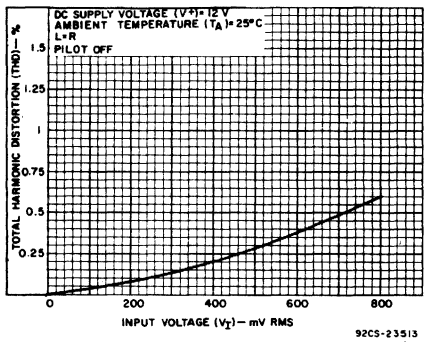


Fig.6 — Total harmonic distortion vs. input level.

CA758E

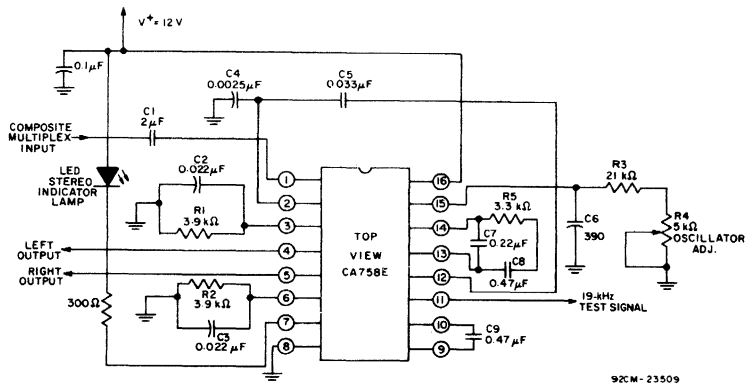


Fig. 7— Test circuit for measurement of dynamic characteristics.

NOTES:

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.

C_1 = +100%, −20%

C_6 = ±1% in test circuit and ±5% in typical application.

R_3 = ±1%

R_4 = ±10%

R_1 and R_2 = ±1% in test circuit and ±5% in typical application.

TYPICAL PERFORMANCE CHARACTERISTICS (Referenced to Fig. 7)

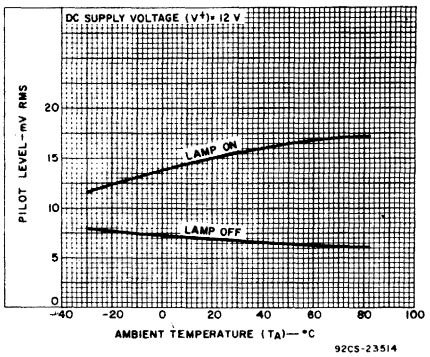


Fig. 8 – Lamp turn-on and turn-off sensitivity vs. ambient temperature.

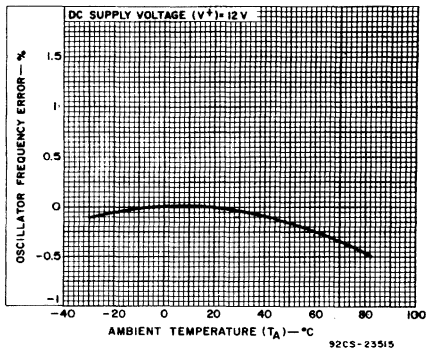


Fig. 9 – Oscillator free running frequency error vs. ambient temperature.

CA810Q, CA810QM

Preliminary Data

7-Watt Audio Power Amplifier With Thermal Shut-Down

The RCA-CA810Q and CA810QM are monolithic audio amplifiers intended for class B operation. They are specifically designed for mobile equipment operating from 12-V battery supplies. They operate over a wide range of supply voltages (4 to 20 V) with very low harmonic and crossover distortion. The maximum repetitive peak output current is 2.5 A, and an integral thermal limiting circuit shuts the device down in case of output overload or excessive package temperature.

The CA810Q and CA810QM are supplied in modified 16-lead quad-in-line plastic packages ("Q" suffix) with integral wing-tab heat sinks. The tabs on the CA810Q are bent down for p.c. board insertion, and on the CA810QM they are flat and pierced for easy attachment to an external heat sink.

The CA810Q and CA810QM are electrically and mechanically equivalent to types TBA810S and TBA810AS, respectively. It should be noted that pin-numbering conventions for these devices may differ from manufacturer to manufacturer, however the devices are pin compatible and interchangeability is not affected.

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25^\circ C$*

SUPPLY VOLTAGE	20 V
PEAK OUTPUT CURRENT (non-repetitive)	3.5 A
PEAK OUTPUT CURRENT (repetitive)	2.5 A
DEVICE DISSIPATION:	
At $T_A = 70^\circ C$	1 W
At $T_{tab} = 100^\circ C$	5 W
AMBIENT TEMPERATURE RANGE:	
Operating	$-40^\circ C$ to (Refer to Fig. 7 for typical high-temperature limit)
Storage	-40 to $+150^\circ C$

THERMAL RESISTANCE:	CA810Q	CA810QM	
Junction to tab	12	10	°C/W
Junction to ambient	70*	80	°C/W

*Value obtained with tabs soldered to printed-circuit board

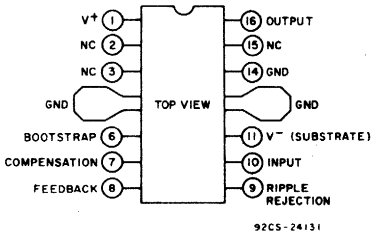


Fig. 1 – Terminal diagram of CA810Q and CA810QM. The wing tabs on the CA810Q are bent down, and on the CA810QM they are flat and pierced.

Features

- **Power output – 7 W with 4Ω load**
- **Supply voltage range – 4 to 20 V**
- **Peak output current – 2.5 A (max.)**
- **Very low harmonic and cross-over distortion**

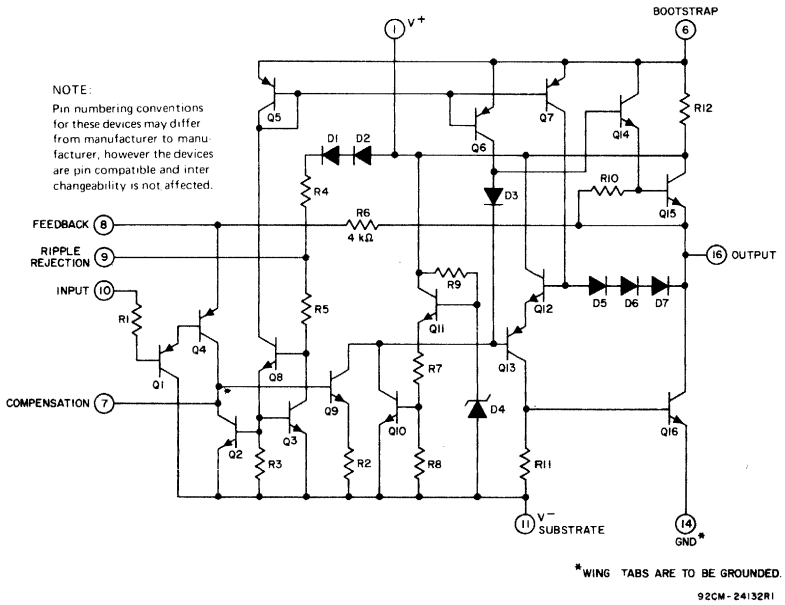


Fig. 2 – Schematic diagram of CA810Q, CA810QM.

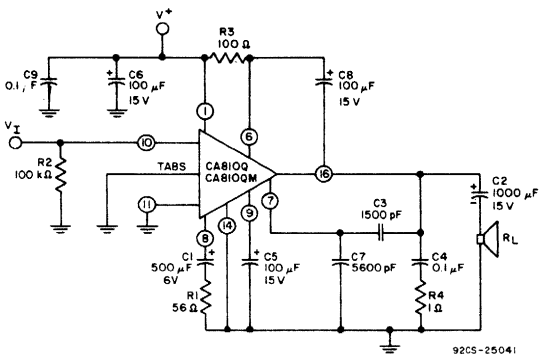
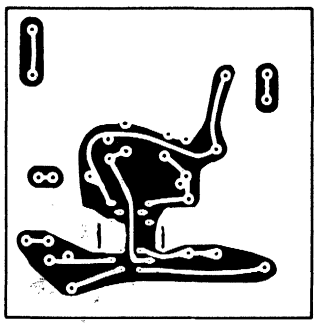


Fig. 3 – Test and circuit application for the CA810Q and CA810QM.

ELECTRICAL CHARACTERISTICS, *at $T_A = 25^\circ C$*

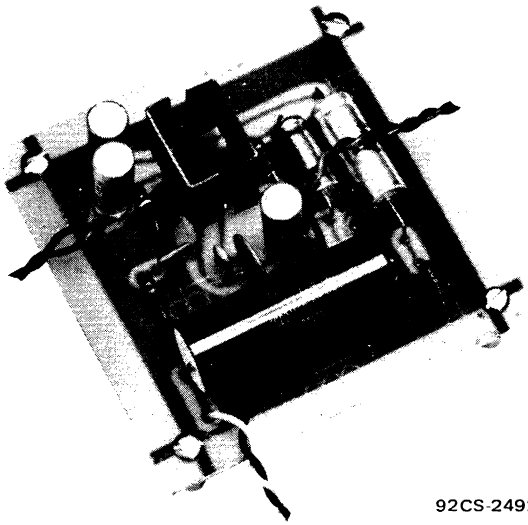
CHARACTERISTIC	SYMBOL	TEST CONDITIONS: Supply Voltage (V^+) = 14.4 V, Unless Otherwise Specified		LIMITS: CA810Q CA810QM MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+			4	–	20	V
Input Voltage	V_I			–	–	220	mV
Input Sensitivity	e_I	P_O=6 W, R_L=4 Ω, R1 = 56 Ω, f = 1 kHz		–	80	–	mV
Quiescent Output Voltage	V_O			6.4	7.2	8	V
Quiescent Current Drain	I_O			–	12	20	mA
Input Noise Voltage	e_N	R_g=0, BW (−3 dB) =20 to 20,000 Hz		–	2	–	μV
Bias Current	I_{IB}			–	0.4	–	μA
Output Power	P_O	f=1 kHz, R_L=4Ω, THD = 10%	V^+= 14.4 V	–	6	–	W
			V^+= 6 V	–	1	–	
Input Resistance	R_I			–	5	–	MΩ
Total Harmonic Distortion	THD	P_O=50 mW to 3W, R_L 4 Ω, f = 1 kHz		–	0.3	–	%
Open-Loop Voltage Gain	A_{OL}	R_L = 4 Ω, f = 1 kHz		–	80	–	dB
Closed-Loop Voltage Gain	A	R_L = 4 Ω, f = 1 kHz, R1 = 56 Ω		34	37	40	dB
Efficiency	η	P_O = 5 W, R_L = 4 Ω, f = 1 kHz		–	70	–	%

CA810Q, CA810QM



92CS-25042

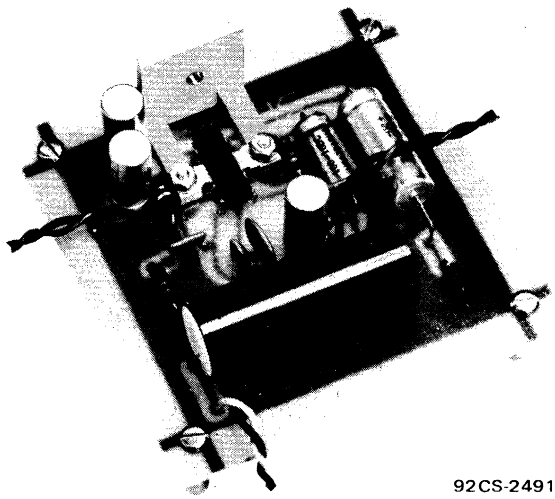
Fig. 4 – Bottom view of printed-circuit boards shown in Figs. 5 and 6.



92CS-24920

Circuit heat is dissipated by a combination of free air and printed-circuit board foil.

Fig. 5 – Component view of printed-circuit board for CA810Q.

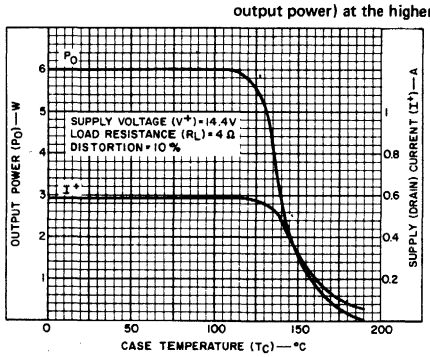


92CS-24919

Circuit arrangement for use with chassis having a thermal resistance of $\leqslant 5^{\circ}C/W$. Vertical bracket should make good thermal contact to chassis.

Fig. 6 – Component view of printed-circuit board for CA810QM.

The thermal-limiting network incorporated in the CA810 Series circuits provides protection against damage due to excessive semiconductor temperatures that may result from high ambient temperatures and/or excessive dissipation, e.g., as encountered in sustained overloads. As indicated in Fig. 7, the thermal-limiting feature automatically reduces the supply current (and output power) at the higher temperatures.



92CS-25043

Fig. 7 – Typical output power and drain current vs. case temperature.

CA920AE

Preliminary Data

TV Horizontal Oscillator

For Colour and Monochrome Receivers

The RCA-CA920AE* is a silicon monolithic integrated circuit intended for use in the horizontal stages of colour and monochrome television receivers. This device performs the functions of a sync separator, noise gate, and horizontal oscillator with dual-time-constant switching in the fly-wheel loop. It also generates automatic phase control between horizontal flyback pulses and the horizontal oscillator frequency and provides fast edge switching drive for transistor or thyristor horizontal output stages.

The CA920AE is compatible with the industry type TBA920 in both lead arrangement and electrical operation, although the CA-920AE features reduced operating current.

The CA920AE is supplied in the 16-lead dual-in-line plastic package.

*Formerly Dev. Type No. TA6773.

Features:

- **Sync separator**
- **Noise gate input**
- **Internal precision timing ramp**
- **Dual-time-constant phase-locked loop**
- **Output suitable for transistor or thyristor deflection systems**
- **Reduced power dissipation**

MAXIMUM RATINGS, *Absolute Maximum*

Values at $T_A = 25^oC$:

DC SUPPLY VOLTAGE . . . . 13.2 V

DEVICE DISSIPATION:

Up to $T_A = 55^oC$ . . . . . 750 mW

Above $T_A = 55^oC$ Derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:

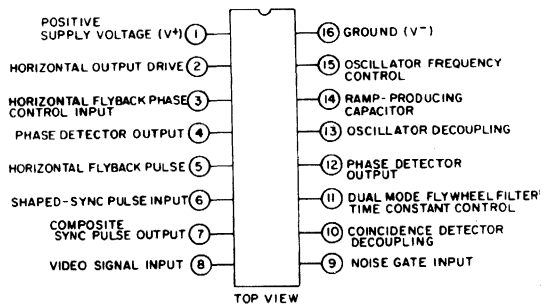
Operating . . . . . −40 to +85°C

Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During soldering):

At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max. . . +265 °C

TOP VIEW



TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, and Supply Voltage (V^+) = 12 V, Unless otherwise specified. See Fig. 1.

CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Supply Current, Term. 1, I^+		Term. 2 open		22		mA
Video Characteristics (Term.8):						
Input Voltage	V_8	Peak to peak	1.5	3	6	V
Input Current	I_8	Peak			10	mA
Noise Gate Characteristics (Term.9):						
Input Current	I_9		0.03		10	mA
Reverse Input Current	I_9				−10	mA
Horizontal Flyback Positive Pulse Characteristics (Term.5):						
Input Voltage	V_5		1		3	V
Input Current	I_5		0.05	1	10	mA
Input Impedance	Z_5			0.4		kΩ
Positive Sync Characteristics (Term.7):						
Output Voltage	V_7	Peak to peak		10		V
Output Impedance	Z_7	Leading edge		50		Ω
Output Impedance	Z_7	Trailing edge		100		Ω
Horizontal Output Characteristics (Term.2):						
Output Current	I_2MAX	Peak			200	mA
Output Current	I_2AV	Average			20	mA
Output Pulse Width	t_W		12		32	μs
Output Impedance	Z_2	Leading edge		2.5		Ω
Output Impedance	Z_2	Trailing edge		15		Ω
Horizontal Oscillator Characteristics (Term.15):						
Free-Running Frequency	f_o	No sync input	14.84	15.625	16.41	kHz
Free-Running Frequency	f_o	$V^+ = 4.5$ V	14.06	(Note 1)	17.19	kHz
Oscillator Cut-out Voltage		V^+ varied		4.0		V
Oscillator Pull-in Range				±1.0		kHz
Phase Control (Note 2)					15	μs

Note 1: Free-running frequency at 12 V adjusted to 15.625 kHz.

Note 2: External delay between the leading edge of output pulse at Term. 3 and the start of the horizontal flyback pulse.

CA920AE

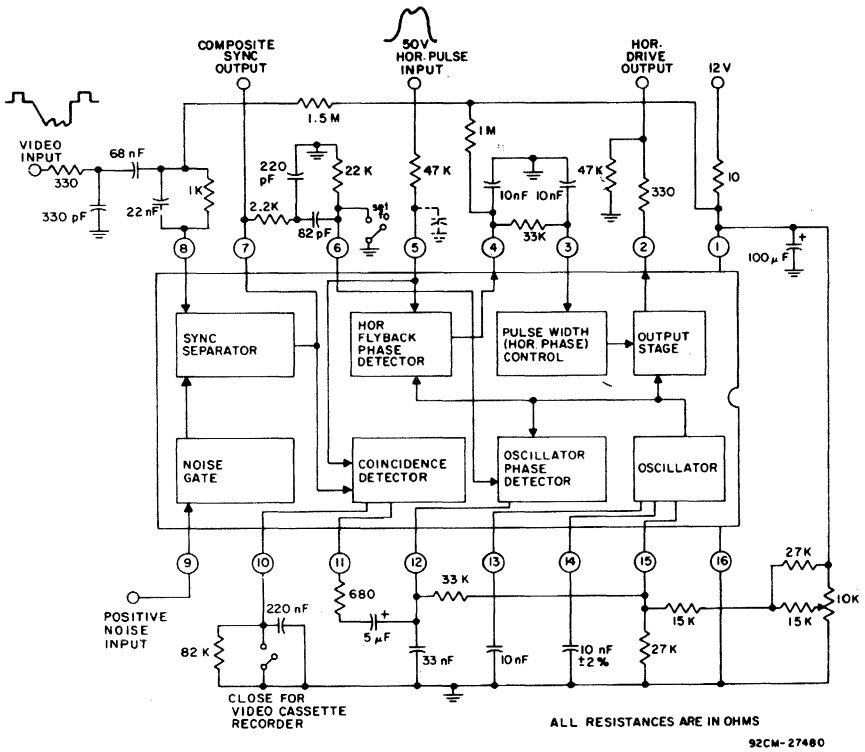


Fig.1 – Functional block diagram of the CA920AE with typical peripheral circuitry.

CA1310E

RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

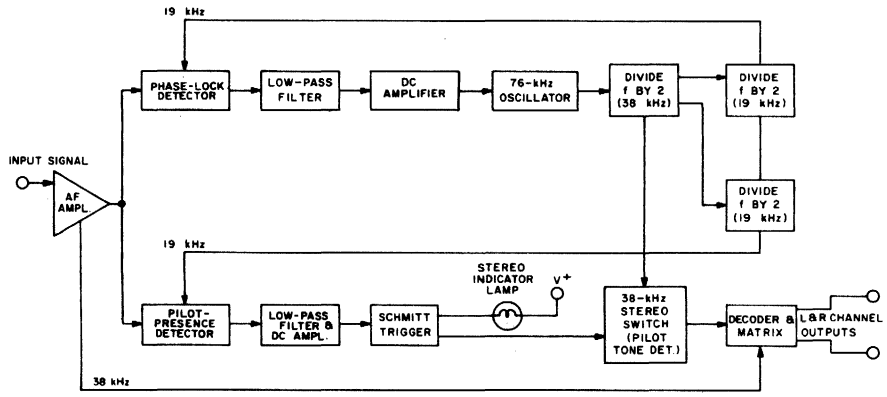


Fig. 1 – Functional block diagram system using the CA1310E. 92CS-23500

Features:

- **Low distortion (THD): 0.3% typ.**
- **Excellent SCA (storecast) rejection: 75 dB typ.**
- **RC oscillator**
- **High audio channel separation: 40 dB**
- **Operates from a wide range of power supplies: 8 to 14 V dc**
- **Requires only one adjustment for complete alignment**
- **Drives a stereo indicator lamp up to 75 mA – surge current limiting**

RCA-CA1310E is a monolithic silicon integrated circuit RC phase-lock-loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA1310E is a direct replacement for industry types MC1310P, LM1310, and SN76115N.

This decoder uses a minimum of external components. In addition the stereo decoder requires only one adjustment (oscillator frequency) for complete alignment.

The CA1310E is supplied in a 14-lead dual-in-line plastic package and operates over an ambient temperature range of –40 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

DC Supply Voltage	14 V
Current (Lamp) at Term. 6	75 mA
Device Dissipation:	
Up to $T_A = 25°C$	625 mW
Above $T_A = 25°C$ derate linearly	5 mW/°C
Ambient Temperature Range:	
Operating	–40 to +85°C
Storage	–65 to +150°C
Lead Temperature (During soldering):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3) $V^+ = 12$ V, $T_A = 25°C$, Composite Multiplex Input Signal = 560 mV RMS (2.8 V p-p), Only L or R Channel modulated; and with 100-mV RMS (10%) Pilot Level	LIMITS Min.	Typ.	Max.	UNITS
Static Characteristics					
DC Supply Voltage	For 8-V operation, reduce load to 2.7 kΩ	8	–	14	V
Total Current	Lamp "OFF"	–	13	–	mA
Dynamic Characteristics					
Input Impedance		20	50	–	kΩ
Channel Separation (Stereo)	50 Hz – 15 kHz	30	40	–	dB
Audio Output Voltage (For any one channel)		–	485	–	mV RMS
Channel Balance (Monaural)	Pilot Tone "OFF"	–	–	1.5	dB
Capture Range (Permissible tuning error of internal oscillator)		–	±3.5	–	%
Total Harmonic Distortion		–	0.3	–	%
Ultrasonic Frequency Rejection:					
19 kHz		–	34.4	–	dB
38 kHz		–	45	–	dB
SCA (Storecast) Rejection	f = 67 kHz, 9-kHz beat note measured with 1-kHz modulation "OFF"	–	75	–	dB
Stereo Switch Level:					
19-kHz Input Level (For lamp on)		–	–	20	mV RMS
19-kHz Input Level (For lamp off)		5	–	–	mV RMS
Maximum Composite (Stereo) Input	0.5% THD	2.8	–	–	V p-p
Maximum Monaural Input	1% THD	2.8	–	–	V p-p

CA1310E

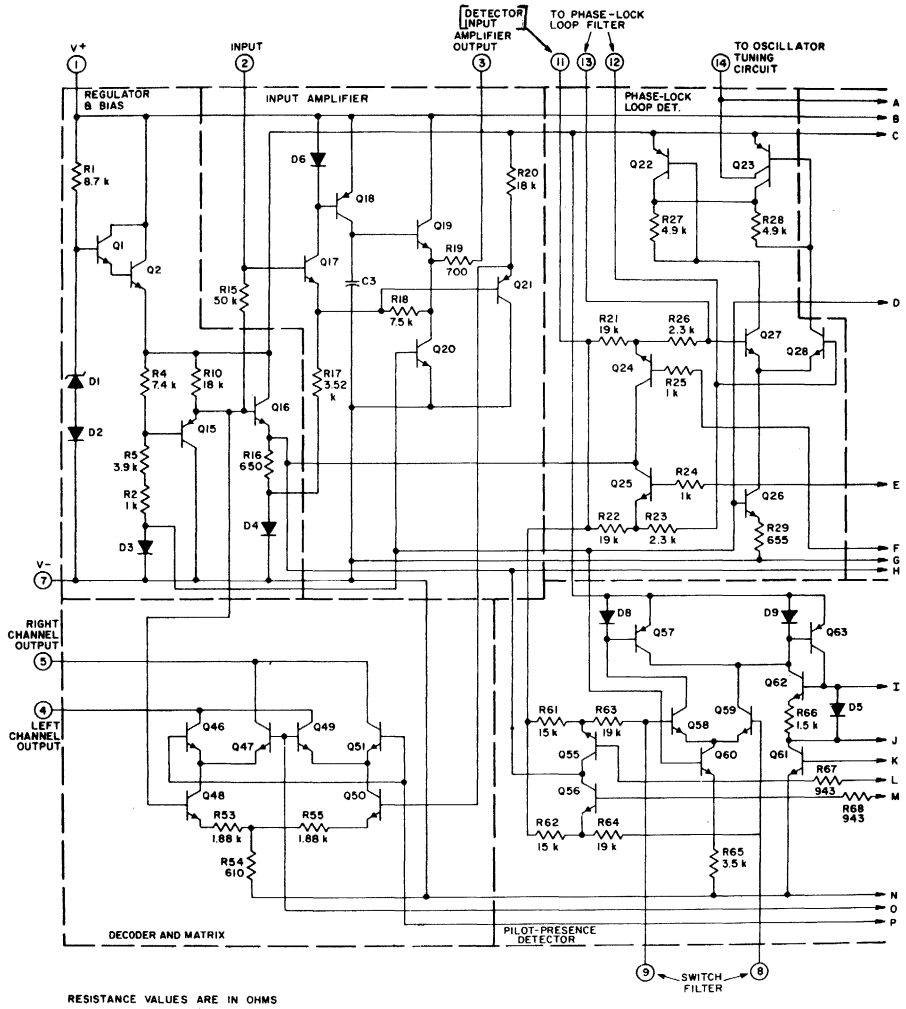
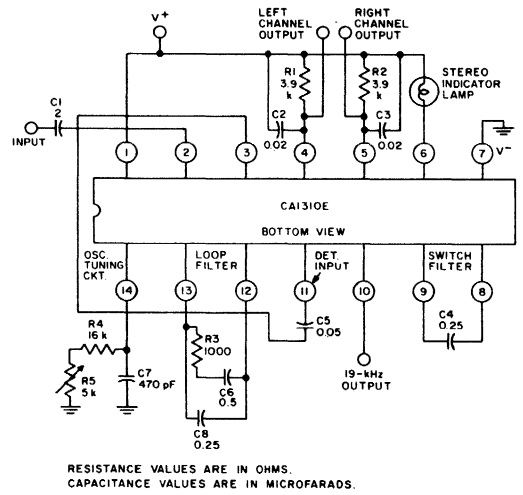


Fig. 2 – Schematic diagram of the CA1310E.



NOTES

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower value input coupling capacitor may be used in place of the 2-μF value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo switch level detector circuit is calculated by C4 x 53,000 ohms ±30% with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05-μF capacitor provides a 1.75° phase lead at 19 kHz.

R1, R2: Load resistance values are related to supply voltage as follows:

Minimum Supply Voltage	8	10	12	V
Maximum Load Resistance	2.7	4.3	6.2	kΩ

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25 μF, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than ±3% typ. is required, reduce value of C7 and increase values of R4, R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. R4, C7 = ±1% in test circuit and ±5% in typical application.

Fig. 3 – Test circuit for measurement of dynamic characteristics.

CA1310E

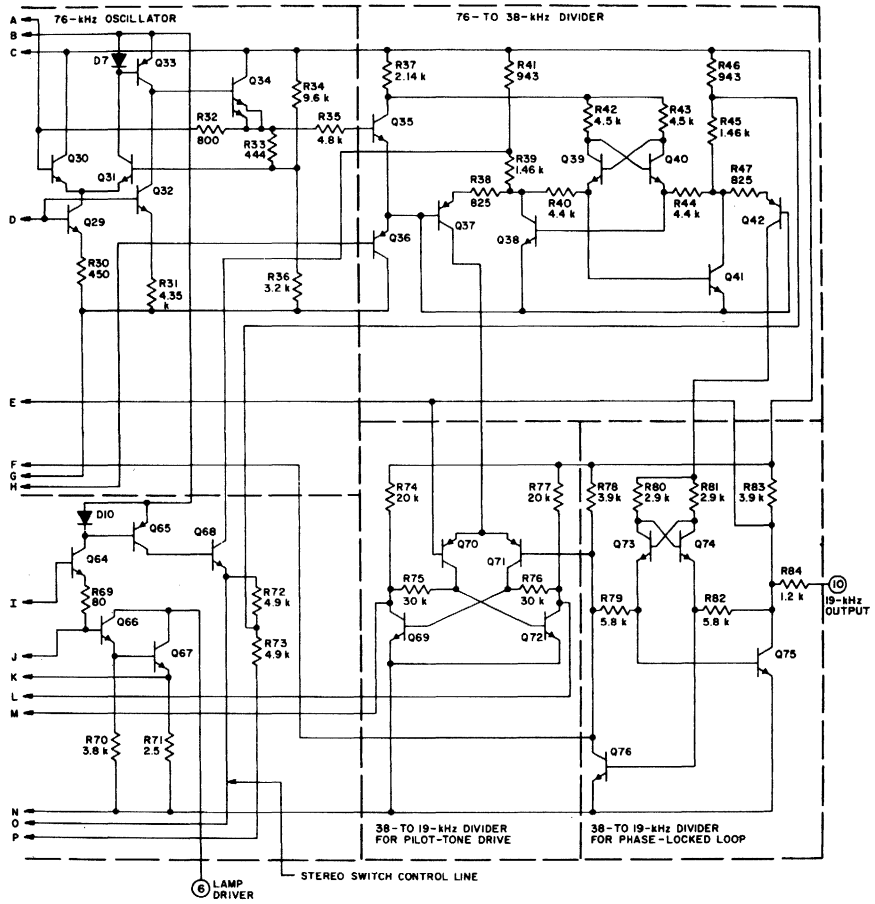


Fig. 2 – Schematic diagram of the CA1310E (Cont'd).

CA1352E

TV Video IF Amplifier

With AGC and Keyer Circuit

The RCA-CA1352E is a monolithic integrated circuit designed for use as an if amplifier in monochrome or color TV receivers. It features a high-gain gated AGC system with a 68-dB range (typ.). A delayed forward AGC output is adjustable by means of a potentiometer. Either positive- or negative-going sync may be used for this system.

The CA1352E is supplied in the 14-lead dual-in-line plastic package, and is directly interchangeable with the industry type 1352 in similar packages.

Features

- **High 45-MHz gain – 53 dB (typ.)**
- **High-gain gated AGC system – with either positive- or negative-going sync.**
- **Adjustable rf AGC delay to tuner**
- **AGC gain reduction – 68 dB (typ.)**

TYPICAL STATIC CHARACTERISTICS
at $T_A = 25°C$, $V^+ = 12$ V

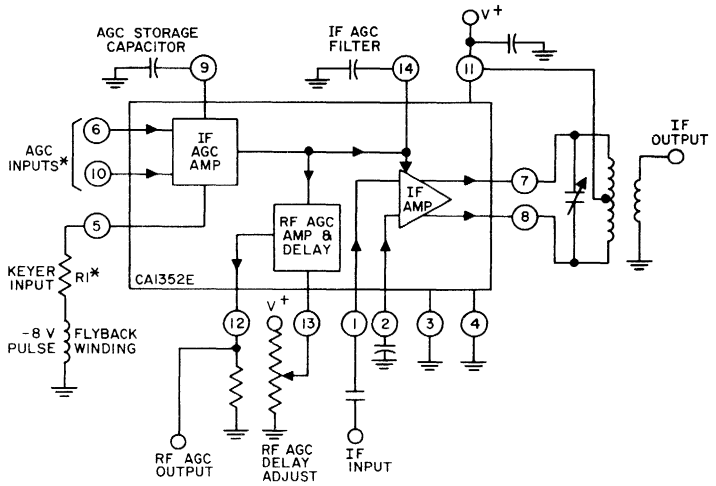
Total Current ($I_7 + I_8 + I_{11}$)	27 mA
Output Stage Current ($I_7 + I_8$)	5.7 mA

TYPICAL DYNAMIC CHARACTERISTICS
at $T_A = 25°C$, $V^+ = 12$ V

AGC Range	**68 dB**
Power Gain	**53 dB**
Minimum rf AGC Range (term. 12)	**0.2 V**
Maximum rf AGC Range (term. 12)	**7 V**

MAXIMUM RATINGS, *Absolute-Maximum Values*
At $T_A = 25$

SUPPLY VOLTAGE:	
Between terminals 4 and 11	18 V
Between terminals 7 or 8 and 4	18 V
INPUT VOLTAGE (terminal 1 or 2)	10 V p-p
AGC INPUT VOLTAGE (terminal 6 or 10)	6 V
DEVICE DISSIPATION:	
Up to $T_A = 55°C$	750 mW
Above $T_A = 55°C$ derate linearly at	7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C



SYNC POLARITY	* VOLTAGE AT TERMINAL 6	* VOLTAGE AT TERMINAL 10	* VALUE OF RI – Ω
NEGATIVE	5.5 V, 2 V, 0 V	1 TO 4 V NOM=2 V	0
POSITIVE	1 TO 8 V NOM=4.5	4.5 V, 0 V	3.9k

92CS-24136RI

Fig. 1 – CA1352E block diagram and typical AGC test set-up.

CA1391E, CA1394E — Preliminary Data

TV Horizontal Processors

CA1391E – Positive Horizontal Sawtooth Input
CA1394E – Negative Horizontal Sawtooth Input

The RCA-CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

These types are supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operate over an ambient temperature range of 0 to +85°C.

Features:

- **Internal shunt regulator**
- **Linear balanced phase detector**
- **Preset hold control capability**
- **±300-Hz pull-in (typ.)**
- **Low thermal frequency drift**
- **Small static phase error**
- **Variable output duty cycle**
- **Adjustable dc loop gain**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY CURRENT	40 mA
DC OUTPUT VOLTAGE	40 V
DC OUTPUT CURRENT	30 mA
SYNC INPUT VOLTAGE	5 V_{p-p}
SAWTOOTH INPUT VOLTAGE	5 V_{p-p}
DEVICE DISSIPATION:	
Up to T_A = 25°C	625 mW
Above T_A = 25°C derate linearly	5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +85°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+260°C
THERMAL RESISTANCE	200°C/W

ELECTRICAL CHARACTERISTICS
At T_A = 25°C

CHARACTERISTIC	TYP.VALUE	UNITS
DC Supply Voltage	8.6	V
DC Supply Current (Term. 6)	20	mA
Collector-to-Emitter Saturation Voltage at Term. 1 (I_I = 20 mA)	0.15	V
Static Phase Error (Δf = 300 Hz)	0.5	μs
DC Input Voltage (Term. 4)	2	V
Oscillator Pull-in Range	±300	Hz
Oscillator Hold-in Range	±900	Hz

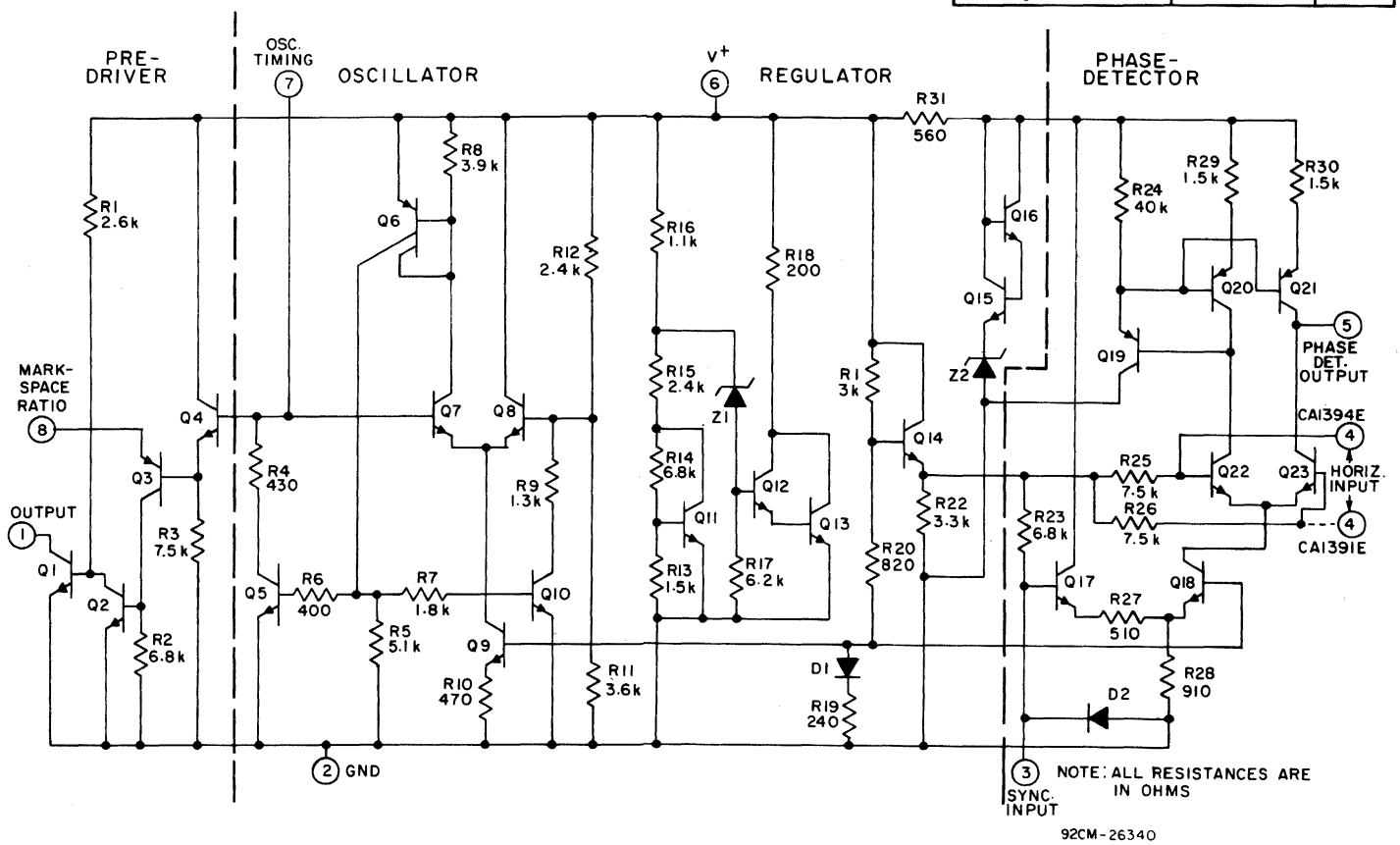


Fig. 1 – Schematic diagram of CA1391E, CA1394E.

CA1391E, CA1394E

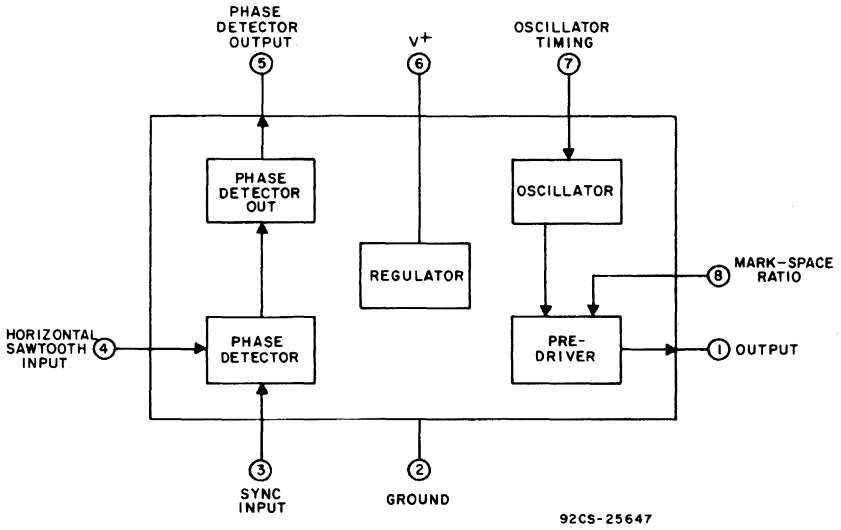


Fig.2 – Functional block diagram of the CA1391E, CA1394E.

CA1398E

Television Chroma Processor

RCA-CA1398E is a monolithic silicon integrated-circuit chroma processor containing chroma-amplifier and gain-control, color-killer, color subcarrier oscillator, hue control, and ACC circuitry. It has been designed for interchangeability with other "1398"-type chroma-processor devices. It functions compatibly with the RCA-CA3125E Chroma Demodulator as well as other commercially available chroma demodulators in color-TV receivers. Fig. 2 shows a functional block diagram of a 2-package TV chroma system incorporating the CA1398E and CA3125E. The CA1398E is supplied in a 14-lead dual-in-line plastic package.

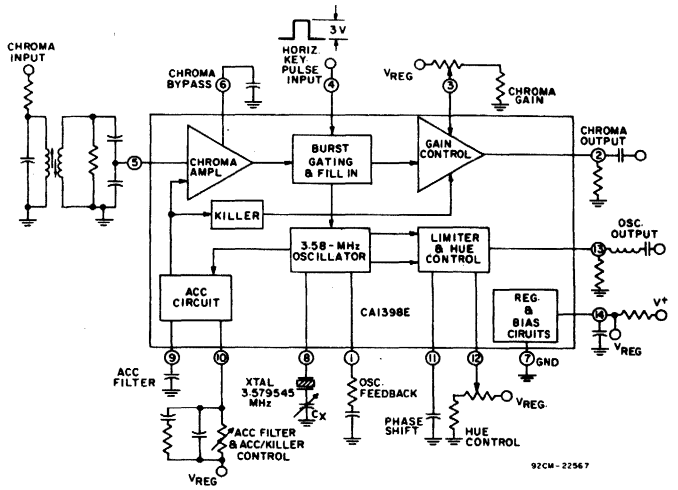


Fig. 1 – Functional block diagram of the CA1398E.

Features

- **Minimum number of external components required**
- **Injection-lock oscillator with internal feedback**
- **DC chroma gain control and hue control circuits**
- **Low-impedance internal voltage regulation**

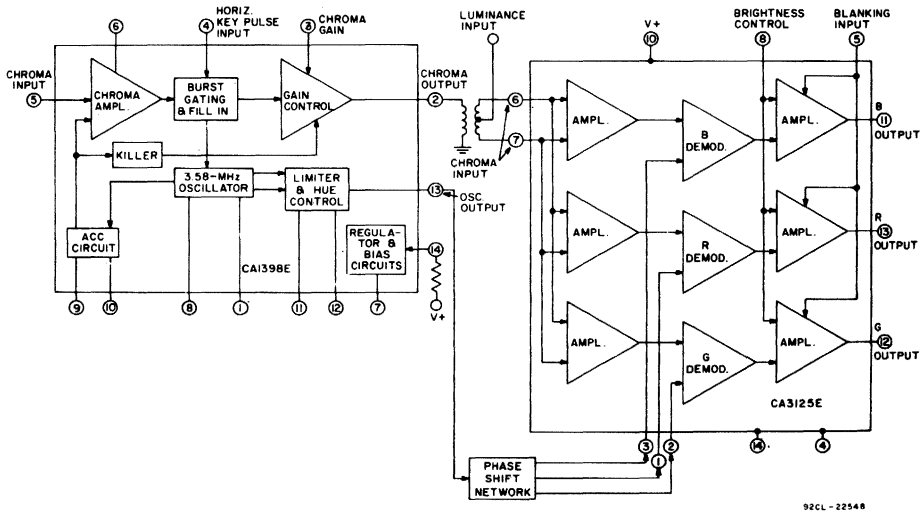


Fig. 2 – TV chroma system functional block diagram.

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^\circ C$

Peak Horizontal-Pulse Input Current	250 μA
Supply Current (Terminal 14)	35 mA
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ and Referenced to Test Circuit (Fig. 4)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS							LIMITS			UNITS
		SWITCH POSITION (S1)	CONTROL SETTING CHROMA	HUE	KILLER	V_{BURST} mV p-p	V_{CHROMA} mV p-p		MIN.	TYP.	MAX.	
Static Characteristics												
Regulated Supply Voltage	V_{14}	2	max.	max.	max.	0	0		8.9	9.5	11.5	V
Chroma Output Bias	V_{14} to V_2	2	max.	max.	max.	6	0		1.2	2.4	3.6	V
Regulator Impedance	See Note 1	2	max.	max.	max.	0	0		–	12	25	Ω
Dynamic Characteristics (Refer to Test Set-Up Procedure for Oscillator)												
Max. Chroma Gain	V_2	1	max.	max.	See Note 2	6	5		310	425	–	mV p-p
Min. Chroma Gain	V_2	1	min.	max.		6	5		–	–	7	mV p-p
ACC Action	V_2 (dB up from gain test)	1	max.	max.		50	50		2	7	11	dB
Killer Function:												
Kill	V_2	2	max.	max.		0	5		–	–	7	mV p-p
Unkill	V_2	1	max.	max.		115	5		100	–	–	mV p-p
Oscillator Lock-Up:												
Voltage	V_{13}	1	max.	max.		6	0		250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	max.		6	0		−20	0	+20	degrees
Hue Control Range:												
Voltage	V_{13}	1	max.	min.		6	0		250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	min.		6	0		95	110	140	degrees

Note 1 – Measure V_{14} at I_{SUPPLY} = 38 mA and 18 mA. Calculate the regulator impedance:
$Z_{reg.} = [V_{14}\text{ (at 38 mA)} - V_{14}\text{ (at 18 mA)}]/0.02$

Note 2 – Increase the killer potentiometer resistance from minimum until the circuit unkills. This condition is evidenced by a shift in bias voltage at Term. 2 Maintain this potentiometer setting for all the dynamic tests.

CA1398E

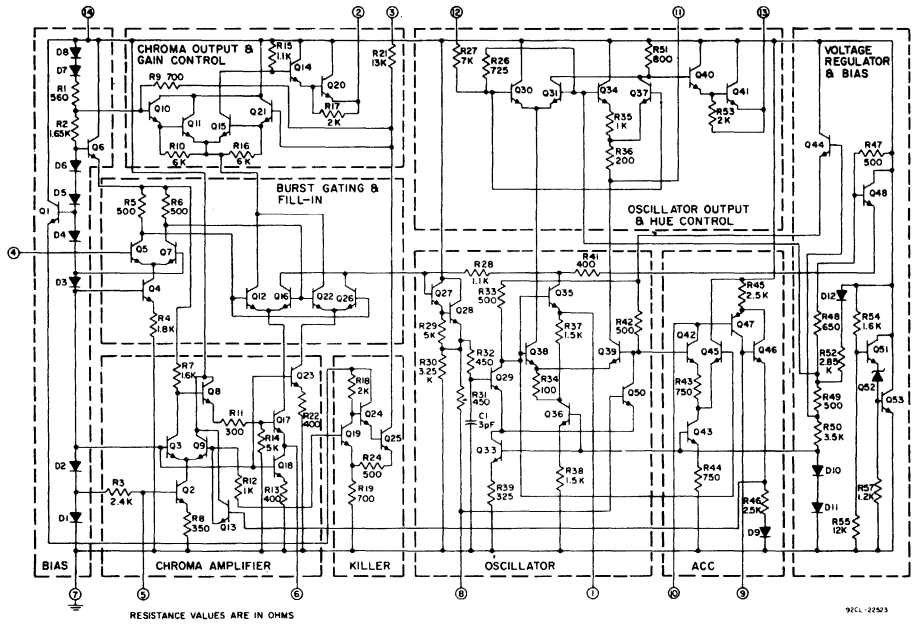


Fig. 3 – Schematic diagram of the CA1398E.

TEST SET-UP PROCEDURE FOR OSCILLATOR

Remove the horizontal keying and chroma inputs and adjust C_X to obtain a free-running oscillator frequency of 3.579545 MHz ±10 Hz. Under the same Test Conditions described in the Electrical Characteristics Chart for Oscillator Lock-Up, vary L1 (approx. 20 μH) and/or C1 (approx. 1000 pF) to obtain the initial conditions for amplitude and phase oscillator lock-up.

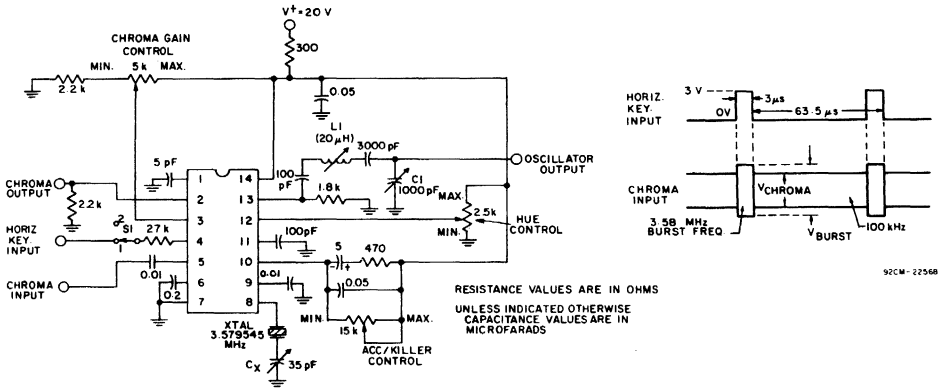


Fig. 4 – Typical static and dynamic characteristics test circuit for the CA1398E.

CA1541D

Dual-Input Memory Sense Amplifier

RCA-CA1541D , a monolithic silicon integrated circuit, is a dual-input memory sense amplifier intended for core memory applications.

The sense amplifier, consisting of two differential input amplifiers, a common second stage amplifier, and an output logic gate (See Fig. 1), converts low-level core-memory "1" pulses to saturated logic-level output pulses. Either one of the input amplifiers may be gated ON with a saturated logic signal so that an incoming "1" pulse of positive or negative polarity can be detected from either of two sense lines.

The CA1541D features an external switching threshold adjustment, plus its gate and strobe inputs are compatible with saturated logic levels. The sense amplifier is suitable for operation with core memories having cycle times equal to or greater than 0.4 μs and is unilaterally interchangeable with industry types 1541L and 1441.

The CA1541D is supplied in 14-lead dual-in-line ceramic package and is rated for operation over the full military temperature range of −55°C to +125°C.

Features

- Complete dual input core memory sense amplifier
- Two available outputs: —Saturated logic output
  —Linear output (positive output for either polarity input)
- Nominal threshold voltage: 17 mV
- Adjustable threshold: 10 to 35 mV
- Low threshold uncertainty range: ±3 mV
- Fast overload recovery time: —Differential-Mode: 15 ns typ.
  —Common-Mode: 30 ns typ.
- Independent channel gate and strobe terminals compatible with saturated logic levels
- Suitable for core memories having cycle times ⩾ 0.4 μs
- Input offset voltage: 6 mV max.

MAXIMUM RATINGS, Absolute Maximum Values, at T_A = 25°C

Except for Differential Input Voltage, all voltages are measured with respect to ground (Term. 8).

DC Supply Voltage:	
V^+ (Term. 2)	+10 V
V^- (Term. 7)	−10 V
Differential Input Voltage	±5 V
Common-Mode Input Voltage	±5 V
"A" or "B"-Gate Input Voltage*	V^- to V^+
Strobe Terminal Voltage	V^- to +6V
Output Terminal Load Current	±25 mA
Device Dissipation:	
Up to T_A = 75°C	750 mW
Above T_A = 75°C	Derate Linearly 8 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125 °C
Storage	−65 to +150 °C
Lead Temperature (during soldering):	
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265°C

*Note: The "A" or "B"-Gate Input Voltage is also referred to, as the Channel-Gate Input Voltage.

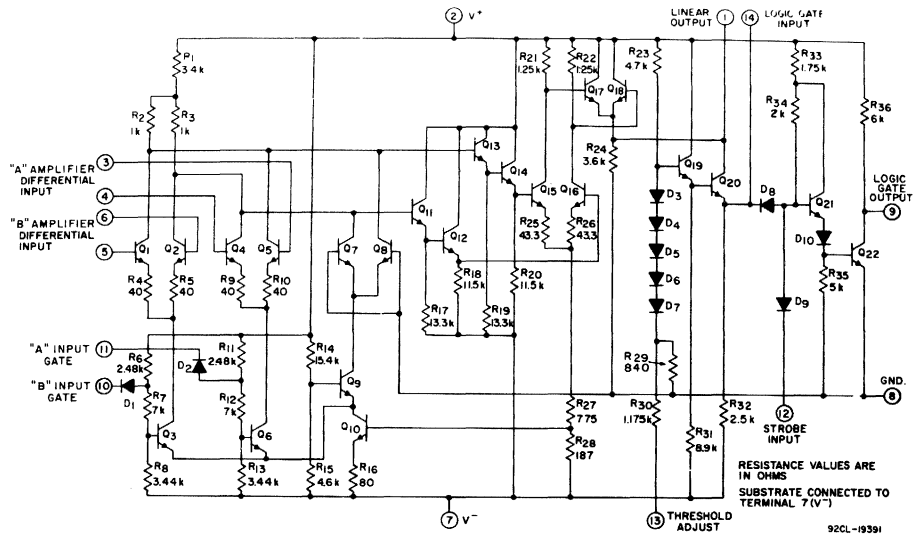


Fig. 2 – Schematic diagram of the CA1541D.

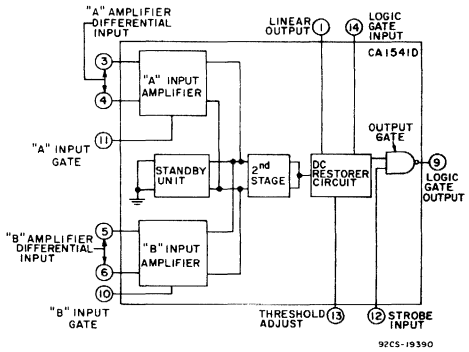


Fig. 1 – Functional block diagram of the CA1541D.

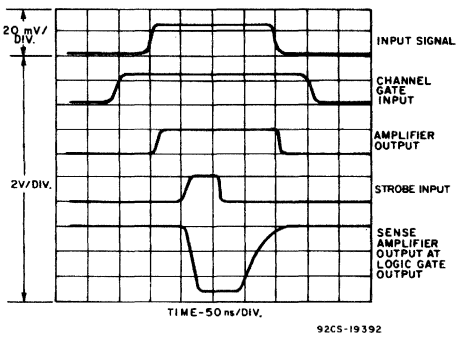


Fig. 3 – Typical operational wave forms.

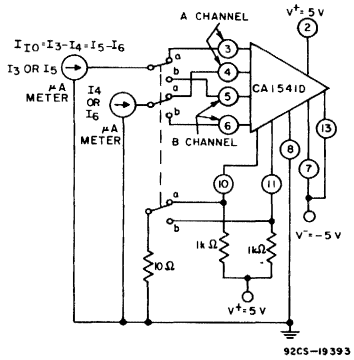


Fig. 4 – Input bias (I_{IB}) and input-offset current (I_{IO}) test circuit.

CA1541D

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS: $V^+ = 5V$, $V^- = -5V$; V_{TH} ADJ. = $-5V \pm 1\%$, (Term. 13) $C_{EXT} = 0.01\ \mu F$; $T_A = 25^oC$ (unless indicated otherwise)		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static (DC) Characteristics							
Power Dissipation	P_D			–	140	180	mW
Input Offset Current	I_{IO}			–	1	2	μA
Input Bias Current: $T_A = 25^oC$	I_{IB}		$V_5 = V_6 = V_3 = V_4 = 0$	–	5	25	μA
$T_A = -55^oC$				–	–	50	
Output Voltage: High	V_{OH}	$I_{OM} = 200\ \mu A$		3	–	–	V
Low – $T_A = 25^oC$	V_{OL}	$V_{14} = 5\ V$, $I_9 = 10\ mA$		–	–	350	mV
$T_A = 125^oC$				–	–	400	
Strobe Load Current	I_S	$V_{12} = 0$		–	–	1.5	mA
Strobe Reverse Current: $T_A = 25^oC$	I_{SR}	$V_{12} = 5V$		–	–	2	μA
$T_A = 125^oC$				–	–	25	
Input Gate Load Current	I_G	$V_{10} = V_{11} = 0$		–	–	2.5	mA
Input Gate Reverse Current: $T_A = 25^oC$	I_{GR}	$V_{10} = V_{11} = 5V$		–		2	μA
$T_A = 125^oC$				–	–	25	
Switching Characteristics							
Input Threshold Voltage: $T_A = 25^oC$	V_{TH}			14	17	20	mV
$T_A = -55$ to 125^oC				12	17	22	
Input Offset Voltage	V_{IO}			–	1	6	mV
Input Gate Voltage: High	V_{GH}	$V_3 = V_5 = 25\ mV$,		–	1.6	–	V
Low	V_{GL}	$V_4 = V_6 = 0$		–	0.7	–	
Common-Mode Range: Input Gate High	V_{CM}			–	±1.5	–	V
Input Gate Low				–	±1.5	–	
Differential-Mode Range: Input Gate High	V_{DH}			–	±600	–	mV
Input Gate Low	V_{DL}			–	±1.5	–	V
Propagation Delay: Input to Amplifier Output	t_{IA}	$V_3 = 25\ mV$ (pulsed),		–	10	15	ns
Input to Output	t_{IO}	$V_{12} = 2V$		–	20	30	
Strobe to Output	t_{SO}	$V_3 = V_4 = V_5 = V_6 = 0$, $V_{12} = 2V$ (pulsed)		–	15	20	
Gate Input to Amplifier Output	t_{GA}	$V_{11} = 2V$ (pulsed)		–	10	15	
Gate Input to Amplifier Input	t_{GI}	$V_3 = 25\ mV$		–	30	35	
Common-Mode Recovery Time: Input Gate High	t_{CMR}	$V_3 = V_5 = 1.5\ V$		–	15	30	ns
Input Gate Low				–	15	30	
Differential-Mode Recovery Time: Input Gate High	t_{DR}	$V_3 = V_5 = 400\ mV$		–	30	–	ns
Input Gate Low				–	0	–	

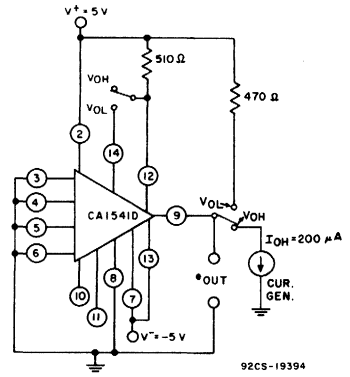


Fig. 5 – Test circuit for measurement of low (V_{OL}) and high (V_{OH}) output voltage levels.

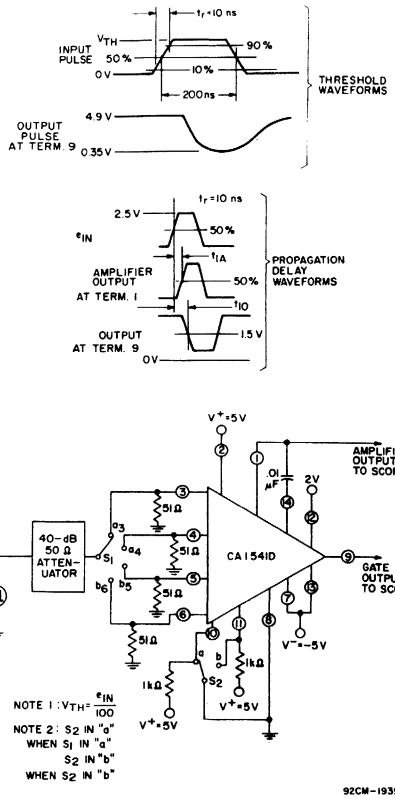


Fig. 6 – Threshold propagation delay, gate and input-offset test circuit with associated pulse wave forms.

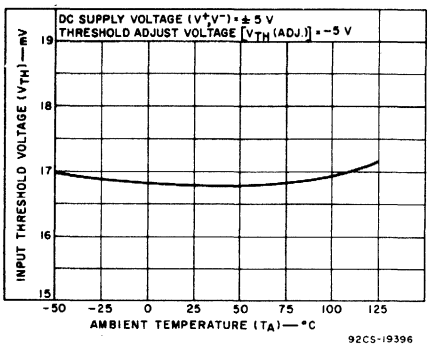


Fig. 7a – Input V_{TH} vs. T_A.

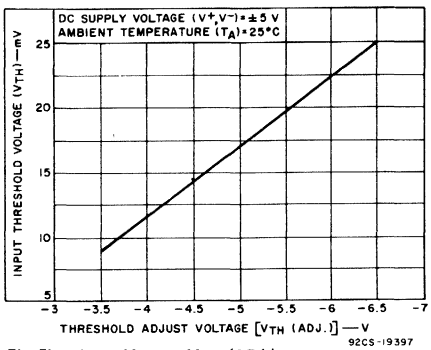


Fig. 7b – Input V_{TH} vs. V_{TH} (ADJ.).

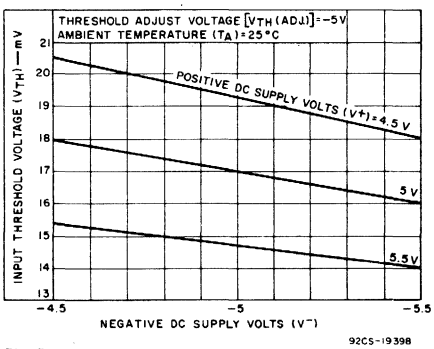


Fig. 7c – Input V_{TH} vs V^-.

CA1541D

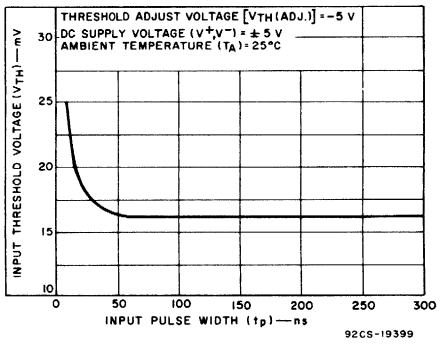
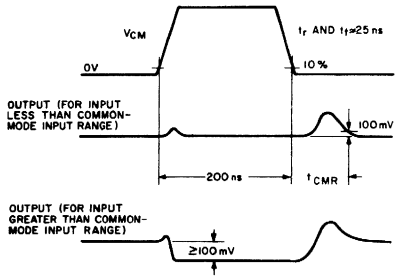


Fig. 7d – Input V_{TH} vs. input pulse width.



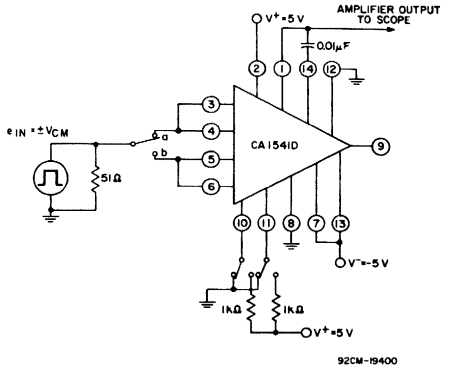


Fig. 8 – Common-mode input range test circuit with associated pulse wave forms.

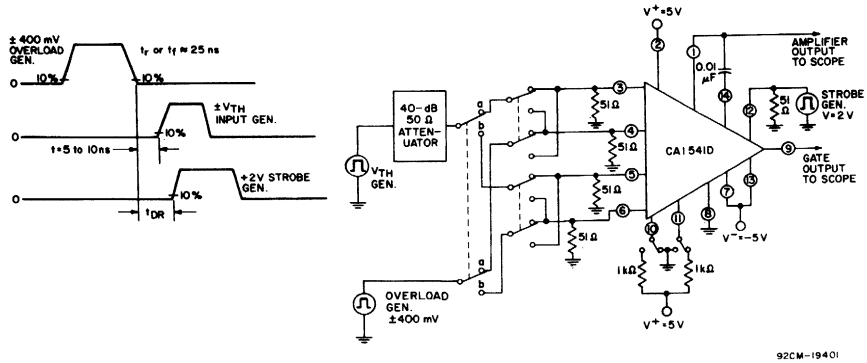


Fig. 9 – Differential-mode input range and recovery test circuit with associated pulse wave forms.

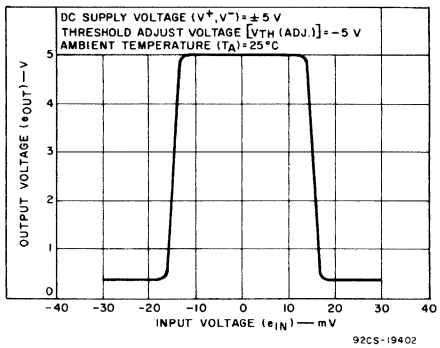


Fig. 10 – Input-output transfer characteristics.

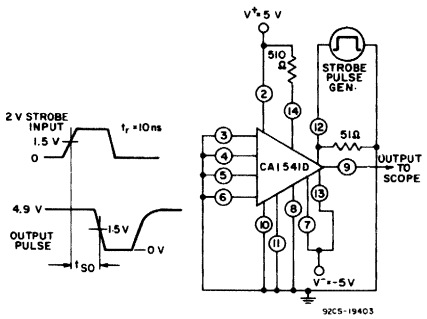


Fig. 11 – Strobe to output test circuit with associated pulse wave-forms.

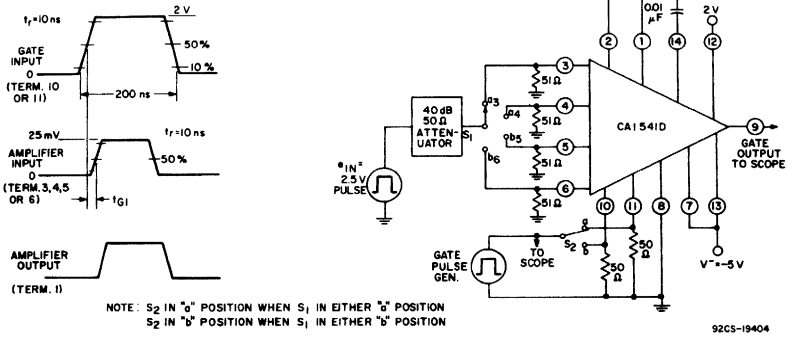


Fig. 12 – Gate input to amplifier input (t_{GI}) test circuit with associated pulse wave forms.

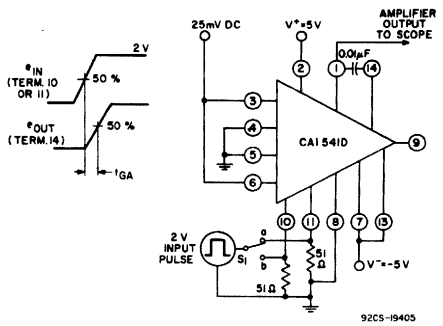


Fig. 13 – Gate input to amplifier output (t_{GA}) with associated pulse wave forms.

CA2111AE, CA2111AQ

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

The CA2111A, on a single monolithic chip, provides a multi-stage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60-dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristics of 3 cascaded differential amplifiers.

The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages (CA2111AE and CA2111AQ, respectively).

Features:

- **Direct replacement for ULN2111A and MC1357**
- **Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)**
- **Excellent AM rejection (45 dB typ. at 10.7 MHz)**
- **Provision for output from 3-stage IF amplifier section**
- **Low harmonic distortion**
- **Quadrature detection permits simplified single-coil tuning**
- **Extremely low AFC voltage drift over full operating-temperature range**
- **Minimum number of external parts required**

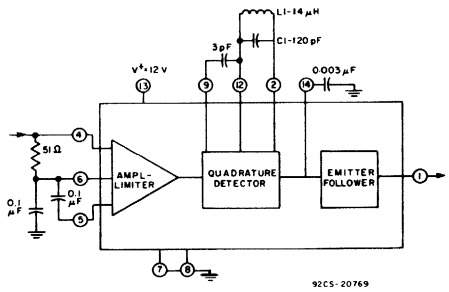


Fig. 1—Block diagram of CA2111A and associated outboard components.

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A=25°C

DC Supply Voltage [between terminals 13 (V^+) and 7 (V^-)]	16	V
Device Dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
DC Voltage:						
At Terminal 1	V_1	V^+ = 12V	–	5.4	–	V
		= 8V	–	3.7	–	
At Terminals 4, 5, 6, 10	$V_{4,5,6,10}$	V^+ = 8V	–	1.35	–	
At Terminals 2, 12	$V_{2,12}$		–	3.5	–	
DC Current (into Terminal 13)						mA
At V^+ = 8V			–	14	–	
At V^+ = 12V	I_{13}		–	16	–	
Amplifier Input Resistance	R_4	f_o = 10.7 MHz	–	7	–	kΩ
Amplifier Input Capacitance	C_4		–	11	–	pF
Detector Input Resistance	R_{12}		–	70	–	kΩ
Detector Input Capacitance	C_{12}		–	2.7	–	pF
Amplifier Output Resistance	R_{10}		–	60	–	Ω
Detector Output Resistance	R_1		–	200	–	Ω
De-Emphasis Resistance	R_{14}		–	8.8	–	kΩ

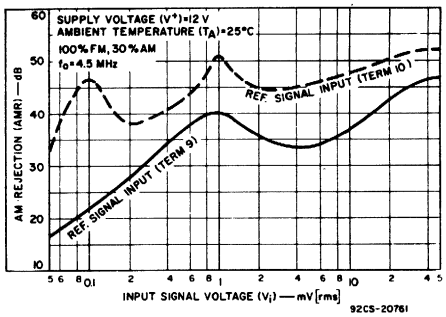


Fig. 2—AM rejection vs input voltage (4.5 MHz).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
FM Modulation Frequency = 400 Hz, Source Resistance = 50Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: f_o = 10.7 MHz, Δf = ± 75 KHz, V^+ = 12V		TEST CONDITIONS: f_o = 10.7 MHz, Δf = ± 75 KHz, V^+ = 8V		TEST CONDITIONS: f_o = 4.5 MHz, Δf = ± 25 KHz, V^+ = 12V		TEST CONDITIONS: f_o = 5.5 MHz, Δf = ± 50 KHz, V^+ = 12V		UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		LIMITS TYP.	LIMITS MAX.	LIMITS TYP.	LIMITS MAX.	LIMITS TYP.	LIMITS MAX.	LIMITS TYP.	LIMITS MAX.		
AMPL-LIMITER											
Input Limiting Threshold Voltage (4)	V_i(lim)	400	600	400	600	250	400	250	400	V (RMS)	7, 6, 8, 9
AM Rejection‡ *	AMR(1)	45	–	37	–	36	–	40	–	dB	2, 7, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	60	–	60	–	dB	7
DETECTOR											
Recovered Audio‡ Output Voltage (1)	V_o(AF)	0.48	–	0.3	–	0.72	–	1.2	–	V (RMS)	6, 7, 8, 9
Total Harmonic‡ Distortion	THD(1)	1	–	1	–	1.5	–	3	–	%	7

‡V_i = 10 mV (RMS) ▲$V_i \leq 50\ \mu V$ (rms) *100% FM, 30% AM

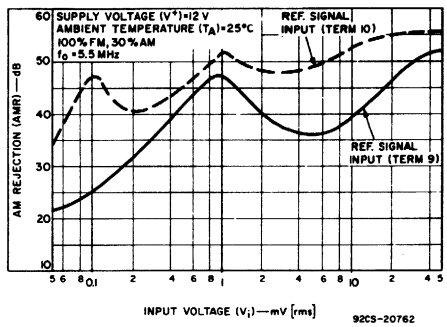


Fig. 3—AM rejection vs input voltage (5.5 MHz).

CA2111AE, CA2111AQ

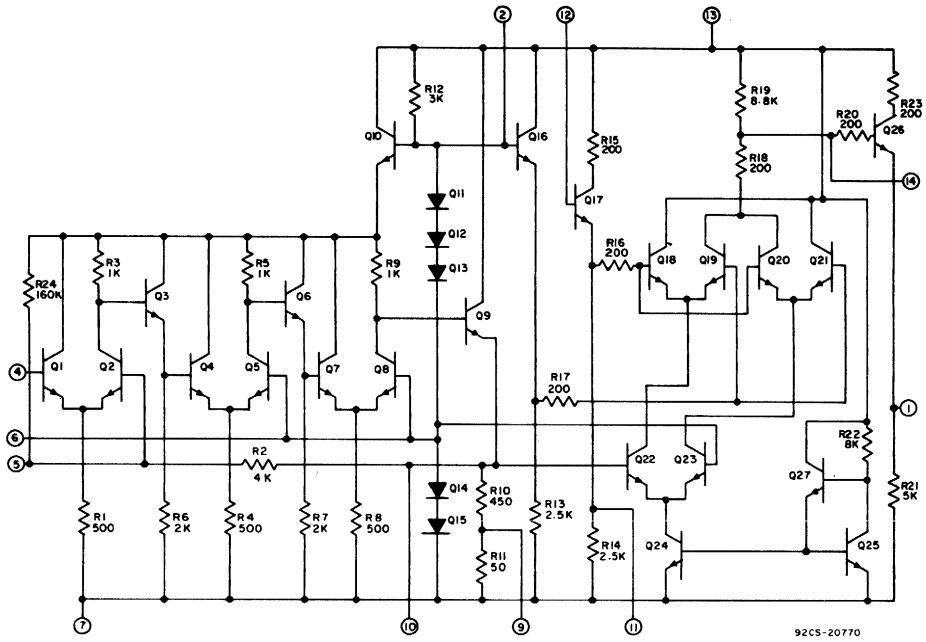


Fig. 4 –Circuit schematic–CA2111A

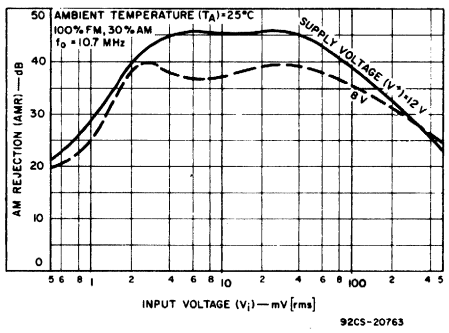


Fig. 5 –AM rejection vs input voltage (10.7 MHz).

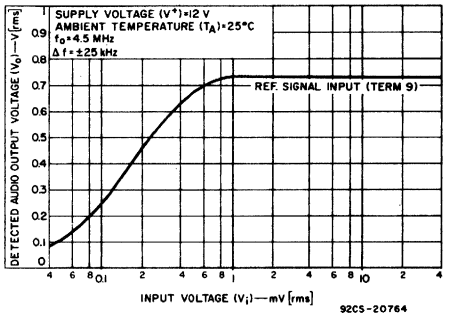
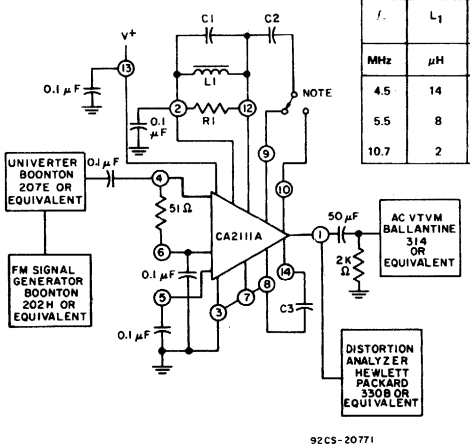


Fig. 6 –Detected audio output vs input voltage (4.5 MHz).

COMPONENT VALUES							DETECTOR TRANSFER CHARACTERISTICS	
f_o	L_1	C_1	R_1	Q	C_2	C_3	UPPER PEAK	LOWER PEAK
MHz	μH	pF	KΩ	–	pF	μF	MHz	MHz
4.5	14	120	20	30	3	0.003	4.58	4.42
5.5	8	100	20	30	3	0.003	5.63	5.37
10.7	2	120	3.9	20	4.7	0.01	10.9	10.5



NOTE:
Input to the quadrature coil can be from either terminal 9 or terminal 10. Terminal 9 is normally used because it lessens the possibility of overloads during tuning. The use of terminal 10 increases the limiting sensitivity significantly and has been used successfully in these tests.

Fig. 7 –Test circuit.

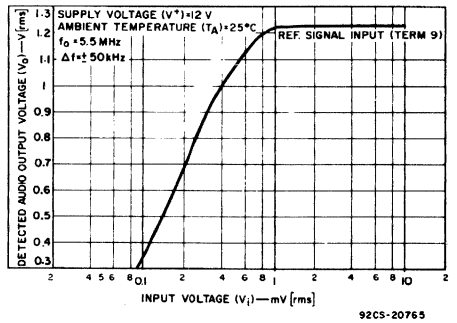


Fig. 8–Detected audio output vs input voltage (5.5 MHz).

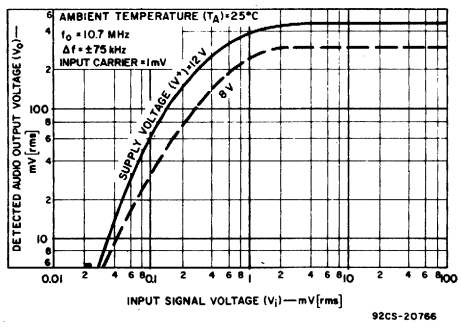


Fig. 9–Detected audio output voltage vs input voltage (10.7 MHz).

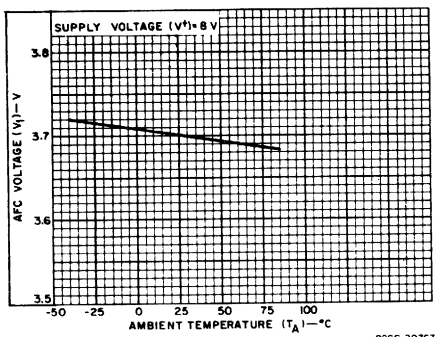


Fig. 10–AFC voltage vs ambient temp.

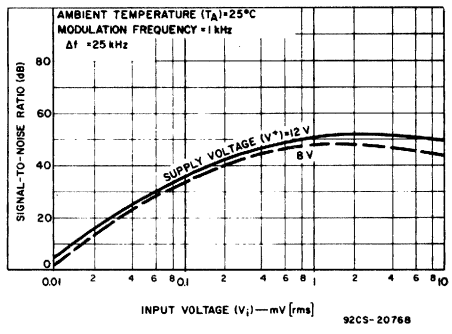


Fig. 11–Signal-to-noise ratio vs input voltage.

CA3000

DC Amplifier

- Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment
- Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- 10-Lead hermetic TO-5 style package
- Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids

HIGHLIGHTS

- Input Impedance . . . . . 195 KΩ typ.
- Voltage Gain. . . . . 30 dB typ.
- Common-Mode Rejection Ratio . . . 98 dB typ.
- Input Offset Voltage. . . . . 1.4 mV typ.
- Push-Pull Input and Output
- Frequency Capability
  DC to 30 MHz (with external C and R)
- Wide AGC Range. . . . . 90 dB typ.

APPLICATIONS

- Schmitt Trigger
- RC-Coupled Feedback Amplifier
- Mixer
- Comparator
- Modulator
- Crystal Oscillator
- Sense Amplifier

ABSOLUTE-MAXIMUM VOLTAGE LIMITS

at $T_{FA} = 25°C$

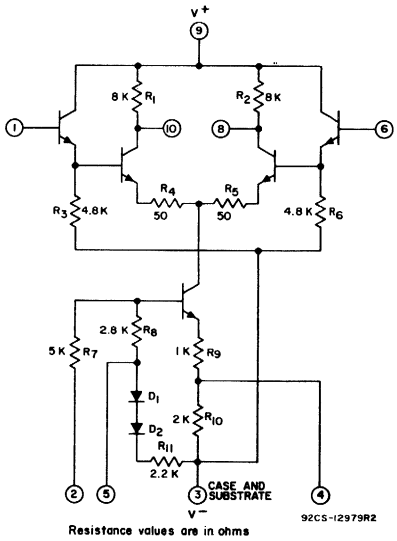
OPERATING-TEMPERATURE RANGE . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . −65°C to +150°C
LEAD-TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM POWER SUPPLY VOLTAGE — 16 or ±8 V

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE . . ±4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE . . ±2 V
MAXIMUM DEVICE DISSIPATION:
From −55°C to 85°C. . . . . 450 mW
Above 85°C . . . . . Derate 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_{FA} = 25°C$, $V_{CC} = +6V$, $V_{EE} = -6V$, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified	TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}			-	1.4	5	mV	2
Input Offset Current	I_{IO}			-	1.2	10	μA	2
Input Bias Current	I_{IB}			-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS 4 / 5						
		NC / NC		-	2.6	-	V	4
		NC / VEE		-	4.2	-	V	4
		VEE / NC		-	-1.5	-	V	4
		VEE / VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC / NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS								
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz	6	28	32	-	dB	5
		Double-Ended Output f = 1 kHz	6	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_i = 10 mV, R_s = 1 kΩ		-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz	6	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz	9	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz	11	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz	13	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}		-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz	15	80	90	-	dB	NONE



Resistance values are in ohms

Fig.1 SCHEMATIC DIAGRAM

STATIC CHARACTERISTICS FOR TYPE CA3000

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

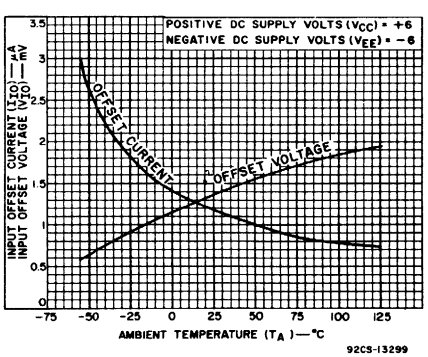


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

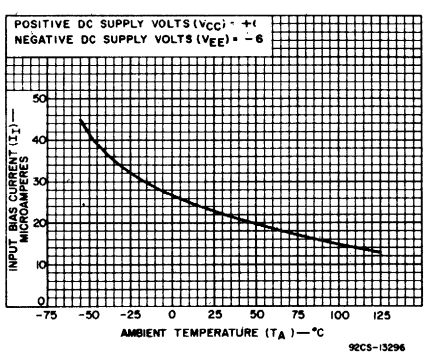


Fig.3

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

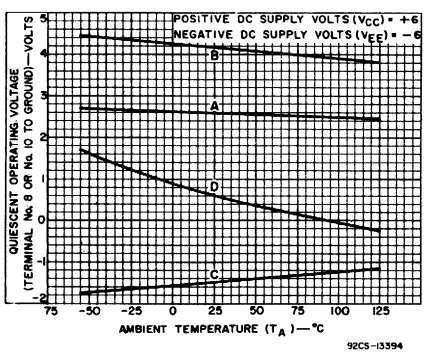


Fig.4

CA3000

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

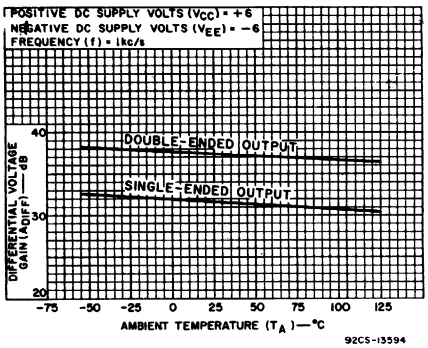


Fig.5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

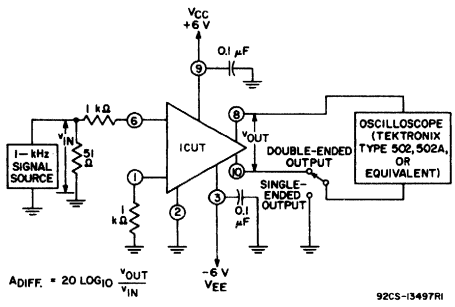


Fig.6

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

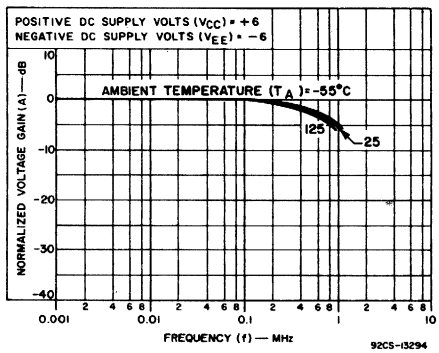


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

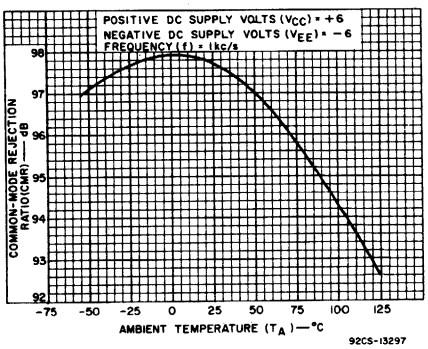


Fig.8

COMMON-MODE REJECTION RATIO TEST CIRCUIT

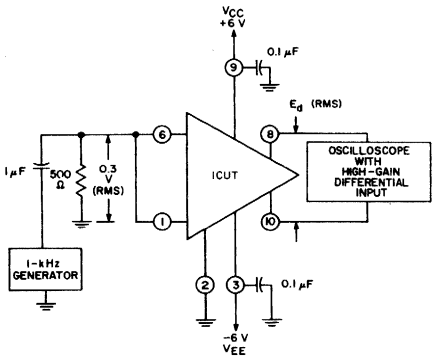


Fig.9

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

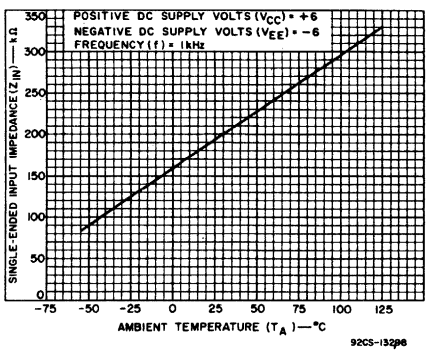


Fig.10

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

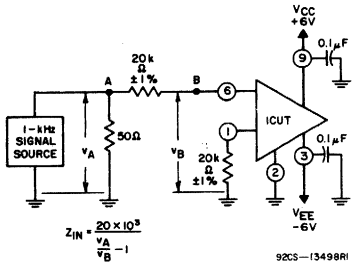


Fig.11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

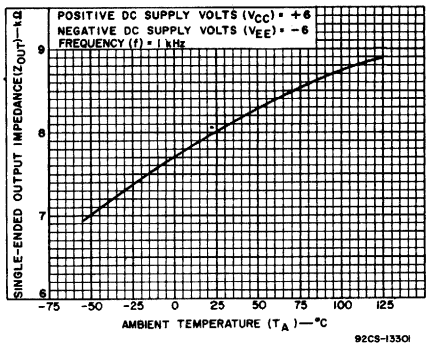


Fig.12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT

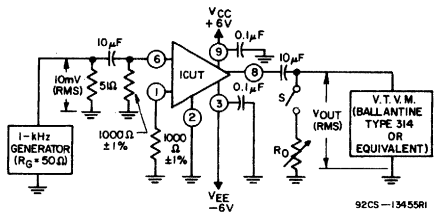


Fig.13

TOTAL HARMONIC DISTORTION vs TEMPERATURE

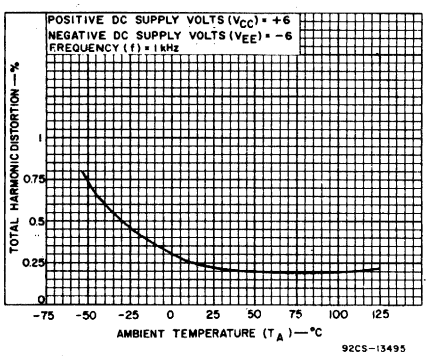


Fig.14

AGC RANGE TEST CIRCUIT

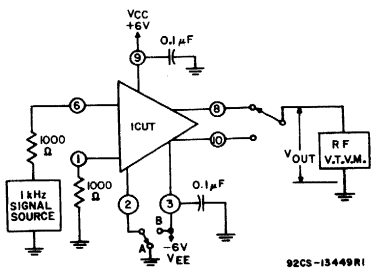


Fig.15

CA3001

Video and Wide-band Amplifier

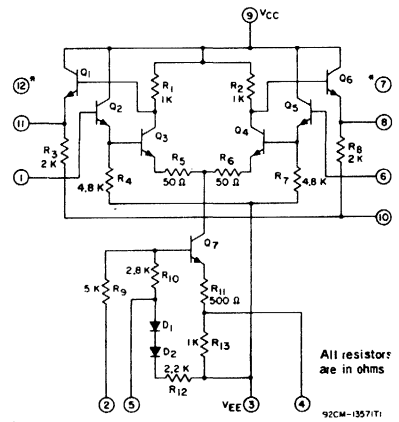
- Designed for use in Video Systems and Communication Equipment
- Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility
- 12-Lead Hermetic TO-5 Style Package
- Built-in temperature stability for operation from -55°C to +125°C
- Emitter follower input & output
- Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.

HIGHLIGHTS

- Push-Pull Input & Output
- AGC Range ..... 60 dB typ.
- Bandwidth ..... 29 MHz
- Input Resistance ..... 150 kΩ typ.
- Output Resistance ..... 45 Ω typ.
- Voltage Gain ..... 19 dB typ.
- Input Offset Voltage .... 1.5 mV typ.

APPLICATIONS

- Schmitt Trigger
- Mixer
- Modulator
- DC, IF, & Video Amplifier



* Internal Connection – DO NOT USE

Fig.1 - Schematic Diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals. All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE	-55°C to +125°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2.5 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

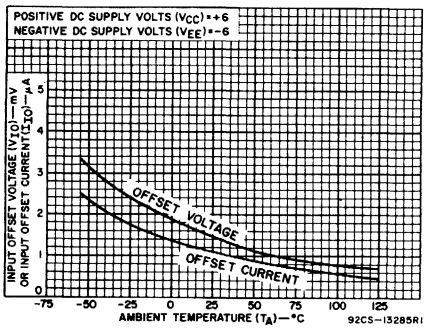


Fig.2 - Input offset voltage and current vs. temperature.

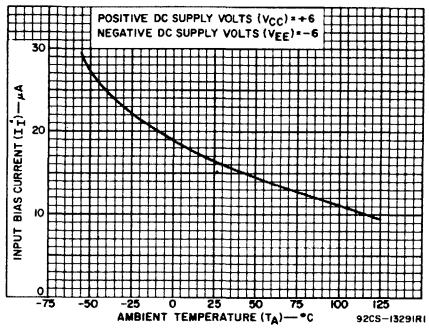


Fig.3 - Input bias current vs. temperature.

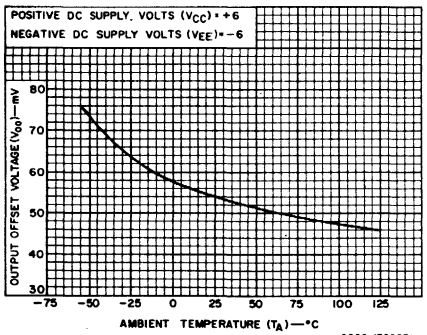


Fig. 4 - Output offset voltage vs. temperature.

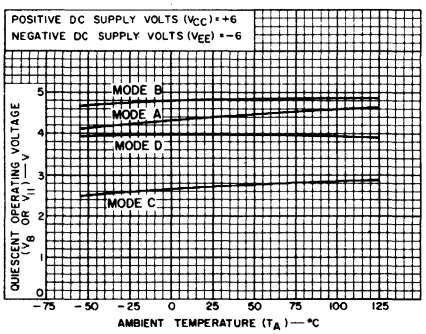


Fig. 5 - Quiescent operating voltage vs. temperature.

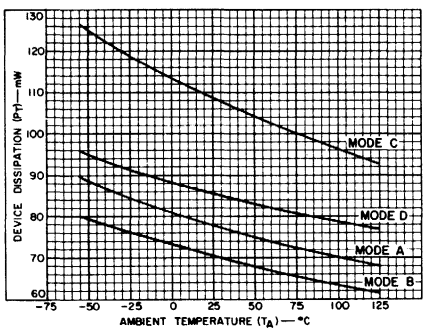


Fig. 6 - Device dissipation vs. temperature.

CA3001

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6 V, V_{EE} = −6 V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified	TEST CIRCUITS	LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		12	-	1.5	-	mV	2
Input Offset Current	I_{IO}		13	-	1	10	μA	2
Input Bias Current	I_I		13	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ		-	54	300	mV	4
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE A: 4 NC, 5 NC		3.8	4.4	5	V	5
		MODE B: 4 NC, 5 V_{EE}		-	4.8	-	V	5
		MODE C: 4 V_{EE}, 5 NC		-	2.7	-	V	5
		MODE D: 4 V_{EE}, 5 V_{EE}		-	4	-	V	5
Device Dissipation	P_D	A: 4 NC, 5 NC		60	78	120	mW	6
		B: 4 NC, 5 V_{EE}		-	71	-	mW	6
		C: 4 V_{EE}, 5 NC		-	110	-	mW	6
		D: 4 V_{EE}, 5 V_{EE}		-	86	-	mW	6
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz		16 10	19 14	- -	dB dB	7, 8
Bandwidth at -3 dB Point	BW	R_S = 50Ω		16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz		-	5	-	V_{P-P}	NONE
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ	11	-	5	8	dB	
		f = 11.7 MHz, R_S 1 KΩ	11	-	7.7	-	dB	9
Common-Mode Rejection Ratio	CMRR	f 1 KHz		70	88	-	dB	10
Input Impedance Components:								
Parallel Input Resistance	R_{IN}	f 1.75 MHz		50	140	-	KΩ	11
Parallel Input Capacitance	C_{IN}	f 1.75 MHz		-	3.4	7	pF	11
Output Resistance	R_{OUT}	f 1.75 MHz		-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f 1.75 MHz		55	60	-	dB	NONE

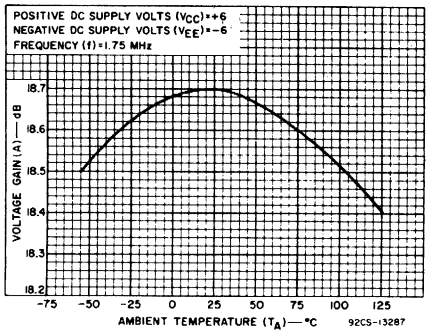


Fig. 7 - Differential voltage gain vs. temperature.

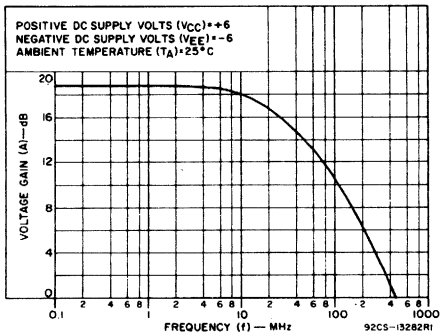


Fig. 8 - Differential voltage gain vs. frequency.

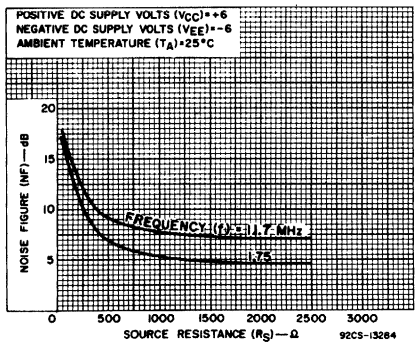


Fig. 9 - Noise figure vs. source resistance and frequency.

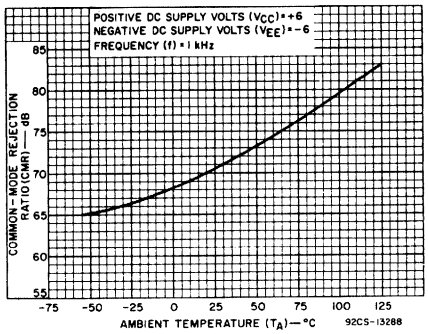


Fig. 10 - Common-mode rejection ratio vs. temperature.

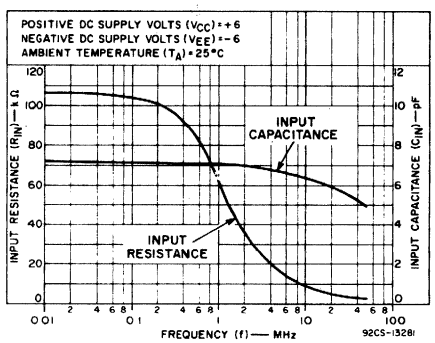
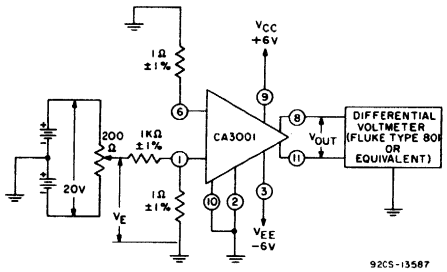


Fig. 11 - Input impedance components vs. frequency.

CA3001



1. Adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig. 12 - Input offset voltage test circuit.

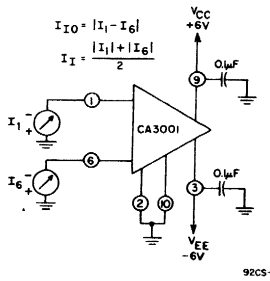
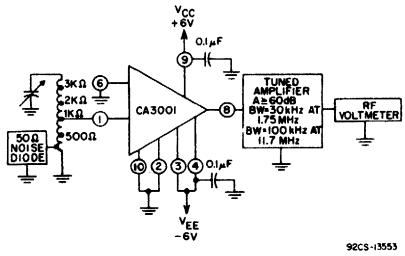
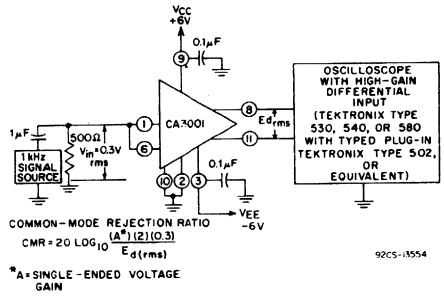


Fig. 13 - Input offset current and input bias current test circuit.



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig. 14 - Noise figure test circuit.



*A = SINGLE-ENDED VOLTAGE GAIN

Fig. 15 - Common-mode rejection ratio test circuit.

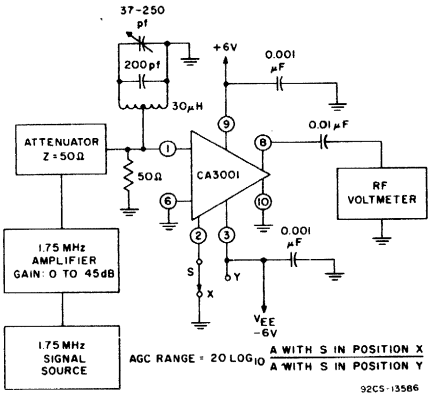


Fig. 16 - AGC range test circuit.

CA3002

IF Amplifier

- Designed for use in Communication Equipment
- Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility
- 10-Lead hermetic TO-5 style package
- Built-in temperature stability for operation from -55°C to +125°C
- Companion Application Note ICAN-5036 "Application of the RCA-3002 Integrated-Circuit IF Amplifier" covers different operating modes, cross modulation, gain control, 4-stage amplifier design, and an envelope and product detector analysis.

HIGHLIGHTS

- Input Resistance . . . . . 100 kΩ typ.
- Output Resistance . . . . . 70 Ω typ.
- Voltage Gain . . 24 dB typ. @ 1.75 MHz
- Push-Pull Input, Single-Ended Output
- -3 dB Bandwidth . . . . . 11 MHz typ.
- AGC Range . . . . . 80 dB typ.
- Useful Frequency Range DC to . .15 MHz

APPLICATIONS

- Product Detector
- AM Detector
- IF & Video Amplifier
- Schmitt Trigger

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at T_A = 25°C

COMMON-MODE INPUT SIGNAL VOLTAGE	±2 V
MAXIMUM POWER SUPPLY VOLTAGE	16 V or ±8 V
OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

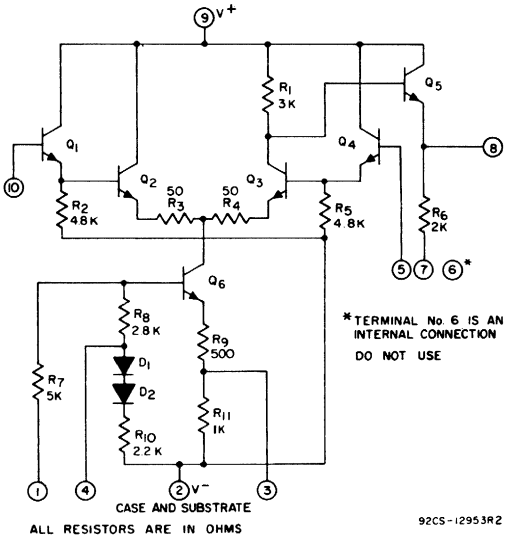


Fig. 1 — Schematic diagram.

STATIC CHARACTERISTICS AND TEST CIRCUITS

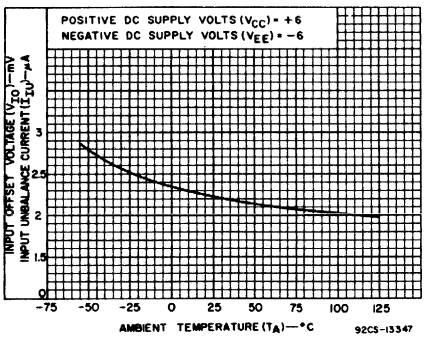


Fig.2 - Input unbalance voltage & current vs temperature.

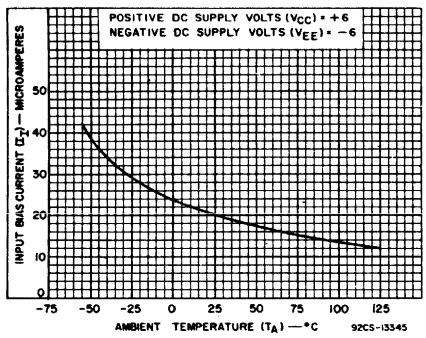


Fig.3 - Input bias current vs temperature.

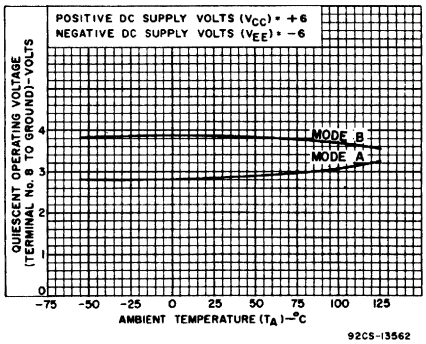


Fig.4 - Quiescent operating voltage vs temperature.

STATIC CHARACTERISTICS AND TEST CIRCUITS

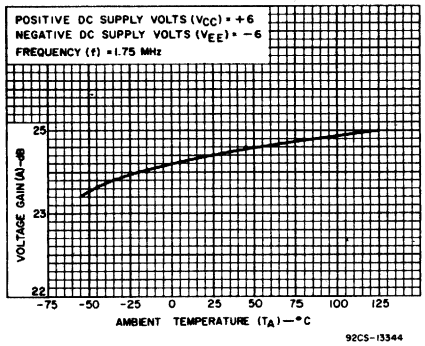


Fig. 5a - Differential voltage gain vs temperature.

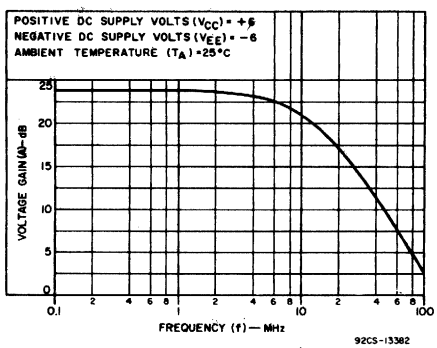


Fig. 5b - Differential voltage gain vs frequency.

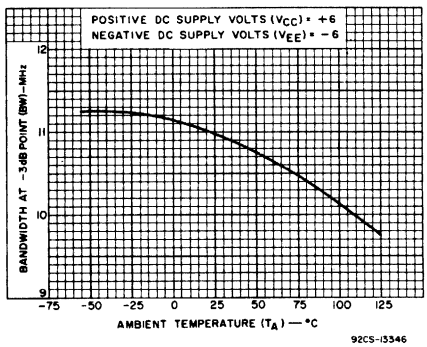


Fig. 6 - Bandwidth at -3 dB point vs temperature.

CA3002

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	2.2	-	mV	2
Input Unbalance Current	I_{IU}			-	2.2	10	μA	2
Input Bias Current	I_I			-	20	36	μA	3
Quiescent Operating Voltage		MODE: A — TERMINAL 2: V_{EE}, TERMINAL 4: NC		-	2.8	-	V	4
		MODE: B — TERMINAL 2: V_{EE}, TERMINAL 4: V_{EE}		-	3.9	-	V	4
Device Dissipation	P_T			-	55	-	mW	None
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-Ended Input and Output)	A_{DIFF}	V_{IN} = 10 mV, f = 1.75 MHz, R_S = 50Ω		19	24	-	dB	5 & 5
Bandwidth at -3 dB Point	BW	R_S = 50Ω, V_{IN} = 10 mV		-	11	-	MHz	6
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	-		-	5.5	-	V_{P-P}	None
Noise Figure	NF	f = 1.75 MHz R_S = 1 kΩ	8	-	4	8	dB	7
Input Impedance Components: Parallel Input Resistance	R_{IN}	f = 1.75 MHz	None	-	100k	-	Ω	None
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz	None	-	4	-	pF	None
Output Resistance	R_{OUT}	f = 1.75 MHz	14	-	70	-	Ω	9a & 9b
AGC Range (Maximum Voltage Gain to Complete Cutoff	AGC	f = 1.75 MHz	13	60	80	-	dB	12

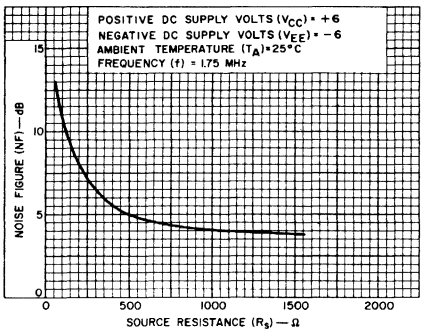
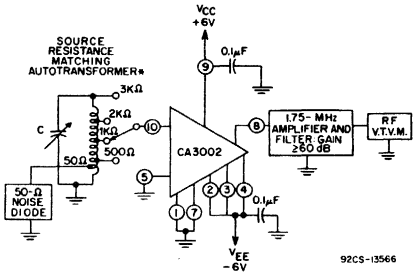


Fig. 7 - Noise figure vs source resistance.



*Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 8 - Noise figure.

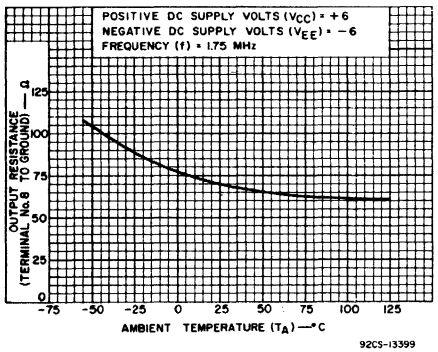


Fig. 9a - Output resistance vs temperature.

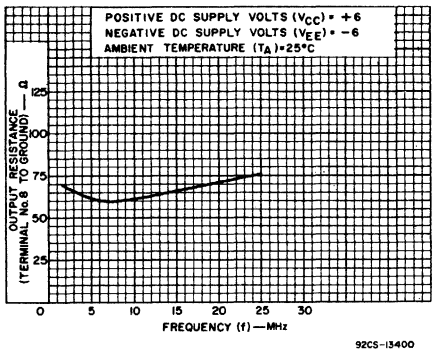


Fig. 9b - Output resistance vs frequency.

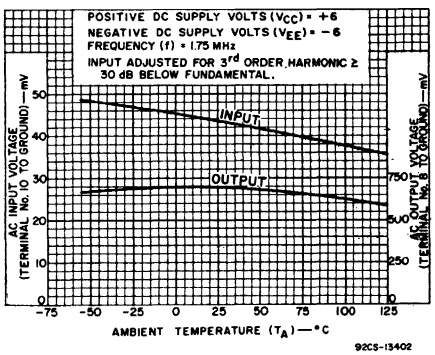
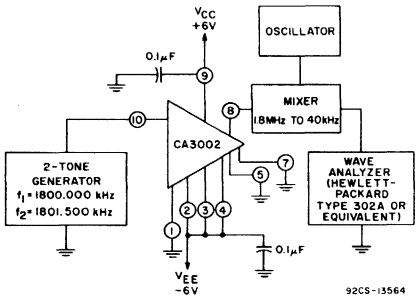


Fig. 10 - Input level for — 30 dB intermodulation vs. temperature



1) Increase both input-signal tones until the $2f_2$-f1 and $2f_1$-f2 output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 11 - Intermodulation Test Circuit.

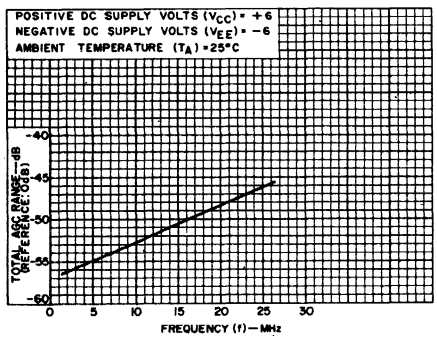
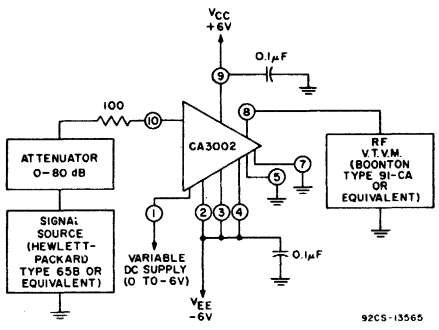


Fig. 12 - AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

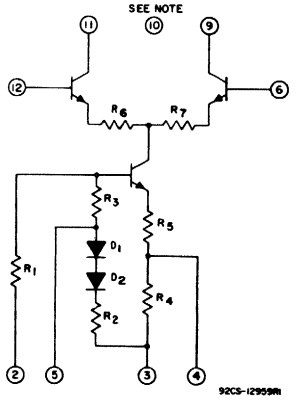
Fig. 13 - AGC range.

CA3004

RF Amplifier

- Designed for use in Communications Equipment
- Balanced Differential-Amplifier Configuration with Controlled Constant-Current Source Provides Unexcelled Versatility
- 12-Lead Hermetic TO-5 Style Package
- Built-in Temperature Stability for Operation from -55° C to +125° C
- Similar to RCA CA3005 and CA3006, plus Emitter-Degeneration Resistors to Provide More Linear Transfer Characteristic and Increased Input-Signal Handling Capability
- Companion Application Note ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC, limiter, detector, and amplifier design considerations.
- Push-Pull Input and Output
- Wide and Narrow-Band Amplifier
- AGC
- Detector
- Operation from DC to 100 Mc/s
- Mixer
- Limiter
- Modulator
- RF, IF, and Video Frequency Capability

SCHEMATIC DIAGRAM FOR CA3004



NOTE: Connect Terminal No. 10 to most positive dc supply voltage used for circuit.

Fig. 1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated circuit conditions for other terminals. All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	NO CONNECTION			
2	-9.5	0	6	0
			12	0
			3	-9.5
			9	+6
			10	+6
			11	+6
3	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
4	-12	0	2	0
			6	0
			9	+6
			10	+6
			11	+6
			12	0
5	-6	0	2,6,12	0
			3	-6
			9	+6
			10	+6
			11	+6
6	-3.5	+3.5	2	0
			3	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
7	NO CONNECTION			
8	NO CONNECTION			
9	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
10	0	+12	2	0
			3	-6
			6	0
			9	+6
			11	+6
			12	0
11	0	+12	2	0
			3	-6
			6	0
			10	+6
			11	+6
			12	0
12	-3.5	+3.5	2	0
			3	-6
			6	0
			9	+6
			10	+6
			11	+6
CASE	INTERNALLY CONNECTED TO TERMINAL NO.3 (SUBSTRATE) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	-2.5 V, +3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004 (Figs. 2 to 8)

INPUT OFFSET VOLTAGE AND CURRENT VS TEMPERATURE

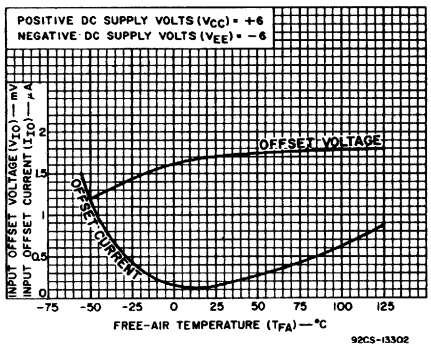


Fig. 2

INPUT BIAS CURRENT VS TEMPERATURE

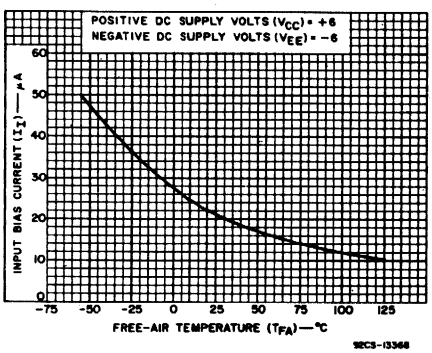


Fig. 3

CA3004

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25° C, V_{CC} = +6V, V_{EE} = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS TYPE CA3004				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
Quiescent Operating Current	I_9 or I_{11}	TERMINALS 4	5						
		NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

INPUT OFFSET VOLTAGE TEST CIRCUIT

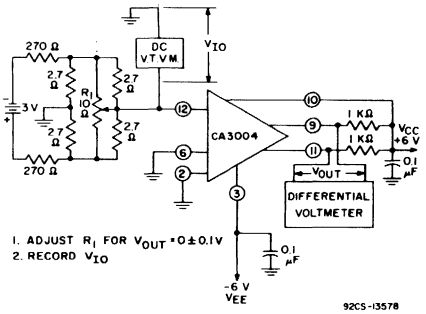


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT

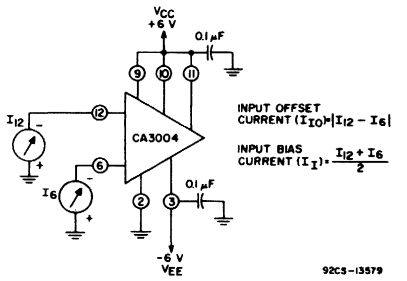


Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

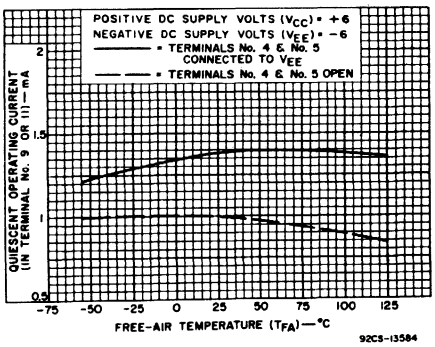
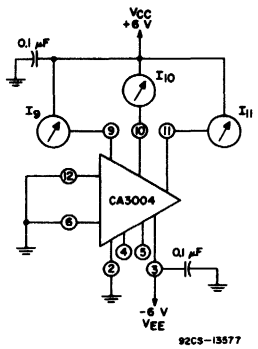


Fig.6

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$

Fig.8

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

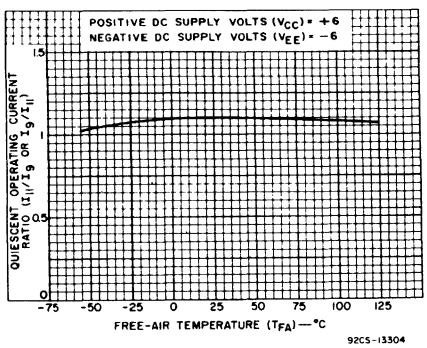


Fig.7

CA3004

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3004 (Figs. 9 to 14)

POWER GAIN VS FREQUENCY

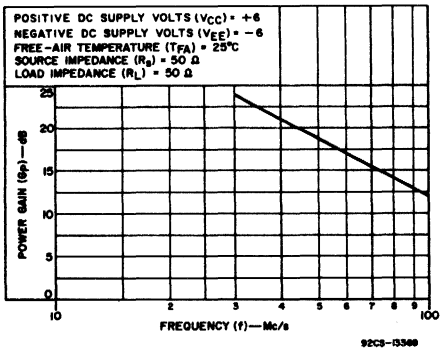


Fig.9

NOISE FIGURE VS FREQUENCY

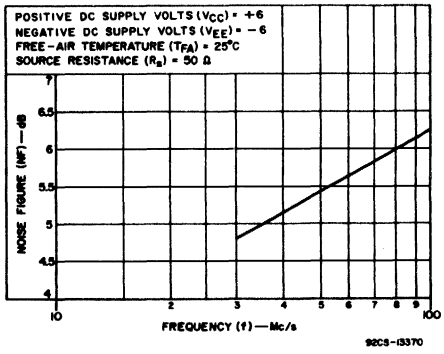


Fig.10

100 Mc/s POWER GAIN AND NOISE FIGURE TEST CIRCUIT

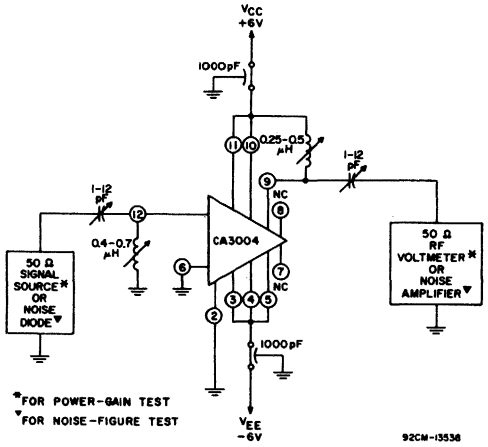


Fig.11

COMMON-MODE REJECTION RATIO VS TEMPERATURE

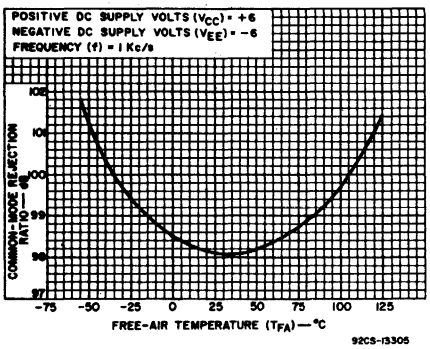


Fig.12

COMMON-MODE REJECTION RATIO TEST CIRCUIT

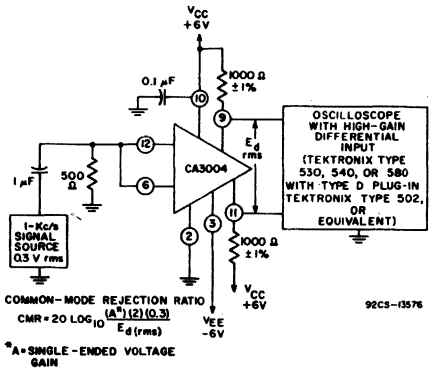


Fig.13

AGC RANGE TEST CIRCUIT

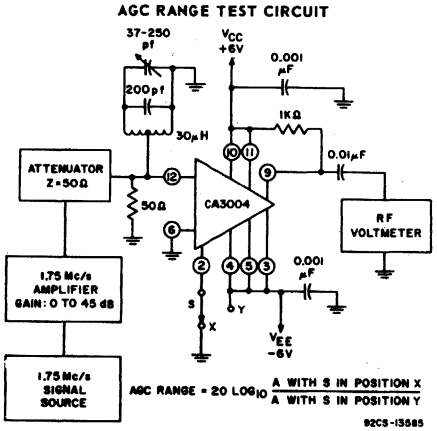


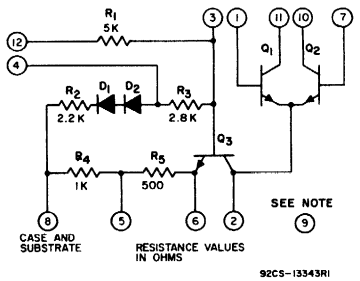
Fig.14

CA3005, CA3006

RF Amplifiers

- Designed for use in Communications Equipment
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility
- 12-Lead Hermetic TO-5 Style Package.
- Built-in Temperature Stability for Operation from -55° C to +125° C
- Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.
- Push-Pull Input and Output
- Wide and Narrow Band Amplifier
- AGC
- Detector
- RF, IF, and Video Frequency Capability
- Operation from DC to 100 MHz
- Mixer
- Limiter
- Modulator
- Cascode Amplifier

SCHEMATIC DIAGRAM FOR CA3005 AND CA3006



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig.1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7 8 9 10 11 12	0 -6 +6 +6 +6 0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1 7 8 9 10 11 12	0 0 -9.5 +6 +6 +6 0
4	-6	0	1 7 8 9 10 11 12	0 0 -6 +6 +6 +6 0
5	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
6	-6	0	1 7 9 10 11 12	0 0 +6 +6 +6 -6
7	-3.5	+3.5	1 8 9 10 11 12	0 -6 +6 +6 +6 0
8	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
9	0	+12	1 7 8 10 11 12	0 0 -6 +6 +6 0
10	0	+12	1 7 8 9 11 12	0 0 -6 +6 +6 0
11	0	+12	1 7 8 9 10 12	0 0 -6 +6 +6 0
12	-9.5	0	8 9 10 11	-9.5 +6 +6 +6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE	-55°C to +125°C
STORAGE-TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	±3.5 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	-2.5 V, +3.5 V
MAXIMUM DEVICE DISSIPATION	300 mW

INPUT OFFSET VOLTAGE AND CURRENT

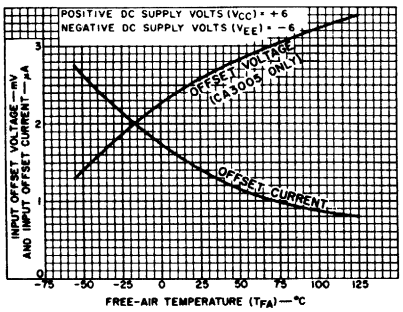


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT

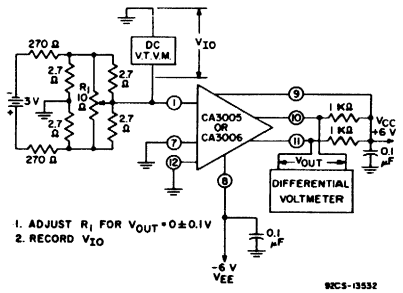


Fig.3

INPUT BIAS CURRENT

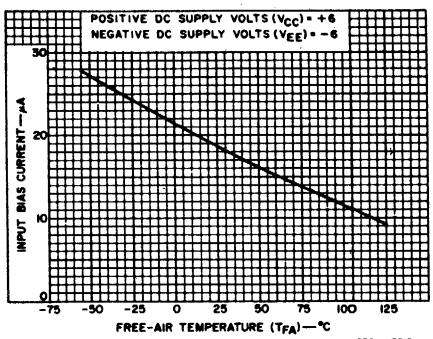


Fig.4

CA3005, CA3006

ELECTRICAL CHARACTERISTICS, at $T_A = 25^o$ C, $V_{CC} = +6V$, $V_{EE} = -6V$

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted			TEST CIRCUITS	LIMITS TYPE CA3005			LIMITS TYPE CA3006				TYPICAL CHARACTERISTICS CURVES
					Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS													
Input Offset Voltage	V_{IO}				Fig.3	–	2.6	5	–	0.8	1	mV	Fig.2
Input Offset Current	I_{IO}				Fig.4	–	1.4	–	–	1.4	–	μA	Fig.2
Input Bias Current	I_{IB}				Fig.4	–	19	40	–	19	40	μA	Fig.5
Quiescent Operating Current	I_{10} or I_{11}	TERMINALS 4	5										
		NC	NC		Fig. 10	–	1	–	–	1	–	mA	Fig.6
		NC	-V_{EE}		Fig. 10	–	2.7	–	–	2.7	–	mA	NONE
		-V_{EE}	NC		Fig. 10	–	0.45	–	–	0.45	–	mA	NONE
		-V_{EE}	-V_{EE}		Fig. 10	–	1.25	–	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	$\frac{I_{10}}{I_{11}}$				Fig. 10	–	1.05	–	–	1.05	–	–	Fig.7
Device Dissipation	P_T				Fig. 10	–	26	–	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS													
Power Gain	G_p	f = 100 MHz	Cascode Configuration		Fig. 11	16	20	–	16	20	–	dB	Fig.9
			Differential-Ampl. Configuration		Fig.12	14	16	–	14	16	–	dB	Fig.11
Noise Figure	NF	f = 100 MHz	Cascode Configuration		Fig. 11	–	7.8	9	–	7.8	9	dB	Fig.13
			Differential Ampl. Configuration		Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
Common-Mode Rejection Ratio	CMR	f = 1 kHz				–	101	–	–	101	–	dB	Fig.15
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz				-60	–	–	-60	–	–	dB	NONE

QUIESCENT OPERATING CURRENT

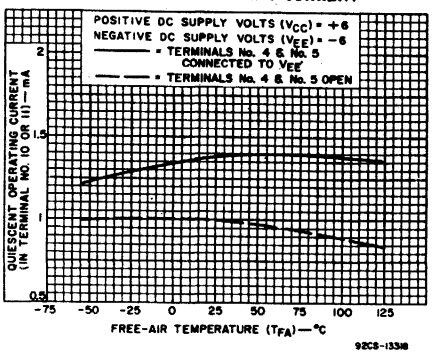


Fig. 5

QUIESCENT OPERATING CURRENT RATIO

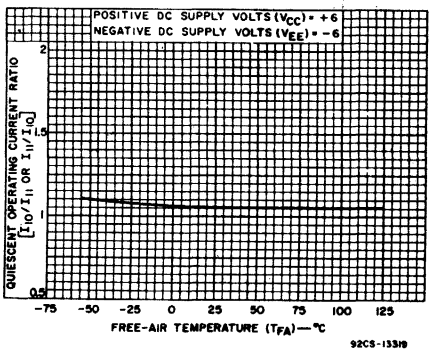


Fig. 6

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

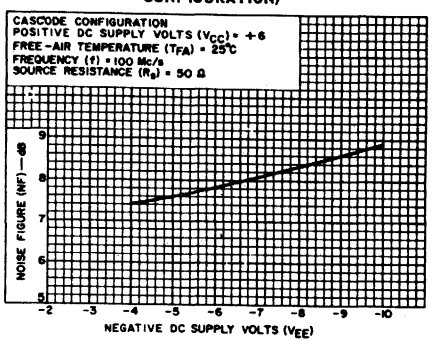


Fig. 9

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

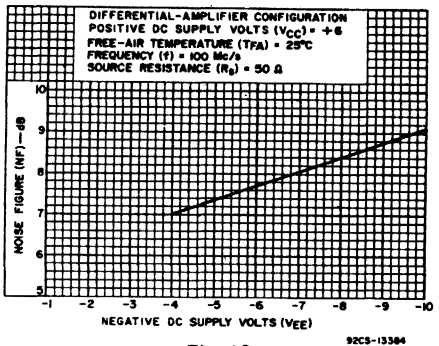


Fig. 12

POWER-GAIN (CASCODE CONFIGURATION)

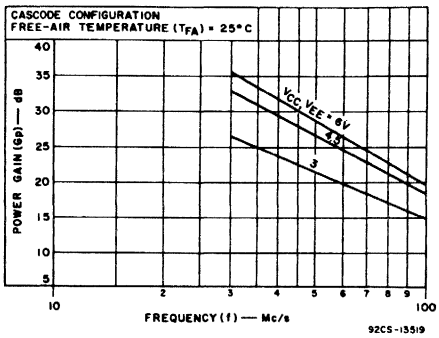


Fig. 7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

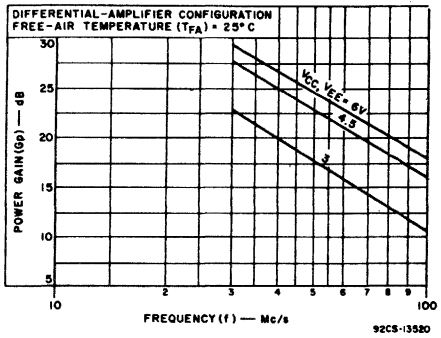
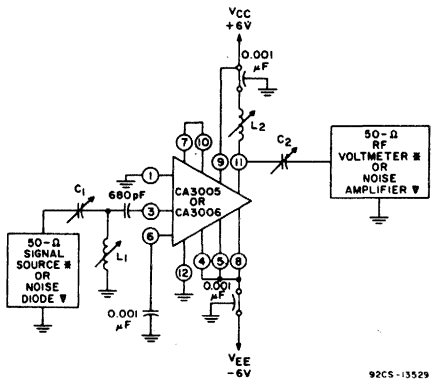


Fig. 8

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)



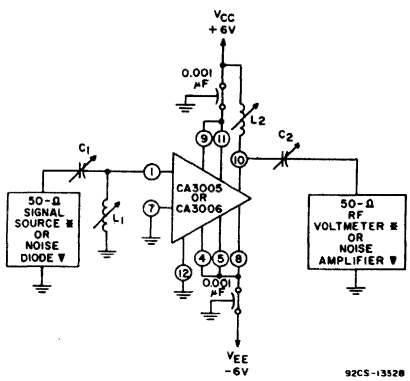
f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 10

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 11

CA3005, CA3006

COMMON-MODE-REJECTION RATIO

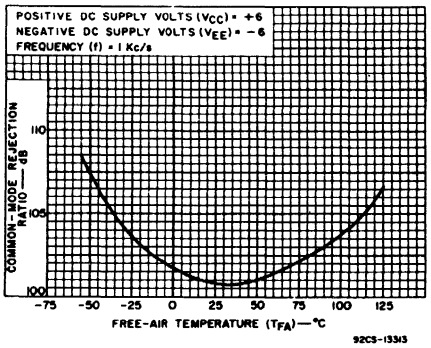


Fig. 13

COMMON–MODE-REJECTION RATIO TEST CIRCUIT

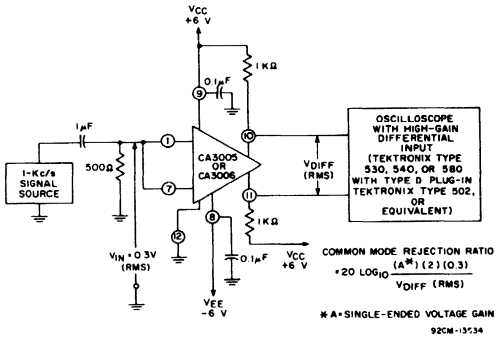


Fig. 14

AGC RANGE TEST CIRCUIT

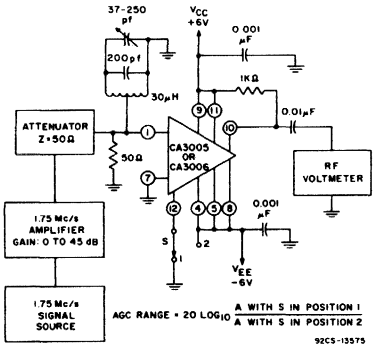


Fig. 15

CA3007

AF Amplifier

- Designed for use in Sound Systems and Communication Equipment
- Balanced differential-amplifier configuration with controlled constant-current source provides for both audio amplification and phase inversion
- Built-in temperature stability for operation from -55°C to +125°C
- Eliminates need for audio driver transformer
- Companion Application Note, ICAN 5037 "Application of the RCA-CA3007 Integrated Circuit Audio Driver" covers design of a dual supply audio driver in a direct-coupled audio amplifier, and a single supply audio driver in a capacitor-coupled audio amplifier
- **Supplied in the hermetic 12-lead TO-5 style package**

HIGHLIGHTS

- Input Impedance. . . . 4 kΩ typ.
- Output Impedance . . . 60 Ω typ.
- Power Gain . . . . . 22 dB typ.
- Push-Pull Input & Output
- Direct Coupling to Class B Audio Output Stage

APPLICATIONS

- Audio Amplifier
- Audio Driver

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C
LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C
MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V
MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . ±2.5 V
MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25°C, V_{CC} = +6 V, V_{EE} = -6 V,

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Pin 4 Not Connected Unless Otherwise Noted	TEST CIRCUITS	LIMITS TYPE CA3007				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS								
Input Unbalance Voltage	V_{IU}		3	–	0.57	5	mV	2
Input Unbalance Current	I_{IU}		3	–	0.57	5	μA	2
Input Bias Current	I_I		3	–	11	34	μA	4
Quiescent Operating Voltage	V_8 or V_{10}		3	–	0.87	–	V	5
Device Dissipation	P_T		3	–	30	–	mW	NONE
DYNAMIC CHARACTERISTICS								
Power Gain	G_P	f = 1 Kc/s	6	20	22	–	dB	NONE
Total Harmonic Distortion	THD	f = 1 Kc/s	6	–	0.28	–	%	NONE
Input Impedance	Z_{IN}	f = 1 Kc/s	7	–	4K	–	Ω	NONE
Common-Mode Rejection Ratio	CMR	f = 1 Kc/s	9(A) 9(B)	–	77	–	dB	8

SCHEMATIC DIAGRAM

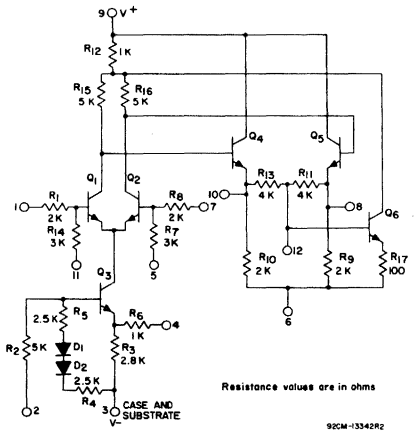


Fig.1

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUIT FOR CA3007

INPUT UNBALANCE VOLTAGE AND CURRENT vs TEMPERATURE

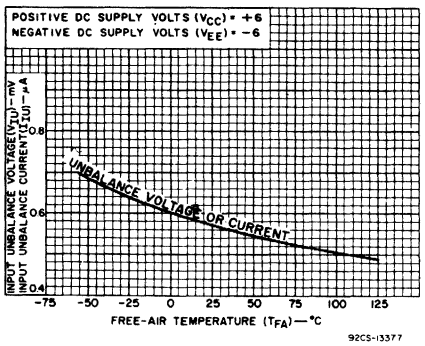
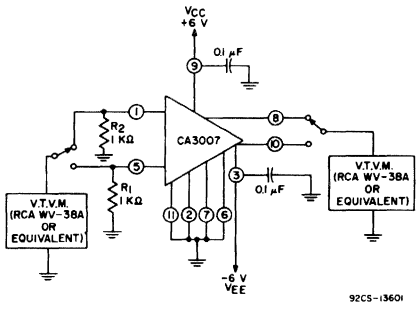


Fig.2

INPUT UNBALANCE VOLTAGE & CURRENT, INPUT BIAS CURRENT, QUIESCENT OPERATING VOLTAGE, AND DEVICE DISSIPATION TEST CIRCUIT



R_1 and R_2 matched to ±1%.
$P_T = V_{CC}I_9 + V_{EE}I_3$
I_9 = Direct Current into Terminal No.9
I_3 = Direct Current out of Terminal No.3

Fig.3

INPUT BIAS CURRENT vs TEMPERATURE

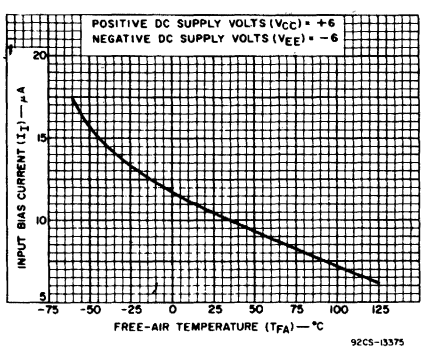


Fig.4

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

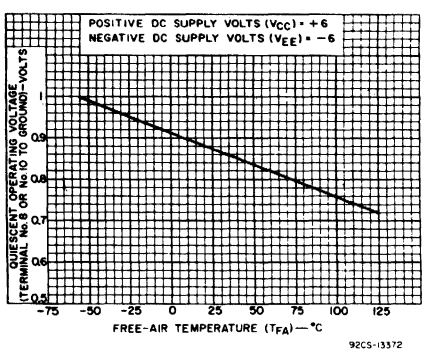


Fig.5

CA3007

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25° C

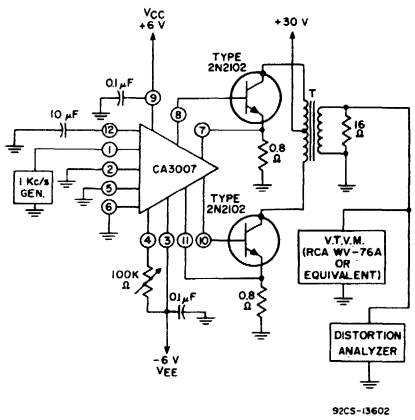
Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
2	-8	0	3	-8
			6	0
			7	0
			9	+6
			11	0
3	-10	0	6	0
			7	0
			9	+6
			11	0
4	-8.5	0	6	0
			7	0
			9	+6
			11	0
5	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
6	-3	0	2	0
			3	-6
			7	0
			9	+6
			11	0
7	-2.5	+2.5	1	0
			2	0
			3	-6
			5	0
			6	0
			9	+6

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
9	0	+10	2	0
			3	-6
			6	0
			7	0
			11	0
10	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
11	-2.5	+2.5	1	0
			2	0
			3	-6
			6	0
			7	0
			9	+6
12	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

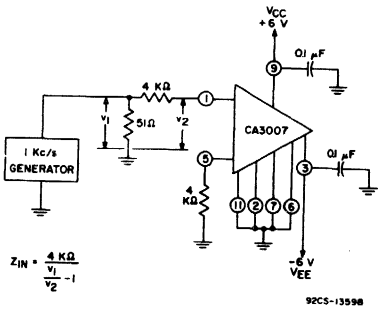


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

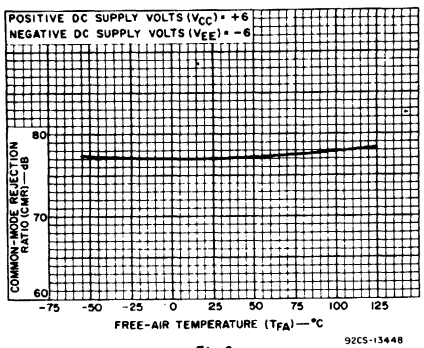
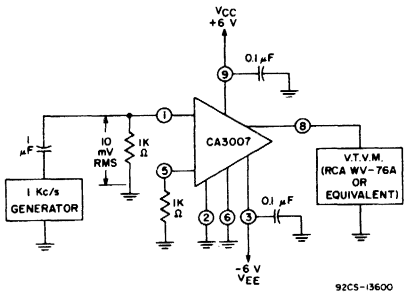
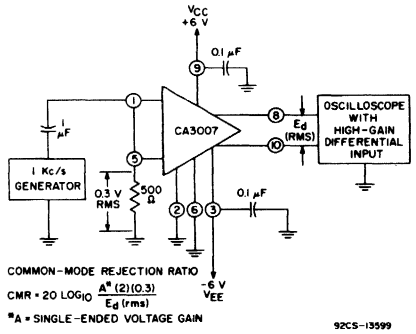


Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS



(A) Single-Ended Differential Voltage Gain



(B) Common-Mode Voltage Gain

Fig.9

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

Operational Amplifiers

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3008	CA3016	14-Lead Flat Pack
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3015L	Beam-Lead Device
CA3037	CA3030	14-Lead Plastic Dual In-Line (TO-116)
	CA3038	14-Lead Ceramic Dual In-Line (TO-116)

HIGHLIGHTS

	6 V Types	12 V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Output Impedance	200	92	Ω typ.
• Input Offset Voltage	1	1	mV typ.
• Static Power Drain at ± 12 V	-	175	mW typ.
± 6 V	30	30	mW typ.
± 3 V	7	7	mW typ.

- All types are electrically identical within their voltage groups
- The CA3105 is available in a sealed-junction Beam-Lead version (CA3015L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications.
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for flatpack, TO-5 style, and ceramic dual in-line packages; 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers"

APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

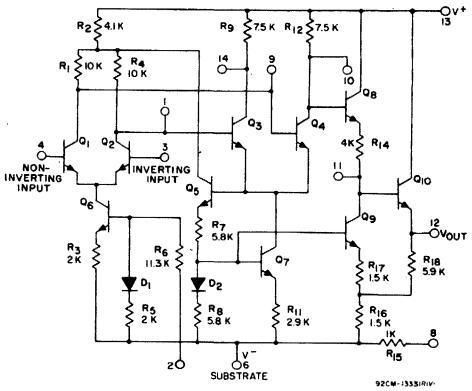
Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

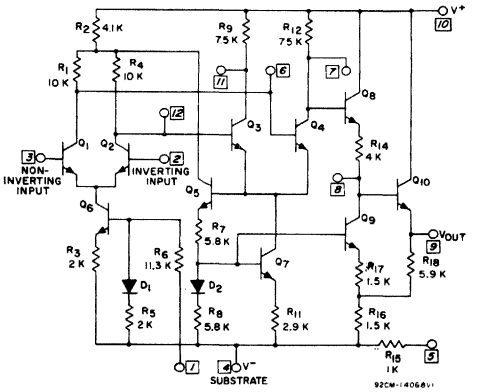
Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3008 CA3029 CA3037	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3008 CA3029 CA3037	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008, CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3016 CA3030 CA3038	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3016 CA3030 CA3038	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016, CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015 (Substrate) DO NOT GROUND				

SCHEMATIC DIAGRAMS



CA3008 CA3030
CA3016 CA3037
CA3029 CA3038



CA3010
CA3015

Fig.1

	CA3008 CA3016 CA3037	CA3010 CA3015 CA3038	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C		-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C		-65°C to +150°C

	CA3016 CA3030	CA3015 CA3038	CA3008 CA3029	CA3010 CA3037
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V		-4 V to +1 V	
MAXIMUM DEVICE DISSIPATION	600 mW		300 mW	

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008 CA3010 CA3029 CA3037 Min.	Typ.	Max.	CA3016 CA3015 CA3030 CA3038 Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	15
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

INPUT OFFSET VOLTAGE AND CURRENT

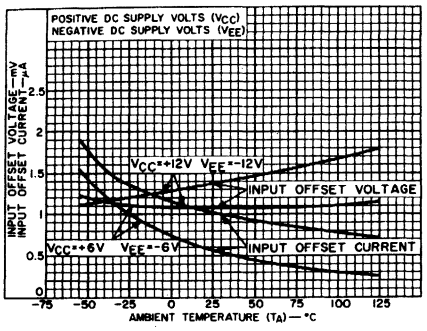


Fig.2

INPUT BIAS CURRENT

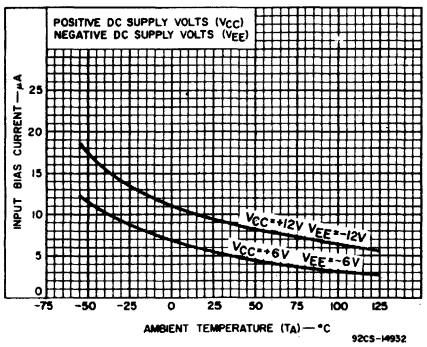


Fig.3

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

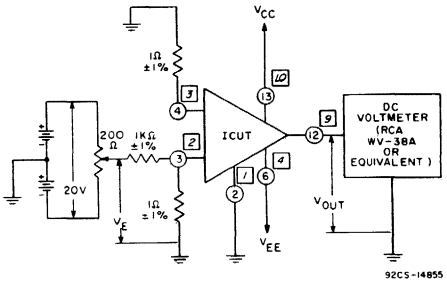


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$
I_C = Direct Current into Terminal (13) or [10]
I_E = Direct Current out of Terminal (6) or [4]

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

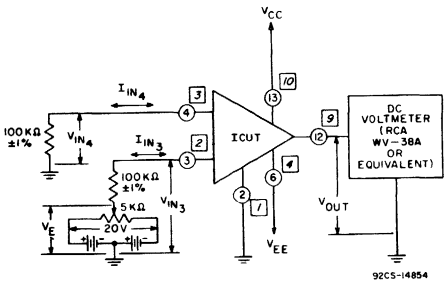


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038

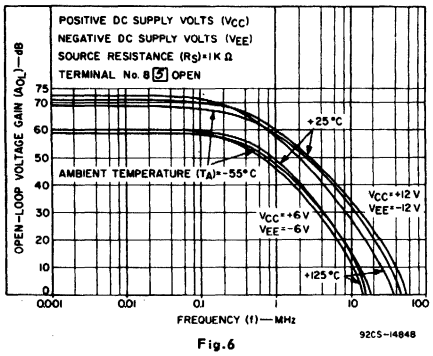


Fig.6

OPEN-LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029 AND CA3030

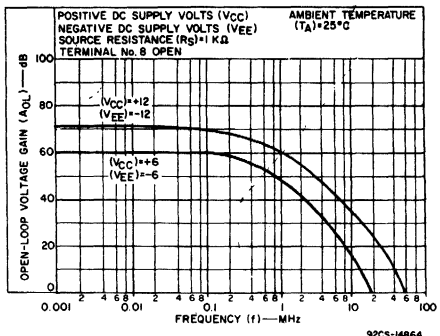
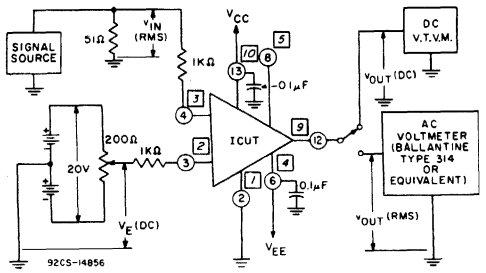


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AND OPEN-LOOP BANDWIDTH AT −3 dB POINT TEST CIRCUIT



Procedure:

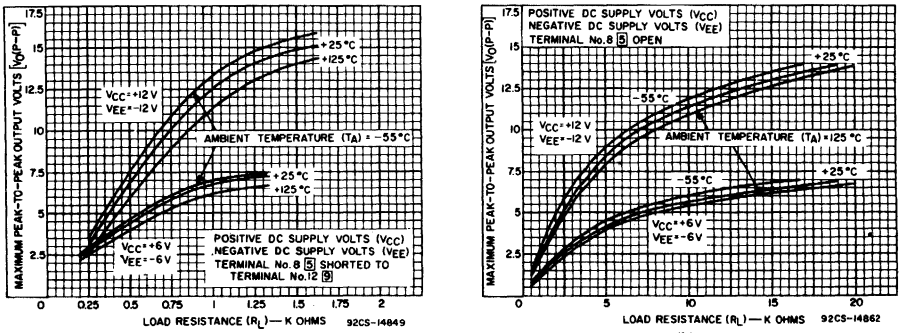
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.
   Reference Level = A_{OL} at 1 kHz.

Fig.8

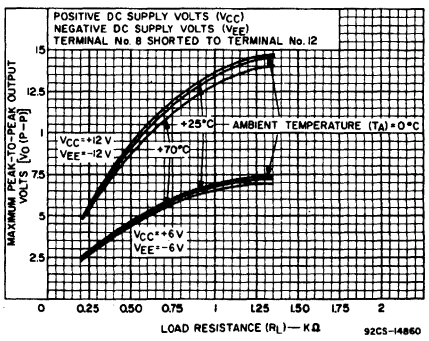
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008, CA3010, CA3015, CA3016, CA3037, CA3038



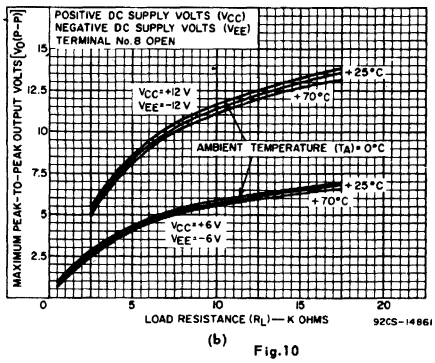
(a) (b)

Fig.9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029 AND CA3030



(a)

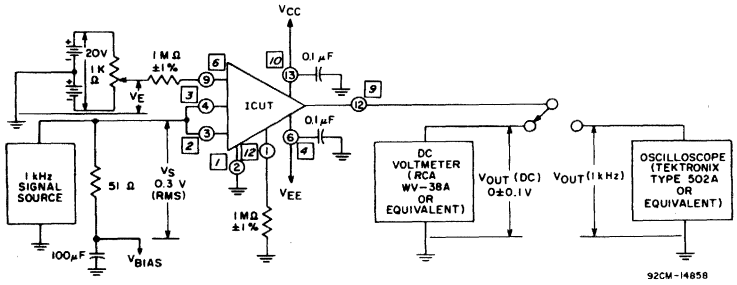


(b)

Fig.10

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig.11

COMMON-MODE REJECTION RATIO vs. FREQUENCY

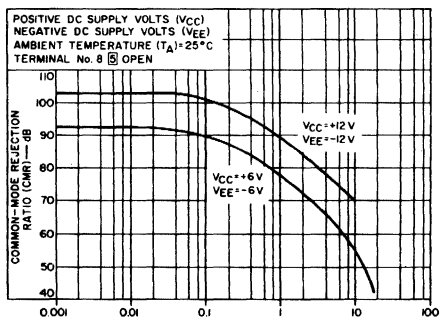


Fig.12

CA3008, CA3010, CA3015, CA3016, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

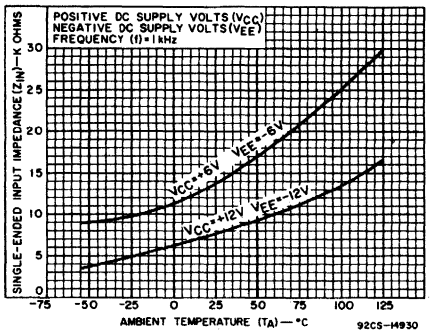


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

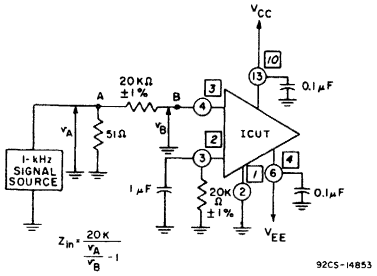


Fig.14

OUTPUT IMPEDANCE vs. TEMPERATURE

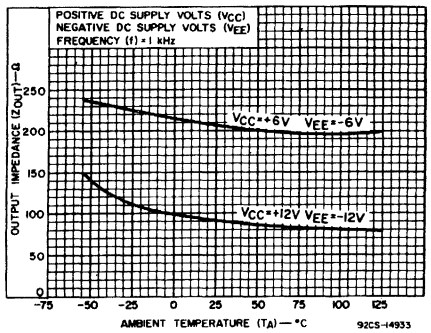


Fig.15

OUTPUT IMPEDANCE TEST CIRCUIT

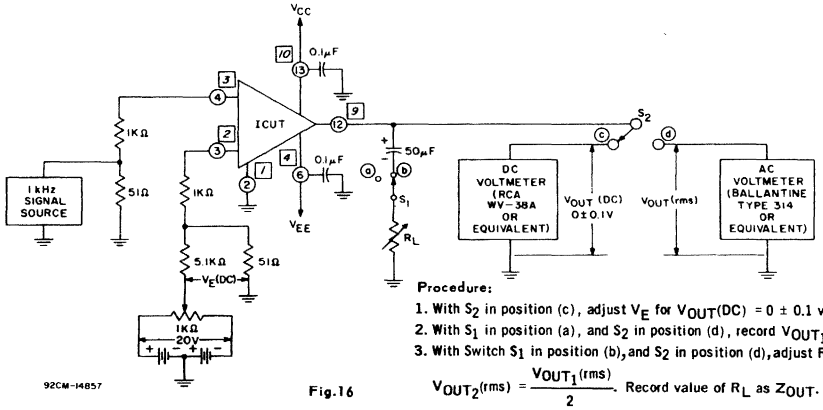


Fig.16

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A,CA3038A

Operational Amplifiers

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3008A	CA3016A	14-Lead Flat Pack
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual In-Line (TO-116)

- These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance.
- All types are electrically identical within their voltage groups
- Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment
- Built-in temperature stability from -55°C to +125°C for Flatpack, TO-5 style, and ceramic dual in-line packages; 0°C to +70°C for plastic dual in-line package
- Companion Application Notes ICAN-5290, "Integrated Circuit Operational Amplifiers"; ICAN-5213, "Application of the RCA-CA3015, CA3016 Integrated Circuit Operational Amplifiers"; and ICAN-5015, "Application of the RCA-CA3008, CA3010 Integrated Circuit Operational Amplifiers" cover Bode characteristics, phase compensation, frequency shaping, and amplifier design.

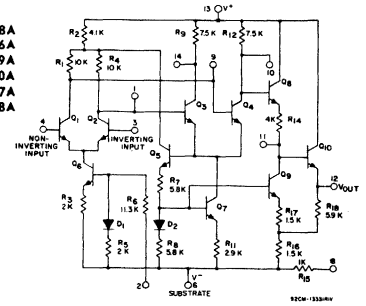
HIGHLIGHTS

	6 V Types	12 V Types	
• Open-Loop Voltage Gain	60	70	dB typ.
• Common-Mode Rejection Ratio	94	103	dB typ.
• Input Impedance	20	10	k typ.
• Input Offset Voltage	0.9	1	mV typ.
• Input Offset Current	0.3	0.5	μA typ.
• Input Bias Current	2.5	4.7	μA typ.
• Static Power Drain at ±12 V	-	175	mW typ.
at ±6 V	30	30	mW typ.
at ±3 V	7	7	mW typ.

APPLICATIONS

- Narrow-Band and Band-pass Amplifier
- Operational Functions
- Feedback Amplifier
- DC and Video Amplifier
- Multivibrator
- Oscillator
- Comparator
- Servo Driver
- Scaling Adder
- Balanced Modulator-Driver

CA3008A
CA3016A
CA3029A
CA3030A
CA3037A
CA3038A



CA3010A
CA3015A

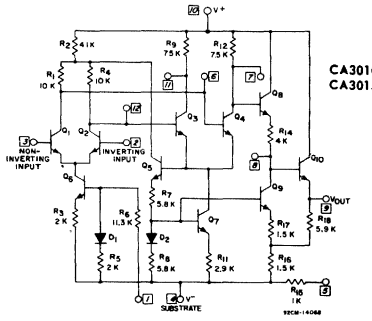


Fig.1

SCHEMATIC DIAGRAMS

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008A CA3010A CA3029A CA3037A Min.	Typ.	Max.	CA3016A CA3015A CA3030A CA3038A Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		5 shorted to 9 V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V, R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 -4 -	- - -	- - -	- +0.65 -8	- - -	- - -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V = +6V = -6V = +9V = -9V = +12V = -12V, R_S = 1 kΩ	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

LEAD TEMPERATURE (During Soldering): ALL TYPES

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A CA3029A CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A CA3029A CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A CA3030A CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A CA3030A CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A CA3016A CA3037A CA3038A	CA3010A CA3015A CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +80°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3016A CA3030A CA3038A	CA3015A CA3008A CA3029A CA3010A CA3037A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A;
Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

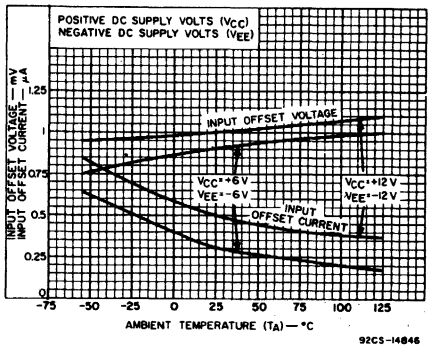


Fig.2

INPUT BIAS CURRENT

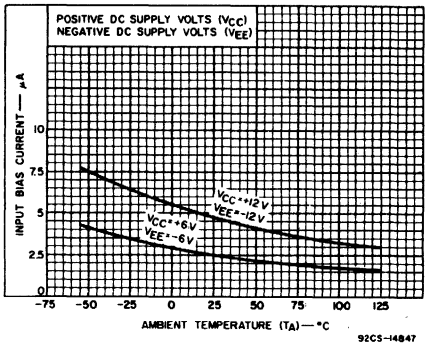


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

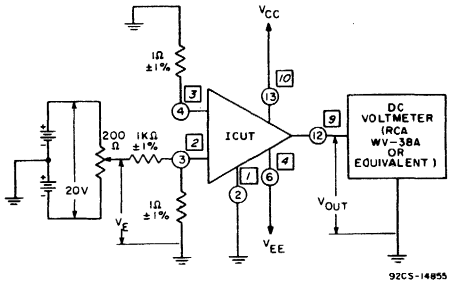


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or [10]

I_E = Direct Current out of Terminal 6 or [4]

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

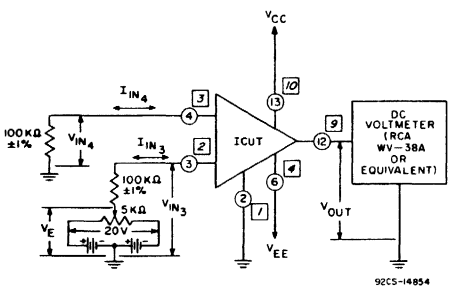


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A

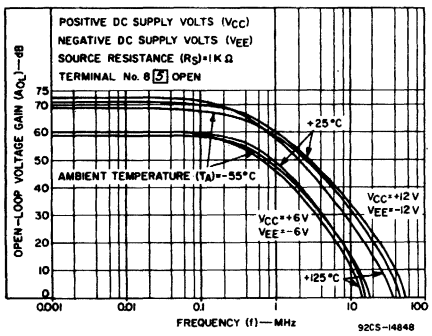


Fig.6

OPEN LOOP VOLTAGE GAIN vs. FREQUENCY FOR CA3029A AND CA3030A.

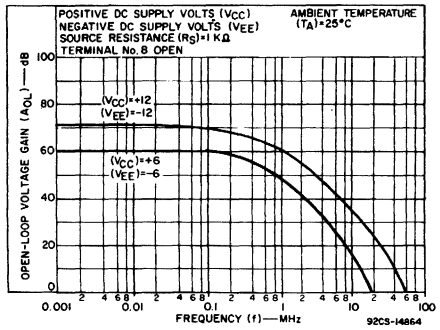
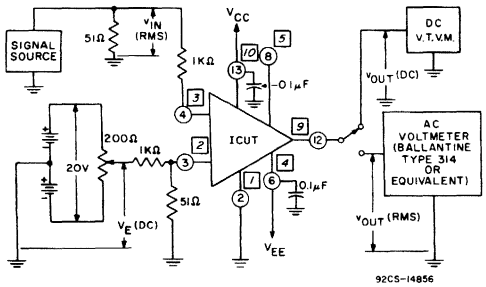


Fig.7

OPEN-LOOP DIFFERENTIAL VOLTAGE GAIN, MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE, AND OPEN-LOOP BAND WIDTH AT −3 POINT TEST CIRCUIT



Procedure:

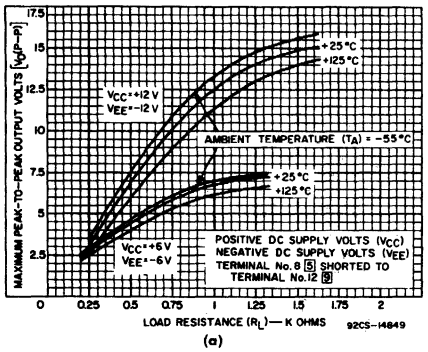
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

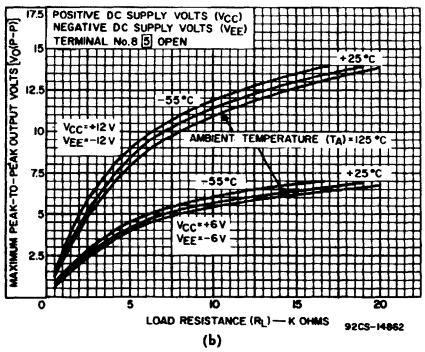
3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
   Reference Level = A_{OL} at 1 kHz

Fig.8

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3008A, CA3010A, CA3015A, CA3016A, CA3037A, CA3038A



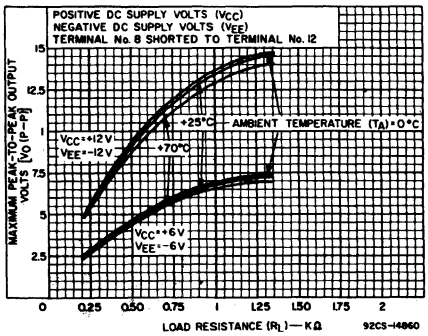
(a)



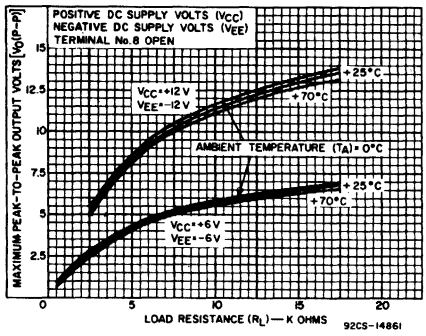
(b)

Fig.9

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. LOAD RESISTANCE FOR CA3029A AND CA3030A



(a)



(b)

Fig.10

COMMON-MODE REJECTION RATIO AND COMMON-MODE INPUT-VOLTAGE-RANGE TEST CIRCUIT

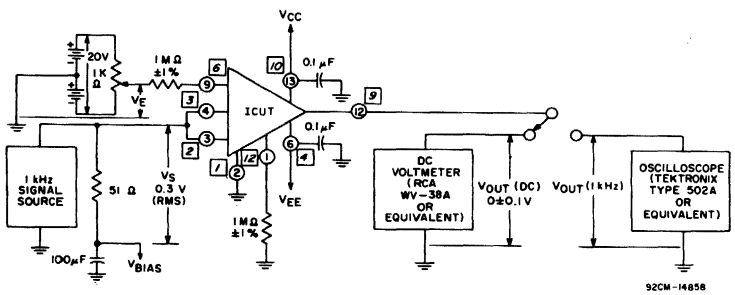


Fig.11

Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \text{ LOG}_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$\text{CMR in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB.}$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

COMMON-MODE REJECTION RATIO vs. FREQUENCY

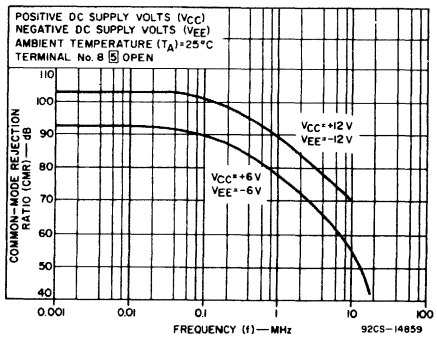


Fig.12

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

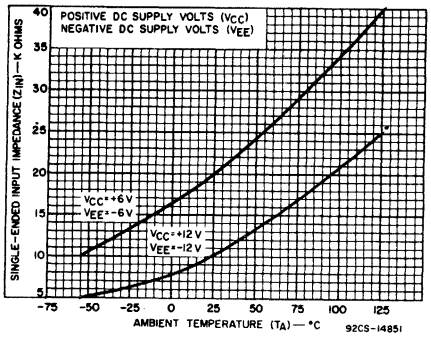


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

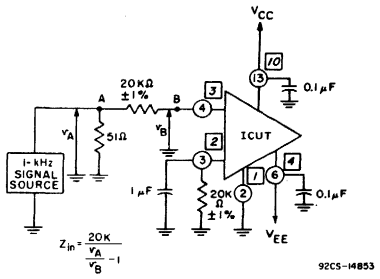


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

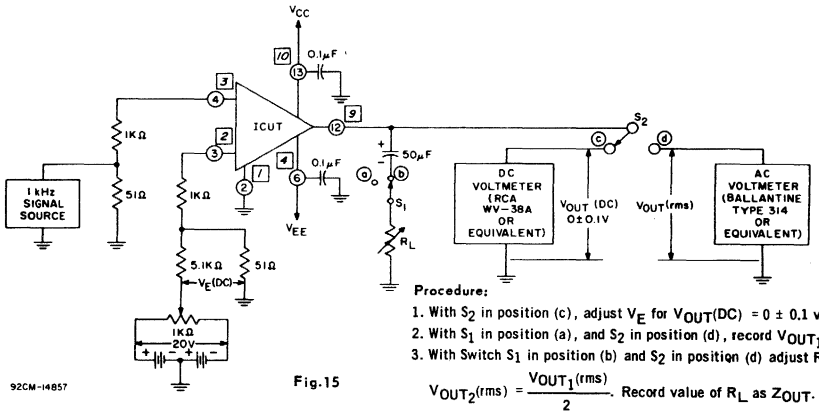
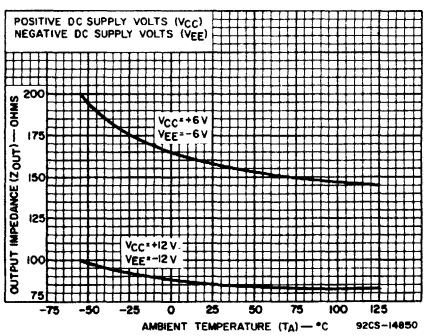


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT(DC)} = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1(rms)}$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2(rms)} = \frac{V_{OUT_1(rms)}}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

NOISE FIGURE vs. FREQUENCY

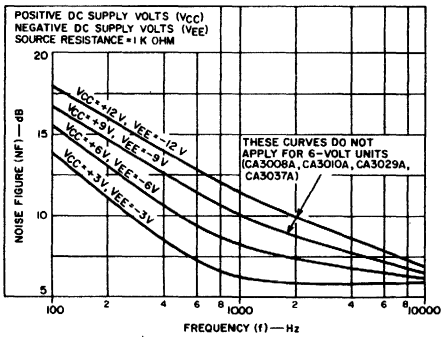


Fig.17

CA3011, CA3012

Wide-Band Amplifiers

FEATURES & APPLICATIONS

- exceptionally high amplifier gain: power gain at 4.5 MHz – 75 dB typ.
- excellent limiting characteristics – Input limiting voltage (knee) = 600 μV typ. at 10.7 MHz
- wide frequency capability – 100 kHz to > 20 MHz
- supplied in the hermetic 10-lead TO-5 style package

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

NOTE: TERMINALS 6, 7, AND 9 OF RCA-CA3011 AND CA3012 ARE USED FOR INTERNAL CONNECTIONS. DO NOT APPLY VOLTAGES OR MAKE EXTERNAL CONNECTIONS TO THESE TERMINALS.

CA3011

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Ground	+7.5
2	-3	+3	Same as 2	–		+2.5 to +7.5	+7.5	Ground	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		–	+7.5	Ground	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	–	Ground	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

CA3012

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Ground	+10
2	-3	+3	Same as 2	–		+2.5 to +10	+10	Ground	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
4	+2.5	+10	-3 to +3	Same as 1		–	+10	Ground	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	–	Ground	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

OPERATING-TEMPERATURE RANGE ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE ..... -65 to +150° C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 2 ..... ±3 V
MAXIMUM DEVICE DISSIPATION ..... 300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC}) .. 5.5 V

Example of Use of LIMITS TABLE:

For RCA-3012, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +10 volts
Terminal 5 is at a dc potential of +10 volts
Terminals 6, 7, and 9 are at 0 dc potential (NOT USED)
Terminal 8 is at dc ground potential
Terminal 10 is at a dc potential of +10 volts

BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING RCA-CA3011 OR CA3012 INTEGRATED CIRCUIT WIDE-BAND AMPLIFIER

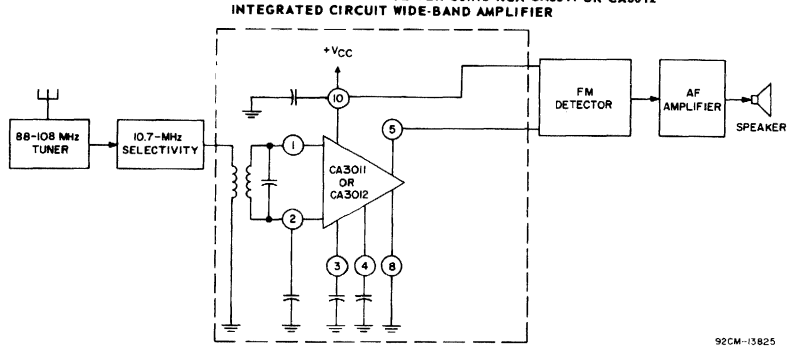


Fig. 4

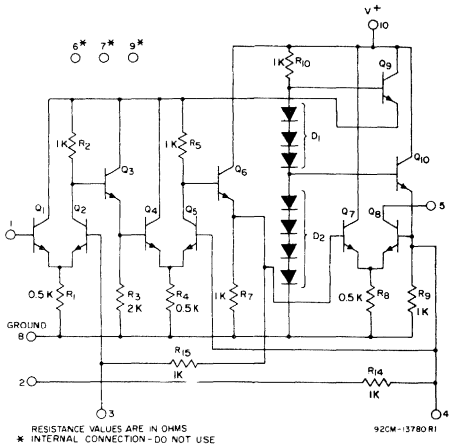


Fig. 1 – Schematic diagram for CA3011 and CA3012.

INPUT-IMPEDANCE COMPONENTS VS FREQUENCY

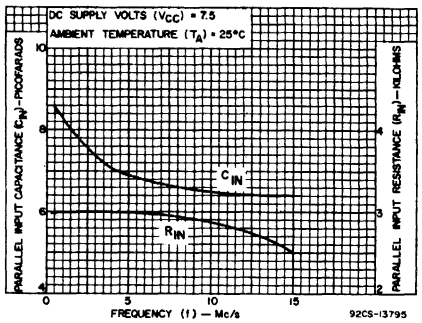


Fig. 2

OUTPUT-IMPEDANCE COMPONENTS VS FREQUENCY

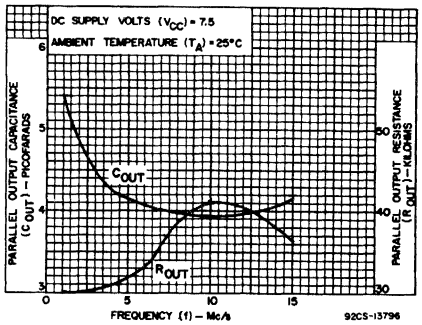


Fig. 3

VOLTAGE GAIN AND INPUT LIMITING VOLTAGE VS FREQUENCY

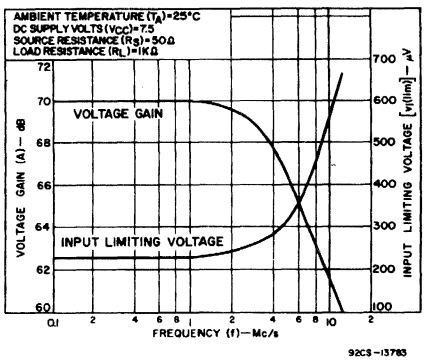


Fig. 5

CA3011, CA3012

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY	DC SUPPLY VOLTAGE	AMBIENT TEMPERATURE	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	6	–	6	-55	–	80	–	66	80	135	mW	
					+25	60	90	133	66	90	121	mW	
					+125	–	70	–	65	70	121	mW	
				7.5	-55	–	130	–	97	130	190	mW	
					+25	95	120	187	97	120	167	mW	
					+125	–	100	–	95	100	167	mW	
				10	-55	–	–	–	150	210	275	mW	
					+25	–	–	–	150	190	255	mW	
					+125	–	–	–	150	160	255	mW	
Voltage Gain**	A	9	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
				7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
				10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
			4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	61	–	55	61	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	7	4.5	7.5	+25	–	3	–	–	3	–	kΩ	2
Parallel Input Capacitance	C_{IN}	7	4.5	7.5	+25	–	7	–	–	7	–	pF	2
Output Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	3
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	3
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	
Input Limiting Voltage (Knee)	$V_i(lim)$	9	4.5	7.5	+25	–	300	450	–	300	400	μV	

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

DISSIPATION TEST SETUP

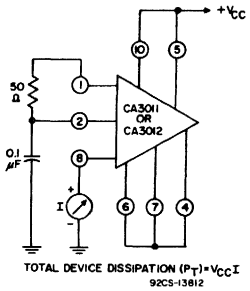


Fig. 6

INPUT-IMPEDANCE COMPONENTS TEST SETUP

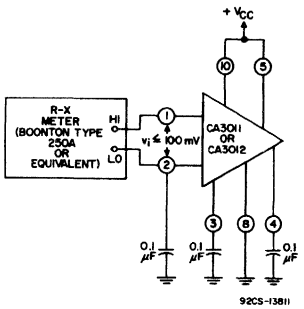


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

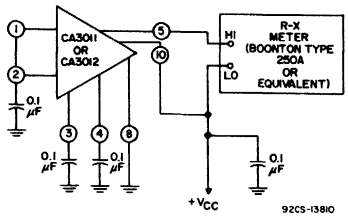
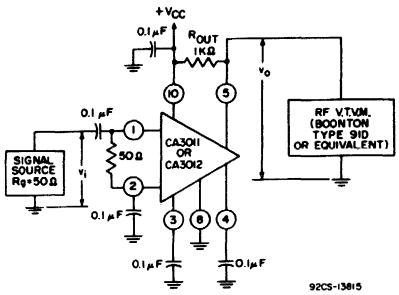


Fig. 8

VOLTAGE-GAIN TEST SETUP



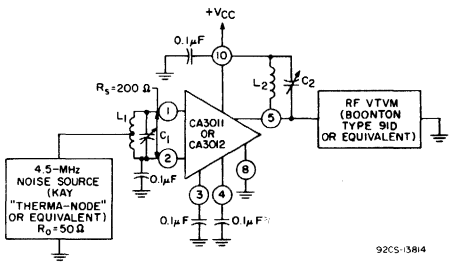
PROCEDURES

A - Voltage Gain:
1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):
1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

Fig. 9

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped
L_2 = 2.36 μH
C_1,C_2 = Arco Type 423 padder, or equivalent

Fig. 10

CA3013, CA3014

Wide-Band Amplifier-Discriminators

SCHEMATIC DIAGRAM FOR CA3013 AND CA3014

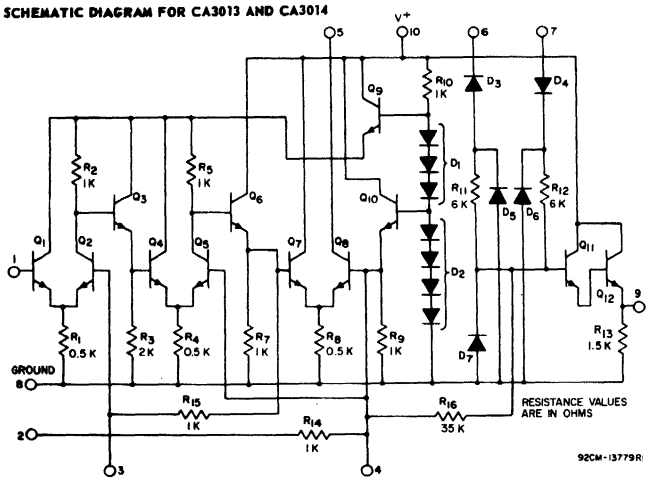


Fig. 1

BLOCK DIAGRAM OF TYPICAL TELEVISION RECEIVER USING RCA INTEGRATED-CIRCUIT SOUND-IF AMPLIFIER AND DETECTOR SECTION

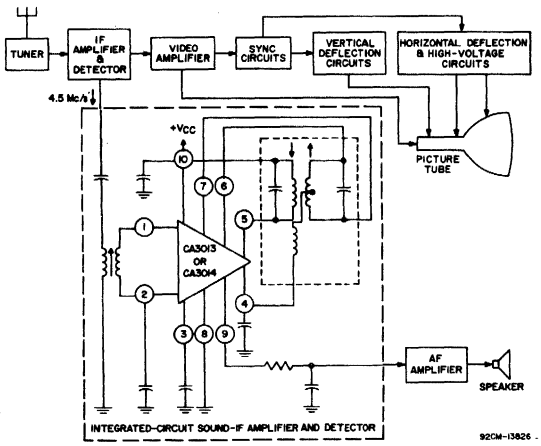


Fig. 2

FEATURES & APPLICATIONS:

- **exceptionally high gain:**
  power gain at 4.5 MHz — 75 dB typ.
- **excellent limiting characteristics — input limiting voltage (knee) = 300 μV typ. at 4.5 MHz**
- **excellent AM rejection: > 50 dB at 4.5 MHz**
- **high audio-voltage recovery — 220 mV typ. at 4.5 MHz 25 kHz deviation**
- **wide frequency capability — 100 kHz to > 20 MHz**
- **comprehensive circuit functions:**
  if amplifier, AM and noise limiter, FM detector, audio preamplifier
- **supplied in the hermetic 10-lead TO-5 style package**

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

CA3013

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
2	-3	+3	Same as 2	-		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		-	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	-	Same as 4	Same as 4	Ground	AF Output	+7.5
6	+2.5	+7.5	-3 to +3	Same as 1		Same as 6	+7.5	-	Same as 4	Ground	AF Output	+7.5
7	+2.5	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	-	Ground	AF Output	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
9	0	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	-	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

CA3014

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
2	-3	+3	Same as 2	-		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
4	+2.5	+10	-3 to +3	Same as 1		-	+10	Same as 4	Same as 4	Ground	AF Output	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	-	Same as 4	Same as 4	Ground	AF Output	+10
6	+2.5	+10	-3 to +3	Same as 1		Same as 6	+10	-	Same as 4	Ground	AF Output	+10
7	+2.5	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	-	Ground	AF Output	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
9	0	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	-	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

TYPICAL CHARACTERISTICS AND TEST SETUPS

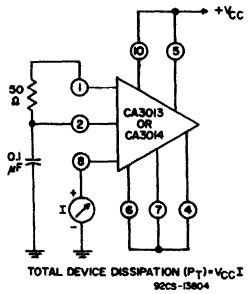


Fig.3

OPERATING-TEMPERATURE RANGE	-55 to +125°C
STORAGE-TEMPERATURE RANGE	-65 to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE: Between Terminals 1 and 2	± 3 V
MAXIMUM DEVICE DISSIPATION	300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC})	5.5 V

Example of use of LIMITS TABLE:

For RCA-CA3013, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +7.5 volts
Terminal 5 is at a dc potential of +7.5 volts
Terminals 6 and 7 are at the same dc potential as Terminal 4
Terminal 8 is at dc ground potential
Terminal 9 is used as the af output terminal
Terminal 10 is at a dc potential of +7.5 volts

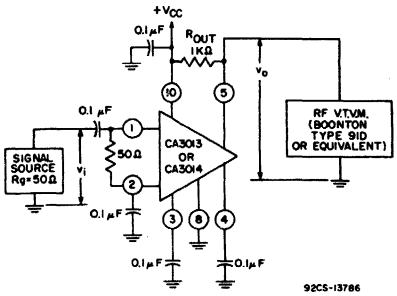
CA3013, CA3014

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	LIMITS: RCA CA3013 Min.	Typ.	Max.	RCA CA3014 Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVES
		Fig.	Mc/s	volts	°C								Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	4	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		4	1	7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		4	1	10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		4	4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	6	4.5	7.5	+25	–	3	–	–	3	–	kΩ	7
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	+25	–	7	–	–	7	–	pF	7
Output-Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	9
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	9
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	11
Input Limiting Voltage (Knee)	v_i(lim)	14	4.5	7.5	+25	–	300	450	–	300	400	μV	13
Recovered AF Voltage	v_o(af)	14	4.5	6	+25	–	155	–	–	155	–	mV	13
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	15	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	R_O(disc)	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	12

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig. 4

VOLTAGE GAIN vs. FREQUENCY

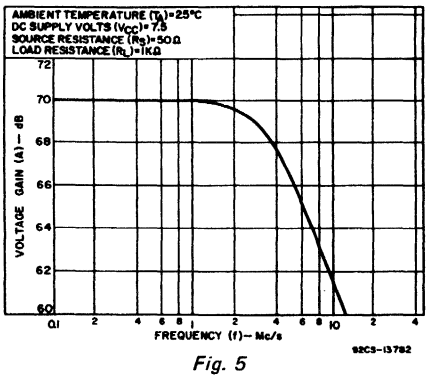


Fig. 5

INPUT-IMPEDANCE COMPONENTS TEST SETUP

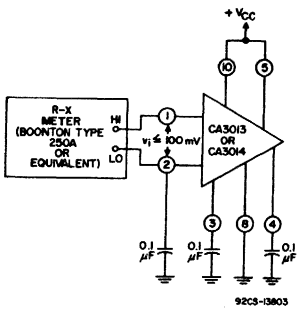


Fig. 6

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

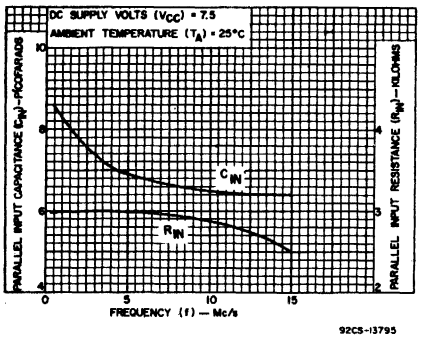


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

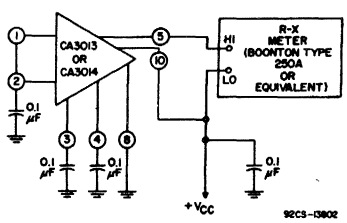


Fig. 8

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

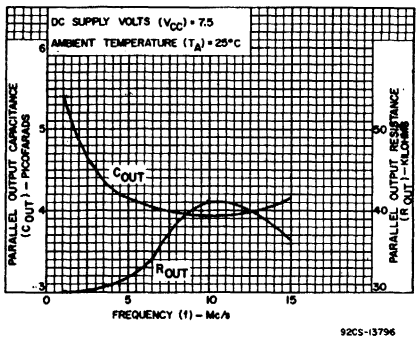
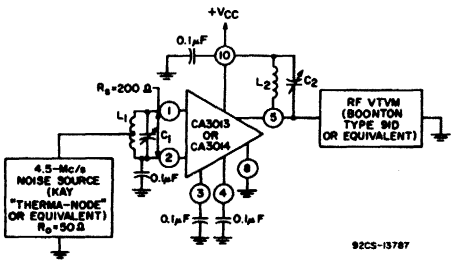


Fig. 9

CA3013, CA3014

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1, C_2 = Arco Type 423 padder, or equivalent

Fig. 10

NOISE FIGURE vs. DC SUPPLY VOLTAGE

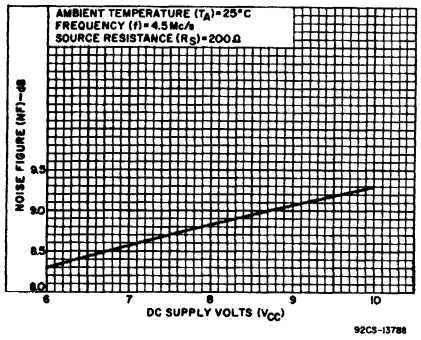


Fig. 11

TOTAL HARMONIC DISTORTION vs. DC SUPPLY VOLTAGE

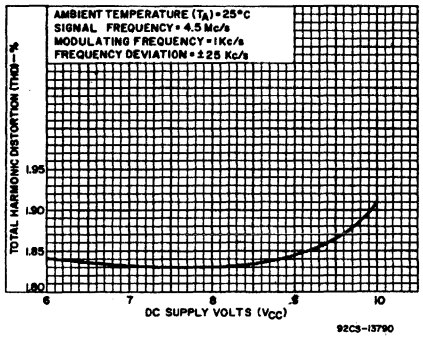
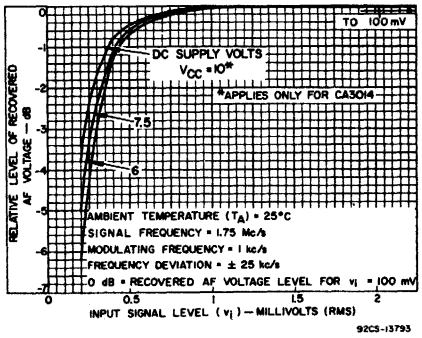


Fig. 12

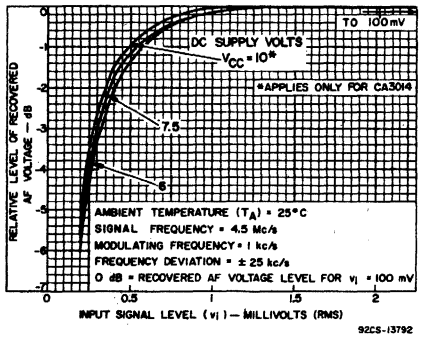
INPUT LIMITING VOLTAGE (KNEE) AND RECOVERED AF VOLTAGE

at 1.75 Mc/s



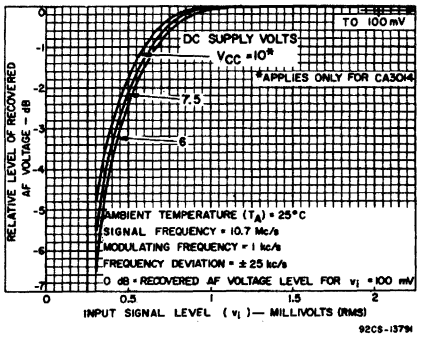
(a)

at 4.5 Mc/s



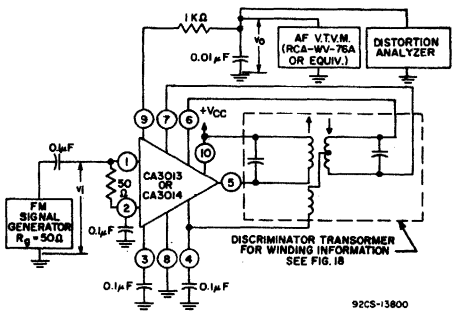
(b)

at 10.7 Mc/s



(c)

Fig. 13



PROCEDURE:

A - Recovered-AF Voltage Output:

1) Set input frequency = 4.5 Mc/s, v_i = 100 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o as Recovered-AF Voltage Output.

B - Input Limiting Voltage (Knee):

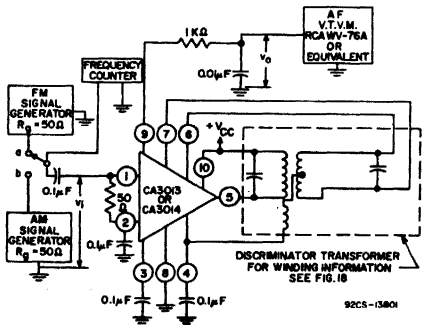
1) Repeat Steps A1 and A2, using v_i = 100 mV rms.

2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.

3) Record v_i as Input Limiting Voltage (Knee).

INPUT LIMITING VOLTAGE, RECOVERED AF VOLTAGE, AND TOTAL HARMONIC DISTORTION TEST SETUP

Fig. 14



PROCEDURE:

1) With Switch S in position "a", set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o.

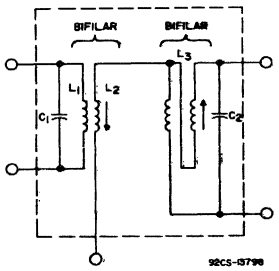
3) Place Switch S in position "b", and set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, % modulation = 50.

4) Measure v_o, and record value in dB below value in Step 2 as AM Rejection.

AM-REJECTION TEST SETUP

Fig. 15

DISCRIMINATOR TRANSFORMER SCHEMATIC



(a)

CONSTRUCTION DETAILS OF DISCRIMINATOR TRANSFORMERS SHOWN IN FIGS. 2, 14 AND 15

Coil-Form Outside Diameter = 7/32 inch

Slugs: Radio Industries, Inc. Type "E" Material, or equivalent

Wire Type: "GRIPEZE"*, or equivalent

Operating Frequency Mc/s	Wire Size (AWG #)	Turns L_1▲	Turns L_2▲	Turns L_3	C_1 pF	C_2 pF
1.75	40	44	20	44 total (22 bifilar wound)	820	820
4.5	36	18	7	22 total (11 bifilar wound)	560	330
10.7	36	18	18	18 total (9 bifilar wound)	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products.

▲ wound bifilar.

NOTE: The mutual coupling between L_1 and L_3 is adjusted for the desired degree of linearity.

(b)

Fig. 16

CA3018, CA3018A

General-Purpose Transistor Arrays

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the VHF Range

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

APPLICATIONS

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10 μA to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)
- The CA3018 is available in a sealed-junction Beam Lead version (CA3018L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package.

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

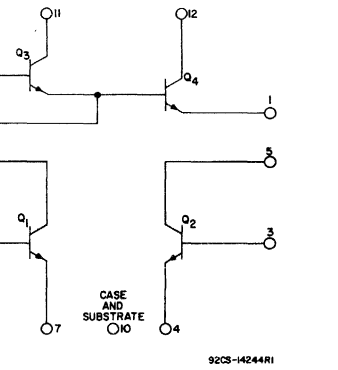


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

STATIC CHARACTERISTICS

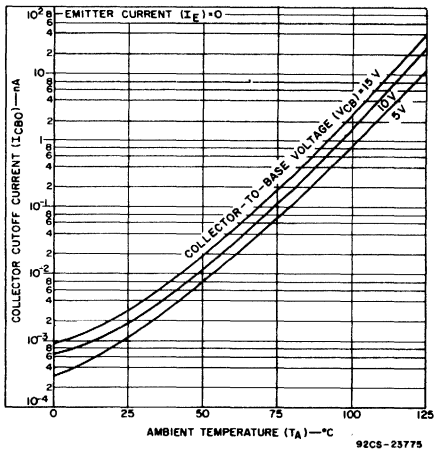


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

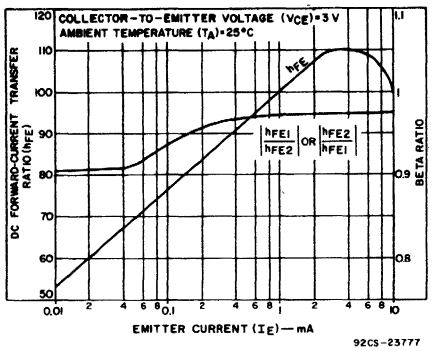


Fig. 3 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q1 and Q2 vs Emitter Current.

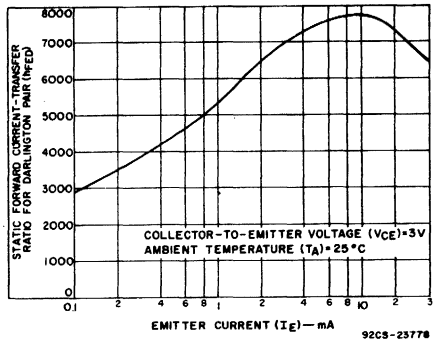


Fig. 4 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q3 and Q4 vs Emitter Current.

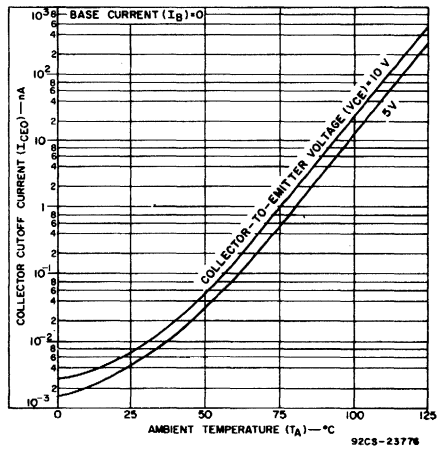


Fig. 7 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

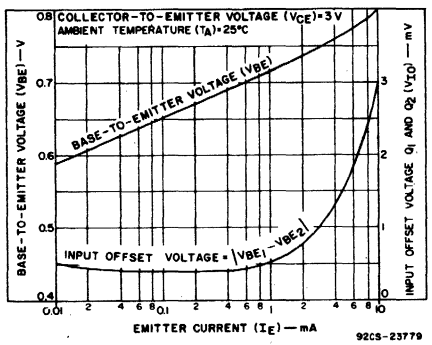


Fig. 5 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q1 and Q2 vs Emitter Current.

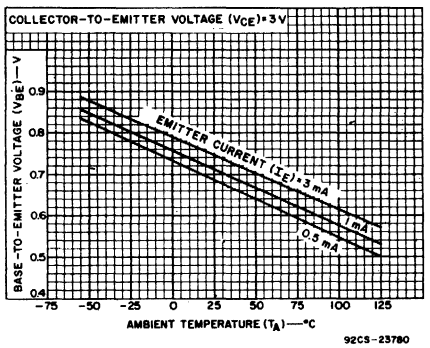


Fig. 6 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

CA3018, CA3018A

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	7
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA	–	100	–	50	100	–	–	3
		I_C= 1mA	30	100	200	60	100	200	–	
		I_C=10μA	–	54	–	30	54	–	–	
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	3
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V, I_C= 1mA	1500	5400	–	2000	5400	–	–	4
		I_C=100μA	–	–	–	1000	2800	–		
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V, I_E=1mA	–	0.715	–	0.600	0.715	0.800	V	5
		I_E=10mA	–	0.800	–	–	0.800	0.900		
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	5,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	1.9	–	–	1.9	–	mV/°C	6
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V, I_E=10mA	–	1.46	–	–	1.46	1.60	V	9
		I_E= 1mA	–	1.32	–	1.10	1.32	1.50		
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

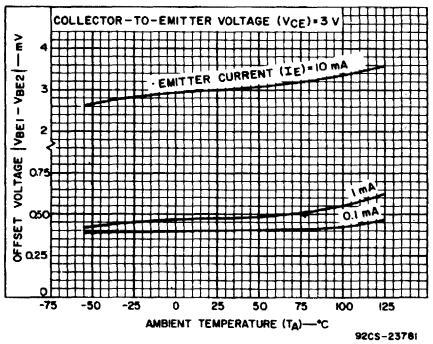


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

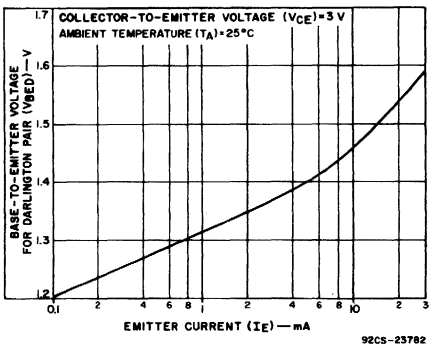


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

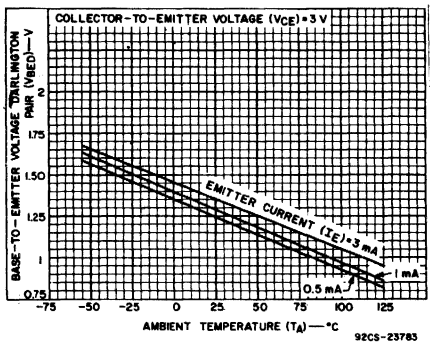


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

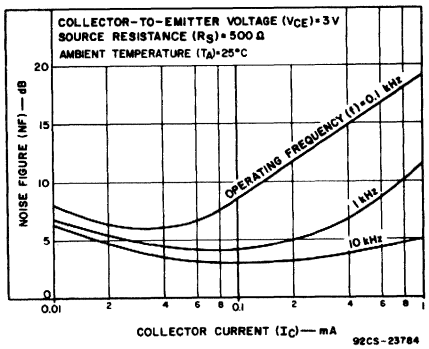


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

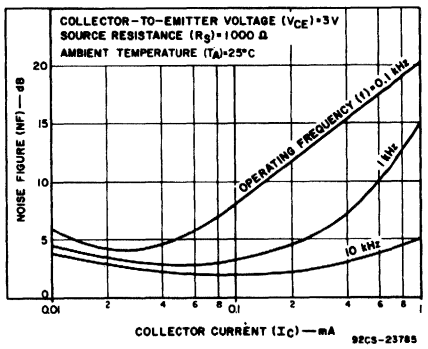


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

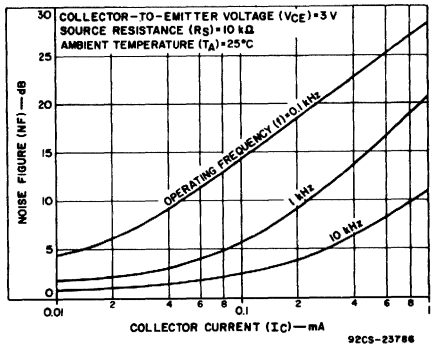


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

CA3018, CA3018A

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS			CA3018			CA3018A				
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

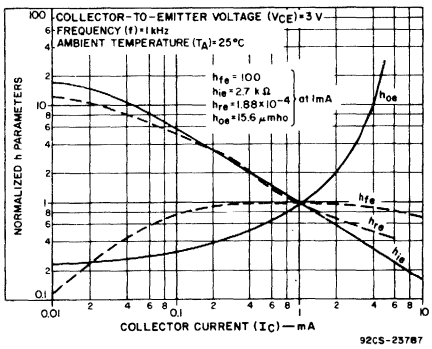


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

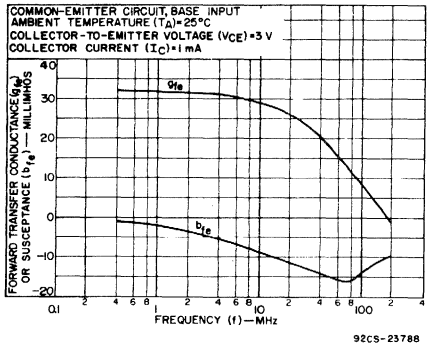


Fig.13 - Forward Transfer Admittance (Y_{fe})

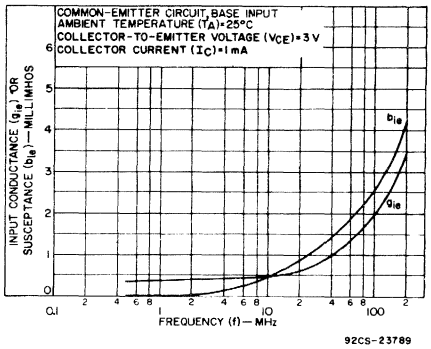


Fig.14 - Input Admittance (Y_{ie})

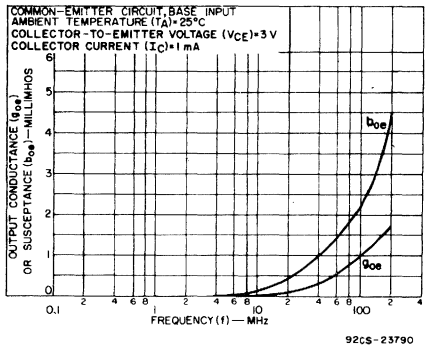


Fig.15 - Output Admittance (Y_{oe})

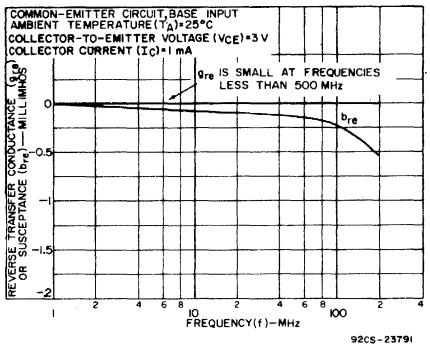


Fig.16 - Reverse Transfer Admittance (Y_{re})

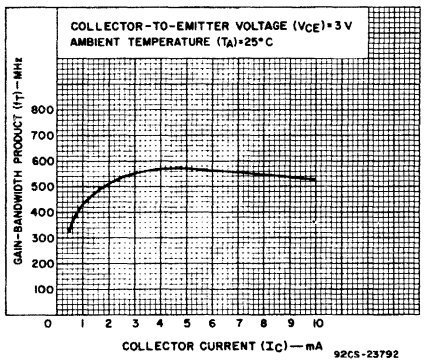


Fig.17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3019

DIODE ARRAY

The CA3019 consists of one Diode "Quad" and two Isolated Diodes on a Common Substrate.

- **Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment**
- **Built-in Temperature Stability for Operation from -55°C to +125°C**
- **10-Terminal TO-5 Package**
- **Hermetically Sealed**
- **Companion Application Note, ICAN-5299 "Application of the RCA CA3019 Integrated-Circuit Diode Array"**

HIGHLIGHTS

- **Excellent Diode Match**
- **Low Leakage Current**
- **Low Pedestal Voltage when Gating**

APPLICATIONS

- **Modulator**
- **Mixer**
- **Balanced Modulator**
- **Analog Switch**
- **Diode Gate for Chopper-Modulator Applications**

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:
Any one diode unit . . . . . 20 max. mW
Total for device . . . . . 120 max. mW

TEMPERATURE RANGE:
Storage . . . . . -65 to +150 °C
Operating . . . . . -55 to +125 °C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

VOLTAGE: See Table

Absolute-Maximum Voltage Limits at $T_A = 25°C$

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

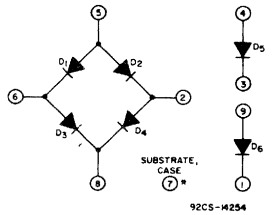


Fig.1 - Schematic Diagram for CA3019.

TYPICAL CHARACTERISTICS

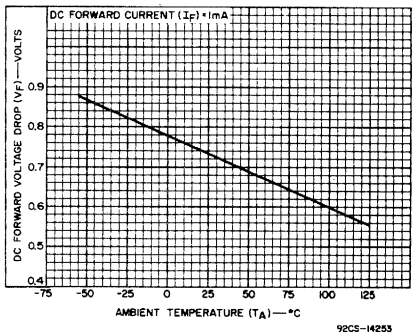


Fig.2 - DC Forward Voltage Drop (any Diode) vs Temperature for CA3019.

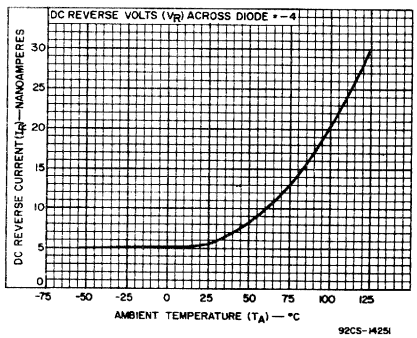


Fig.3 - Reverse (Leakage) Current (any Diode) vs Temperature for CA3019.

ELECTRICAL CHARACTERISTICS, at an Ambient Temperature, T_A, of 25°C
CHARACTERISTICS APPLY FOR EACH DIODE UNIT, UNLESS OTHERWISE SPECIFIED.

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	SPECIAL TEST CONDITIONS	LIMITS				TYPICAL CHARACTERISTICS CURVES
				TYPE CA3019				
		Fig.		Min.	Typ.	Max.	Units	Fig.
DC Forward Voltage Drop	V_F	-	DC Forward Current (I_F) = 1 mA	-	0.73	0.78	V	2
DC Reverse Breakdown Voltage	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	4	6	-	V	-
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	25	80	-	V	-
DC Reverse (Leakage) Current	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.0055	10	μA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.010	10	μA	-
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F1} - V_{F2} \rvert$	-	DC Forward Current (I_F) = 1 mA	-	1	5	mV	-
Single Diode Capacitance	C_D	-	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = -2 V	-	1.8	-	pF	4
Diode Quad-to-Substrate Capacitance	C_{DQ-I}		Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = -2 V					
			Terminal 2 or 6 to Terminal 7	-	4.4	-	pF	5
			Terminal 5 or 8 to Terminal 7	-	2.7	-	pF	6
Series Gate Switching Pedestal Voltage	V_S	7		-	10	-	mV	-

CA3019

TYPICAL CHARACTERISTICS (Cont'd)

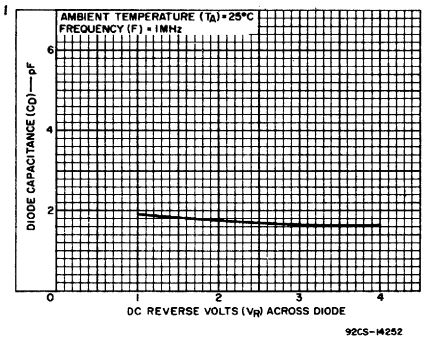


Fig.4 - Diode Capacitance (any Diode) vs Reverse Voltage for CA3019.

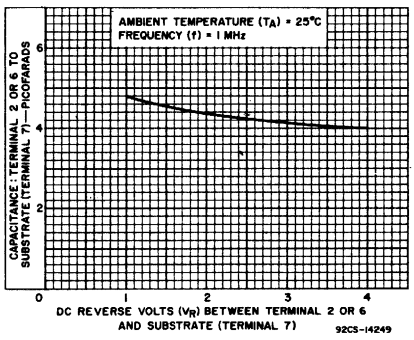


Fig.5 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

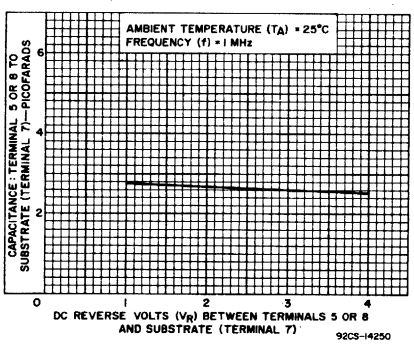


Fig.6 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

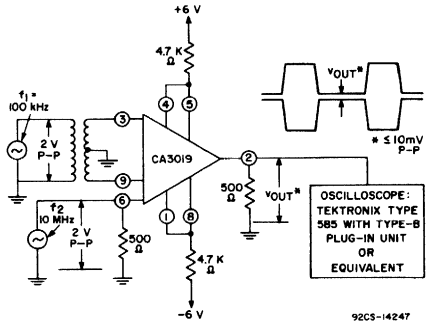


Fig.7 - Series Gate Switching Test Setup for CA3019.

CA3020, CA3020A

MULTIPURPOSE WIDE-BAND POWER AMPLIFIERS

The RCA-CA3020 and CA3020A are Integrated-Circuit, Multistage, Multipurpose, Wide-Band Power Amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

The CA3020 and CA3020A are particularly suited for service as Class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt DC supply with a typical power gain of 75 dB. The CA3020 provides 0.5 watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed, TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

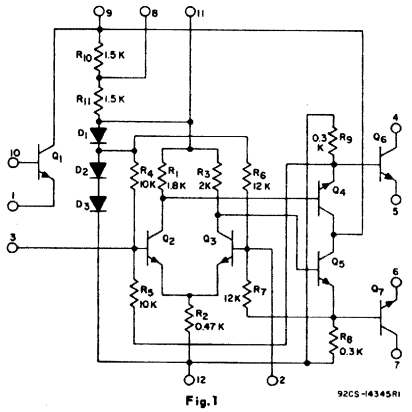


Fig. 1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:	WITHOUT HEAT SINK	WITH HEAT SINK
	At T_A = 25°C . . . . . 1 W	At T_C = 25°C . . . . . 2 W
	Above T_A = 25°C . . . . . derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C . . . . . 2 W
		Above T_C = 55°C . . derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C

Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

FEATURES

- High power output - class B amplifier --
  CA3020 .... 0.5 watt typ. at V_{CC} = +9V
  CA3020A ... 1.0 watt typ. at V_{CC} = +12V
- Wide frequency range --
  Up to 8 MHZ with resistive loads
- High power gain ..... 75db typ.
- Single power supply for class B operation with transformer --
  CA3020 ..... 3 to 9V
  CA3020A ..... 3 to 12V
- Built-in temperature-tracking voltage regulator provides stable operation over -55°C to +125°C temperature range

APPLICATIONS

- AF power amplifiers for portable and fixed sound and communications systems
- Servo-control amplifiers
- Wide-band linear mixers
- Video power amplifiers
- Transmission-line driver amplifiers (balanced and unbalanced)
- Fan-in and fan-out amplifiers for computer logic circuits
- Lamp-control amplifiers
- Motor-control amplifiers
- Power multivibrator
- Power switches
- Companion Application Note, ICAN 5766 "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers."

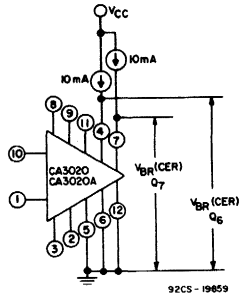
CA3020, CA3020A

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

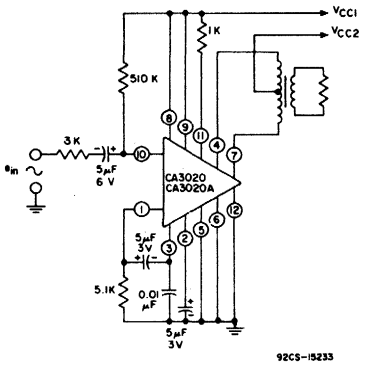
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE FIG.	DC SUPPLY VOLTAGE V_{CC1}	DC SUPPLY VOLTAGE V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	4	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	4	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	4	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	4	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	4	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	4	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	4	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}	-	3.0	-	-	-	0.1	-	-	0.1	μA
Collector-to-Base	I_{CBO}	-	3.0	-	-	-	0.1	-	-	0.1	μA
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW		6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	6	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	mW
			9.0	12.0	-	-	-	800	1000[b]	-	mW
Sensitivity for P_{OUT} = 400 mW	e_{IN}	6	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	6	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	9	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω



a. Collector-to-emitter breakdown voltage (Q_6 & Q_7) circuit



b. Typical audio amplifier circuit utilizing the CA3020 or CA3020A as an audio preamplifier and class B power amplifier

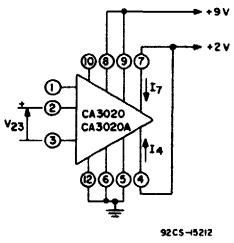
Fig.2

TYPICAL PERFORMANCE DATA

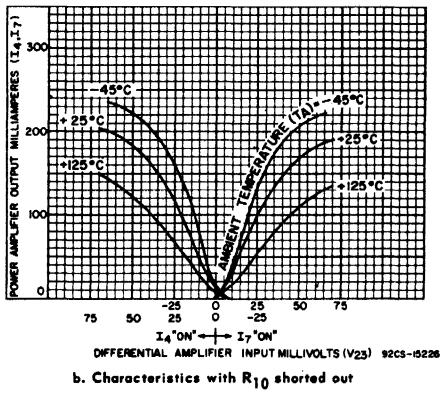
An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	V
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	mA
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	mA
Maximum Power Output at THD = 10%	Po	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

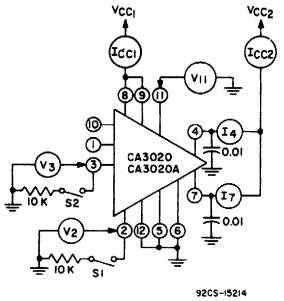


b. Characteristics with R_{10} shorted out

Fig.3

CA3020, CA3020A

STATIC CURRENT AND VOLTAGE TEST CIRCUIT

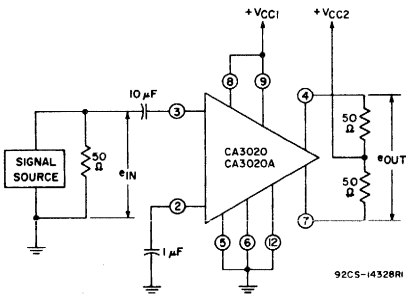


CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.4

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

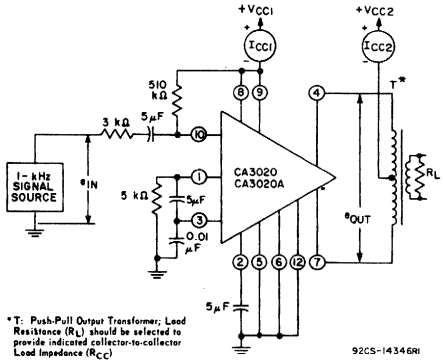


PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

Fig.5

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



*T- Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Fig.10

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100\,\frac{P_{OUT}}{V_{CC_1}I_{CC_1}+V_{CC_2}I_{CC_2}}$$

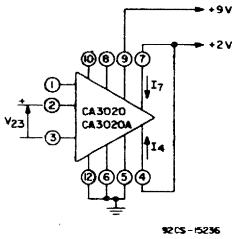
where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

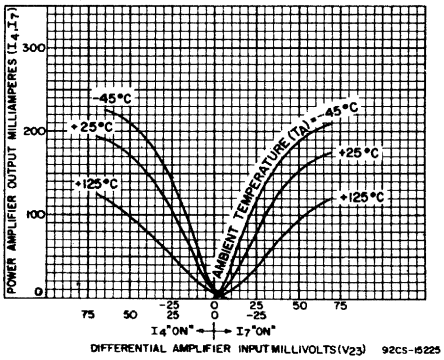
$$G_p = 10\log_{10}\frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) $= \dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

Fig.6



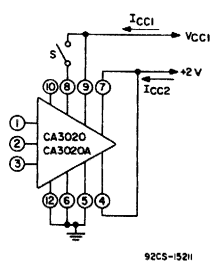
a. Test Setup



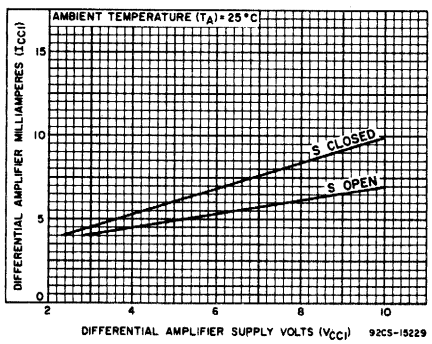
b. Characteristics with R_{10} in circuit

Fig.7

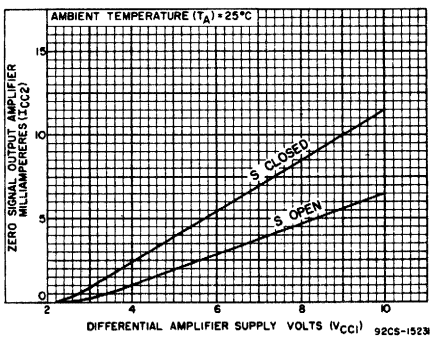
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



b. Differential Amplifier Characteristics



c. Output Amplifier Characteristics

Fig.8

CA3020, CA3020A

MEASUREMENT OF INPUT RESISTANCE

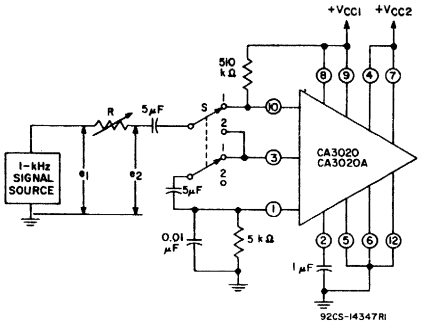


Fig.9

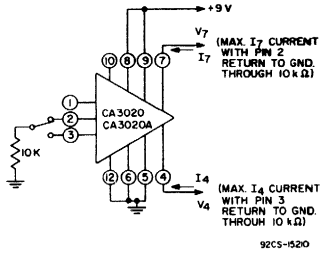
PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

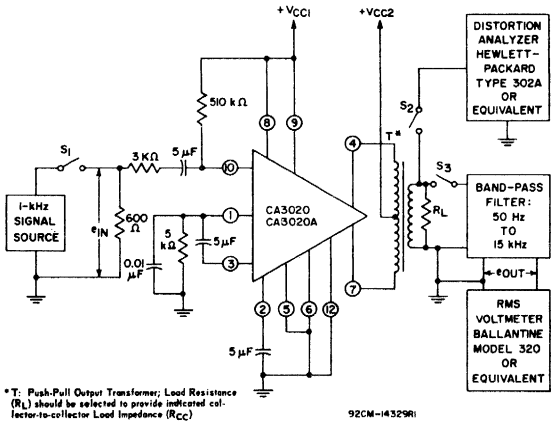
Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}



a. Test Setup

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



PROCEDURES:

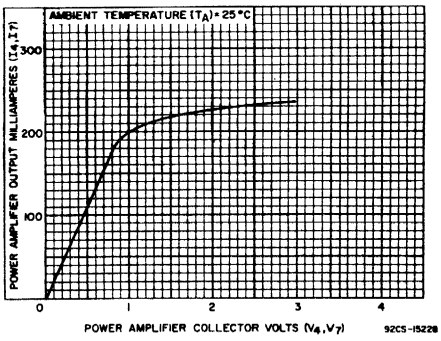
Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10} \frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

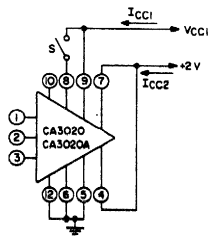
Fig.10



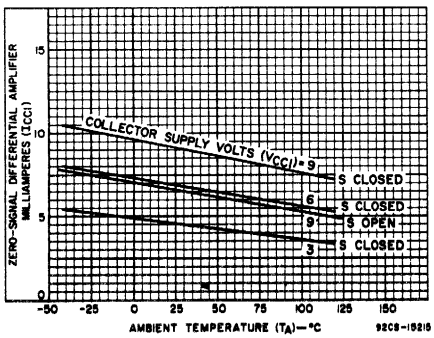
b. Characteristic

Fig.11

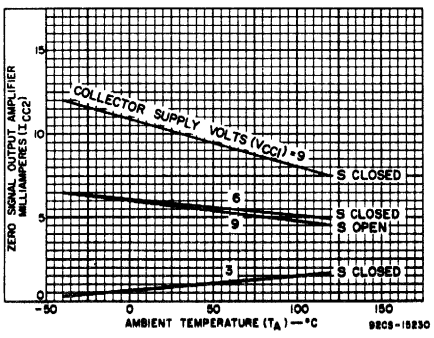
ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



a. Test Setup



b. Differential Amplifier Characteristics



c. Output Amplifier Characteristics

Fig.12

CA3021, CA2022, CA2023

Low-Power Video and Wideband Amplifiers

RCA-CA3021, CA3022, and CA3023 are low-power integrated-circuit wideband amplifiers with a wide range of applications in industrial, military, and commercial communications equipment. Each consists of a multistage amplifier circuit and unconnected diodes on a single chip, hermetically sealed in a 12-lead TO-5 style package. The diodes may be connected to provide limiting in FM applications.

The CA3021, CA3022, and CA3023 have the same maximum ratings, and differ principally in dissipation (dc power requirements) and bandwidth capability. All three devices are designed for operation over the temperature range from -55° C to +125° C.

APPLICATIONS

- Gain-Controlled Linear Amplifiers
- AM/FM IF Amplifiers • Video Amplifiers • Limiters

SCHEMATIC DIAGRAM FOR CA3021, CA3022, AND CA3023

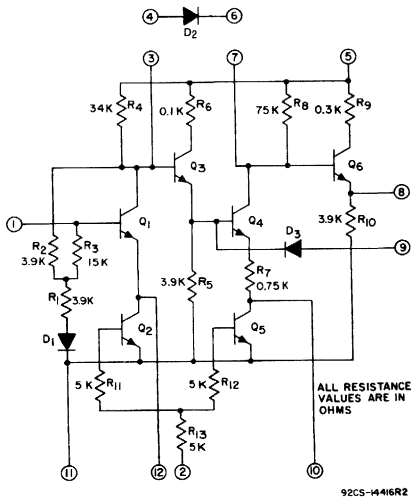


Fig.1

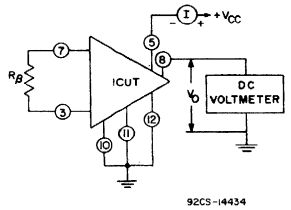
ABSOLUTE-MAXIMUM RATINGS:

OPERATING-TEMPERATURE RANGE	-55°C to +125°C	
STORAGE-TEMPERATURE RANGE	-65°C to +150°C	
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C	
DEVICE DISSIPATION, P_T	120 max.	mW
INPUT-SIGNAL VOLTAGE	-3, +3 max.	V
DC VOLTAGES AND CURRENTS	See Table Below	

HIGHLIGHTS

- Low DC Power Drain: P_D { CA3021 = 4 mW typ. / CA3022 = 12.5 mW typ. / CA3023 = 35 mW typ. } at V_{CC} = 6 V
- Excellent frequency response: -3 dB BW { CA3021 = 2.4 MHz typ. / CA3022 = 7.5 MHz typ. / CA3023 = 16 MHz typ.
- High Voltage Gain: A { CA3021 = 56 dB typ. at 0.5 MHz / CA3022 = 57 dB typ. at 2.5 MHz / CA3023 = 53 dB typ. at 5 MHz
- Wide AGC Range: 33 dB typ.
- Only one power supply (4.5 to 12 V) required
- Hermetically Sealed 12-Lead TO-5-style package
- Operation from -55° C to +125° C

TEST SETUP FOR MEASUREMENT OF DEVICE DISSIPATION AND QUIESCENT OUTPUT VOLTAGE



$P_T = V_{CC}$ (I)

Fig.2

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
1	-3V	+3V	1	Connected to Voltage Source through 100Ω Resistor
			5	+12V
			10, 11, 12	Ground
2	-3V	+12V	5	+12V
			10, 11, 12	Ground
3	0V	+12V	5	+12V
			10, 11, 12	Ground
4	-12V	+12V	6, 11	Ground
	10 max. mA			
5	0V	+18V	10, 11, 12	Ground
6	-12V	+12V	5, 11	Ground
	10 max. mA			

	VOLTAGE OR CURRENT LIMITS		CIRCUIT CONDITIONS	
TERMINAL	NEGATIVE	POSITIVE	TERMINAL	CONDITIONS
7	0V	+12V	5	+12V
			10, 11, 12	Ground
8	20 max. mA		5	+12V
			10, 11, 12	Ground
9	-0.5V	+3V	5	+12V
			10, 11, 12	Ground
10	0V	+4V	2,5	+12V
			11	Ground
11	-6V	+12V	2	Ground
			5	+12V
12	0V	+4V	2,5	+12V
			11	Ground

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3021

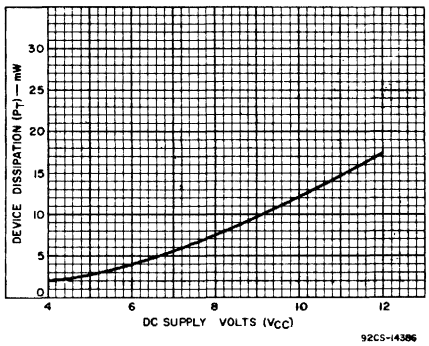


Fig.3(a)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3022

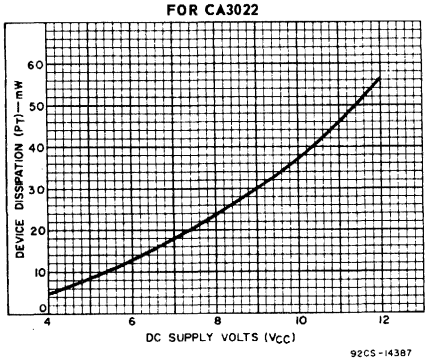


Fig.3(b)

DEVICE DISSIPATION VS DC SUPPLY VOLTAGE FOR CA3023

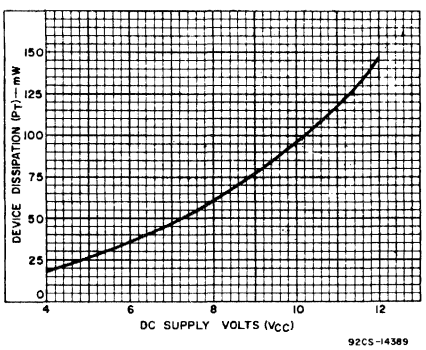


Fig.3(c)

DEVICE DISSIPATION VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

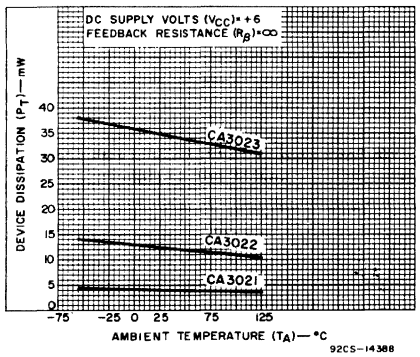


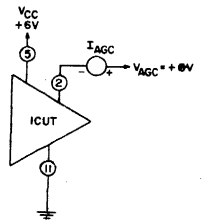
Fig.3(d)

CA3021, CA3022, CA3023

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, unless otherwise specified

CHARACTERISTIC		SYMBOL	TEST CONDITIONS			LIMITS									UNITS	TYPICAL CHARACTERISTIC CURVE
			TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FREQUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)				
			Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation		P_T	2	∞	-	1	4	8	-	-	-	-	-	-	mW	3a,d
				∞	-	-	-	-	5	12.5	24	-	-	-	mW	3b,d
				∞	-	-	-	-	-	-	-	24	35	48	mW	3c,d
Quiescent Output Voltage		V_O	2	39k	-	-	2.2	-	-	-	-	-	-	-	V	-
				10k	-	-	-	-	-	1.9	-	-	-	-	V	
				4.7k	-	-	-	-	-	-	-	-	1.3	-	V	
AGC Source Current		I_{AGC}	4	V_{AGC} =+6V		-	0.8	-	-	0.8	-	-	0.8	-	mA	-
Voltage Gain		A	5	560k	0.5	50	56	-	-	-	-	-	-	-	dB	6a
				39k	0.8	40	46	-	-	-	-	-	-	-	dB	6a,d
				39k	2.5	-	-	-	50	57	-	-	-	-	dB	6b
				10k	3	-	-	-	40	44	-	-	-	-	dB	6b,d
				18k	5	-	-	-	-	-	-	50	53	-	dB	6c
				4.7k	10	-	-	-	-	-	-	40	44	-	dB	6c,d
Bandwidth at -3 dB Point		BW	5	39k	-	0.8	2.4	-	-	-	-	-	-	-	MHz	6a
				10k	-	-	-	-	3	7.5	-	-	-	-	MHz	6b
				4.7k	-	-	-	-	-	-	-	10	16	-	MHz	6c
Input-Impedance Components	Input Resistance	R_{IN}	7	39k	1	-	4000	-	-	-	-	-	-	-	Ω	-
				10k	5	-	-	-	-	1300	-	-	-	-	Ω	
				4.7k	10	-	-	-	-	-	-	-	300	-	Ω	
	Input Capacitance	C_{IN}	7	39k	1	-	11	-	-	-	-	-	-	-	pF	-
				10k	5	-	-	-	-	18	-	-	-	-	pF	
				4.7k	10	-	-	-	-	-	-	-	13	-	pF	
Output Resistance		R_{OUT}	8	39k	1	-	300	-	-	-	-	-	-	-	Ω	-
				10k	5	-	-	-	-	120	-	-	-	-	Ω	
				4.7k	10	-	-	-	-	-	-	-	100	-	Ω	
Noise Figure		NF	9	39k	1	-	4.2	8.5	-	-	-	-	-	-	dB	-
				10k	1	-	-	-	-	4.4	8.5	-	-	-	dB	
				4.7k	1	-	-	-	-	-	-	-	6.5	8.5	dB	
AGC Range		AGC	10	-	1	-	33	-	-	-	-	-	-	-	dB	-
				-	5	-	-	-	-	33	-	-	-	-	dB	
				-	10	-	-	-	-	-	-	-	33	-	dB	
Maximum Output Voltage (RMS Value)		v_{out}	5	39k	1	-	0.6	-	-	-	-	-	-	-	V(rms)	-
				10k	5	-	-	-	-	0.7	-	-	-	-	V(rms)	
				4.7k	10	-	-	-	-	-	-	-	0.5	-	V(rms)	

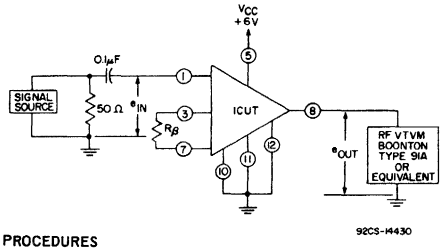
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig.4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mVat frequency specified, read e_{out} Voltage Gain (A) = $20 \log_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig.5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

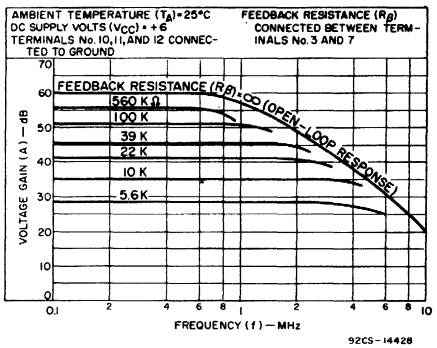


Fig.6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

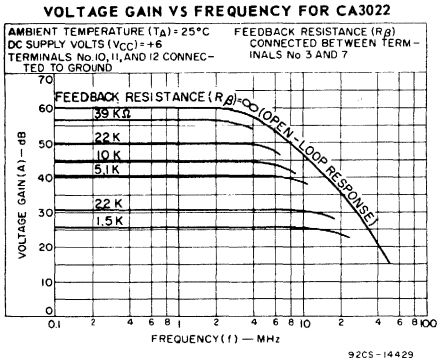


Fig.6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

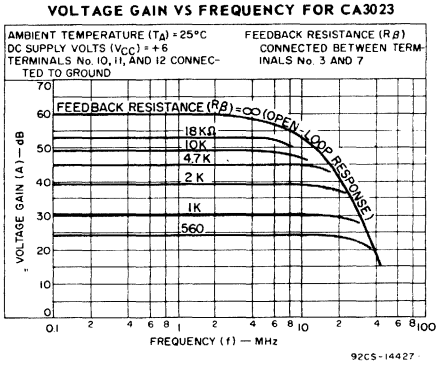


Fig.6(c)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

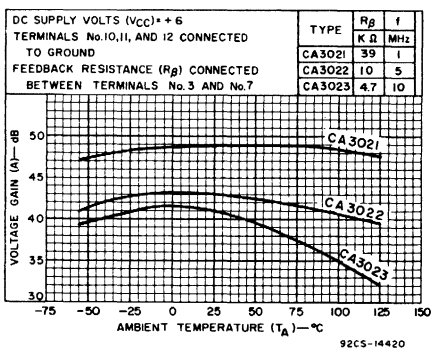
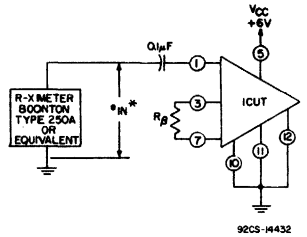


Fig.6(d)

CA3021, CA3022, CA3023

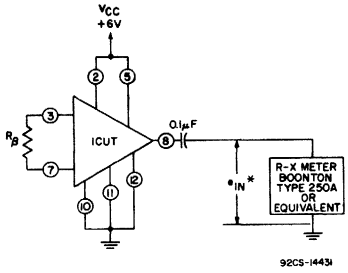
TEST SETUP FOR MEASUREMENT OF INPUT-IMPEDANCE COMPONENTS



* $e_{in} \leq 10$ mV

Fig.7

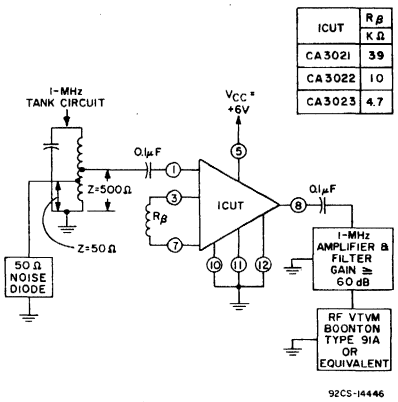
TEST SETUP FOR MEASUREMENT OF OUTPUT RESISTANCE



* $e_{in} \leq 10$ mV

Fig.8

TEST SETUP FOR MEASUREMENT OF NOISE FIGURE

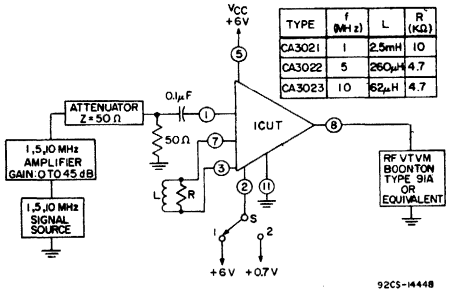


ICUT	Rβ KΩ
CA3021	39
CA3022	10
CA3023	4.7

CA3021 - $R_\beta = 39\ k\Omega$
CA3022 - $R_\beta = 10\ k\Omega$
CA3023 - $R_\beta = 4.7\ k\Omega$

Fig.9

TEST SETUP FOR MEASUREMENT OF AGC RANGE



TYPE	f (MHz)	L	R (KΩ)
CA3021	1	2.5mH	10
CA3022	5	260μH	4.7
CA3023	10	62μH	4.7

$$\text{AGC RANGE} = 20 \log_{10} \frac{\text{A WITH S IN POSITION 1}}{\text{A WITH S IN POSITION 2}}$$

(A = VOLTAGE GAIN)

	f MHz
CA3021	1
CA3022	5
CA3023	10

Fig. 10

CA3026, CA3054

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies from DC to 120 MHz

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF/Mixer/ Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascode limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ±5 mV
- Full military temperature range capability -- -55°C to +125°C
- Limited temperature range -- 0°C to 85°C for CA3054

- **The CA3054 is available in a sealed-junction Beam-Lead version (CA3054L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**
- **CA3026—Hermetic 12-lead TO-5 package**
- **CA3054—14-lead dual-in-line plastic package**

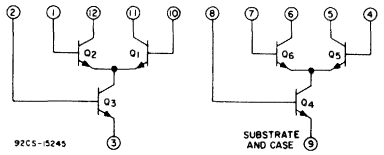


Fig.1a - Schematic Diagram for CA3026.

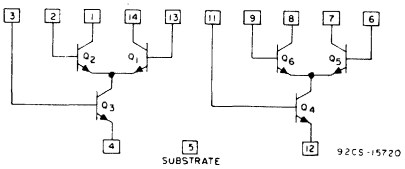


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3026	CA3054	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125		°C
Storage	-65 to + 150		°C
Lead Temperature (During Soldering):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 → TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*.	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

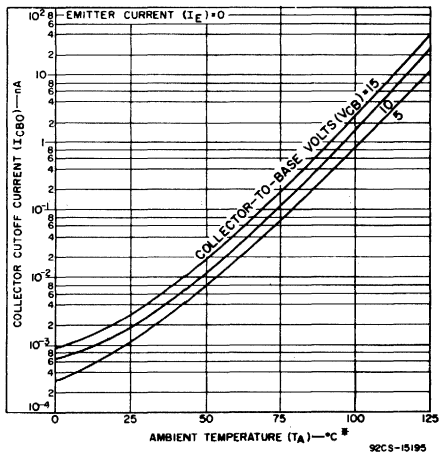
Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

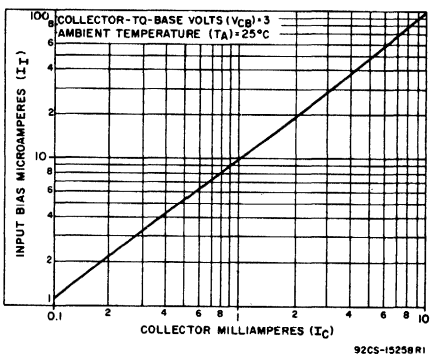


Fig.3 - Input bias current characteristic vs collector current for each transistor.

CA3026, CA3054

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	CA3026 CA3054 LIMITS			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V; I_C = 50 μA	-	-	0.630	0.700	V	6
		I_C = 1 mA	-	-	0.715	0.800		
		I_C = 3 mA	-	-	0.750	0.850		
		I_C = 10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_x = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D

1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003+j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

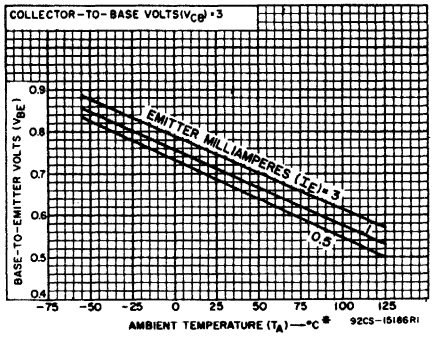


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

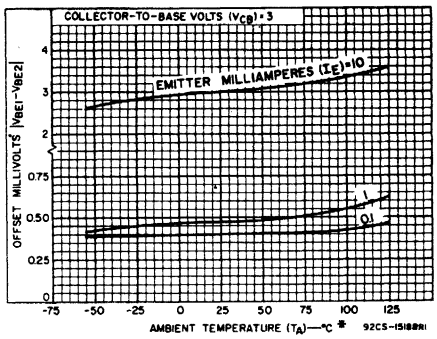


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

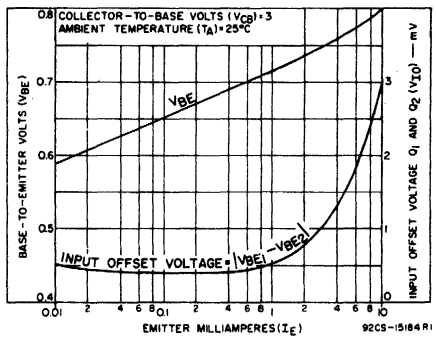


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

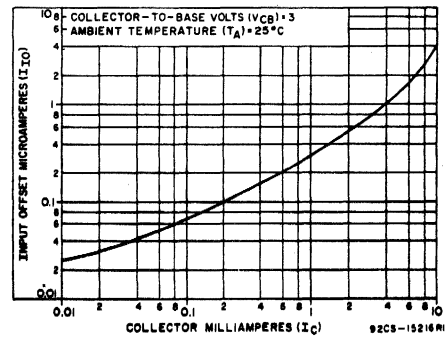
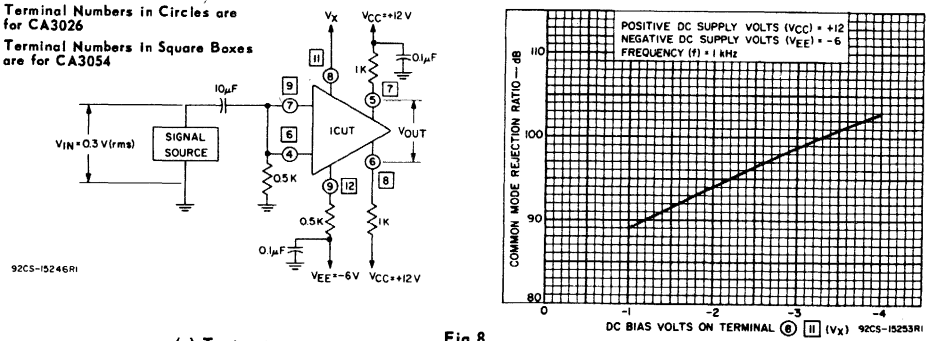


Fig.7 - Input offset current for matched differential pairs vs collector current.

CA3026, CA3054

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO

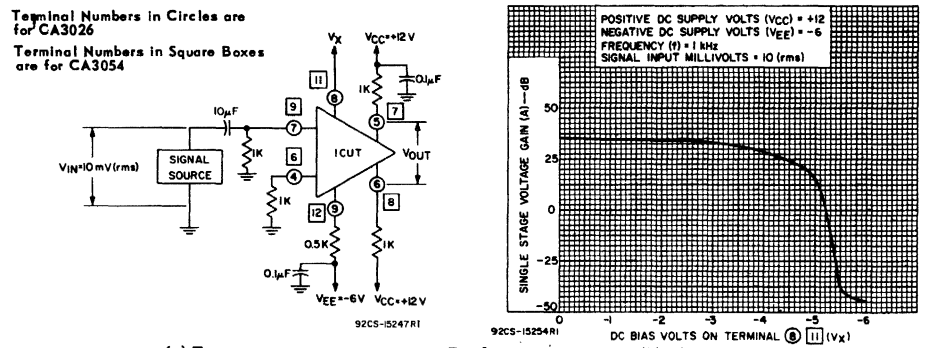


(a) Test setup

Fig.8

(b) Characteristic

SINGLE-STAGE VOLTAGE GAIN

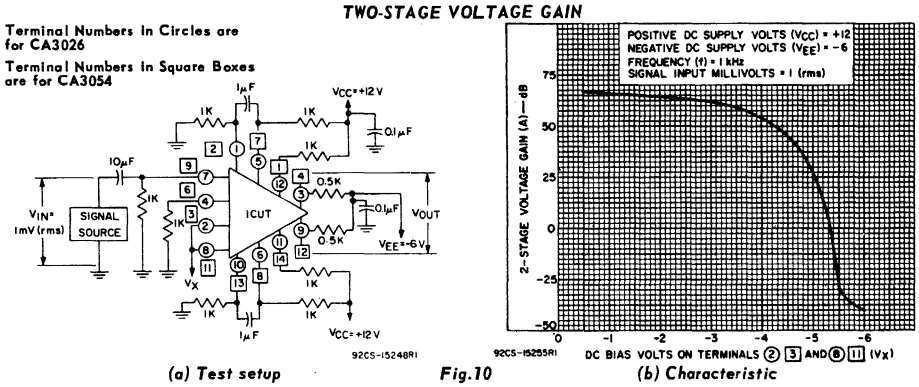


(a) Test setup

Fig.9

(b) Characteristic

TWO-STAGE VOLTAGE GAIN



(a) Test setup

Fig.10

(b) Characteristic

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

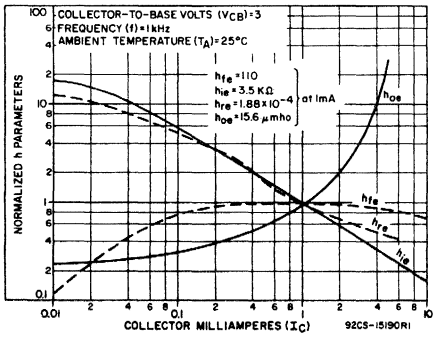


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

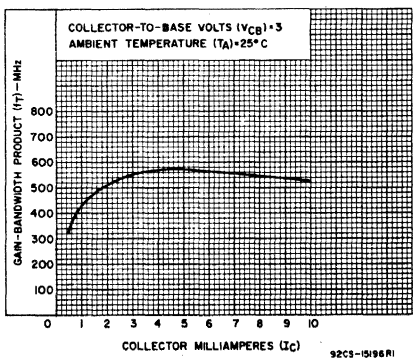


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

CA3026, CA3054

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

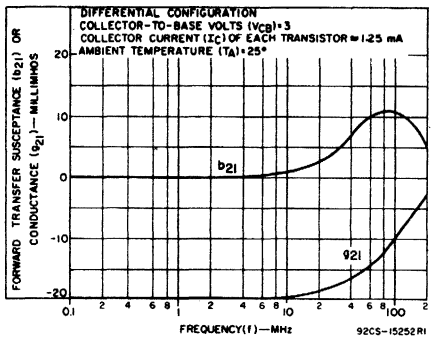


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

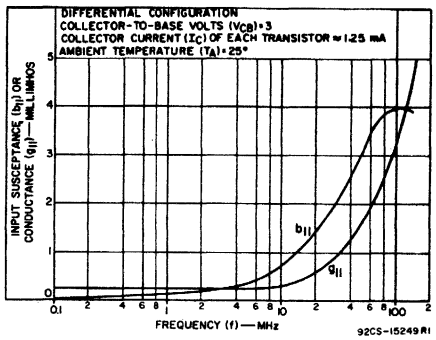


Fig.13(b) - Input admittance (Y_{11}).

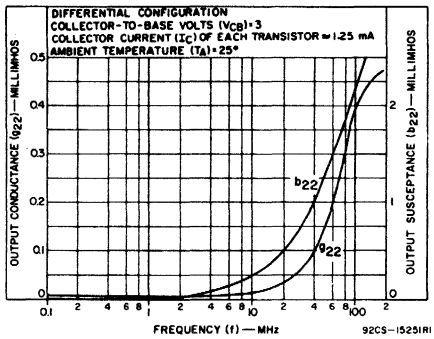


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

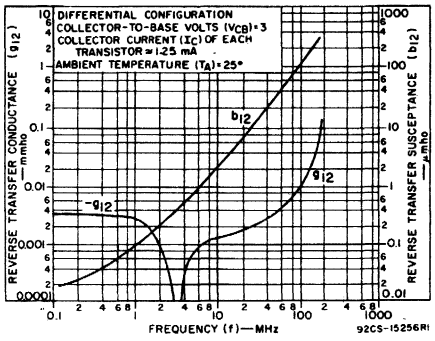


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

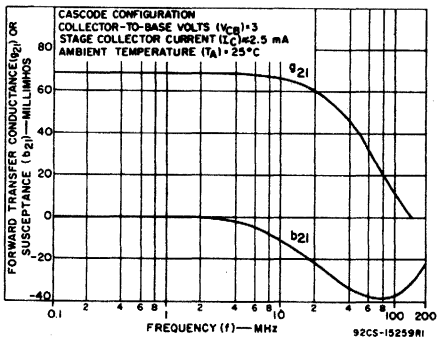


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

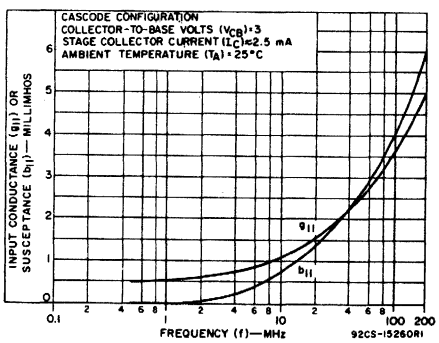


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

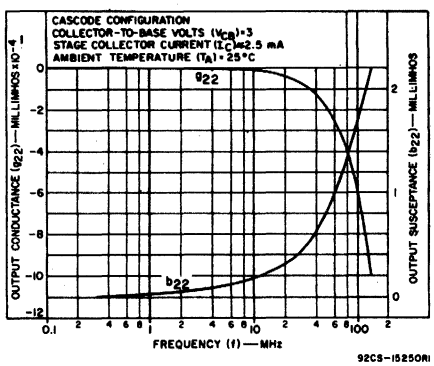


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

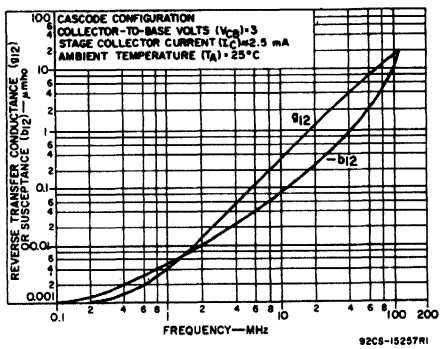


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

CA3028, CA3028A, CA3053

DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are supplied in a hermetic 8-lead TO-5-style package. The "F" versions are supplied in a frit-seal package and the "S" versions in formed-lead (DIL-CAN) packages.

FEATURES

- **Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028B)**
- **Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility**
- **Single- and Dual-Ended Operation**
- **Operation from DC to 120 MHz**
- **Balanced-AGC Capability**
- **Wide Operating-Current Range**

• The CA3028A is available in a sealed-junction Beam-Lead version (CA3028AL). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

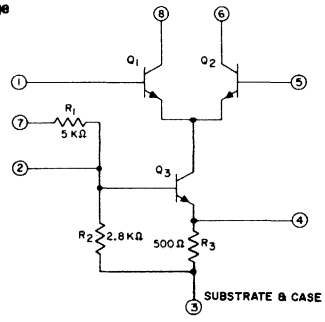


Fig.1 - Schematic diagram for CA3028A, CA3028B and CA3053.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:
- At T_A up to 55°C (CA3028AF, CA3028BF, CA3053F) ..... 750 mW
- At T_A > 55°C (CA3028AF, CA3028BF, CA3053F) ..... Derate linearly 6.67 mW/°C
- At T_A up to 85°C (CA3028A, CA3028B, CA3053) ..... 450 mW
- At T_A > 85°C (CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:
- Operating ..... −55°C to +125°C
- Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	-	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	-	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} = +9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	-	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	-	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

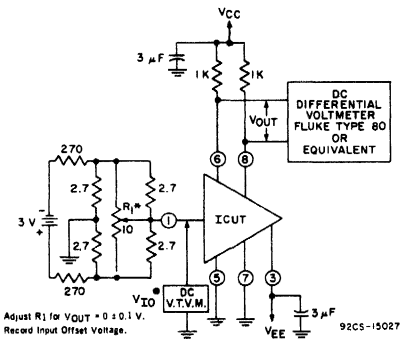


Fig.2 - Input offset voltage test circuit for CA3028B.

CA3028, CA3028A, CA3053

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A Min.	Typ.	Max	LIMITS TYPE CA3028B Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS												
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	dB	10b
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-		11b
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	dB	10c
		11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz, V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-	mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-		13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-	mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-		15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-	mmho	16
		-		Diff.-Ampl.				-	-37 + j0.5	-		17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-	mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-		19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	dB	21b
Voltage Gain, at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	dB	22b
		22c	V_{CC} = +0V, R_L = 1 kΩ	Diff.-Ampl.	-	30	-	-	30	-		22d
Voltage Gain, Differential at f = 1 kHz		23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	15	23	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	-2.5	(-3.2 - 4.5)	4	V	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-5	(-7 - 9)	7		
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V		-	-	-	60	110	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	90	-		
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V		-	-	-	-	5.5	-	kΩ	-
			V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	3	-		
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V	f = 10.7 MHz, e_{in} = 400 mV Diff.-Ampl.	2	4	7	2.5	4	6	mA	-
			V_{CC} = +12V		3.5	6	10	4.5	6	8		

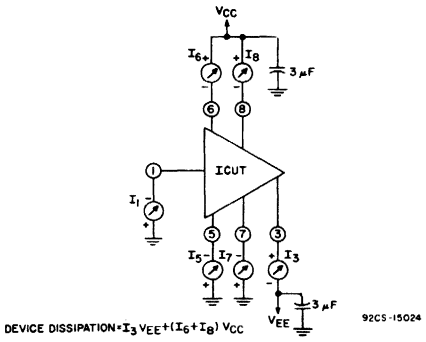


Fig.3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

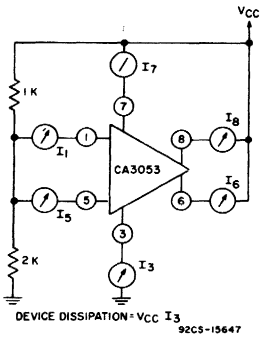


Fig.3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3053 Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	10a	f = 10.7 MHz	Cascode	35	39	-	dB	
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32			
Input Admittance	Y_{11}	-	f = 10.7 MHz, V_{CC} = +9V	Cascode	-	0.6 + j 1.6	-	mmho	12
		-		Diff.-Ampl.	-	0.5 + j 0.5	-		13
Reverse Transfer Admittance	Y_{12}	-		Cascode	-	0.0003 - j0	-	mmho	14
		-		Diff.-Ampl.	-	0.01 - j0.0002	-		15
Forward Transfer Admittance	Y_{21}	-		Cascode	-	99 - j18	-	mmho	16
		-		Diff.-Ampl.	-	-37 + j0.5	-		17
Output Admittance	Y_{22}	-		Cascode	-	0. + j0.08	-	mmho	18
		-		Diff.-Ampl.	-	0.04 + j0.23	-		19
Voltage Gain, at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	dB	22b
		22c	V_{CC} = +0V, R_L = 1 kΩ	Diff.-Ampl.	-	30	-		22d
Peak-to-Peak Output Current	P-P		V_{CC} = +9V	f = 10.7 MHz, e_{in} = 400 mV Diff.-Ampl.	2	4	7	mA	
			V_{CC} = +12V		3.5	6	10		

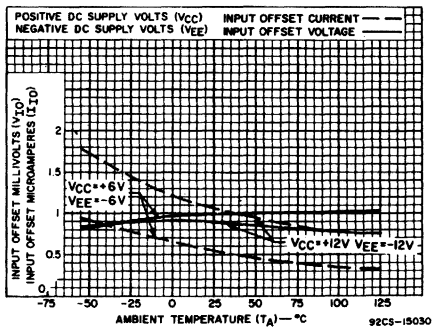


Fig.4 - Input offset voltage and input offset current for CA3028B.

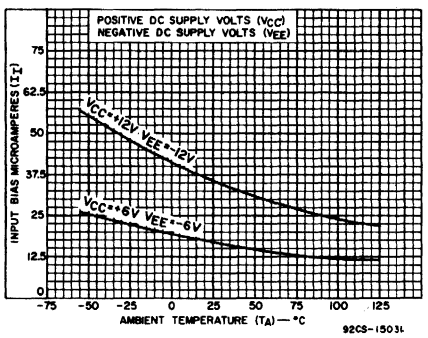


Fig.5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

CA3028,CA3028A, CA3053

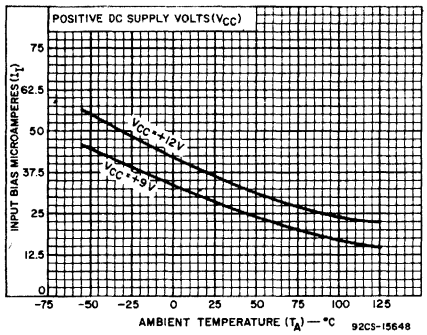


Fig.5b - Input bias current vs. ambient temperature for CA3053.

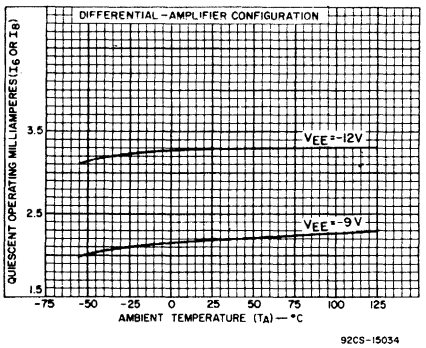


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

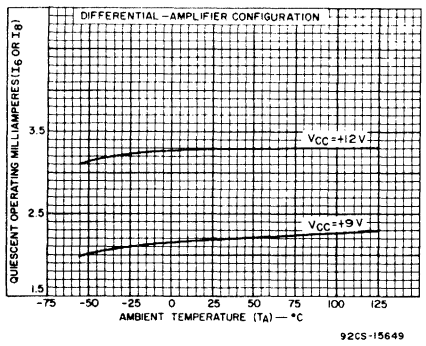


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

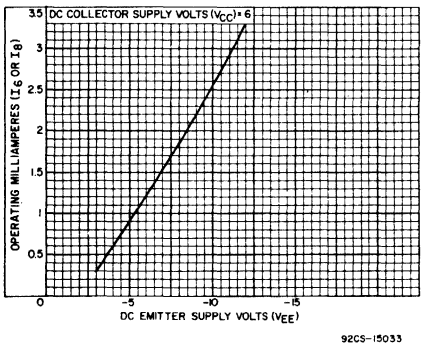


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

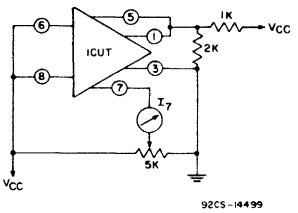


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

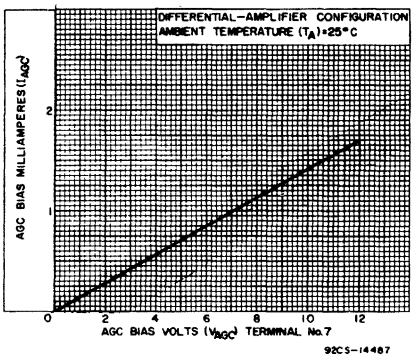


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

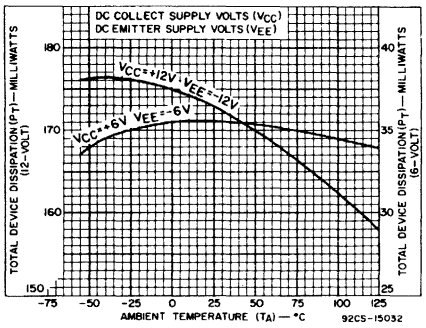
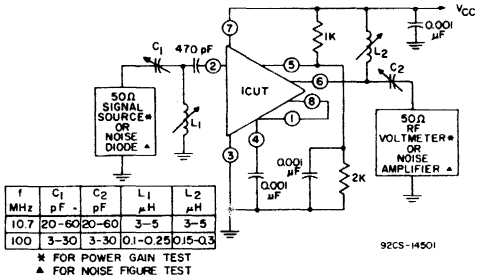


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

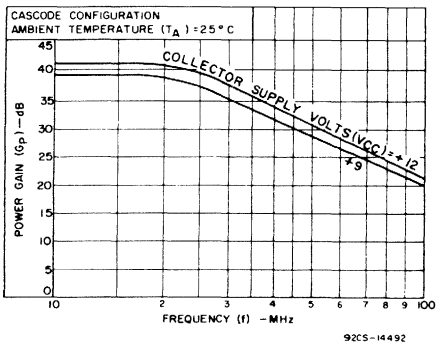


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

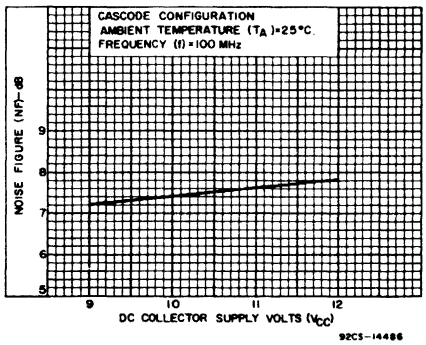
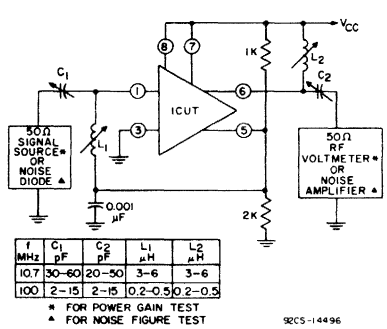


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

CA3028, CA3028A, CA3053

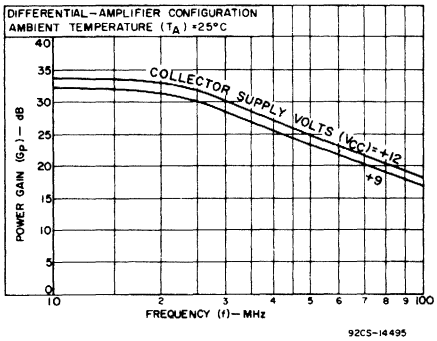


Fig.11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

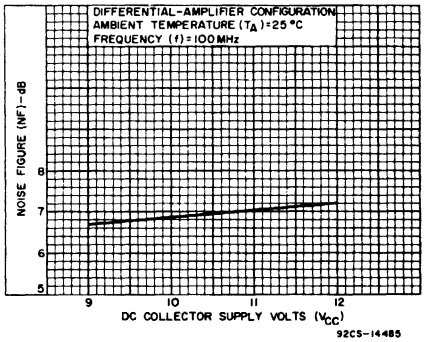


Fig.11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.

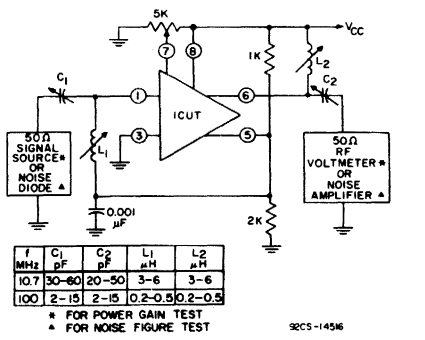


Fig.11d - Power gain and noise figure test circuit (differential-amplifier configuration for CA3028A and CA3028B.

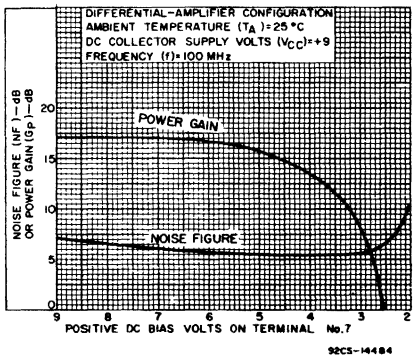


Fig.11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No.7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

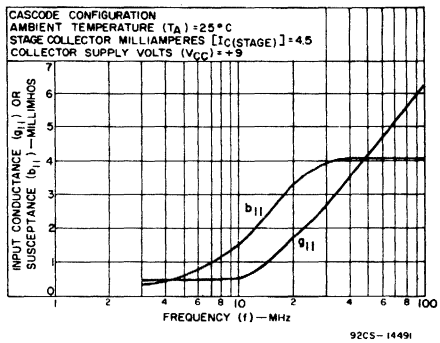


Fig.12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

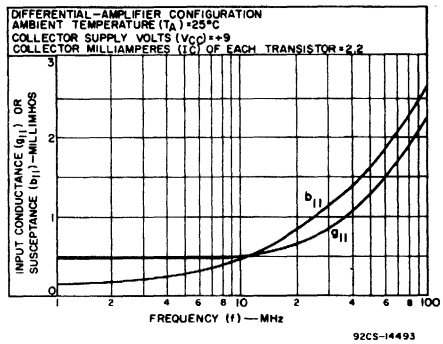


Fig.13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

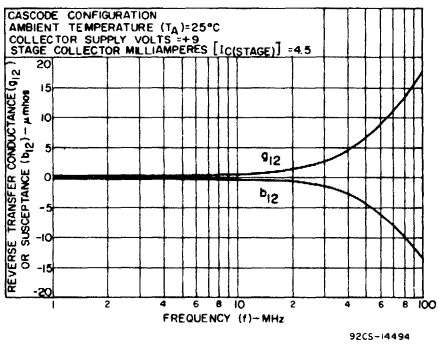


Fig.14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

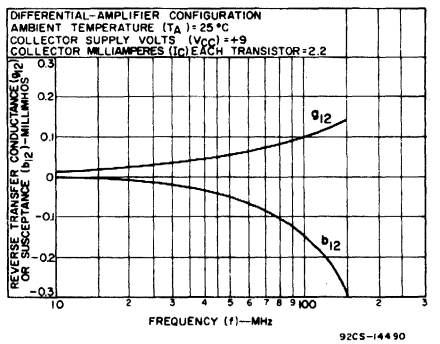


Fig.15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

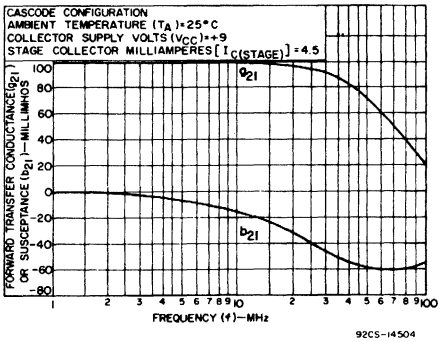


Fig.16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

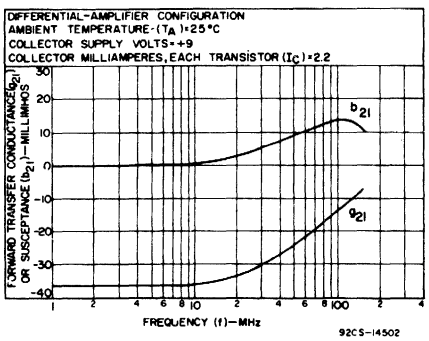


Fig.17 - Forward transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

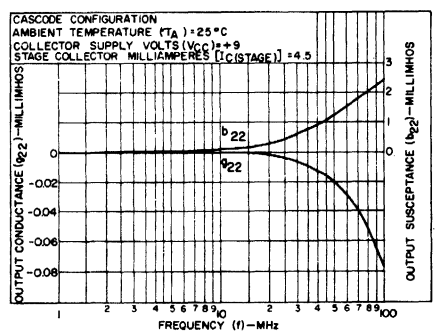


Fig.18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

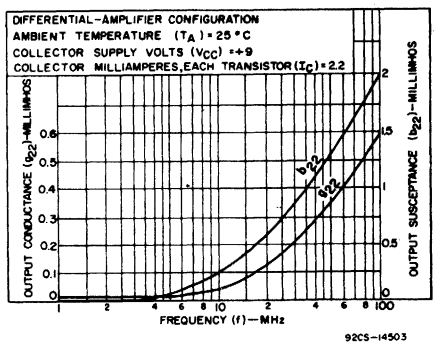


Fig.19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

CA3028, CA3028A, CA3053

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

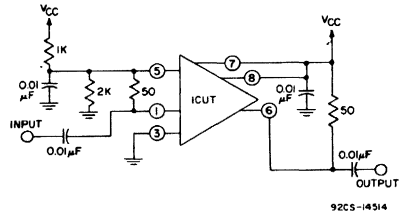


Fig.20a - Output power test circuit for CA3028A and CA3028B.

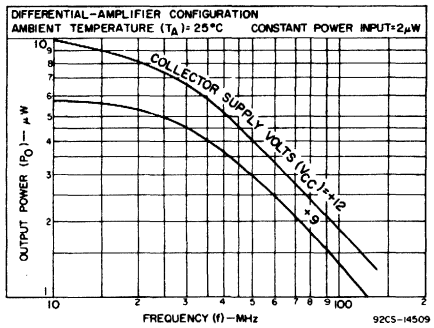
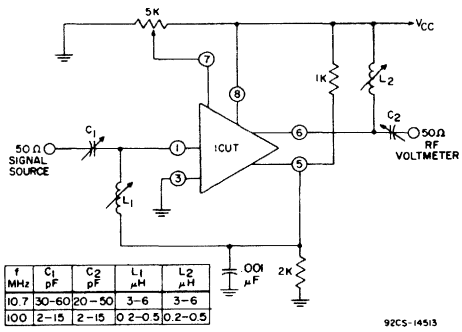


Fig.20b - Output power vs. frequency — 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C1 pF	C2 pF	L1 μH	L2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

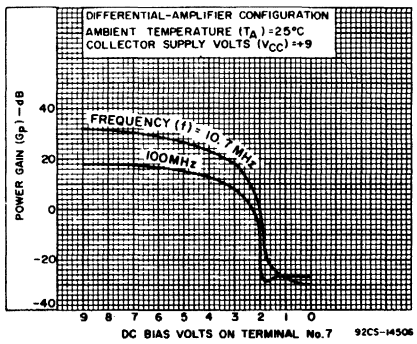


Fig.21b - AGC characteristics for CA3028A and CA3028B.

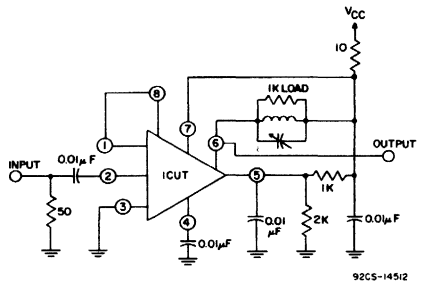


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

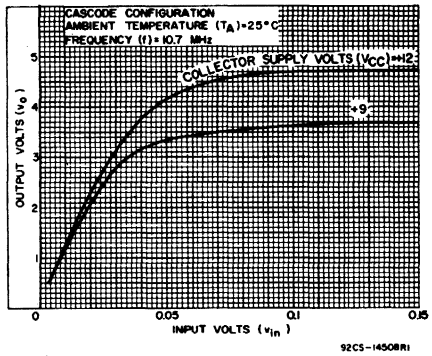


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

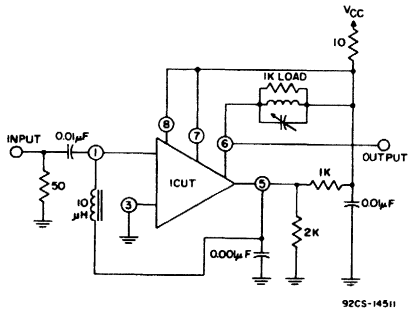


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

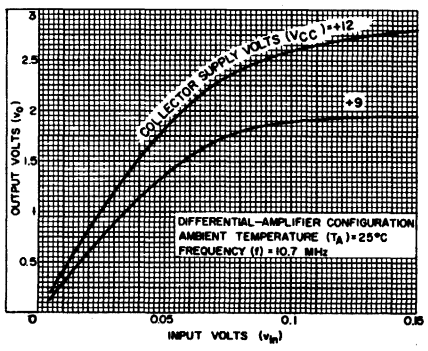
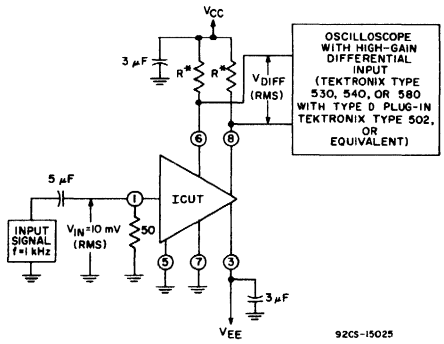
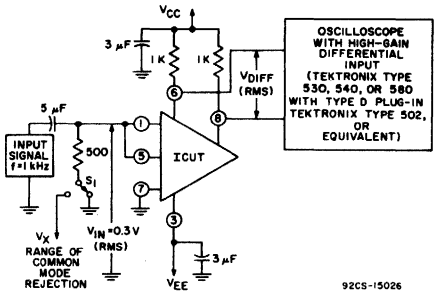


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.



* For R = 1.6 kΩ — (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ — (V_{CC} = 6V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\ (2)\ (0.3)}{V_{DIFF\ (RMS)}}$

* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

CA3033, CA3047 Types
Operational Amplifiers

For High-Output-Current Applications

RCA-CA3033 is a high-performance integrated circuit operational amplifier featuring high input impedance, high gain, high power output, and low input-offset voltage and current. The device consists of two differential amplifiers in cascade and a single-ended class-B power output stage on a single monolithic silicon chip.

RCA-CA3033A has all the superior features and characteristics of the CA3033 but, in addition, can be operated at higher supply voltages to provide higher gain, higher common mode rejection, greater maximum output voltage swing, and more than double the power output.

RCA-CA3033 and CA3033A are hermetically sealed in 14-lead "dual-in-line" ceramic packages and are designed for operation over the full military temperature range of −55 °C to +125 °C.

The RCA-CA3047 and CA3047A are supplied in 14-lead "dual-in-line" plastic packages and are designed to operate over the temperature range of 0 °C to +70 °C, ambient.

Companion Application Note, ICAN-5641 "Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers."

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

The RCA-CA3047 and CA3047A are electrically identical to the CA3033 and CA3033A, respectively, but are limited in operating and storage temperature range.

FEATURES

	CA3033 CA3047 V⁺ = +12 V V⁻ = −12 V	CA3033A CA3047A V⁺ = 15 V V⁻ = −15 V	
■ Output Current	36	76	mA min.
■ Input Offset Current	35	25	nA max.
■ Open Loop Differential Gain	84	87	dB min.
■ Output Voltage Swing	18	23	V_{p-p} min.
■ Input Bias Current	350	180	nA max.
■ Power Output	80	220	mW min.
■ Common Mode Rejection Ratio	84	93	dB min.

APPLICATIONS

- Comparator
- Integrator
- Differentiator
- Audio Amplifier
- Summing Amplifier
- Servo Driver
- DC Amplifier
- Multivibrator
- Narrow Band and Band Pass Amplifier

ABSOLUTE-MAXIMUM RATINGS

	CA3033	CA3033A	CA3047	CA3047A
INPUT SIGNAL VOLTAGE	±10 V	−13 V, +10 V	±10 V	−13V, +10 V
DEVICE DISSIPATION:				
Up to T_A = 25 °C	1.2 W	1.2 W	750 mW	750 mW
Above T_A = 25 °C	Derate at 8 mW/°C		Derate at 6.67 mW/°C	
TEMPERATURE RANGE:				
Operating	−55 °C to +125 °C		0 °C to +70 °C	
Storage	−65 °C to +150 °C		−65 °C to +150 °C	
LEAD TEMPERATURE (During Soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265 °C			

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — CA3033, CA3047

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+26 0
3				*	*	0 −26	*	*	*	*	*	*	*	+26 0
4					+5 −1	0 −15	*	*	*	*	*	*	*	+26 0
5						0 −26	*	+20 −1 Note 1	*	*	*	*	+20 −1 Note 1	*
6							+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0
7								+20 −2 Note 1	*	*	*	*	+20 −2 Note 1	+26 0
8									+20 −1 Note 2	+20 −2 Note 3	+20 −2 Note 3	+20 −1 Note 2	*	+26 0
9										+1 −5	*	+5 −5	+1 −20 Note 2	+26 −5
10											+10 −10	*	+2 −20 Note 3	+26 −10
11												+1 −5	+2 −20 Note 3	+26 −10
12													+1 −20 Note 2	+26 −5
13														*
14														Substrate

MAXIMUM CURRENT RATINGS — CA3033 CA3047 CA3033A CA3047A

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	20	-
3	50	50
4	10	10
5	5	5
6	-	-
7	5	5
8	1	1
9	1	0.1
10	1	0.1
11	1	0.1
12	1	0.1
13	1	1
14	-	-

Notes: 1. This rating applies to the more positive terminal of terminals 8 and 13.
2. This rating applies to the more positive terminal of terminals 9 and 12.
3. This rating applies to the more positive terminal of terminals 10 and 11.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

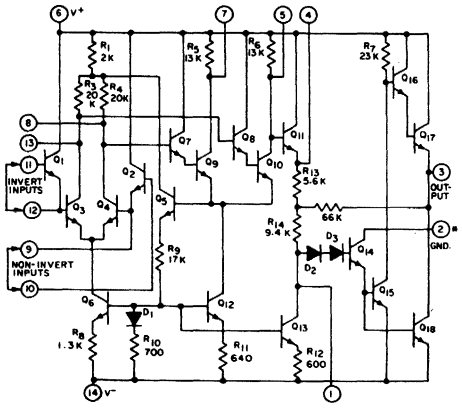


Fig. 1 - Schematic diagram of operational amplifiers, CA3033, CA3033A, CA3047, CA3047A.

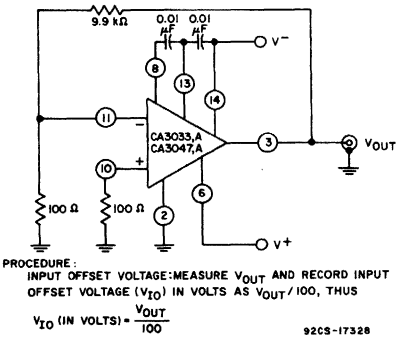


Fig. 2a - Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.

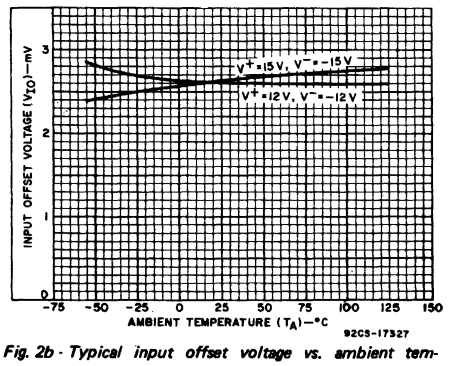


Fig. 2b - Typical input offset voltage vs. ambient temperature.

CA3033, CA3047 Types

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — **CA3033A, CA3047A**

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+38 0
3				*	*	0 -38	*	*	*	*	*	*	*	+38 0
4					+5 -1	0 -22	*	*	*	*	*	*	*	+38 0
5						0 -38	*	+30 -1 Note 1	*	*	*	*	+30 -2 Note 1	*
6							+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0
7								+30 -2 Note 1	*	*	*	*	+20 -2 Note 1	+38 0
8									+30 -1 Note 2	+30 -2 Note 3	+30 -2 Note 3	+30 -1 Note 2	*	+38 0
9										+1 -5	*	+5 -5	+1 -30 Note 2	+38 -5
10											+10 -10	*	+2 -20 Note 3	+38 -10
11												+1 -5	+2 -30 Note 3	+38 -10
12													+1 -30 Note 2	+38 -5
13														*
14														Sub-strate

Notes: See CA3033, CA3047 Rating Chart Notes.

MAXIMUM CURRENT RATINGS are identical for all four types (See CA3033, CA3047 chart)

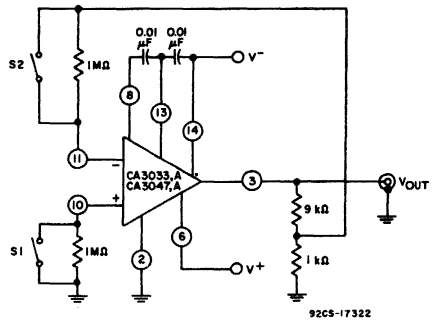


Fig. 3a - Input offset current and input bias current test circuit.

PROCEDURES:

A. Inverting Input Current

Set switch, S_1 in closed position and set switch, S_2 in open position.

Measure output voltage and convert this reading to inverting input current using the following relation:

$$I_I \text{ inverting (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

B. Non-inverting Input Current

Set switch, S_1 in open position and set switch, S_2 in closed position.

Measure output voltage and convert this reading to non-inverting input current using the following relation:

$$I_I \text{ non-inverting (in } \mu A) = \frac{-V_{OUT} \text{ (in volts)}}{10}$$

C. Input Offset Current

Set switches, S_1 and S_2 in open positions.

Measure output voltage and convert this reading to input offset current using the following relation:

$$I_{IO} \text{ (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

ELECTRICAL CHARACTERISTICS
For Equipment Design

Characteristics	Symbols	Test Conditions			Typical Characteristics Curves	LIMITS CA3033 CA3047 DC Supply Voltage V^+ = 12 V, V^- = −12 V			LIMITS CA3033A CA3047A DC Supply Voltage V^+ = 15 V, V^- = −15 V			Units
		Circuit Fig.	T_A = 25° C		Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	2a			2b	–	2.6	5	–	2.9	5	mV
Input Offset Current	I_{IO}	3a			3b	–	5	35	–	9	25	nA
Input Bias Current	I_I	3a			3c	–	70	350	–	100	180	nA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V^-$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Device Dissipation	P_T	2a			–	60	120	180	80	170	300	mW
Open-Loop Differential Voltage Gain	A_{OL}	–	f = 1 kHz		4	84	90	–	87	93	–	dB
Common-Mode Rejection Ratio	CMRR	–			5	84	100	–	93	105	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–			–	−7.5	+5,−9	+3.5	−9.7	6,−11	4.7	V
Maximum Output-Voltage Swing	$V_{O(P-P)}$	–	f = 1 kHz	R_L = 500 Ω	–	18	22	–	–	–	–	V_{P-P}
				R_L = 300 Ω		–	–	–	23	25	–	
Input Impedance	Z_I	–			–	0.25	1.5	–	0.6	1	–	MΩ
Output Current	I_O	–		R_L = 500 Ω	6	35	44	–	–	–	–	mA-(P-P)
				R_L = 300 Ω		–	–	–	76	83	–	
Power Output THD <5%	P_o	–		R_L = 500 Ω	7	80	122	–	–	–	–	mW
				R_L = 300 Ω		–	–	–	220	255	–	

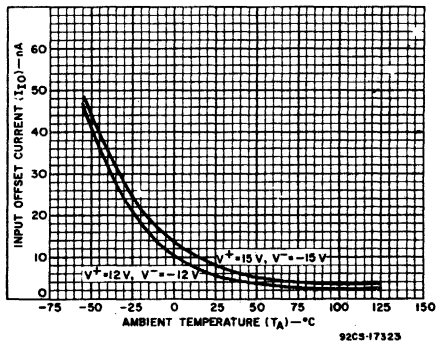


Fig. 3b - Typical input offset current vs. ambient temperature.

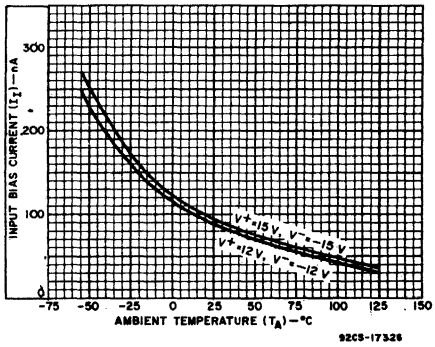


Fig. 3c - Typical input bias current vs. ambient temperature.

CA3033, CA3047 Types

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

Input Offset Voltage Drift −55°C to 125°C	$V_{IO}/\Delta T$	2a		2b	–	6.6	–	–	6.6	–	μV/°C
Input Offset Current Drift											
−55°C to 25°C	$I_{IO}/\Delta T$	3a		3b	–	1	–	–	1	–	nA/°C
25°C to 125°C					–	0.08	–	–	0.08	–	
60-dB Amplifier Bandwidth	BW	8a	C_X, C_Y = 0.001 μF	8b,c	–	230	–	–	350	–	kHz
Slew Rate	SR	9	(amplifier circuit only)	–	–	2.7	–	–	3	–	V/μs

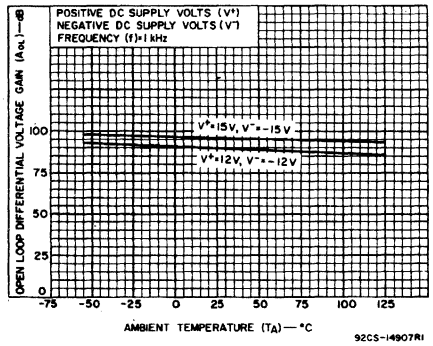


Fig. 4 - Typical open-loop differential voltage gain vs. ambient temperature.

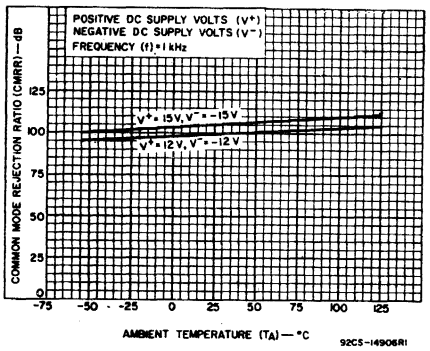


Fig. 5 - Typical common mode rejection ratio vs. ambient temperature.

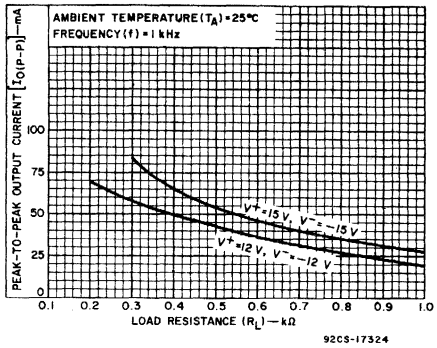


Fig. 6 - Typical peak-to-peak output current vs. load resistance.

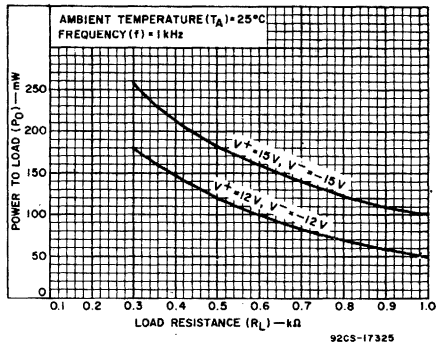


Fig. 7 - Typical power output vs. load resistance.

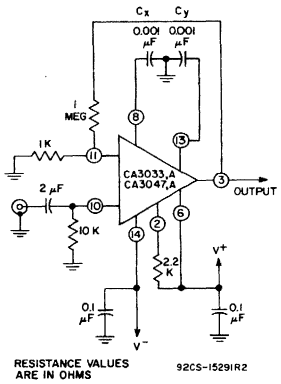


Fig. 8a - Typical 60-dB amplifier.

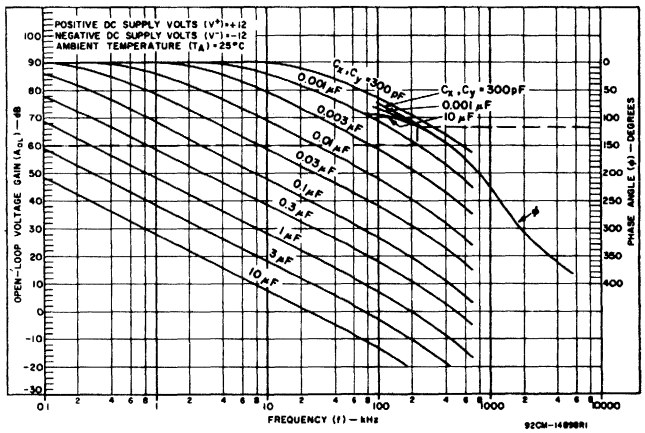


Fig. 8b - Typical phase compensation characteristics for CA3033, CA3047 (V^+ = +12 V, V^- = −12 V)

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network. As the closed loop gain approaches unity, the compensating capacitors required (0.3 μF to 1.0 μF) are bulky and costly. A capacitor one-half the value shown on the chart, connected between terminals 8 and 13, and a 0.001 μF capacitor from either terminals 8 or 13 to ground or V^- is an acceptable alternative method. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of more readily available, lower-voltage disc capacitors which are smaller and cost less. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

Figure 8a shows the phase compensating capacitors (C_X, C_Y) returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V^-) supply may result in more stable operation.

CA3033, CA3047 Types

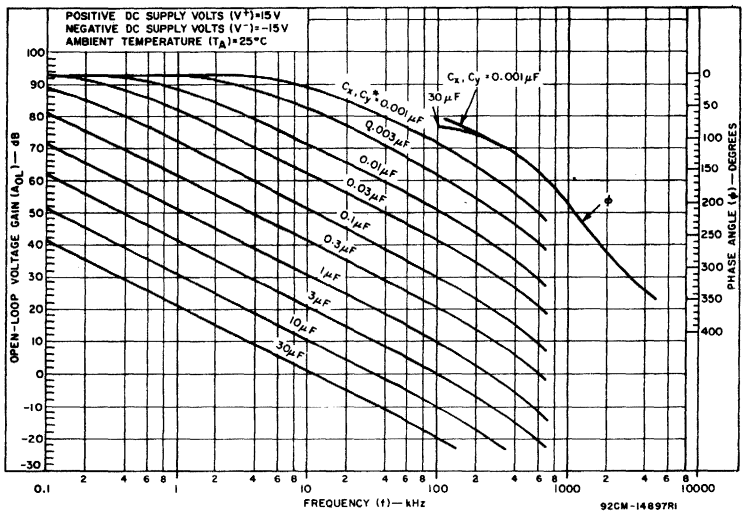
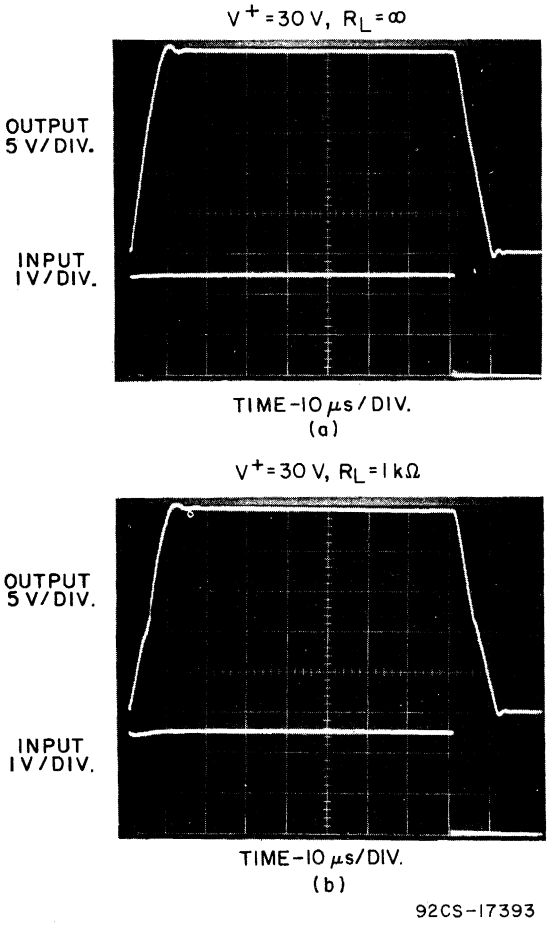
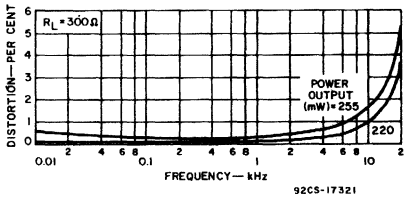


Fig. 8c - Typical phase compensation characteristics for CA3033A, CA3047A ($V^+ = 15$ V, $V^- = -15$ V).





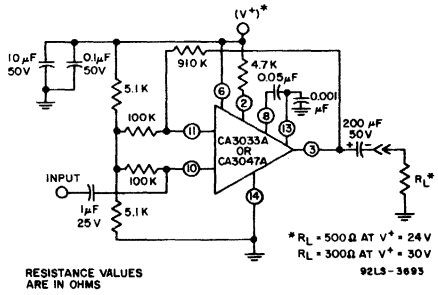


Fig. 9 - Amplifier with single voltage supply and associated pulse response waveforms and distortion curves.

OPERATING CONSIDERATIONS

The CA3033, CA3033A, CA3047, and CA3047A operational amplifiers have very high peak-pulse current capability. The open-loop output impedance is typically less than 30 ohms at 10 kHz and the peak short-circuit output current may exceed 100 milliamperes. To prevent possible damage to the chip because of excessive dissipation it is important that the output stage is not subjected to sustained high peak currents. To minimize the possibility of damage from accidental shorts, it is recommended that a 51-ohm resistor be placed in series with the output circuit.

When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q_{14}. This resistor may be returned to ground, or, if its value is increased to 4700 ohms; it may be returned to the V^+ terminal.

CA3035, CA3035V1

Ultra-High-Gain Wide-Band Amplifier Array

Monolithic Silicon

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

HIGHLIGHTS

- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to +125°C
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Device Dissipation ..... 300 mW
Input Voltage ..... 1 V p-p
Supply Voltage ..... +15V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARACTERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	 f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_1in R_2in R_3in	 f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_1out R_2out R_3out	f = 40 kHz		– – –	270 170 100K	– – –	Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	 V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	 NF_1	 f = 1 kHz, R_S = 1 KΩ	 Fig.4	 –	 6	 7	 dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μV

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

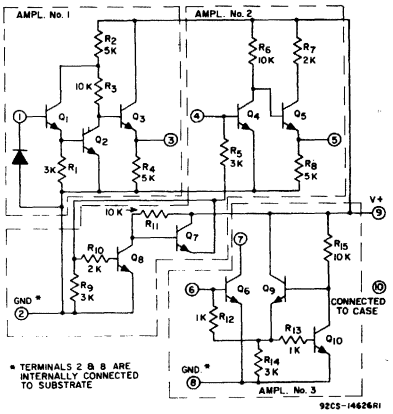


Fig. 1

TYPICAL REMOTE CONTROL SYSTEM

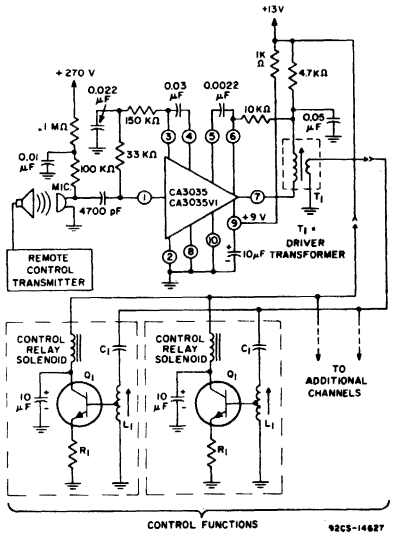


Fig. 2

STATIC CHARACTERISTICS TEST CIRCUIT

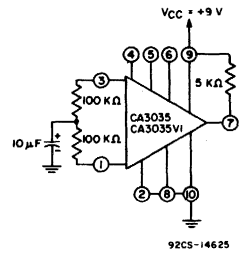
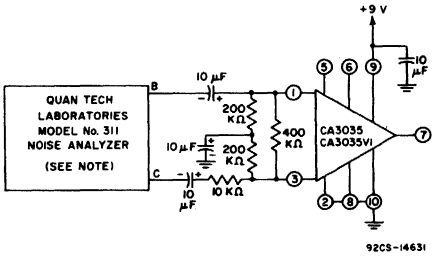


Fig. 3

NOISE FIGURE TEST CIRCUIT

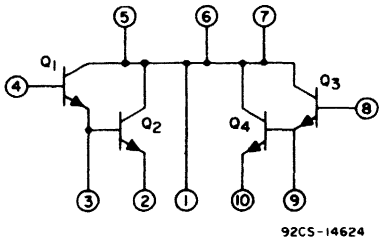


NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig. 4

CA3036
DUAL DARLINGTON ARRAY

- Two independent low-noise wide-band amplifier channels
- Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems
- Wide application in low-noise industrial instrumentation amplifiers



92CS-14624

Fig.1 – Schematic Diagram for CA3036.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036 Min.	Typ.	Max.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	V_{CB} = 5V, I_E = 0	–	–	0.5	μA
	Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	20	–	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	30	44	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	6	–	V
For Either Input Transistor (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or I_{C3} = 1 mA	30	82	–	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breadkown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or I_{E4} = 10 μA	10	12.6	–	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540	–	–
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, I_{C1} or I_{C3} = 1 mA	–	82	–	–
	Short-Circuit Input Impedance	h_{ie}		–	2.6K	–	Ω
	Open-Circuit Output Admittance	h_{oe}		–	7	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	9.8 x 10-5	–	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	–	1300	–	–
	Short-Circuit Input Impedance	$h_{ie(D)}$		–	82K	–	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		–	108	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		–	2.7 x 10-3	–	–
	Voltage Gain	$A_{(D)}$		–	26	–	dB
	Power Gain	$G_{p(D)}$		–	47	–	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	f = 100 Hz	–	0.2	3	$\mu V/\sqrt{f(Hz)}$
			f = 1 kHz	–	0.05	0.3	
			f = 10 kHz	–	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	f = 50 MHz, I_{C1} or I_{C3} = 2 mA	–	0.68 + j 7.9	–	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		–	4.14 + j 5.95	–	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		–	1.94 + j 2.64	–	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		–	Negligible	–	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA	–	1.71 + j 2.8	–	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		–	3.96 + j 2.6	–	mmho
	Gain-Bandwidth Product	$f_T(D)$		150	200	–	MHz

HIGHLIGHTS

- Matched transistors with emitter-follower outputs
- Low-noise performance
- 200-MHz gain-bandwidth product
- Operation from -55°C to +125°C
- Hermetically sealed, all-welded 10-lead TO-5-style metal package

APPLICATIONS

- Stereo phonograph preamplifiers
- Low-level stereo and single channel (B) amplifier stages
- Low-noise, emitter-follower differential amplifiers
- Operational amplifier drivers

MAXIMUM RATINGS, Absolute-Maximum Values:

POWER DISSIPATION, P:

Any one transistor	300 max. mW
Total for array	600 max. mW

TEMPERATURE RANGE:

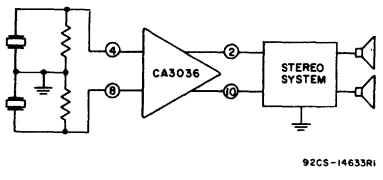
Operating	–55 to +125 °C
Storage	–65 to +150 °C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C

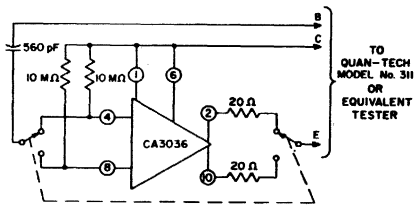
The following ratings apply for each transistor in the array:

Collector-to-Emitter Voltage, V_{CEO}	15 max. V
Collector-to-Base Voltage, V_{CBO}	30 max. V
Emitter-to-Base Voltage, V_{EBO}	5 max. V
Collector Current, I_C	50 max. mA



92CS-14633RI

Fig.2 - Block Diagram of Stereo System using CA3036 as Phono Preamplifier.



92CS-14628

Fig.3 - Noise Voltage Test Circuit for CA3036.

CA3039

Diode Array

Six Matched Diodes on a Common Substrate

ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES

For Applications in Communications and Switching Systems

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

APPLICATIONS

- Balanced modulators or demodulators
- Ring modulators
- High speed diode gates
- Analog switches

FEATURES

- Excellent reverse recovery time – 1 ns typ.
- Matched monolithic construction – V_F matched within 5 mV
- Low diode capacitance – C_D = 0.65 pF typical at V_R = –2 V
- The CA3039 is available in a sealed-junction Beam-Lead version (CA3039L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package

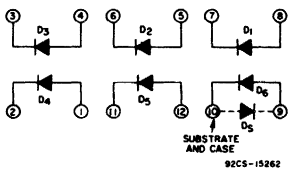


Fig. 1 - Schematic Diagram for CA3039

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:	
Any one diode unit	100 mW
Total for device	600 mW
For T_A > 55°C	derate linearly 5.7 mW/°C
TEMPERATURE RANGE:	
Operating	–55 to +125°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C
PEAK INVERSE VOLTAGE, PIV for: D_1–D_5	5 V
D_6	0.5 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE, V_{DI} for D_1–D_5 (term. 1,4,5,8 or 12 to term. 10)	+20, –1 V
DC FORWARD CURRENT, I_F	25 mA
PEAK RECURRENT FORWARD CURRENT, I_f	100 mA
PEAK FORWARD SURGE CURRENT, I_f(surge)	100 mA

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = –4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	–1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_5)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = –2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

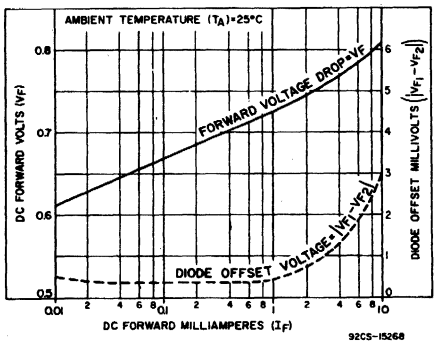


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

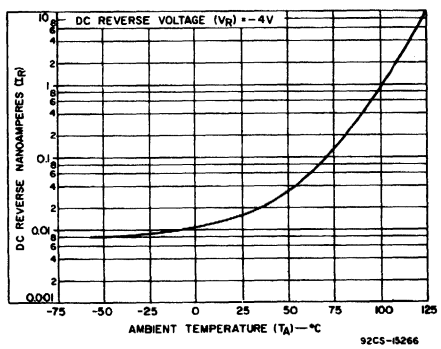


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

CA3039

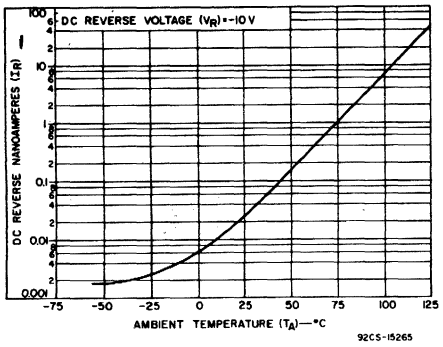


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

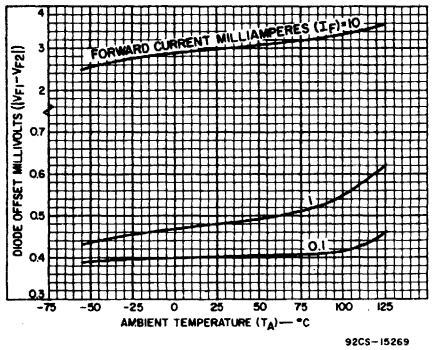


Fig. 5 - Diode offset voltage (any diode) vs temperature

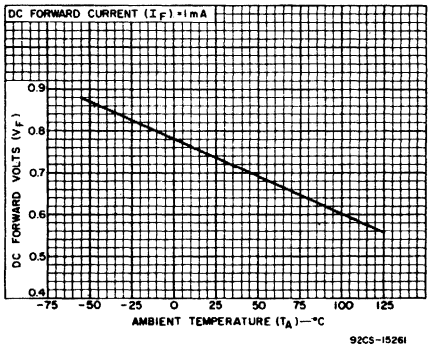


Fig. 6 - DC forward voltage drop (any diode) vs temperature

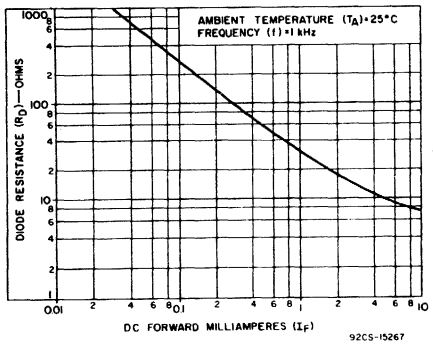


Fig. 7 - Diode resistance (any diode) vs DC forward current

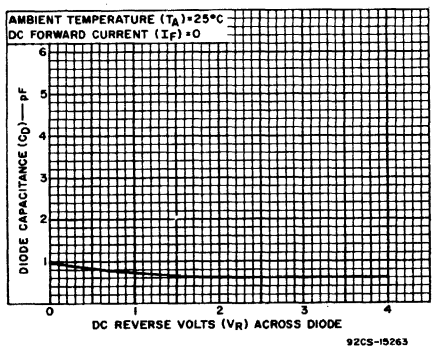


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

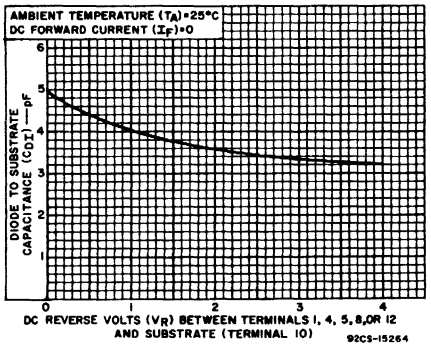


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

CA3040

VIDEO and WIDE-BAND AMPLIFIER

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and low output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of -55 to +125°C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ±2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ±0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

FEATURES

- High Differential Push-Pull Voltage Gain ..... 37 dB typ.
  Single-Ended Voltage Gain..... 31 dB typ.
- Wide (3dB) Bandwidth..... 55 MHz typ.
- Balanced Input and Output
- High Input Resistance..... 150 kΩ typ.
- Low Output Resistance..... 125 Ω typ.
- Bias Options for Temperature Compensation:
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain
- **Supplied in the hermetic 12-lead TO-5 style package**

APPLICATIONS

- Video Amplifier
- Modulator
- Mixer
- Schmitt Trigger
- IF Amplifier
- DC Amplifier
- Sense Amplifier

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * ..... 450 mW
Derating factor for T_A > 85°C..... 5 mW/°C
TEMPERATURE RANGE:
Operating ..... -55°C to +125°C
Storage..... -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

* Limitation imposed by the thermal resistance of package.

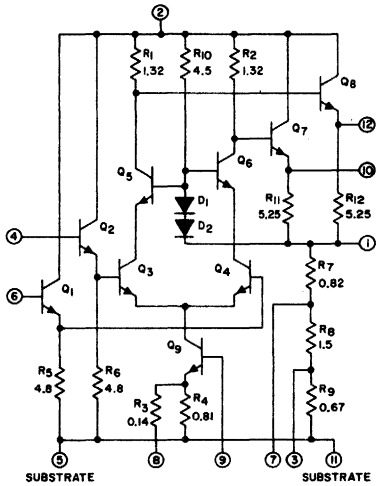


Fig.1 - Schematic Diagram for CA3040

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

STATIC CHARACTERISTICS TEST CIRCUITS

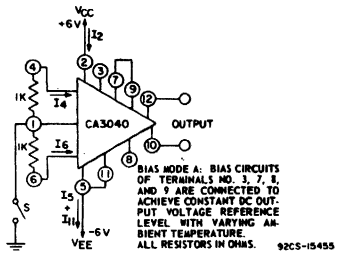


Fig.2(a) - Bias Mode A

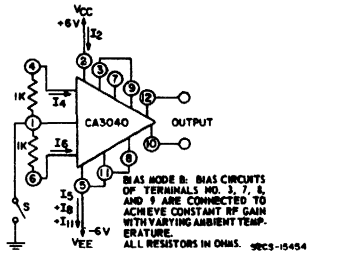


Fig.2(b) - Bias Mode B

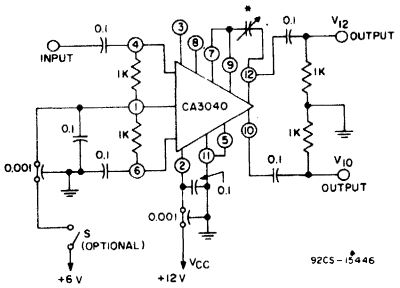
CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V						
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed				
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V						
Differential Voltage Gain							
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz, R_S = 50 Ω	34	37	-	dB
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz, R_S = 50 Ω	28	31	-	dB
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz, R_S = 50 Ω	-	0.5	-	VRMS
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz, R_S = 400 Ω	-	7.5	9	dB
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF
Output Resistance	R_O	3(a)		-	125	-	Ω
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: $-55°C \leq T_A \leq +125°C$							
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C
		3(b)	Bias Mode B	-	6.4	-	mV/°C
Power Supply Current Drain	$\Delta I_2/°C$	3(a)	Bias Mode A	-	5	-	μA/°C
Differential Voltage Gain	$A_{DIFF}/°C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C
		3(b)	Bias Mode B	-	0	-	

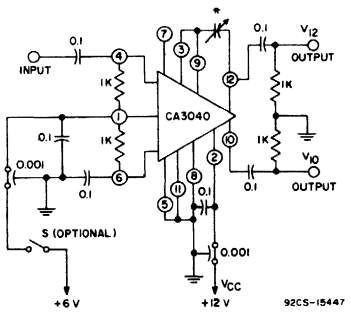
Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MHz exceeds 5kΩ

DYNAMIC CHARACTERISTICS TEST CIRCUITS



* VARIABLE CAPACITANCE (0.5-1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG. 2(a)

Fig.3(a) - Bias Mode A



* SEE FIG. 3(a)
BIAS MODE B IS AS DEFINED IN FIG. 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

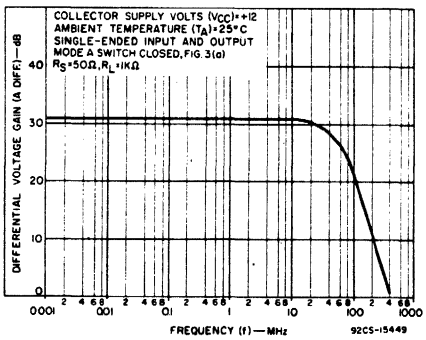


Fig.4 - Differential Voltage Gain vs Frequency

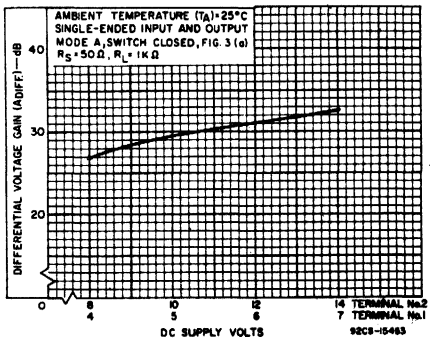


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

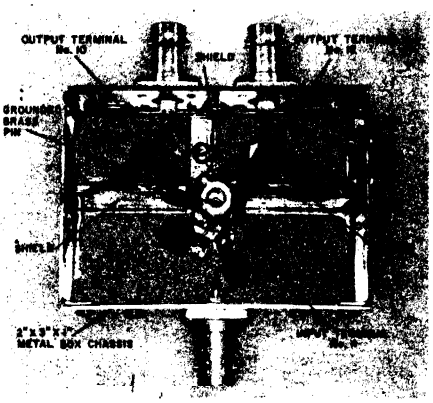


Fig.6 - Test Circuit Layout

CA3040

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

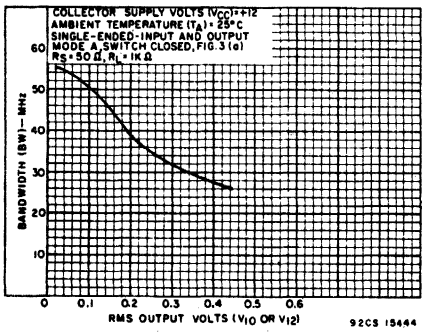


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

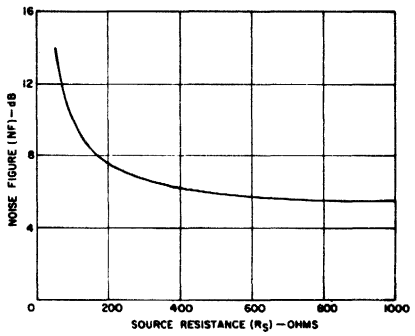


Fig.8 - Noise Figure (NF) vs Source Impedance

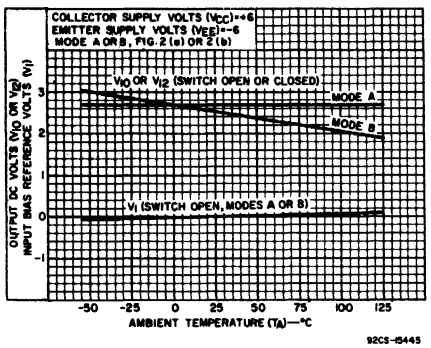


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

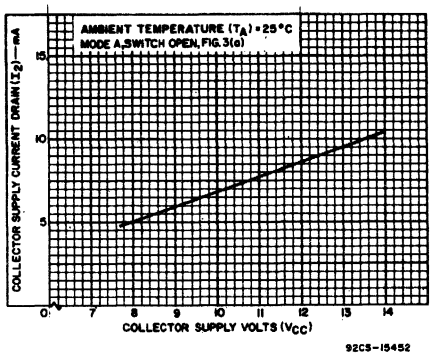


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

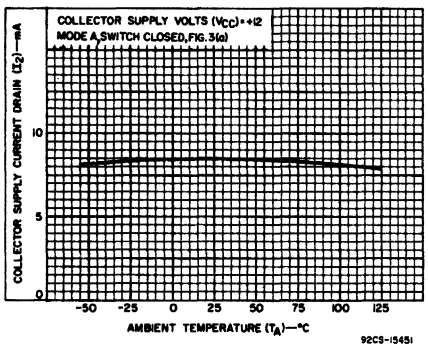


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

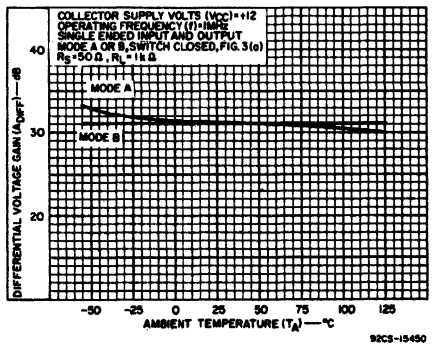


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

CA3041

WIDE-BAND AMPLIFIER, FM DETECTOR AF-PREAMPLIFIER/DRIVER

For Sound Sections of TV Receivers Using Tube-Type AF Output Amplifiers

FEATURES

- high-sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- large audio drive voltage capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internal Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to > 20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3041 provides, in a single monolithic silicon chip, a major subsystem for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig. 1) and the TV Receiver Block Diagrams (Fig. 12), the CA3041 contains a multistage wide-band if-amplifier/limiter section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly a 6AQ5 beam power tube or other audio output tube of similar characteristics.

In FM receivers, the CA3041 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3041 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3041 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

MAXIMUM RATINGS, *Absolute Maximum Values:*

OPERATING-TEMPERATURE RANGE ..... –40° to +85°C
STORAGE-TEMPERATURE RANGE ..... –65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 ..... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient up to +25°C ..... 950 mW
Temperatures above +25°C ..... Derate at 10.8 mW/°C

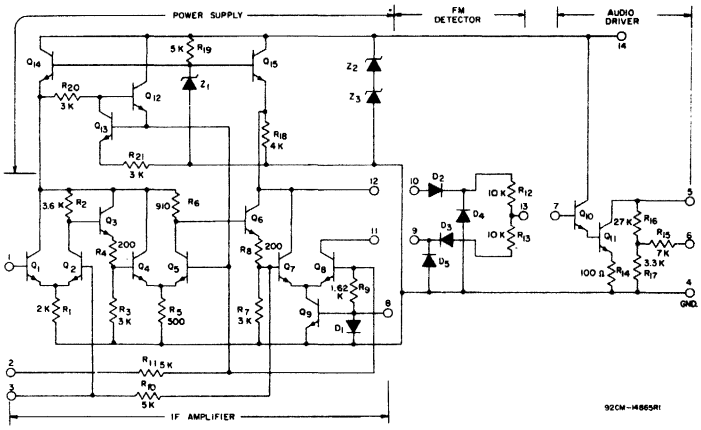


Fig. 1 - Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	CONNECTED TO +140 V THROUGH 47 kΩ RESISTOR*	CONNECTED TO TERMINAL 7 THROUGH 100 kΩ RESISTOR*	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	0V	+10 V	-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2.5 V	+5 V	-3 to +3													
12	+2.5 V	+5 V	-3 to +3													
13	+2.5 V	+5 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.

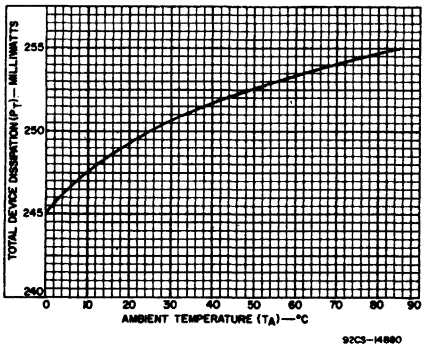


Fig. 2 - Typical dissipation characteristic for CA3041.

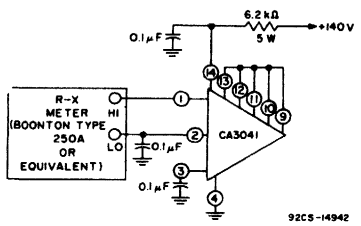


Fig. 3 - Test setup for measurement of input-impedance components.

CA3041

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3041 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	11	T_A = 0°C	220	245	270	mW	2
			T_A = +25°C	225	250	275	mW	
			T_A = +85°C	230	255	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	-		10.5	11.2	12.3	V	-
Quiescent Operating Current (into Terminal 11)	I_{11}	11		0.25	0.63	1	mA	-
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	11	V_{CC} = +9 V applied directly to Terminal 14	7	11	16	mA	-
Input-Impedance Components: Parallel Input Resistance	R_i	3	f = 4.5 MHz	-	11	-	kΩ	-
Parallel Input Capacitance	C_i	3		-	5	-	pF	-
Output-Impedance Components: Parallel Output Resistance	R_o	-		-	100	-	kΩ	-
Parallel Output Capacitance	C_o	-		-	4	-	pF	-
Input Limiting Voltage (Knee)	$V_{i(lim)}$	7		-	150	200	μV (rms)	4
Amplitude-Modulation Rejection	AMR	10		45	58	-	dB	9
IF-Amplifier Voltage Gain	$A_{(IF)}$	5		-	67	-	dB	4
Recovered AF Voltage: 1. At FM-Detector Output	$V_{o(af)}$	-	R_L = 50 kΩ, Δf = ±25 kHz THD = 0.7% (typ.)	-	250	-	mV (rms)	-
2. At AF-Driver Output in Test Setup		-	THD < 5%	8	9	-	V (rms)	-
Total Harmonic Distortion	THD	7	$V_{o(af)}$ = 8 V(rms)	-	1.5	5	%	-
Discriminator Output Resistance	$R_{o(dis)}$	-	f = 1 kHz	-	10	-	kΩ	-
AF-Amplifier Input Resistance	$R_{i(af)}$	-		-	100	-	kΩ	-
AF-Amplifier Output Resistance	$R_{o(af)}$	-		-	30	-	kΩ	-
AF-Driver Voltage Gain	A_{af}	6		-	41	-	dB	8

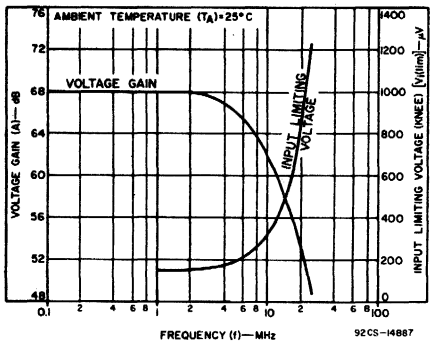
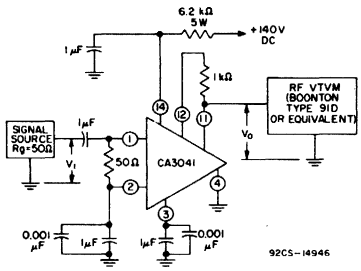


Fig.4 - Typical IF-amplifier voltage gain and input-limiting voltage (knee) characteristics.



PROCEDURE:

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.5 - Test setup for measurement of IF-amplifier voltage gain.

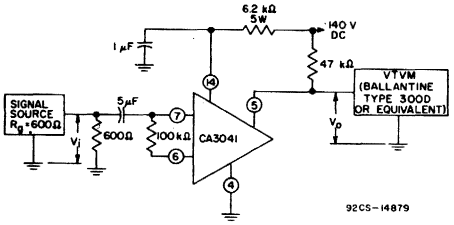
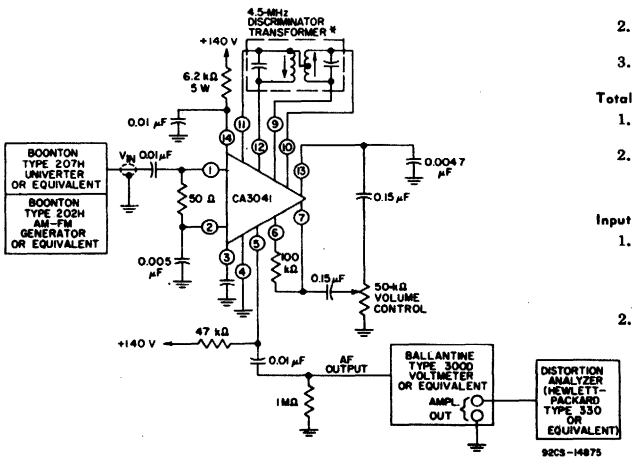


Fig.6 - Test setup for measurement of AF-amplifier voltage gain.



* TRW Electronics, Des Plaines, Illinois. Part No. E023874, or equivalent.

Fig.7 - Test setup for measurement of input limiting voltage (Knee), recovered AF voltage, and total harmonic distortion.

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output.
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 300 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (300 mV - 3 dB = 210 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

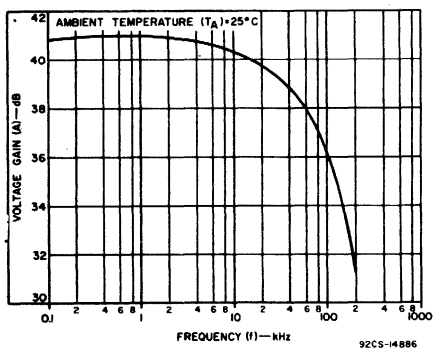


Fig.8 - Typical AF-driver voltage-gain characteristic

CA3041

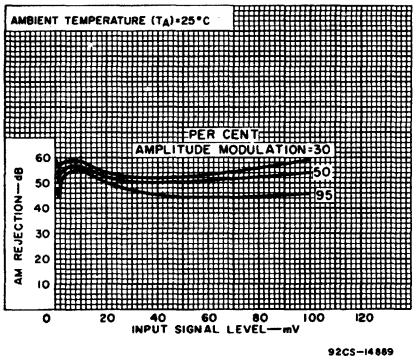
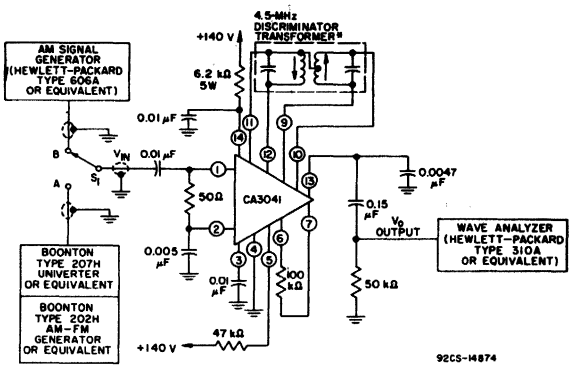


Fig.9 - Typical AM rejection characteristics for CA3041.

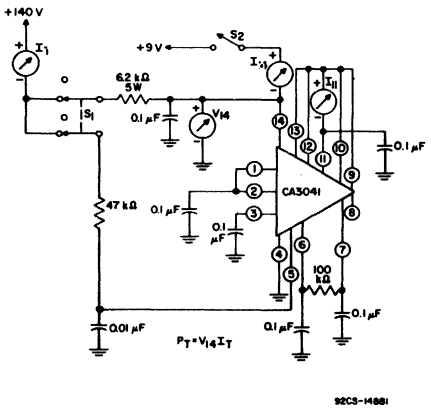


PROCEDURES:

1. Set FM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $V_{o(FM)}/V_{o(AM)}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.10 - Test setup for measurement of AM rejection.



PROCEDURES:

Total Device Dissipation:

1. Close S_1, open S_2.
2. Measure and record V_{14} and I_T.
3. Determine Total Device Dissipation from $P_T = V_{14}I_T$.

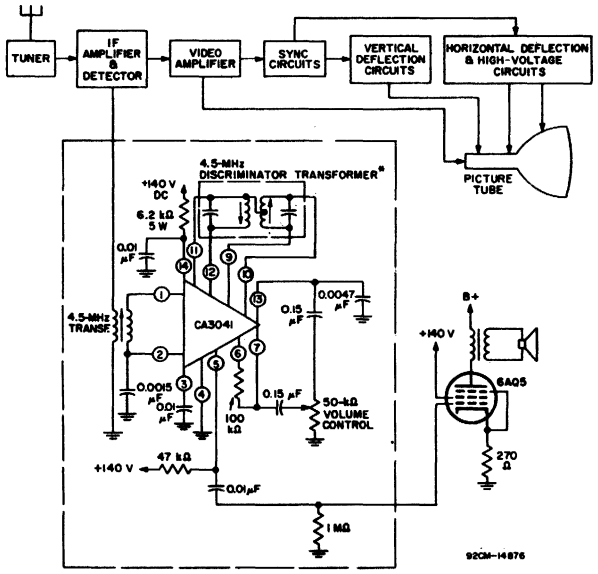
Quiescent Operating Current into Terminal 11:

1. Close S_1, open S_2.
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Open S_1, close S_2.
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.11 - Test setup for total dissipation, quiescent operating current into terminal No.11, and 9-volt current drain.



* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.12 - Block diagram of typical TV receiver using CA3041.

CA3042

WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

For Sound Sections of TV Receivers Using Transistor-Type AF Output Amplifiers

FEATURES

- high sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- 6-mA audio drive capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internally Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to >20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3042 provides, in a single monolithic silicon chip, a major sub-system for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Figs.2A and 2B) the CA3042 contains a multistage wide-band if-amplifier section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly an n-p-n audio output transistor or a high-gain audio output pentode tube.

In FM receivers, the CA3042 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3042 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3042 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

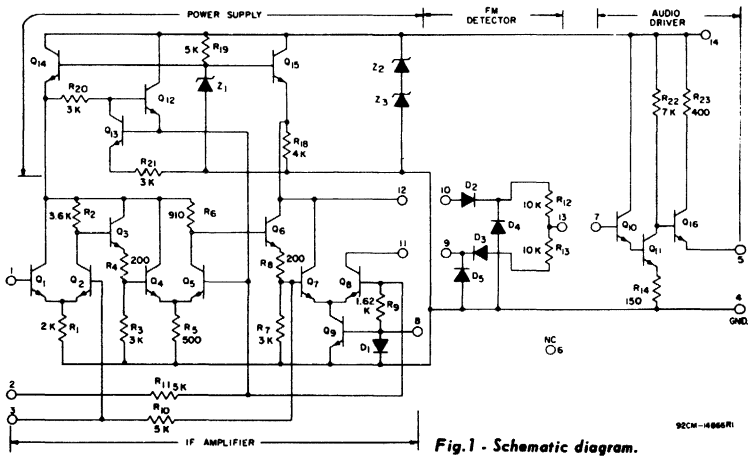


Fig.1 - Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING-TEMPERATURE RANGE	−40° to +85°C
STORAGE-TEMPERATURE RANGE	−65° to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:	
Between Terminals 1 and 3	±3 V
MAXIMUM DEVICE DISSIPATION:	
At Ambient up to +25°C	950 mW
Temperatures above +25°C	Derate at 10.8 mW/°C

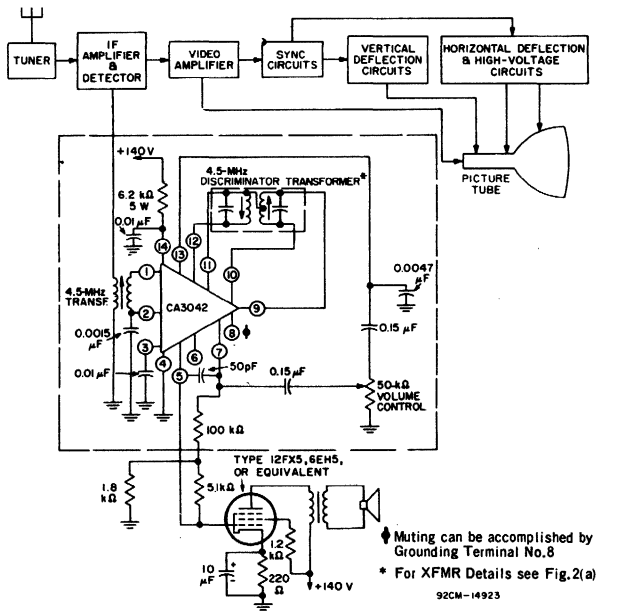


Fig.2(b) - Block diagram of typical TV receiver utilizing the CA3042 and a 12FX5, 6EH5, or equivalent.

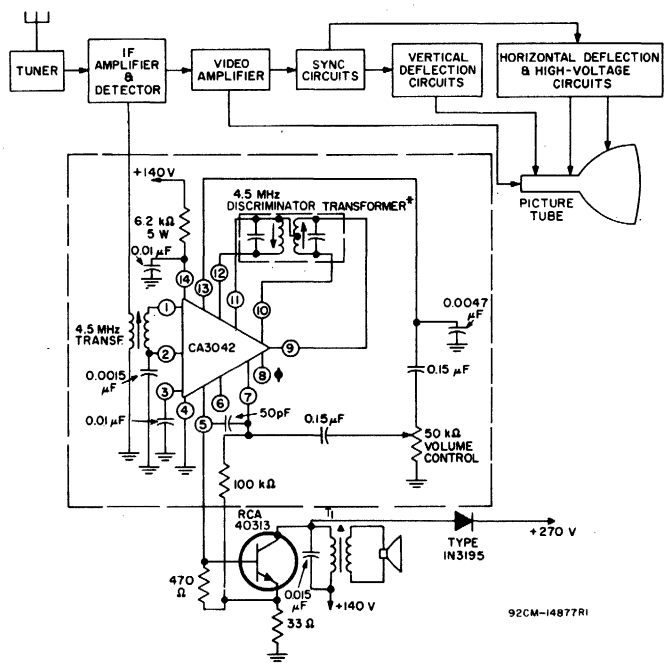
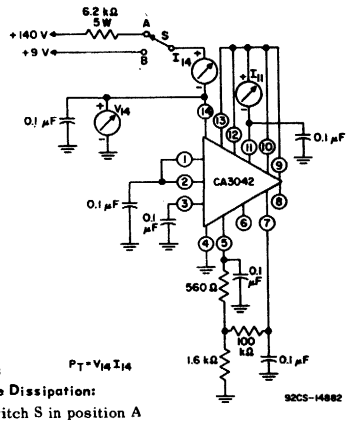


Fig. 2(a) - Block diagram of typical TV receiver utilizing transistor RCA-40313.



PROCEDURES: $P_T = V_{14} I_{14}$

Total Device Dissipation:

1. Set switch S in position A
2. Measure and record V_{14} and I_{14}.
3. Determine Total Device Dissipation from $P_T = V_{14} I_{14}$

Quiescent Operating Current into Terminal 11:

1. Turn switch S to position B
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Set switch S in position B
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for measurement of total device dissipation, quiescent current into terminal No.11, and 9-volt current drain.

CA3042

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS
			1
1	-3 V	+3 V	–
2	-3 V	+3 V	-3 to +3
3	-3 V	+3 V	-3 to +3
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3
5	20 mA		-3 to +3
6	NO CONNECTION		-3 to +3
7	10 mA		-3 to +3
8	10 mA		-3 to +3
9	10 mA		-3 to +3
10	10 mA		-3 to +3
11	+2 V	+10 V	-3 to +3
12	+2.5 V	+10 V	-3 to +3
13	0 V	+10 V	-3 to +3
14	50 mA		-3 to +3

2	3	4	5	6	7	8	9	10	11	12	13	14
AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	AF-DRIVER OUTPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	NO CONNECTION	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	MUTING TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL EXCEPT THAT TERMINAL MAY BE GROUNDED TO OBTAIN MUTING ACTION)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.

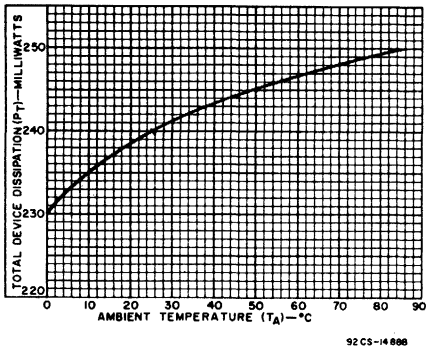


Fig.4 - Typical dissipation characteristic.

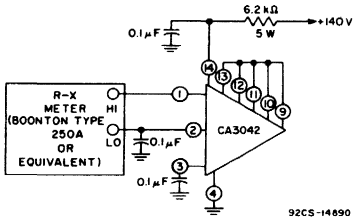
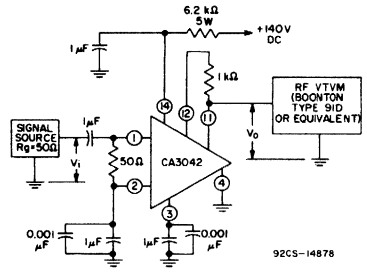


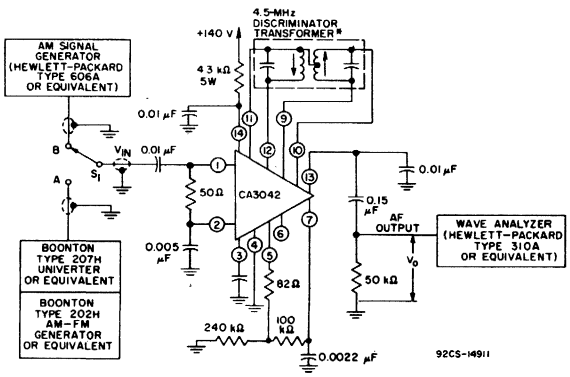
Fig.5 - Test setup for measurement of input-impedance components.



PROCEDURE Voltage Gain:

1. Set input frequency at desired value, v_i = 100 μV rms.
2. Record v_o.
3. Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4. Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.6 - Test setup for measurement of IF amplifier voltage gain.



PROCEDURES:

1. Set FM Signal Generator as follows:
   Output Frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ±25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $\frac{V_{o(FM)}}{V_{o(AM)}}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.7 - Test setup for measurement of AM rejection.

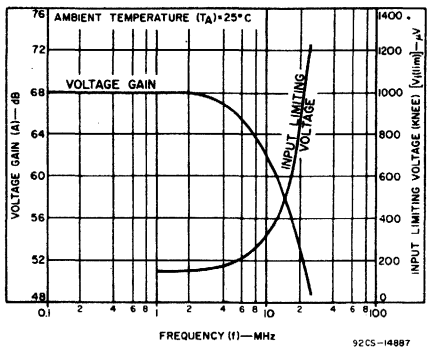


Fig.8 - Typical IF amplifier voltage gain and input limiting voltage (knee) characteristics.

CA3042

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3042 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	3	T_A = 0°C	200	230	260	mW	4
			T_A = +25°C	210	240	270	mW	
			T_A = +85°C	220	250	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–		10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3		0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14	8	12	18	mA	–
Input-Impedance Components: Parallel Input Resistance	R_I	5	f = 4.5 MHz	–	11	–	kΩ	–
Parallel Input Capacitance	C_I	5	f = 4.5 MHz	–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_O	–	f = 4.5 MHz	–	100	–	kΩ	–
Parallel Output Capacitance	C_O	–	f = 4.5 MHz	–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	11	f = 4.5 MHz	–	150	200	μV (rms)	8
Amplitude-Modulation Rejection	AMR	7	f = 4.5 MHz	45	58	–	dB	
IF-Amplifier Voltage Gain	A(IF)	6	f = 4.5 MHz	–	67	–	dB	8
Recovered AF Voltage: 1. At FM-Detector Output	$V_{o(af)}$	11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 50 kΩ THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 322 Ω THD < 5%	500	800	–	mV (rms)	–
3. At AF-Driver Output in TV-Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, R_L = 150 kΩ THD = 1.5% (typ.)	–	3	–	V (rms)	–
Total Harmonic Distortion: 1. In Test Setup	THD	11	f = 4.5 MHz, Δf = ±25 kHz, $V_{o(af)}$ = 500 mV (rms)	–	1.5	5	%	–
2. In TV Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, $V_{o(af)}$ = 1.3 V (rms)	–	1	–	%	–
FM-Detector Output Resistance	$R_{o(det)}$	–	f = 1 kHz	–	10	–	kΩ	–
AF-Driver Input Resistance	$R_{I(af)}$	–	f = 1 kHz	–	100	–	kΩ	–
AF-Driver Output Resistance	$R_{O(af)}$	–	f = 1 kHz	–	250	–	Ω	–
AF-Driver Voltage Gain	A_{af}	9	f = 1 kHz, R_S = 50 Ω, C_1 = 0	–	30	–	dB	10

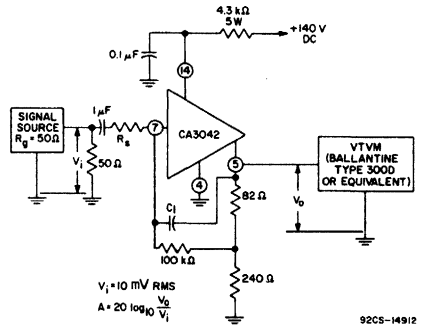


Fig.9 - Test setup for measurement of AF amplifier voltage gain.

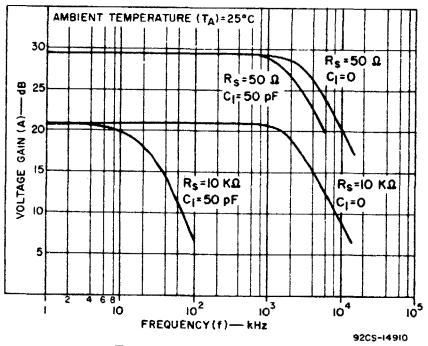
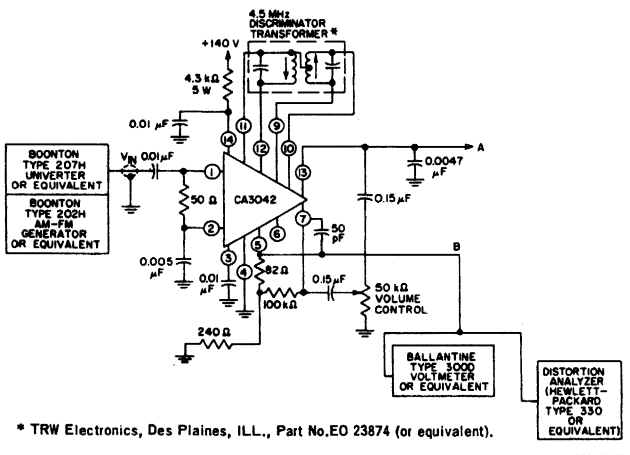


Fig.10 - Typical AF amplifier voltage gain characteristics.



* TRW Electronics, Des Plaines, ILL., Part No.EO 23874 (or equivalent).

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   - Output frequency = 4.5 MHz
   - Modulating frequency = 1 kHz
   - Deviation = ± 25 kHz
   - Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 500 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (500mV - 3 dB = 350 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

Fig.11 - Test setup for measurement of input limiting voltage (knee), recovered AF voltage, and total harmonic distortion.

CA3043

Special-Function Sub-System

HIGH-GAIN IF AMPLIFIER, LIMITER, FM DETECTOR, AND AF PREAMPLIFIER/DRIVER

For FM IF Amplifier Applications in Communications Receivers and High-Fidelity FM Receivers up to 20 MHz

FEATURES

- high sensitivity - - input limiting voltage (knee) 50 μV typ. at 10.7 MHz
- excellent AM rejection - - 58 dB typ. at 10.7 MHz
- inherent high stability - - internally shielded
- internal Zener-diode regulated voltage supply
- low harmonic radiation
- wide frequency capability - - <100 kHz to >20 MHz
- low harmonic distortion
- hermetic 12-lead TO-5 style package

RCA Integrated Circuit Type CA3043 provides in a single monolithic silicon chip, a major sub-system for the IF sections of Communications and high-fidelity FM receivers. As shown in the Schematic Diagram (Fig.2) and the FM Receiver Block Diagram (Fig.1), the CA3043 contains a multistage if-amplifier/limiter section, an FM-detector stage, a Zener-diode regulated power-supply section, and an af-amplifier section. In FM receivers, the CA3043 can be used to provide if amplification and limiting, FM detection, and af preamplification. The CA3043 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The four stage emitter-follower-coupled if amplifier section provides 80-dB voltage gain at 10.7 MHz, and features an output stage with exceptionally good limiting characteristics because of its transistor constant-current sink.

The FM detector section is distinguished by circuitry which provides forward bias to the detector diodes, D2 and D3, and also provides a reference voltage for AFC.

The audio amplifier provides a low-impedance drive for subsequent audio amplifiers.

The power supply section provides zener-regulated, decoupled voltages for the IF amplifier, detector, and audio amplifier sections.

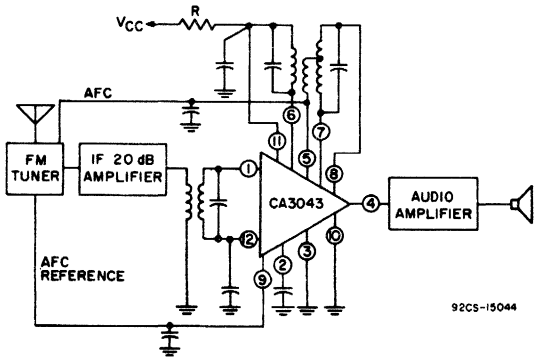


Fig.1 - Typical application of the CA3043 as a high-gain limiter, amplifier-detector in an FM receiver.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C

DISSIPATION:
At T_A = 25°C to T_A = 85°C . . . . . 450 mW
Above T_A = 85°C . . . . . Derate linearly 5 mW/°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 min) from case for 10 seconds max . . . . . + 265°C

TEMPERATURE RANGE:
Operating . . . . . -55°C to + 125°C
Storage . . . . . -65°C to + 150°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUIT AND PROCEDURE	LIMITS TYPE CA3043			UNITS
			Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Current Drain at 6V into Pin No.11	I_{11}	V_{CC} = +6V	3	10	16	20	mA
Regulator Voltage Pin No.11	V_{11}	V_{CC} = +30V, R_S = 750 Ω	3	6.9	7.4	8	V
Total Device Dissipation	P_T		3	200	225	260	mW
Quiescent Operating Current into Pin No.6	I_6		3	-	0.65	-	mA
DYNAMIC CHARACTERISTICS at V_{CC} = +30V, R_S = 750 Ω, f = 10.7 MHz							
Voltage Gain	A_V		4	72	80	-	dB
Input Limiting Voltage (knee)	v_i(lim)	v_o(af) at -3 dB point	6	-	50	-	μV (RMS)
Limiting Current from Pin No.6	I_6(lim)		4	-	0.42	-	mA (RMS)
Recovered AF Voltage	v_o(af)	v_i = 1 mV (RMS) f(modulating) = 1 kHz Deviation = ± 75 kHz	6	75	110	150	mV (RMS)
Amplitude-Modulation Rejection	AMR	v_i = 10 mV f(modulating) = 1 kHz % modulation = 50%	8	-	58	-	dB
Total Harmonic Distortion	THD	v_i = 1 mV (RMS)	6	-	0.3	-	%
Input Impedance Components:							
Parallel Input Resistance	R_I		-	-	7	-	kΩ
Parallel Input Capacitance	C_I		-	-	5	-	pF

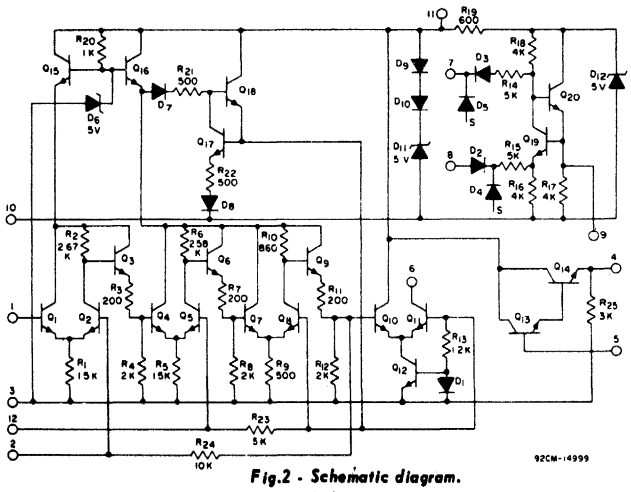
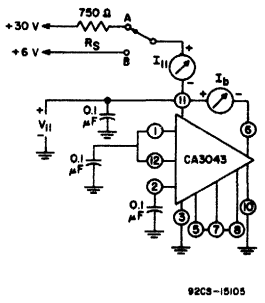


Fig.2 - Schematic diagram.

Notes:
S = Substrate
Terminal No.3 wire-connected to the case.
Terminal No.10 connected to the case through the substrate
Terminals No.3 and 10 which are connected to the substrate should be connected to the most negative point in the circuit.
Diodes D_4 and D_5, act as capacitors and are used to balance the detector substrate capacitances.



Switch in Position A for:
Regulator-Voltage, Quiescent-Operating-Current, and Device Dissipation Test
Switch in Position B for Current into Pin No.11

Fig.3 - Regulator voltage, device dissipation, quiescent operating current, and current at 6 volts into Pin No. 11.

CA3043

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range between horizontal terminal 5 and vertical terminal 3 is +6 to 0 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		+4 -4	0 -5	*	*	*	*	*	*	0 -5	*	Note(1)
2			0 -3	*	*	*	*	*	*	0 -3	*	*
3				+6 0	+6 0	+15 +2	+6 0	+6 0	+6 0	0	Note(2)	+3 0
4					+2 -4	*	*	*	*	0 -6	*	*
5						*	*	*	*	0 -6	+6 0	*
6							*	*	*	-2 -15	*	*
7								Note(1)	*	0 -6	*	*
8									*	0 -6	*	*
9										0 -6	*	*
10											Note(2) 0	+3 0
11												*
12												

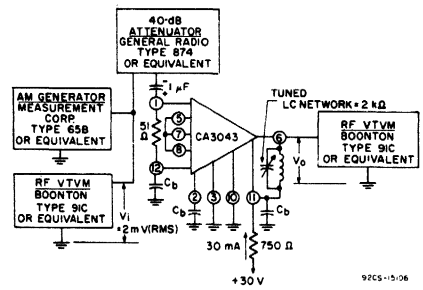
MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	-
2	-	-
3	0.1	40
4	-	20
5	-	-
6	-	-
7	-	-
8	-	-
9	-	20
10	0.1	40
11	40	0.1
12	-	-

Note 1: These terminals should be connected through a dc resistance to any terminal which does not exceed 100 ohms.

Note 2: Pin 11 may be connected to any positive voltage source through a suitable resistor provided its current rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



Voltage Gain = $20 \log_{10} 100 \frac{V_o}{V_i}$

C_b - Bypass Capacitor, 0.1 μF electrolytic in parallel with 0.01 μF

$I_{6(lim)} = \frac{V_o}{2K\Omega}$, V_i = 100 mV(RMS)

* Output circuit should be completely shielded from the input circuit at the socket.

Fig.4 - Voltage gain test circuit.

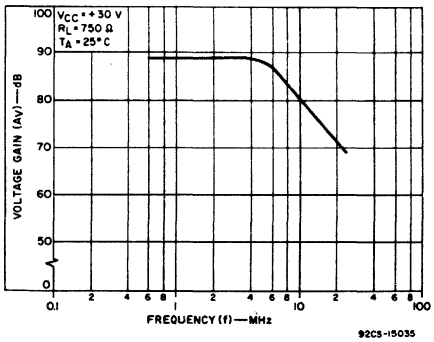
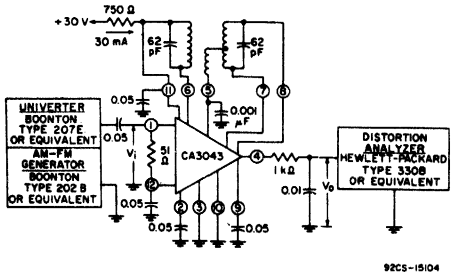


Fig.5 - Voltage gain vs frequency.



PROCEDURE:

1. Recovered Audio Voltage $v_{o(af)}$ —
   Set input frequency to 10.7 MHz,
   v_i = 1 mV(RMS), modulating frequency = 1 kHz
   Deviation = ±75 kHz
   Record v_o as measured on the Distortion Analyzer meter scale.
   This is the recovered Audio Voltage $v_{o(af)}$
2. 3 dB Limiting Sensitivity $v_{i(lim)}$ —
   Reduce v_i until $v_{o(af)}$ drops 3 dB.
   Record this value of v_i as $v_{i(lim)}$
3. Total Harmonic Distortion THD —
   Reset v_i to 1 mV(RMS) and operate Distortion Analyzer per manufacturer's instructions to measure THD.

* See Fig.9 for details on Discriminator Transformer.

Fig.6 - Input limiting voltage (knee), recovered AF voltage, and total harmonic distortion test circuit.

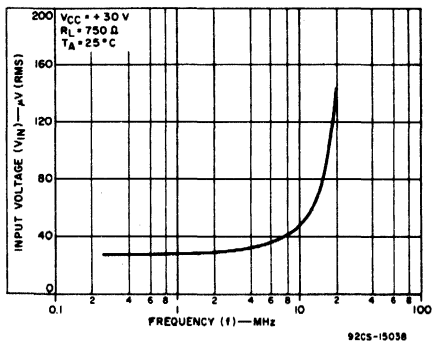
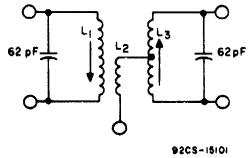
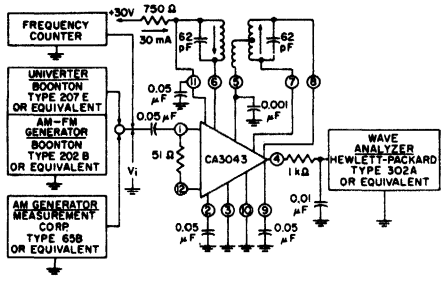


Fig.7 - Input limiting voltage (knee) at -3 dB point vs frequency.



Coil Form, Outside Diameter = 7/32"
Can = 1/2" square X 1-1/8" long
Slugs - Radio Industries Type MP34/MP100 Material
L_1 & L_3 = 20 Turns 5-44 litz wire universal wound
L_2 = 10 Turns 5-44 litz wire wound bifilar with L_1
L_1 & L_3 coupling adjusted to 520 kHz peak to peak separation on S curve when operated in circuit shown in Fig.6.

Fig.9 - 10.7-MHz discriminator transformer for CA3043.



PROCEDURE:

A. Connect FM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz
   Deviation = ±75 kHz.
   Tune Wave Analyzer to peak reading at 1 kHz and record recovered Audio Voltage $v_{o(af)FM}$.

B. Disconnect FM Generator and Connect AM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz, percent modulation = 50%.
   Tune Wave Analyzer to peak reading and record recovered audio voltage $v_{o(af)AM}$
   Amplitude Modulation Rejection Ratio = $20 \log_{10} \frac{V_{o(af)FM}}{V_{o(af)AM}}$

Fig.8 - Amplitude modulation rejection test circuit.

CA3044, CA3044V1

Special-Function Sub-System

WIDE-BAND AMPLIFIER/PHASE DETECTOR WITH ZENER DIODE VOLTAGE REGULATOR

For AFC (Automatic Frequency Control) Applications

The RCA CA3044 and CA3044V1 represent a second generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications.

The CA3044V1 is electrically identical to the CA3044 but is supplied with formed leads for easier PC board design and construction.

FEATURES

- Primarily intended for AFC (automatic frequency control) Applications
- Internal Zener Diode Voltage Regulator
- Differential Input Amplifier/Limiter
- Full-Wave Diode Bridge Detector
- Differential Output Voltage Amplifier
- Available in Two Electrically Identical Versions of the 10-lead TO-5 style package,

  CA3044 With Straight Leads;

  CA3044V1 With Formed Leads
- Wide Operating Temperature Range; -55 to +125°C

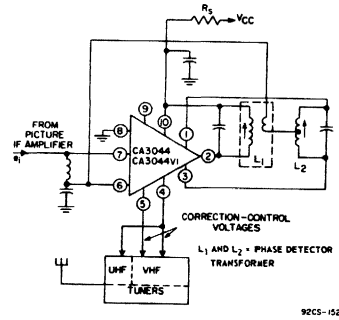


Fig.1 - Block diagram of Typical Automatic Fine Tuning (AFT) Application using CA3044 or CA3044V1 in Color-TV Receiver.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:
- At T_A = 25°C ..... 830 mW
- Above T_A = 25°C ..... Derate linearly 5.6 mW/°C

TEMPERATURE RANGE:
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... + 265C

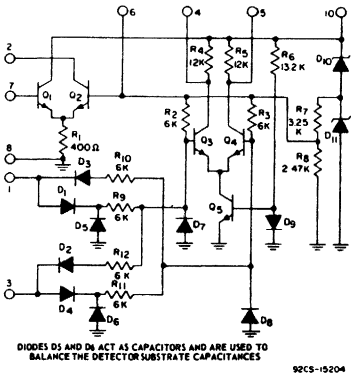


Fig.2 - Schematic diagram CA3044, CA3044V1

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 6 is +20 to 0 volts.

TERMINAL No.	9	10	1	2	3	4	5	6	7	8
9	NO INTERNAL CONNECTION									-
10			+20 0	+20 -10	+20 0	+20 0	+20 0	+20 0	+20 0	▲
1				*	+12 -12	*	*	+6 -6	*	+6 0
2					*	*	*	+20 0	*	+20 0
3						*	*	+6 -6	*	+6 0
4							*	*	*	+12 0
5								*	*	+12 0
6									+5 -5	+5 0
7										+8 -5
8										REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	-	-
10	50	50
1	5	5
2	20	20
3	5	5
4	5	5
5	5	5
6	5	5
7	5	5
8	50	50

▲ Terminal No. 10 may be connected to any positive voltage source through a suitable dropping resistor—provided the dissipation rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

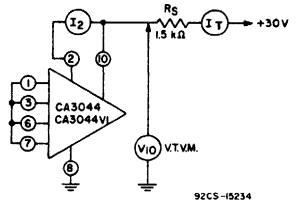


Fig.3 - Test setup: Measurement of total device dissipation, Zener regulating voltage, quiescent operating current (terminal 2).

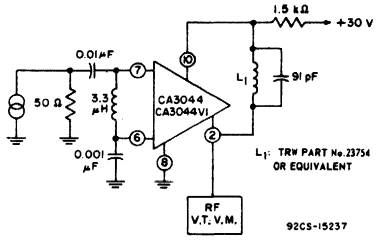


Fig.4 - Input limiting sensitivity test circuit.

CA3044, CA3044V1

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS	LIMITS CA3044 and CA3044V1 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = -55°C	90	120	150	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = 25°C	110	140	170	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = +125°C	130	160	190	mW	-
9-Volt Current Drain	I_T	3	V_{10} = 9 V	2.5	4	5.5	mA	-
Zener Regulating Voltage - DC Supply Voltage at Terminal 10	V_{10}	3	V_{CC} = 30 V, R_S = 1.5 kΩ	10.5	11.2	11.9	V	-
Quiescent Operating Current into Terminal 2	I_2	3		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4	V_4	-		5.0	6.5	8.0	V	-
Quiescent Operating Voltage at Terminal 5	V_5	-		5.0	6.5	8.0	V	-
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	-		-1.5	0	1.5	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER)								
Input Limiting Voltage (Knee)	V_i Limiting	4	f=45.75 MHz	-	75	-	mV	-
Input Admittance	y_{11}	-	f = 45.75 MHz, V_{CC} = 30 V, R_S = 1.5 kΩ	-	0.5+j1.1	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	3.8+j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	-11.7 +10.1	-	mmho	-
Output Admittance	y_{22}	-		-	0.077+j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4	V corr. (4)	5	V_{CC} = +30 V, V_{in} = 200 mV RMS, f_o = MHz as indicated	% of V_{10}		% of V_{10}		
			45.750 - 0.025	85	-	-	V	6,7
			45.750 + 0.025	-	-	33	V	
			45.750 - 0.900	75	-	-	V	7
			45.750 + 0.900	-	-	43	V	
			45.750 - 1.500	-	-	85	V	
			45.750 + 1.500	33	-	-	V	
Correction-Control Voltage at Terminal 5	V corr. (5)	5	45.750 - 0.025	-	-	33	V	6,7
			45.750 + 0.025	85	-	-	V	
			45.750 - 0.900	-	-	43	V	7
			45.750 + 0.900	75	-	-	V	
			45.750 - 1.500	33	-	-	V	
			45.750 + 1.500	-	-	85	V	

DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

The CA3044 and CA3044VI are specifically intended for use in the AFT system of color television receivers. Each device is tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 is the schematic diagram of the test circuit.

Figure 6 and 7 show the control voltages generated at terminals 4 and 5 of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 25 KHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on Terminal 10 and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is -25 KHz the control voltage at Terminal 4 is greater than the reference A voltage; the control voltage at Terminal 5 is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit board shown in Figure 8 and the parts layout shown in Figure 9 should be followed as closely as possible.

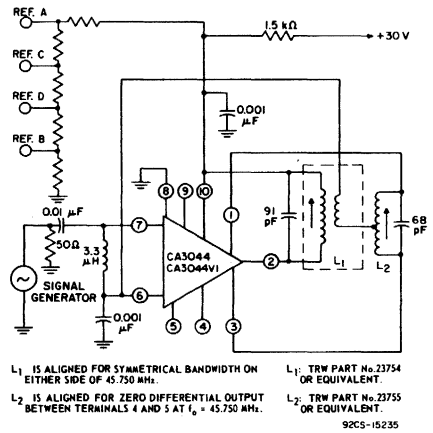


Fig.5 - Correction voltage test circuit for CA3044 and CA3044VI.

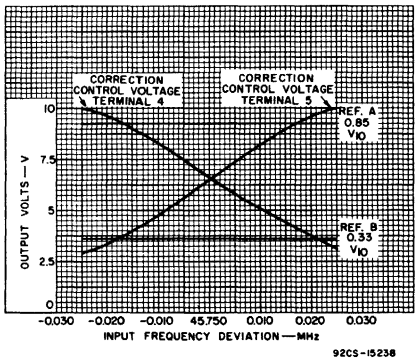


Fig.6 - Typical narrow-band dynamic control voltage characteristics.

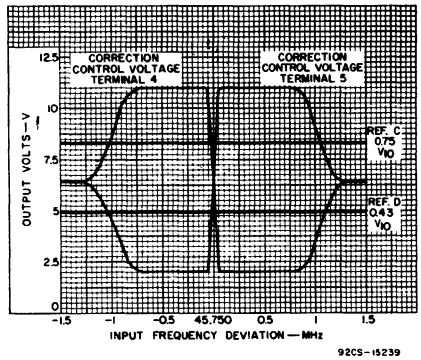


Fig.7 - Typical wide-band dynamic control voltage characteristics.

DEFINITIONS OF TERMS

Input Limiting Voltage (Knee) [v_i(lim)]
The input signal voltage which will cause the output signal to decrease 3 dB from its maximum level.

Total Device Dissipation (P_T)
The total power drain of the device with no signal applied and no external load current.

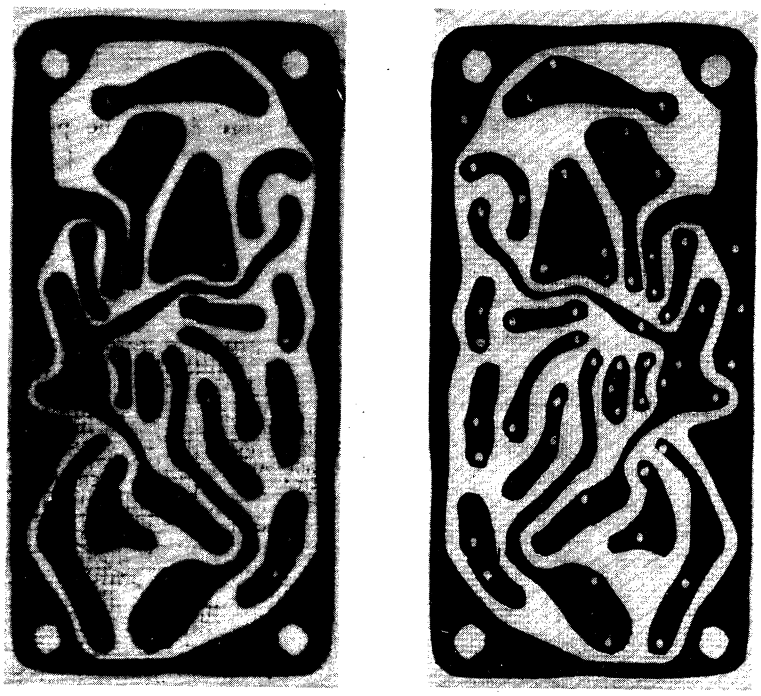
Quiescent Operating Voltage
The dc voltage at the output terminal, with respect to ground, with no signal applied.

Quiescent Operating Current
The average (dc) value of the current in either output, terminal, with no signal applied.

Output Offset Voltage
The dc voltage between output terminals with no signal applied.

Control Voltage
The dc voltage at either output terminal with respect to ground with an RF signal of specified frequency applied.

CA3044, CA3044V1



a) Top view

b) Bottom view

Fig.8 - Printed Circuit Board for Test Circuit -- Full Size

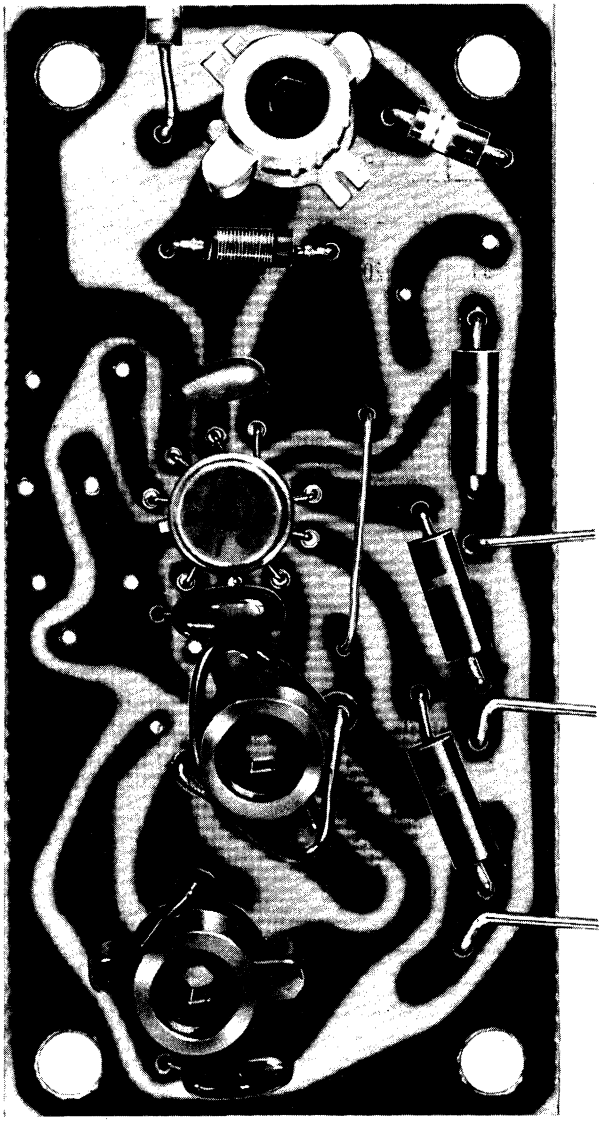


Fig.9 - Top view of wired test board.

CA3045, CA3046 Types

General-Purpose Transistor Arrays For Low-Power Applications at Frequencies from DC through the VHF Range

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

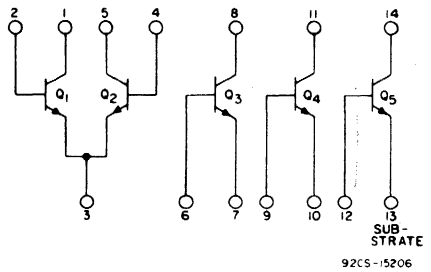


Fig.1 - Schematic diagram.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3045F, CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Temperature Range:					
Operating	−55 to +125		−55 to +125		°C
Storage	−65 to +150		−65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max:	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2: $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-	
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} 3 V, I_C 1 mA	-	1.1	-	μV/°C

FEATURES

- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045 -55 to +125°C
- The CA3045 is available in a sealed-junction Beam-Lead version (CA3045L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

APPLICATIONS

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

STATIC CHARACTERISTICS

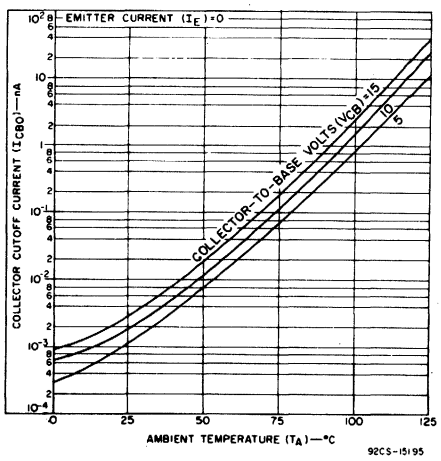


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

CA3045, CA3046 Types

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

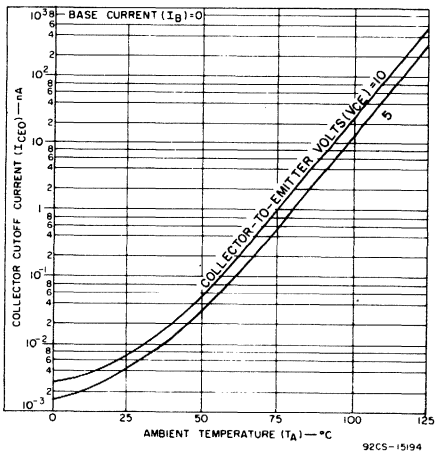


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

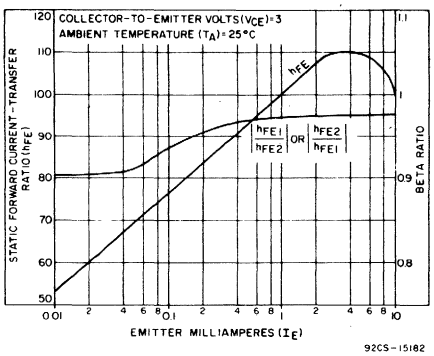


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

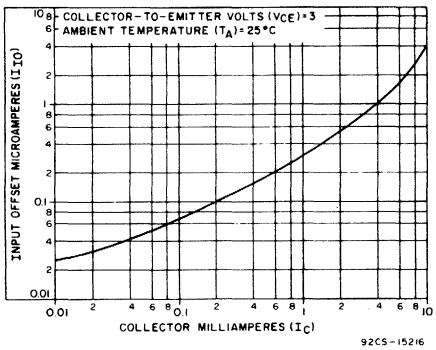


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

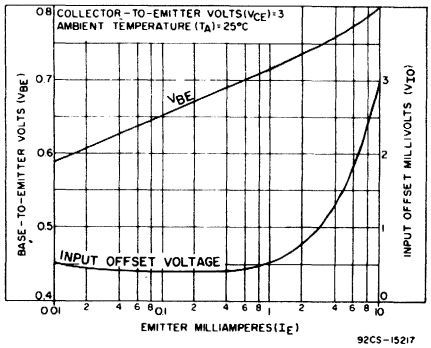


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

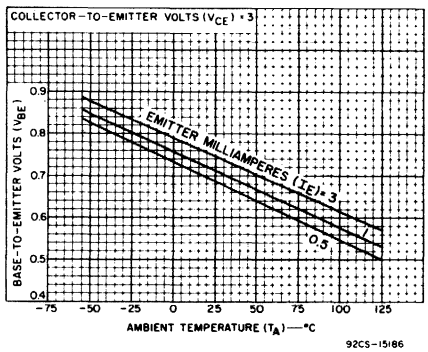


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

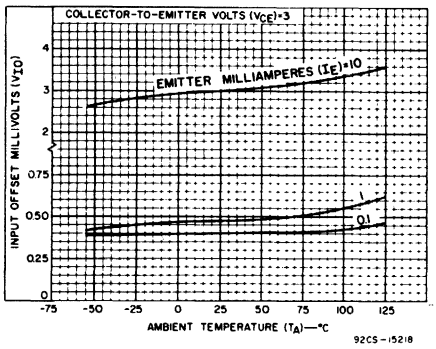


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

CA3045, CA3046 Types

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

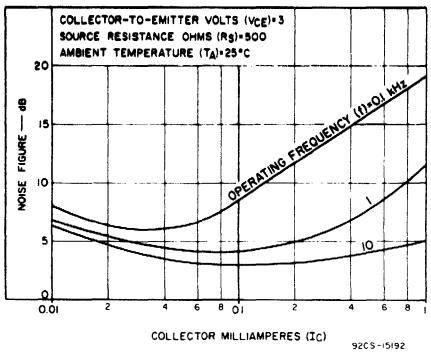


Fig.9(a) - Typical noise figure vs collector current.

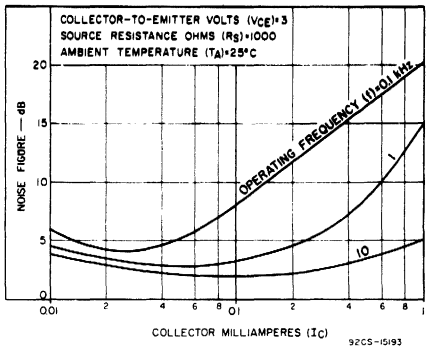


Fig.9(b) - Typical noise figure vs collector current.

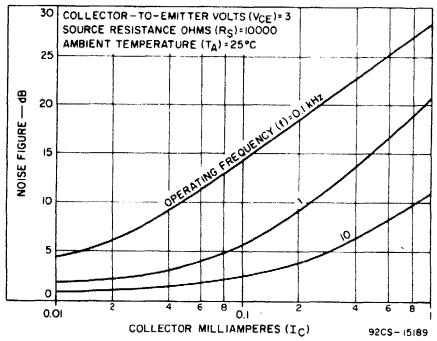


Fig.9(c) - Typical noise figure vs collector current.

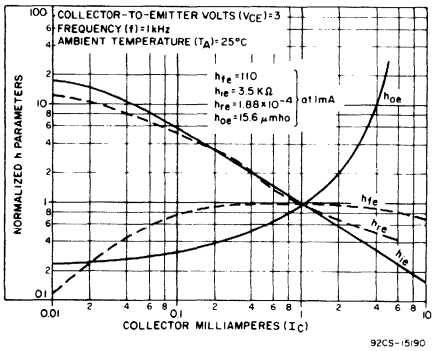


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

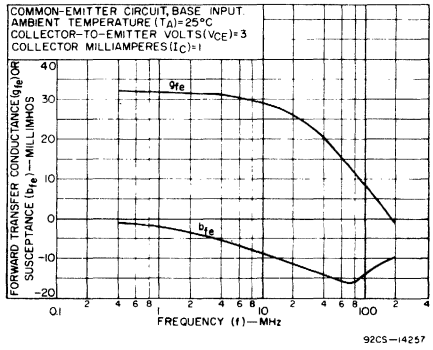


Fig.11 - Typical forward transfer admittance vs frequency.

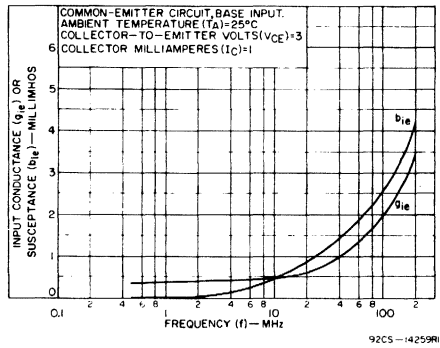


Fig.12 - Typical input admittance vs frequency.

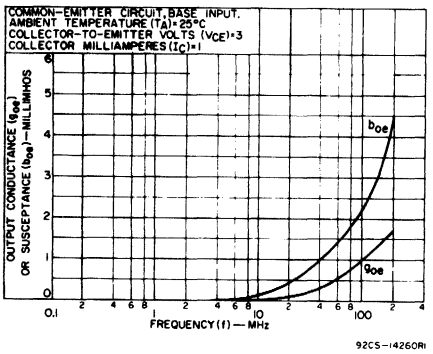


Fig.13 - Typical output admittance vs frequency.

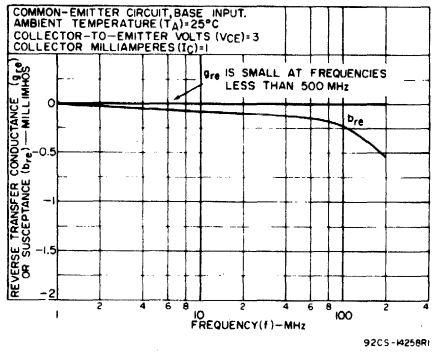


Fig.14 - Typical reverse transfer admittance vs frequency.

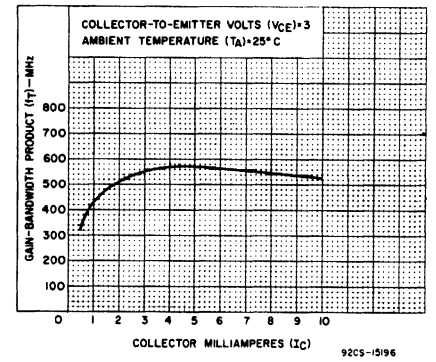


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3048

Amplifier Array

FOUR INDEPENDENT AC AMPLIFIERS

For Low-Noise and General AC Applications in Industrial Service

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

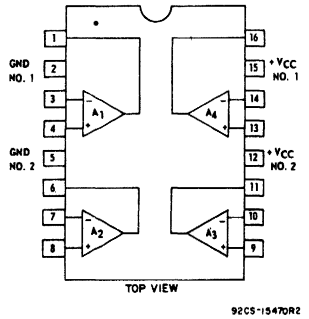


Fig. 1 - Block diagram for CA3048.

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1 kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage ..... 2 V rms min.
- Output Impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A = 55°C ..... 750 mW
- Above T_A = 55°C ..... Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating ..... -40°C to +85°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ±0.79mm) from case for 10 seconds max. ..... +265°C

POWER SUPPLY VOLTAGE ..... +16 V

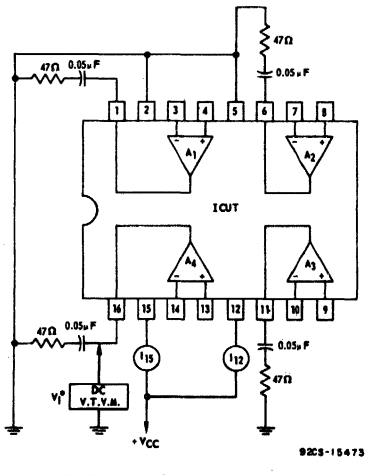
AC INPUT VOLTAGE ..... 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



* CONNECT TO APPROPRIATE TERMINAL TO READ VOLTAGE

Fig. 2 - Test circuit for measurement of collector supply voltage and currents.

CA3048

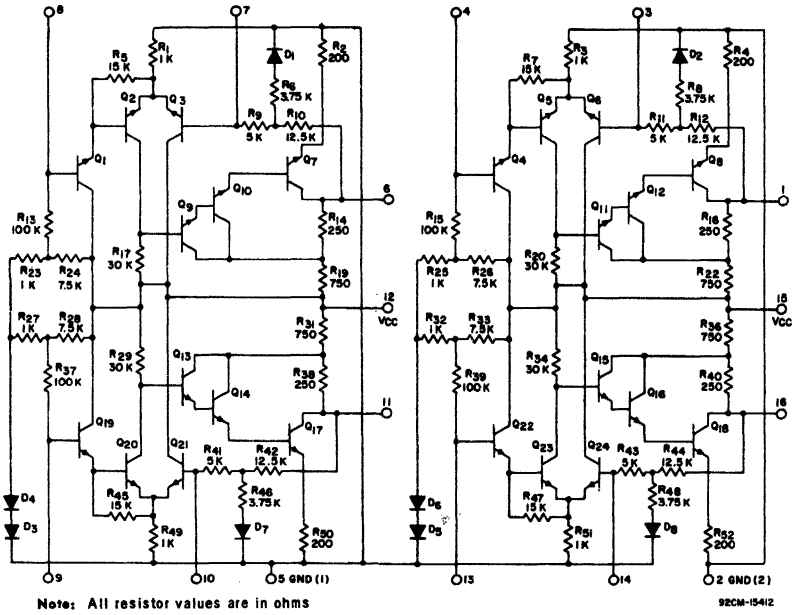


Fig.3 - Schematic diagram for CA3048.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	LIMITS CA3048 MIN.	LIMITS CA3048 TYP.	LIMITS CA3048 MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	2	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V1, V6, V11, V16	V_{CC} = +12V	2	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V3, V7, V10, V14	V_{CC} = +12V	2	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V4, V8, V9, V13	V_{CC} = +12V	2	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)								
Open-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
Output Voltage Swing	V_O(rms)	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground f = 1kHz	-	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
Output Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	E_N(WT)		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5 kΩ)	f = 10Hz	-	-	10	-	dB	-
		f = 100Hz	-	-	5.8	-	dB	
		f = 1kHz	-	-	2	-	dB	
		f = 10kHz	-	-	1.1	-	dB	
		f = 100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-

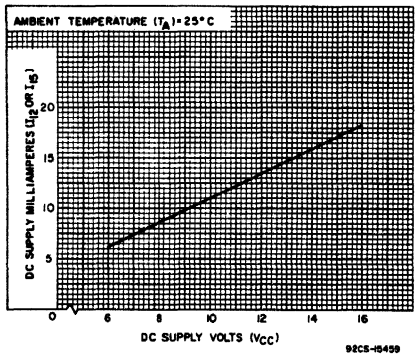


Fig.4 - Typical DC supply current vs supply voltage.

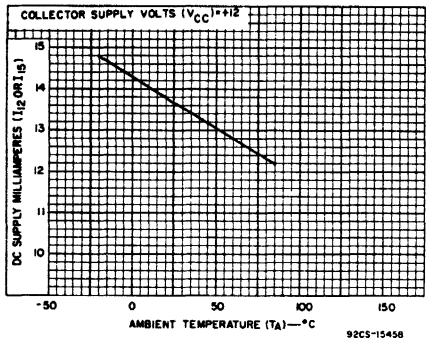
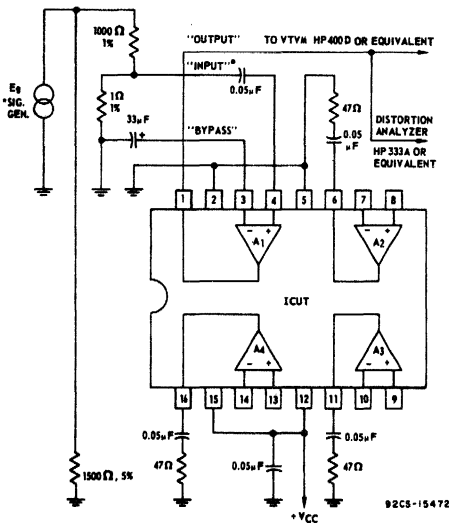


Fig.5 - Typical DC supply current vs ambient temperature.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

CA3048

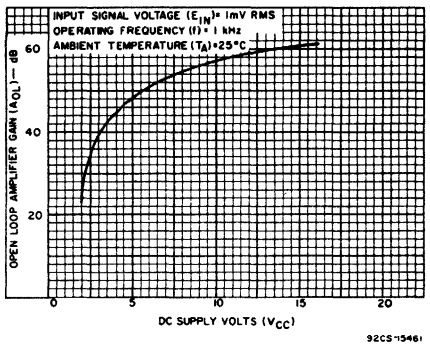


Fig.7 - Typical amplifier gain vs DC supply voltage.

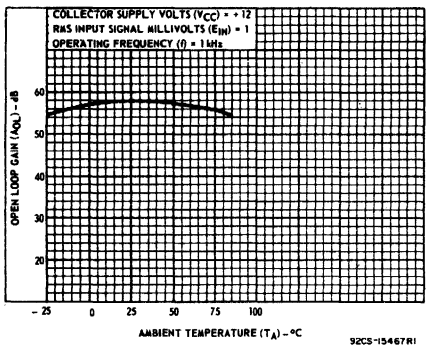


Fig.8 - Typical open-loop gain vs ambient temperature.

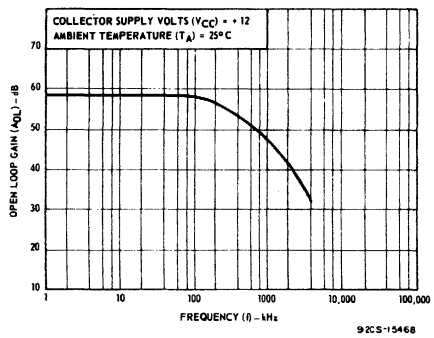


Fig.9 - Typical open-loop gain vs frequency.

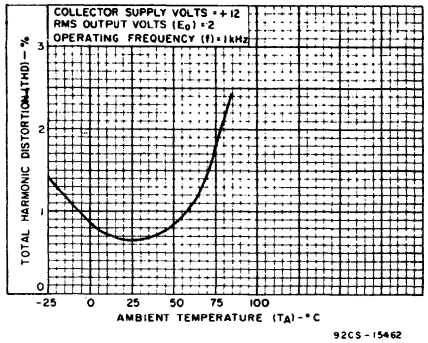
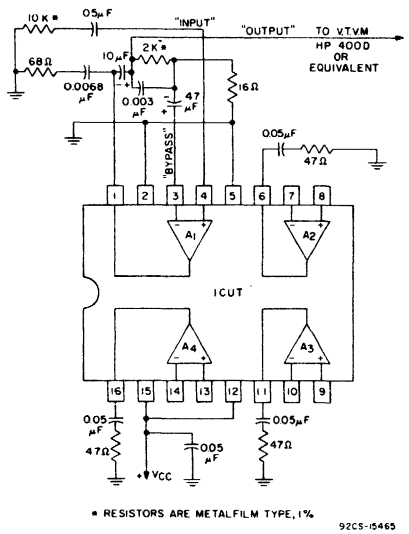


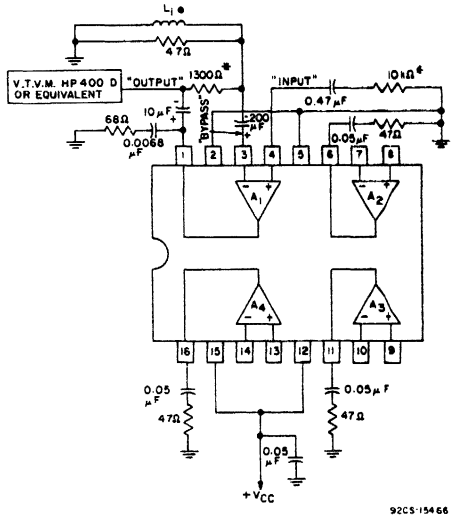
Fig.10 - Typical total harmonic distortion vs ambient temperature.



To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

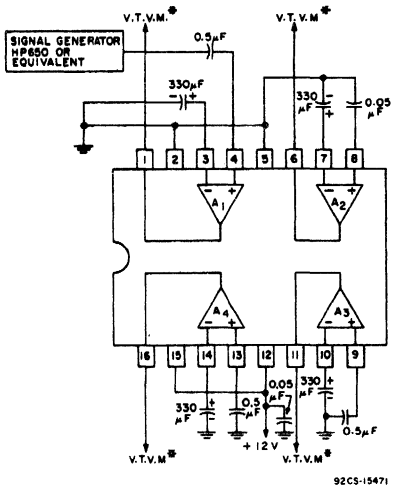


• L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

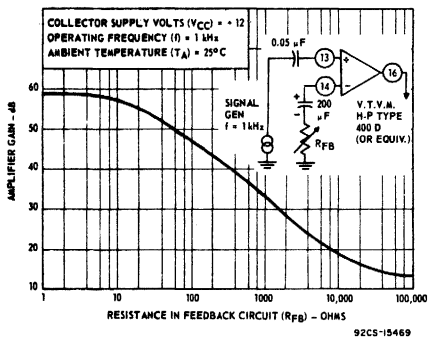


Fig.14 - Typical amplifier gain vs feedback resistance.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

CA3049T, CA3102E

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T
- **The CA3049 is available in a sealed-junction Beam-Lead version (CA3049L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

RCA-CA3049T and CA3102E consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

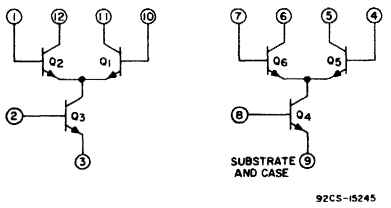
Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating.....	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

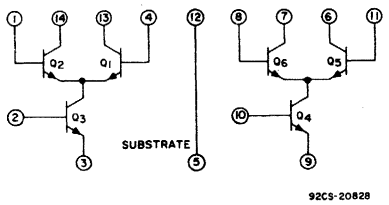
The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

Typical Characteristics for CA3049T and CA3102E

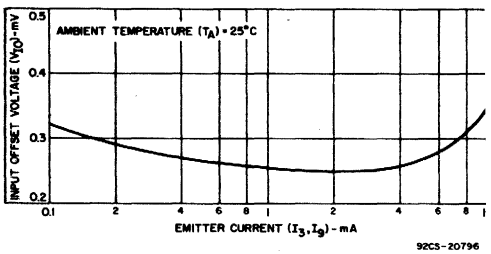


Fig. 4—Input offset voltage vs. emitter current.

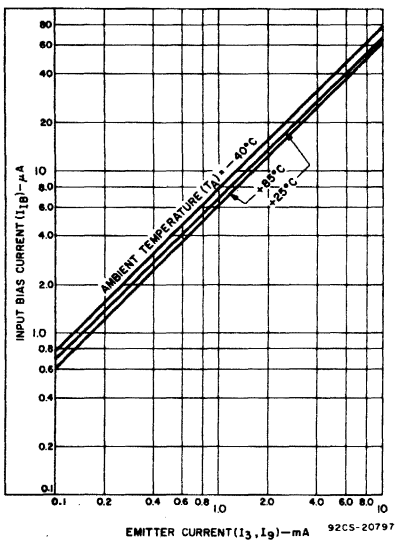


Fig. 5—Input bias current vs. emitter current.

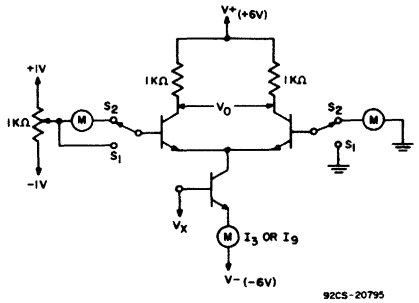


Fig. 1—Static characteristics test circuit for CA3102E.

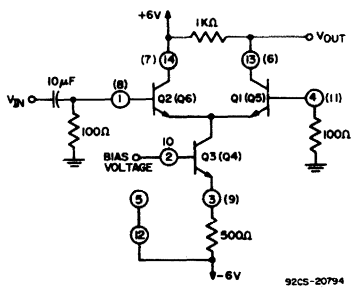
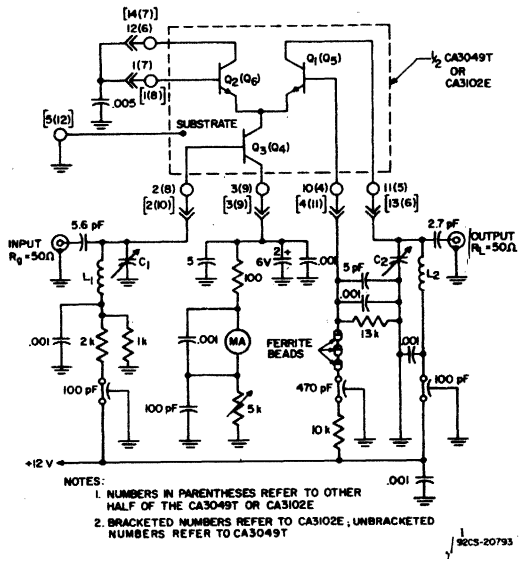


Fig. 2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3—200 MHz cascode power gain and noise figure test circuit.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT FIG.	CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARAC-TERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	---	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\left\|\frac{\Delta V_{IO}}{\Delta T}\right\|$			1	---	1.1	---	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0, V_{CB} = 5V	*	---	---	0.28	---	pF	8
			**	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0, V_{CI} = 5V			---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz, V_{CC} = 12V	Cascode	3	---	23	---	dB	---
Noise Figure	NF		Cascode	3	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

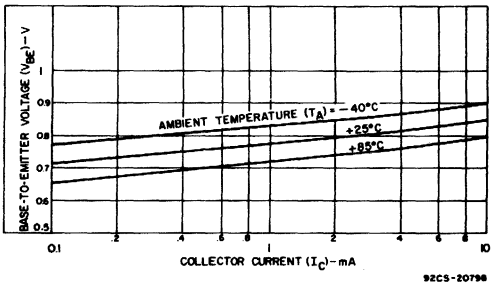


Fig. 6—Base-to-emitter voltage vs. collector current.

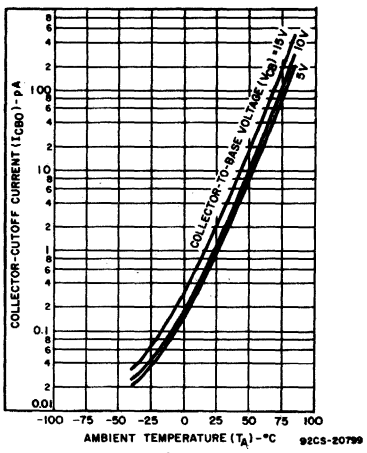


Fig. 7—Collector-cutoff current vs. temperature.

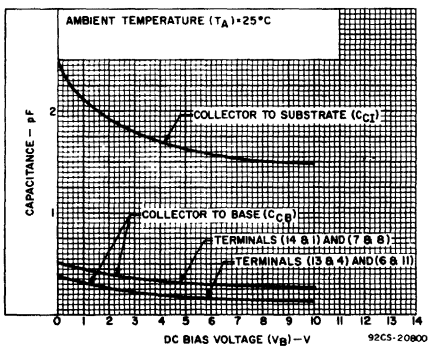


Fig. 8—Capacitance vs. dc bias voltage.

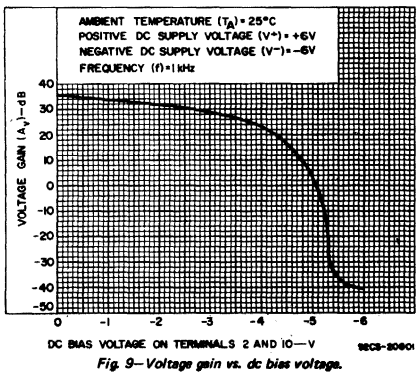


Fig. 9—Voltage gain vs. dc bias voltage.

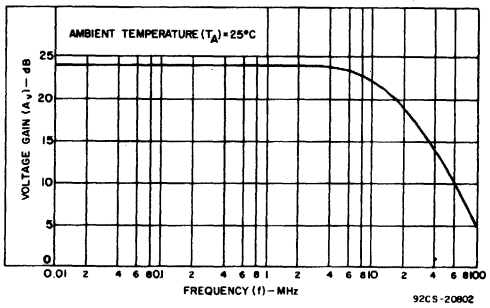


Fig. 10—Voltage gain vs. frequency.

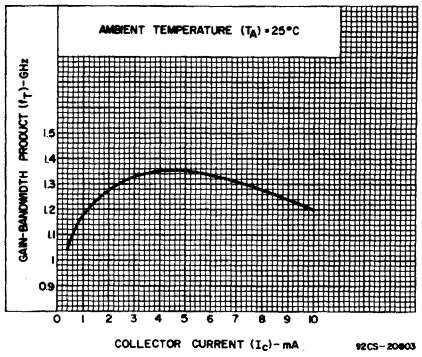


Fig. 11—Gain-bandwidth product vs. collector current.

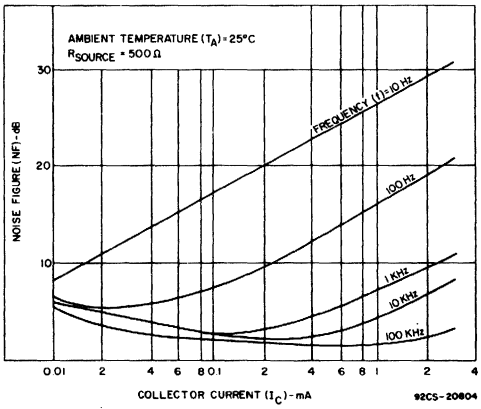


Fig. 12—1/f noise figure vs. collector current.

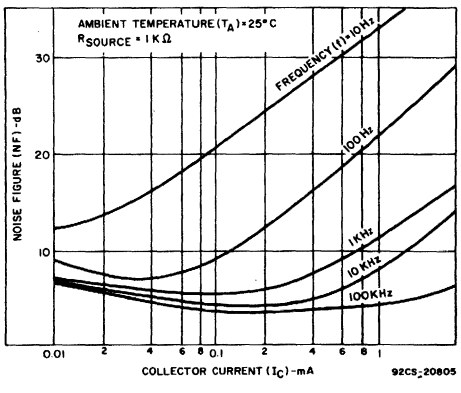


Fig. 13—1/f noise figure vs. collector current.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3102E LIMITS				TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.	UNITS	FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	5	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	3	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\lvert\frac{\Delta V_{IO}}{\Delta T}\rvert$			1	---	1.1	---	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	674	774	874	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	GH$_z$	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	*	---	0.28	---	pF	8
				**	---	0.15	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V		---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

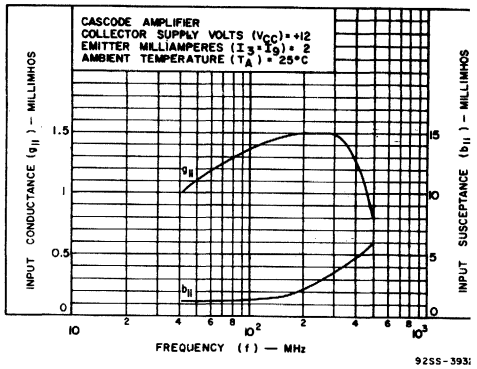


Fig. 14—Input admittance (Y_{11}) vs. frequency.

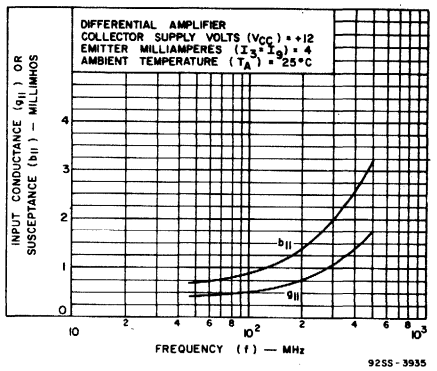


Fig. 15—Input admittance (Y_{11}) vs. frequency.

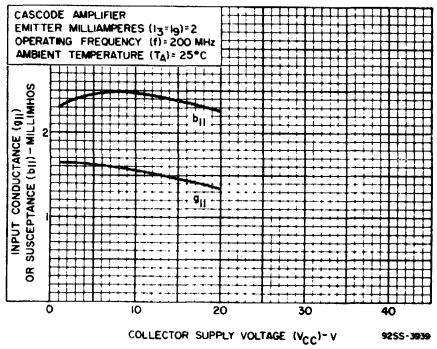


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

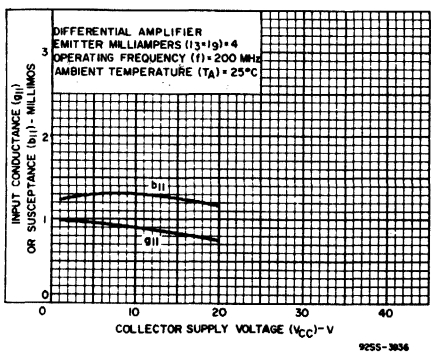


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

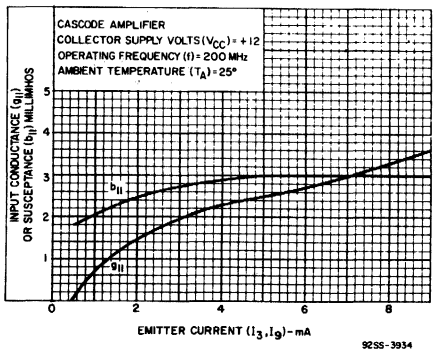


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

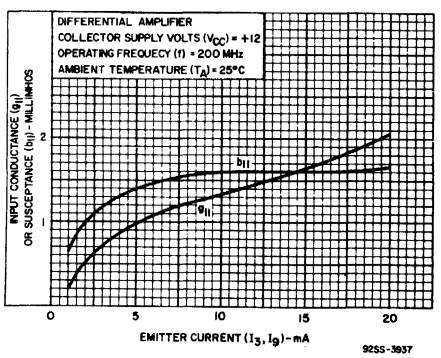


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

CA3049T, CA3102E

Typical Output Admittance Characteristics for CA3049T and CA3102E

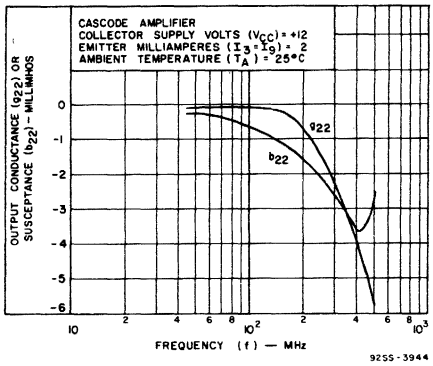


Fig. 20—Output admittance (Y_{22}) vs. frequency.

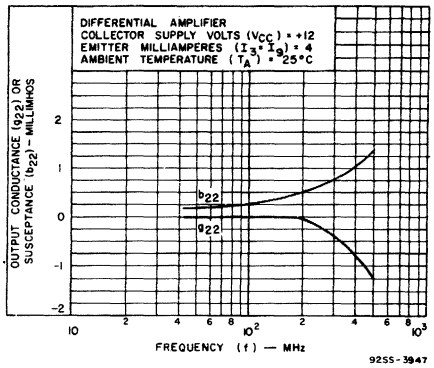


Fig. 21—Output admittance (Y_{22}) vs. frequency.

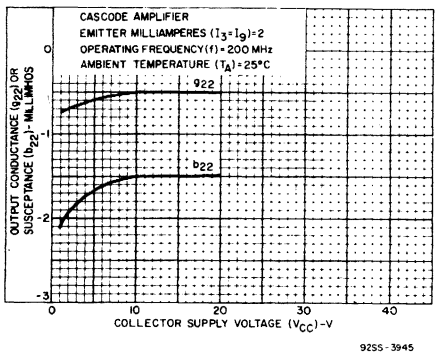


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

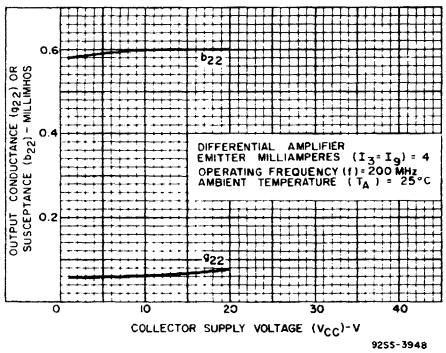


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

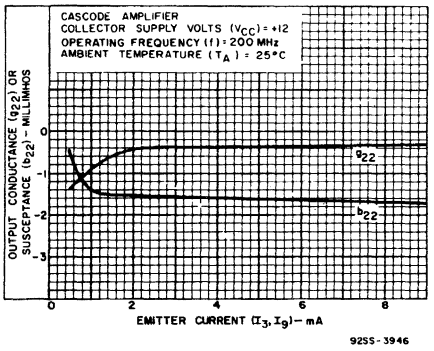


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

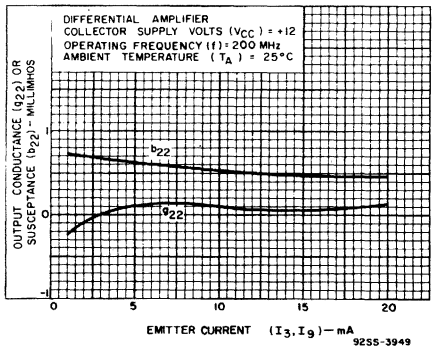


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

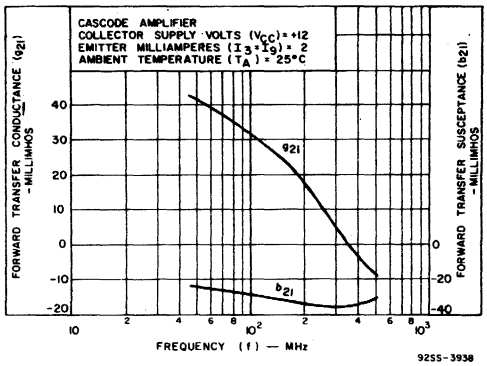


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

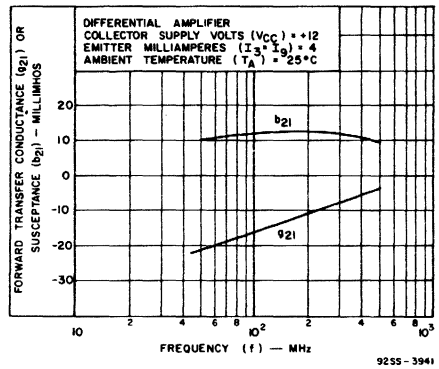


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

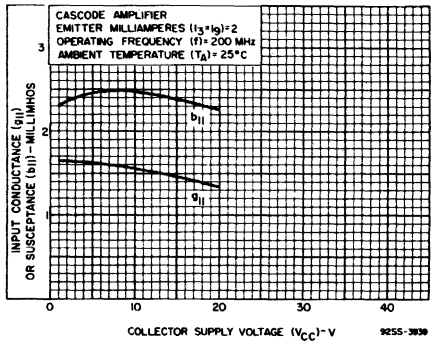


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

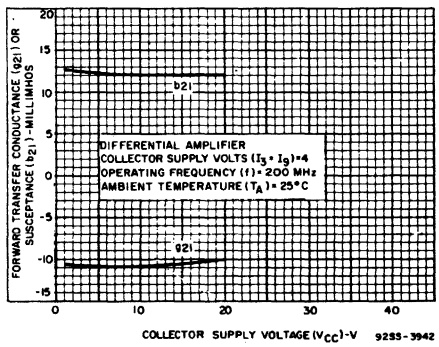


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

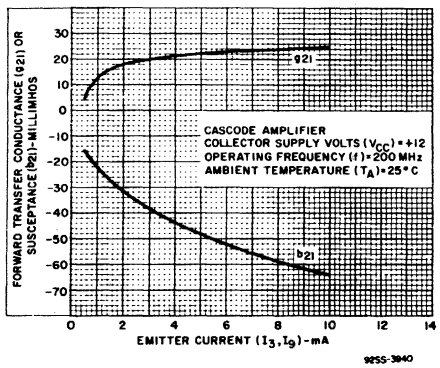


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

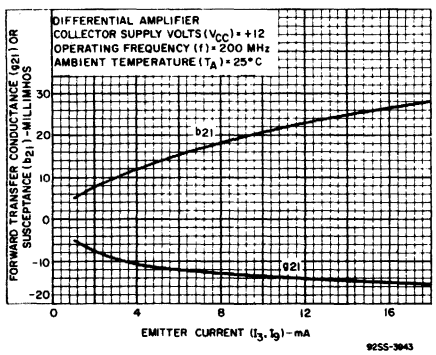


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

CA3050, CA3051

Dual Differential Amplifiers

TWO DARLINGTON-CONNECTED DIFFERENTIAL AMPLIFIERS WITH DIODE BIAS STRING

For Low-Power Applications at Frequencies from DC to 20 MHz

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

APPLICATIONS

- Matched dual amplifiers
- Dual sense amplifiers
- Dual Schmitt triggers
- Dual multivibrators
- Doubly balanced detectors and modulators
- Balanced quadrature detectors
- Synthesizer mixers
- Product detectors

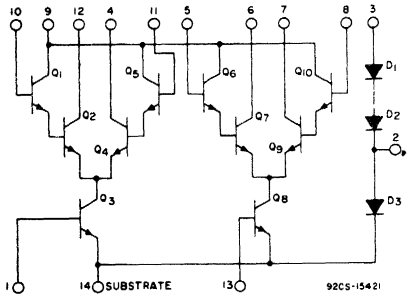


Fig.1 - Schematic diagram.

FEATURES

- Input offset current . . . . . 70 nA max.
- Input bias current . . . . . 500 nA max.
- Input offset voltage . . . . . 5 mV max.
- Input impedance . . . . . 460 kΩ typ.
- Independently accessible inputs and outputs

- **CA3050—14-lead dual-in-line ceramic package**
- **CA3051—14-lead dual-in-line plastic package**

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at . .	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125		°C
Storage	-65 to +150		°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to −2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	—	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -1
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 20	*	*	*	*	+16 -1
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -1
11												+2.5 -14 Note 4	*	+16 -1
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

NOTE 1: This rating is important only when terminal 5 is more positive than terminal 8.

NOTE 2: This rating is important only when terminal 8 is more positive than terminal 5.

NOTE 3: This rating is important only when terminal 10 is more positive than terminal 11.

NOTE 4: This rating is important only when terminal 11 is more positive than terminal 10.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

TYPICAL STATIC CHARACTERISTICS

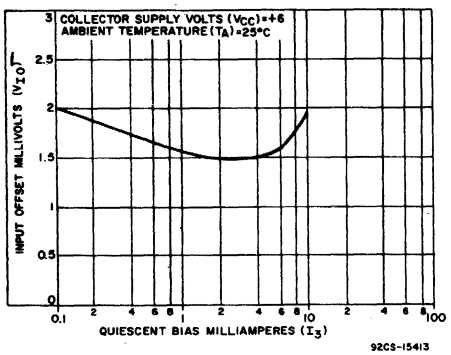


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

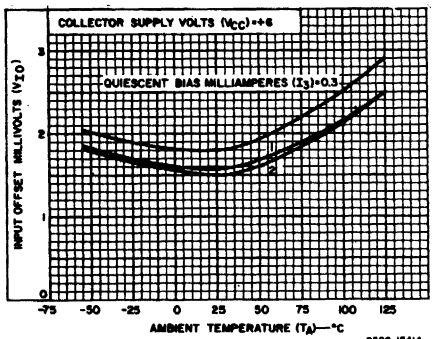


Fig.2(b) - Typical input offset voltage vs ambient temperature.

CA3050, CA3051

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_{IB}		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_I	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_O	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

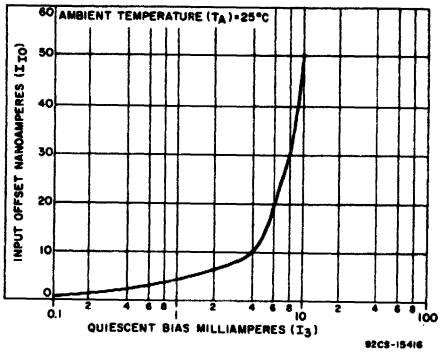


Fig.3(a) - Typical input offset current vs quiescent bias current.

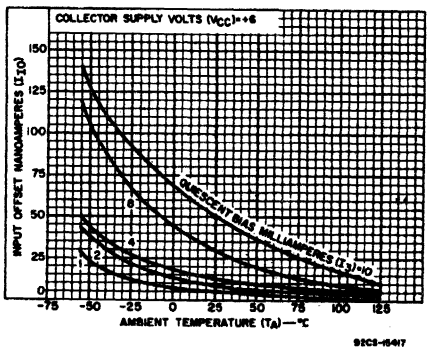


Fig.3(b) - Typical input offset current vs ambient temperature.

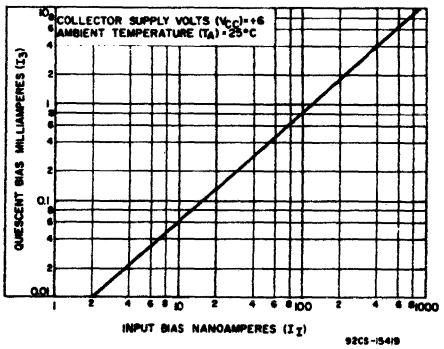


Fig.4(a) - Typical quiescent bias current vs input bias current.

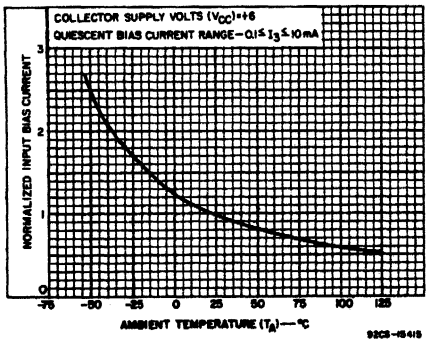


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

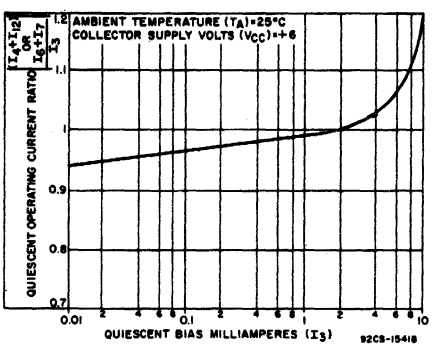


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

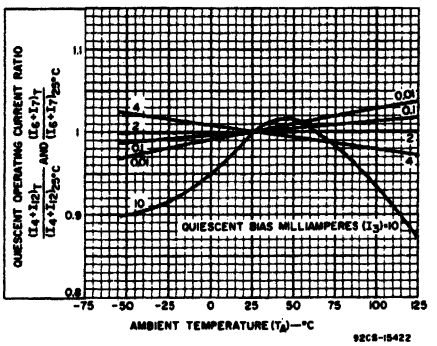


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

CA3050, CA3051

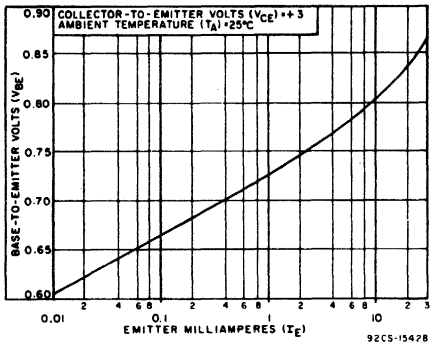


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

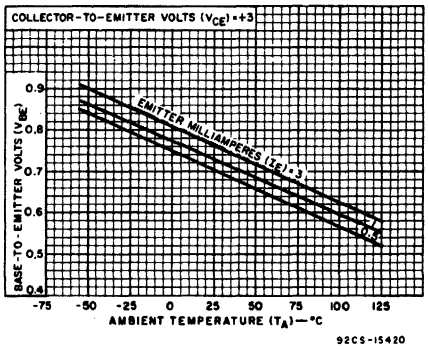


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

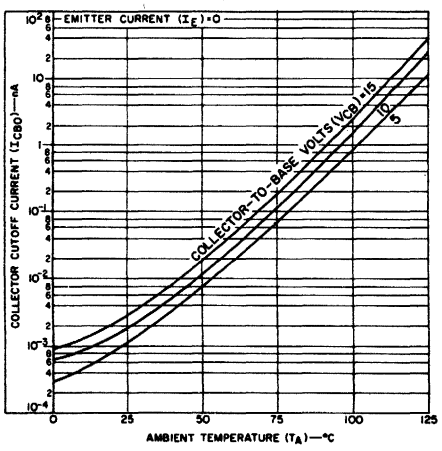


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

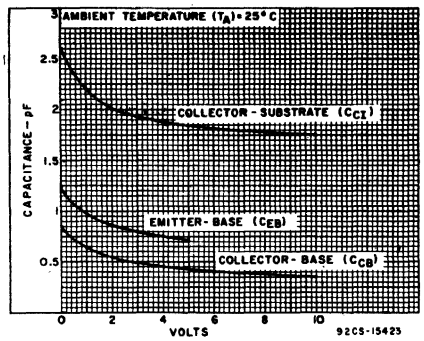


Fig.9 - Typical capacitance for each transistor.

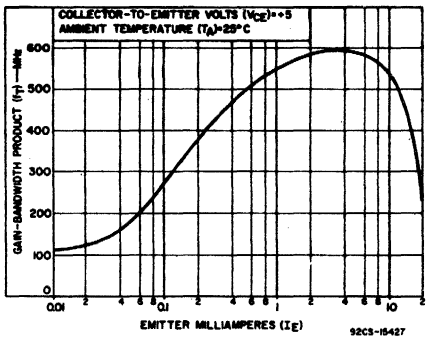
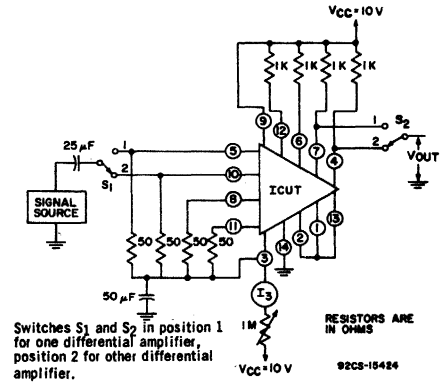


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

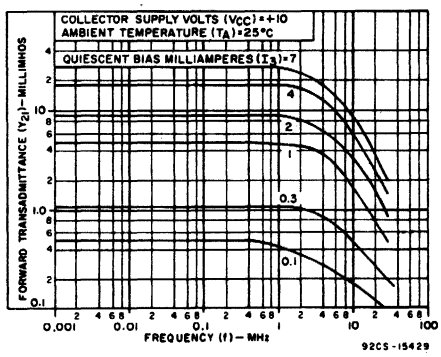
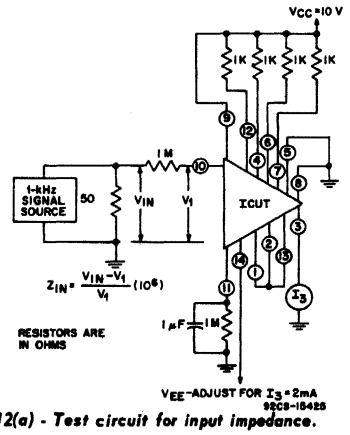


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.



$$Z_{IN} = \frac{V_{IN} - V_1}{V_1}(10^6)$$

Fig.12(a) - Test circuit for input impedance.

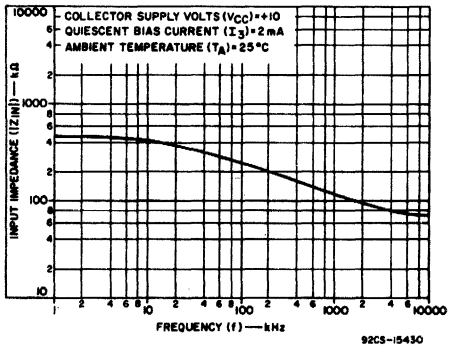
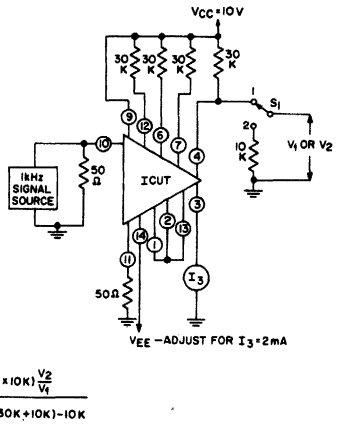


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K + 10K) - 10K}$$

Fig.13(a) - Test circuit for output impedance.

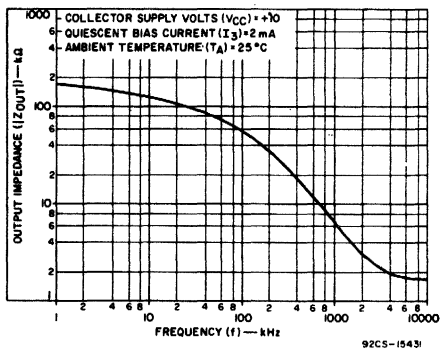


Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

CA3052

Special-Function Sub-System Stereo Preamplifier

FOUR INDEPENDENT AC AMPLIFIERS

For Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

The RCA CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent AC amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. The CA3052 can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Full-function stereo preamplifiers
- Tape recorder and playback preamplifiers
- Tone Generators

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- High voltage gain . . . . . 53 dB min.
- High input resistance . . . . . 90 k Ω typ.
- Undistorted output voltage . . . . . 2 V rms min.
- Output Impedance . . . . . 1 k Ω typ.
- Open-loop bandwidth . . . . . 300 kHz typ.

RCA CA3048 Amplifier Array (File No.377) is schematically identical with the CA3052. Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

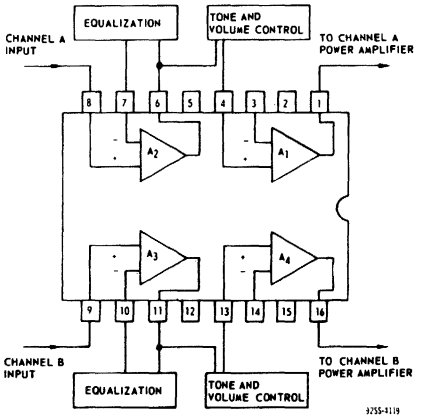


Fig.1 – Block diagram of stereo preamplifier using CA3052.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- Up to T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C . . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . −40°C to +85°C
- Storage . . . . . −65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

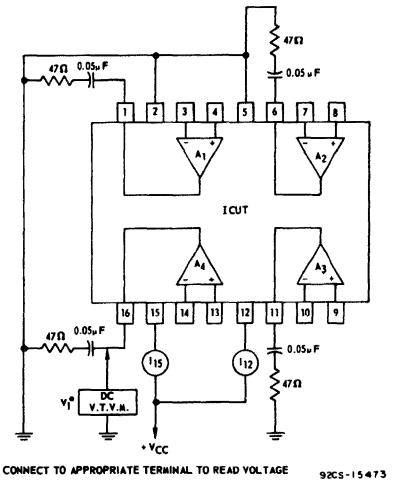


Fig. 3 - Test circuit for measurement of collector supply voltage and currents.

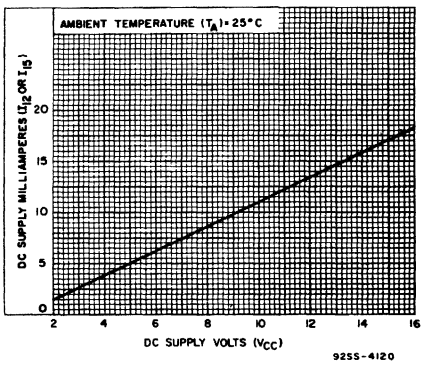
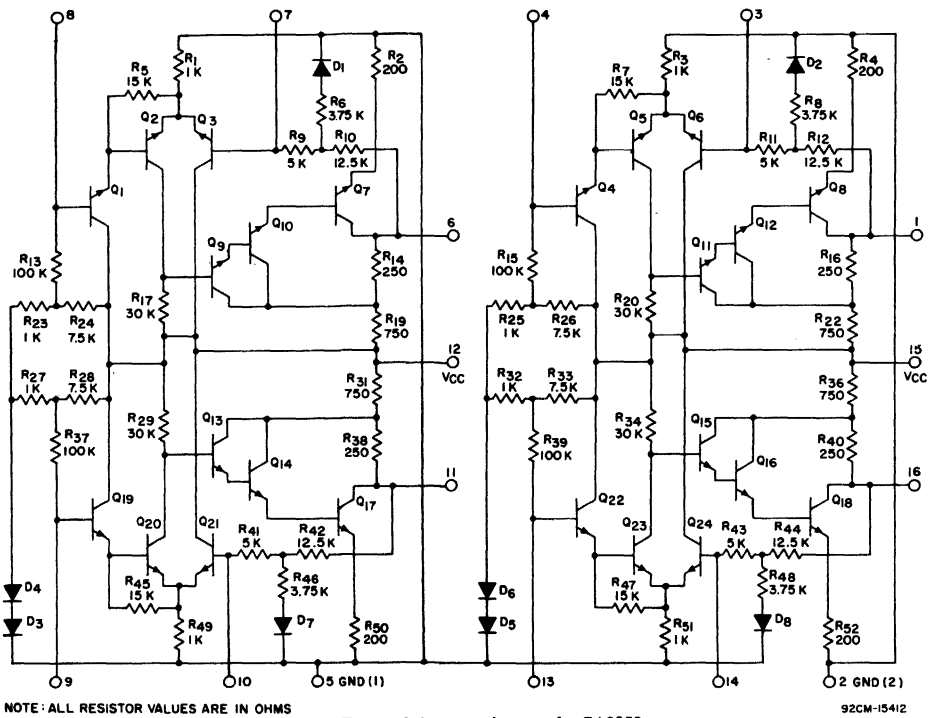


Fig. 4 - Typical DC supply current vs supply voltage.



NOTE: ALL RESISTOR VALUES ARE IN OHMS

Fig. 2 - Schematic diagram for CA3052.

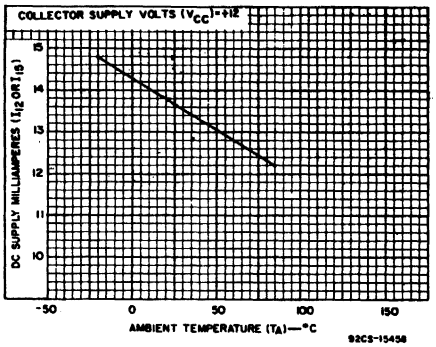


Fig. 5 - Typical DC supply current vs ambient temperature.

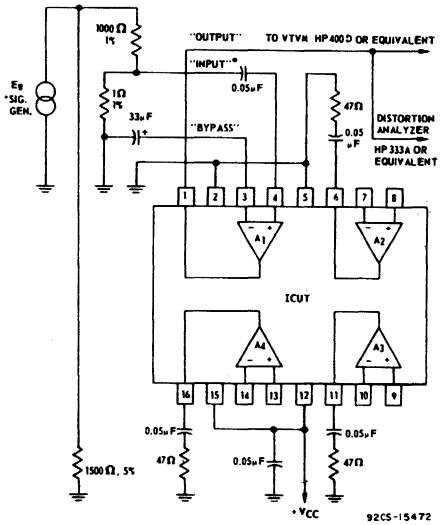
CA3052

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



* Sig. Gen. should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_s = 2 mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 - Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

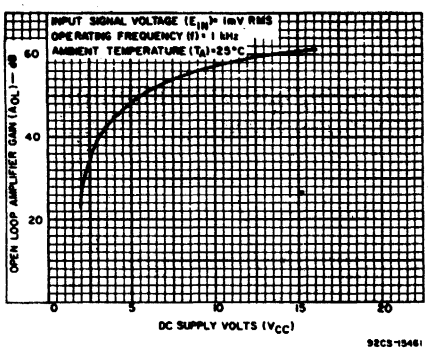


Fig. 7 - Typical amplifier gain vs DC supply voltage.

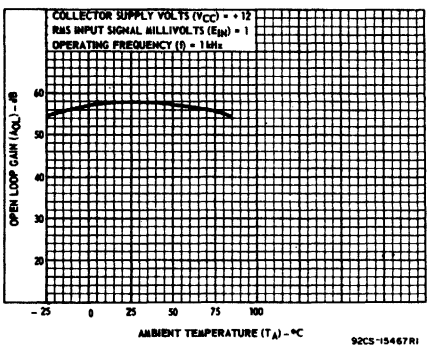


Fig. 8 - Typical open-loop gain vs ambient temperature.

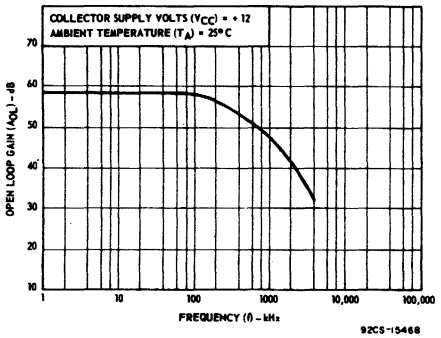


Fig. 9 - Typical open-loop gain vs frequency.

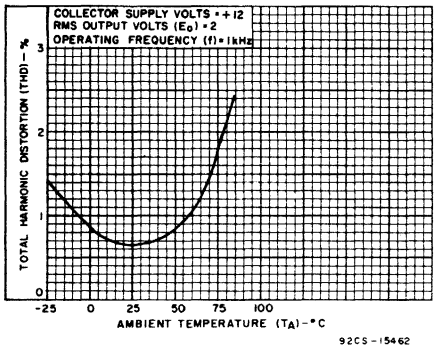
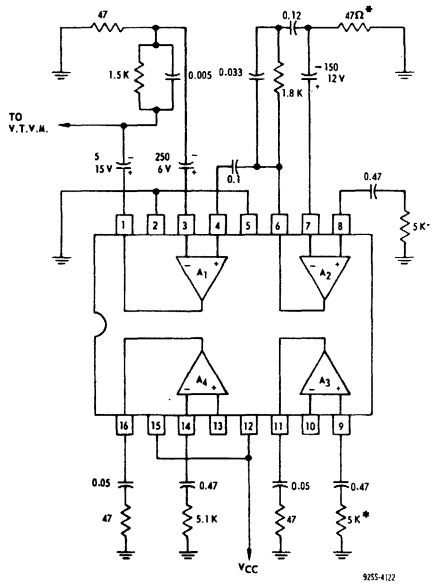


Fig. 10. - Typical total harmonic distortion vs ambient temperature.



*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 - Test circuit for equivalent input noise voltage measurement, RIAA compensated.

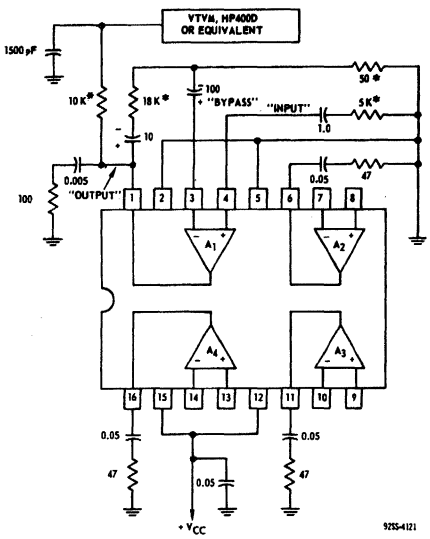
CA3052

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3052			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	3	9.5	13.5	17.5	mA	4, 5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	3	6.1	6.9	8.1	V	–
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	3	1.7	2.0	2.3	V	–
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	3	2.2	2.5	2.8	V	–
DYNAMIC each amplifier with no AC feedback unless otherwise noted–terminals 3, 7, 10, & 14 bypassed to ground								
Open-Loop Gain	A_{OL}	V_{CC} = +12 V, E_{IN} = 2 mV, f = 10 kHz	6	53	58	–	dB	7, 8
Open-Loop Output Voltage Swing	$V_{O(rms)}$	V_{CC} = +12 V, f = 1 kHz, THD = 5%	6	2.0	2.4	–	V	–
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V, E_{IN} = 2 mV	6	–	300	–	kHz	9
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz, E_{OUT} = 2 V rms	6	–	0.65	–	%	10
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	–	90	–	kΩ	–
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	–	9	–	pF	–
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	–	1	–	kΩ	–
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V, f = 1 MHz	–	–	<0.1	–	pF	–
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{NI}‡	V_{CC} = +10 V, R_S = 5 kΩ, A = 45 dB	12	–	1.7	6.4	μV	–
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V, R_S = 5 kΩ, A = 64 dB (1 kHz)	11	–	4	15.0	μV	–
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12 V, f = 1 kHz, 0 dB = 0.78 V	13	–	<-45	–	dB	–
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V, f = 1 MHz	–	–	< 0.02	–	pF	–

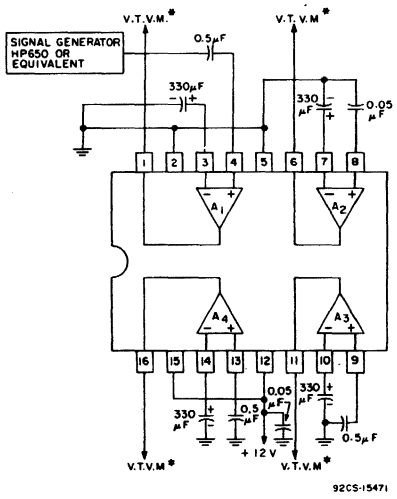
*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12 - Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.



*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

CA3058, CA3059, CA3079

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply—Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier—Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector—Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit—Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

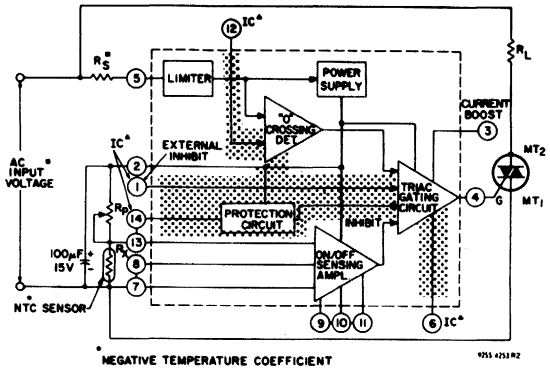
1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages.

Applications:

- **Relay control**
- **Heater control**
- **Valve control**
- **Lamp control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **Photosensitive control**
- **Power one-shot control**



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:
Circuitry, within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1—Functional block diagram of CA3058, CA3059, and CA3079.

Features	CA3058	CA3059	CA3079
■ 24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
■ Differential Input	√	√	√
■ Low Balance Input Current (max.) -μA	1	1	2
■ Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
■ Sensor Range (R_X) - kΩ	2 to 100	2 to 100	2 to 50
■ DC Mode (Term 12)	√	√	
■ External Trigger (Term. 6)	√	√	
■ External Inhibit (Term. 1)	√	√	
■ DC Supply Volts (max.)	14	14	10
■ Operating Temperature Range - °C		−55 to +125	

MAXIMUM RATINGS,
Absolute-Maximum Values at T_A = 25°C

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8):
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ±50 mA

OUTPUT PULSE CURRENT (TERM. 4) ..... 150 mA

POWER DISSIPATION:
Up to T_A=75°C − CA3058 ..... 700 mW
Up to T_A=55°C − CA3059,CA3079 ... 700 mW
Above T_A=75°C − CA3058 ..... Derate Linearly 8 mW/°C
Above T_A=55°C − CA3059,CA3079 ..... Derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

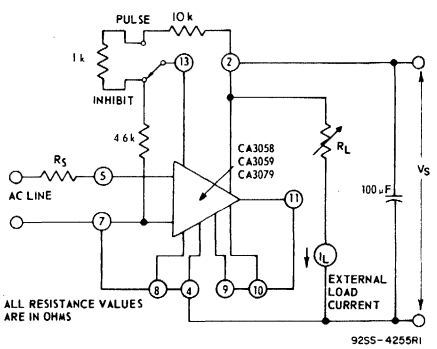


Fig. 2(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

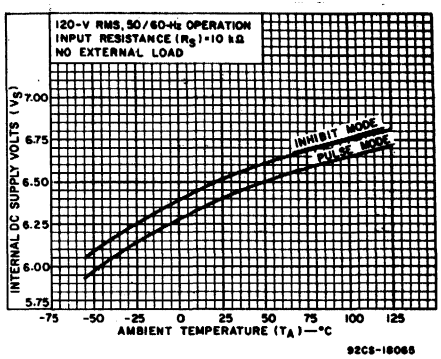


Fig. 2(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059 and CA3079.

CA3058, CA3059, CA3079

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0▲ -14	0▲ -14	0 -14	0 -14	0 -14	* .	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to −10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

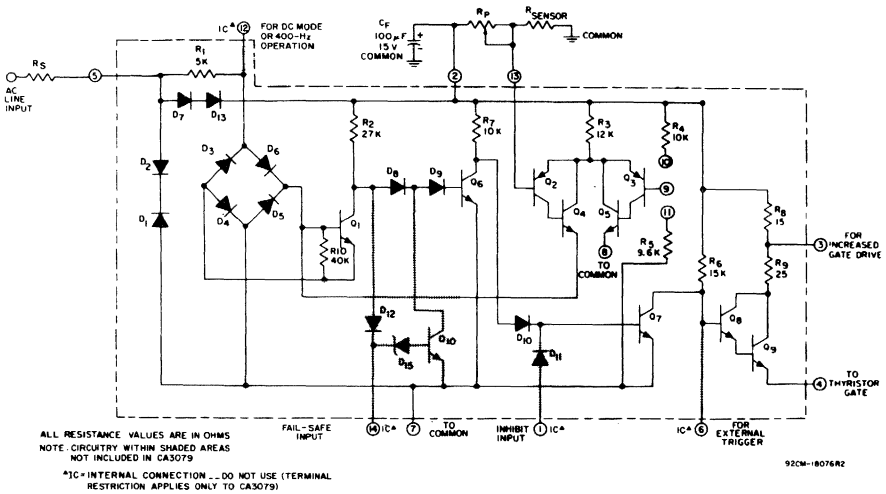


Fig. 4—Schematic diagram of CA3058, CA3059, and CA3079.

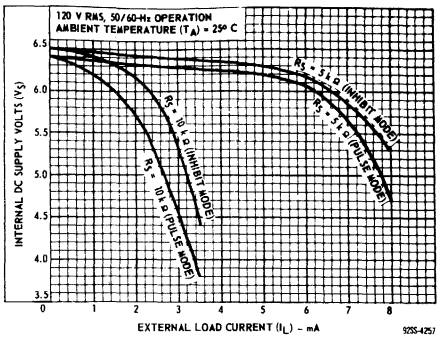


Fig. 2(c)—DC supply voltage vs. external load —current for CA3058, CA3059, and CA3079.

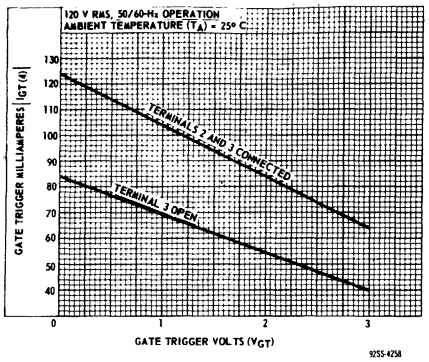


Fig. 3—Gate trigger current vs. gate trigger voltage for CA3058, CA3059, and CA3079.

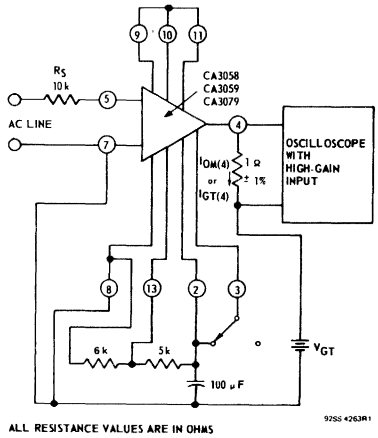


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059, and CA3079.

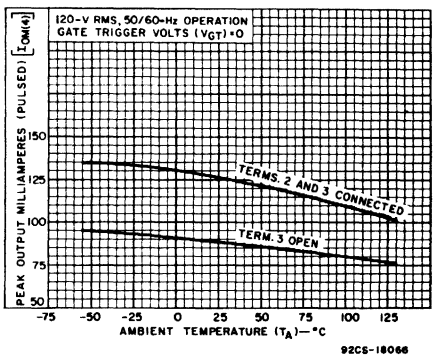


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3058, CA3059, and CA3079.

CA3058, CA3059, CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	Typ.	Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.8	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.7	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 2*	R_S = 8 kΩ, I_L = 0, T_A = −55 to +125°C	5.5	–	7.5	V
Gate Trigger Current, I_{GT}(4) *See Figs. 3, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}(4)	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
With Internal Power Supply	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
With External Power Supply *See Figs. 5, 6*	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2					
All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058 *See Fig. 7*	T_A = −55 to +125°C	0.450	–	0.520	–
Total Gate Pulse Duration:*					
For positive dv/dt, t_P					
50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N					
50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz):					
For positive dv/dt, t_{P1}	C_{EXT} = 0, R_{EXT} = ∞	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*		–	60	–	μs
Output Leakage Current, I_4					
Inhibit Mode:					
All Types		–	0.001	10	μA
CA3058 *See Fig. 9*	T_A = −55 to +125°C	–	–	20	μA
Input Bias Current, I_I					
CA3058, CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA

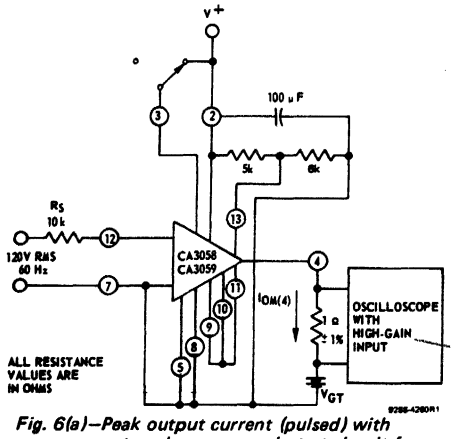


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

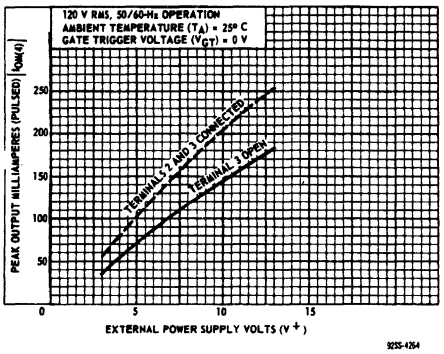


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

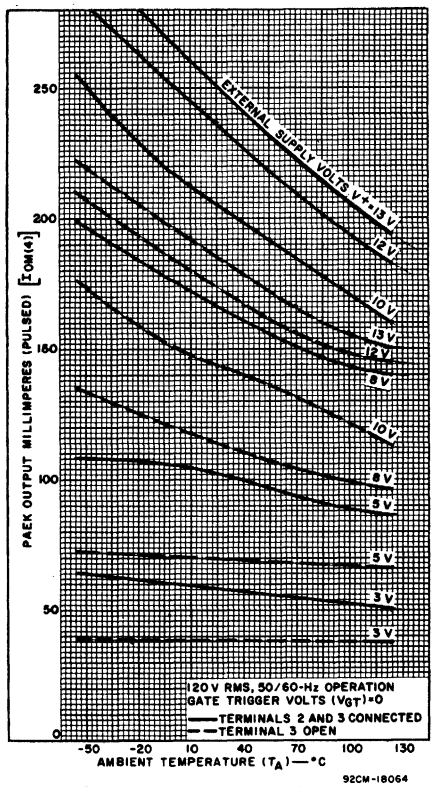


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

CA3058, CA3059, CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS			UNITS
		Min.	Typ.	Max.	
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, ΔV_{13} ≠ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠ Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

* Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

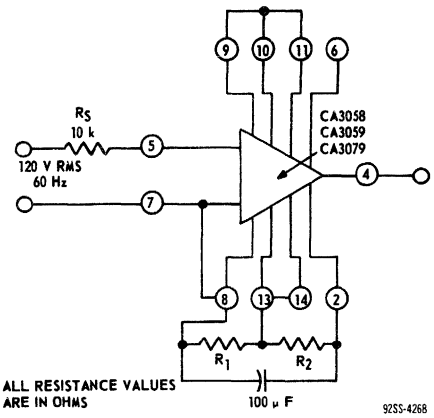


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3058, CA3059, and CA3079.

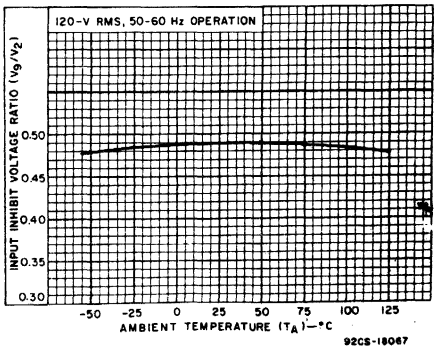


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3058, CA3059, and CA3079.

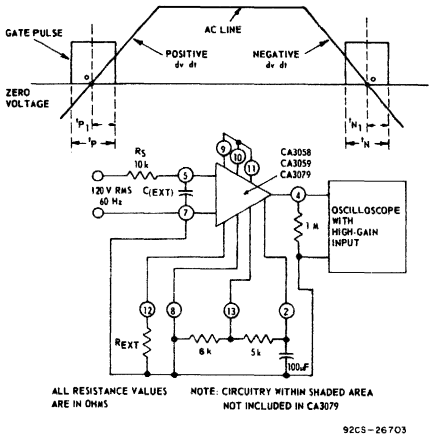


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3058, CA3059, and CA3079.

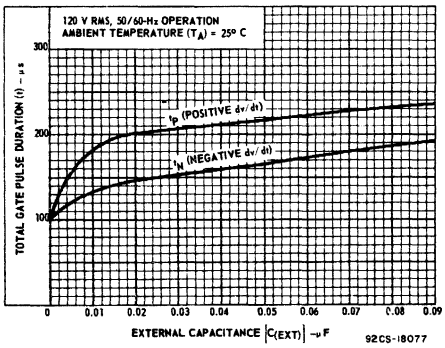


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3058, CA3059, and CA3079.

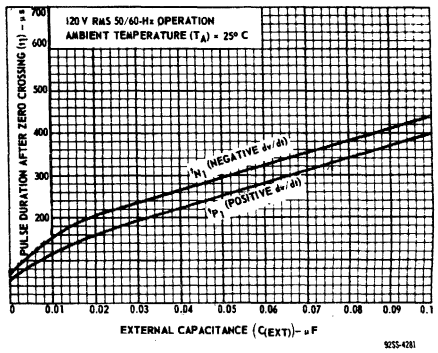


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059, and CA3079.

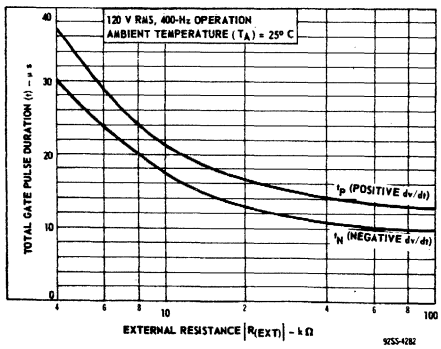


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

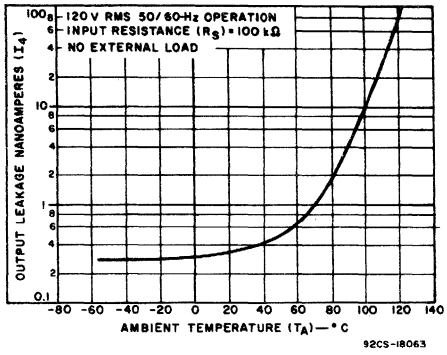


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3058, CA3059, and CA3079.

CA3058, CA3059, CA3079

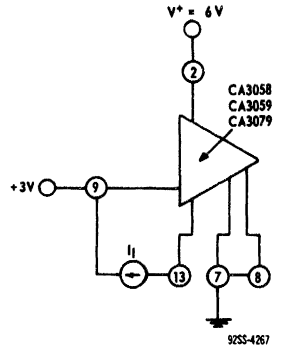


Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.

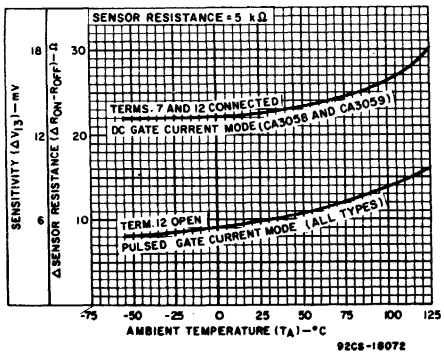


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

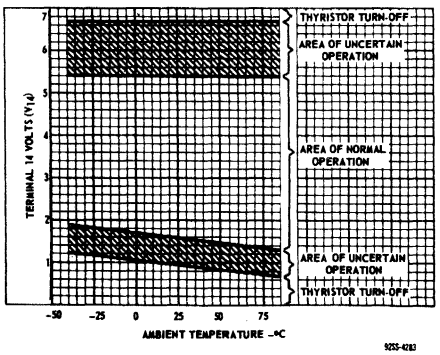
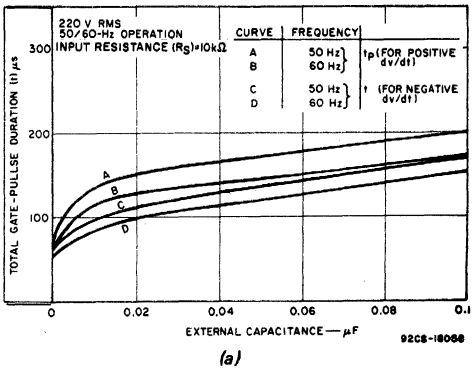
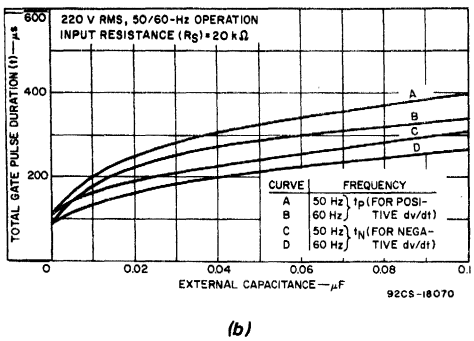


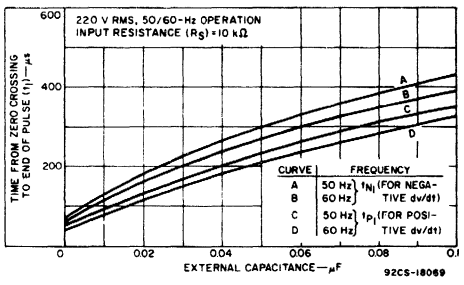
Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.



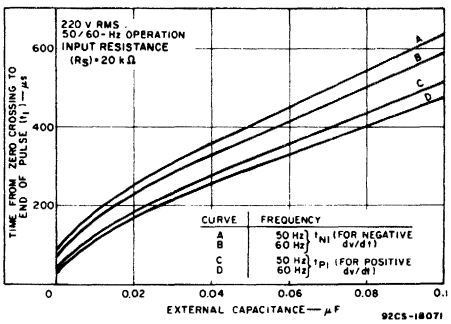
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

CA3060, CA3060A Types

Operational Transconductance Amplifier Arrays

APPLICATIONS

- **For low power conventional operational amplifier applications**
- **Active filters**
- **Comparators**
- **Gyrators**
- **Mixers**
- **Modulators**
- **Multiplexers**
- **Multipliers**
- **Strobing and gating functions**
- **Sample and hold functions**

FEATURES

- **Low power consumption – as low as 100 μW per amplifier**
- **Independent biasing for each amplifier**
- **High forward transconductance**
- **Programmable range of input characteristics**
- **Low input bias and input offset current**
- **High input and output impedance**
- **No effect on device under output short-circuit conditions**
- **Zener diode bias regulator**

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific applications. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition; the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, and CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, -55°C to +125°C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from -40°C to +85°C.

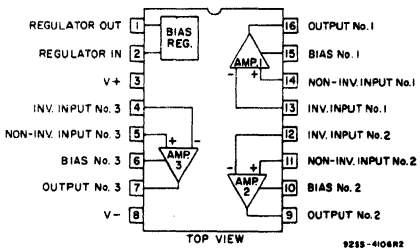


Fig. 1—Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals):
- CA3060AD, CA3060BD, CA3060E ..... 36V (±18V)
- CA3060D ..... 14 V (±7V)

Differential Input Voltage (each amplifier):
- CA3060AD, CA3060BD, CA3060E ..... ±5V
- CA3060D ..... ±5V

DC Input Voltage ..... V^+ to V^-

Input Signal Current (each amplifier of each type): ..... ±1 mA

Amplifier Bias Current (each amplifier of each type) ..... 2 mA

Bias Regulator Input Current ..... 5 mA

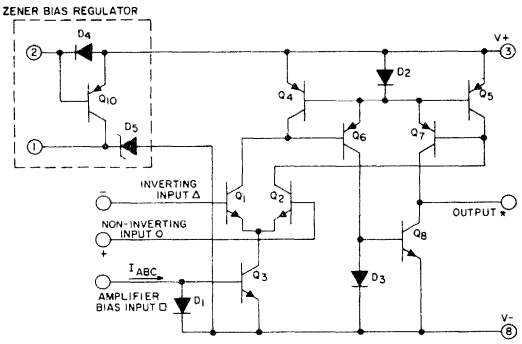
Output Short-Circuit Duration* ..... No limitation

*Short circuit may be applied to ground or to either supply.

Device Dissipation:
- Total Package of each type up to T_A = 75°C ..... 490 mW
- Above T_A = 75°C ..... Derate linearly 6.67 mW/°C

Temperature Range:
- Operating –
  - CA3060AD, CA3060BD, CA3060D ..... -55 to +125°C
  - CA3060E ..... -40 to +85°C
- Storage –
  - CA3060AD, CA3060BD, CA3060D, CA3060E ..... -65 to +150°C

Lead Temperature (During Soldering):
- At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max ..... +300°C



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
○ NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860R1

Fig. 2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

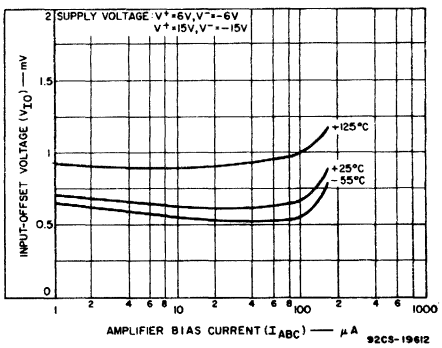


Fig. 3—Input offset voltage vs. amplifier bias current.

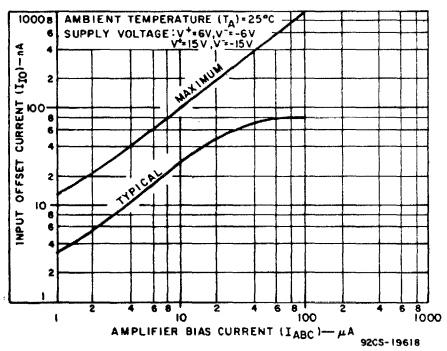


Fig. 4—Input offset current vs. amplifier bias current.

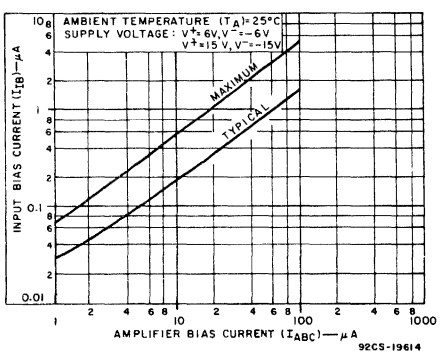


Fig. 5a—Input bias current vs. amplifier bias current

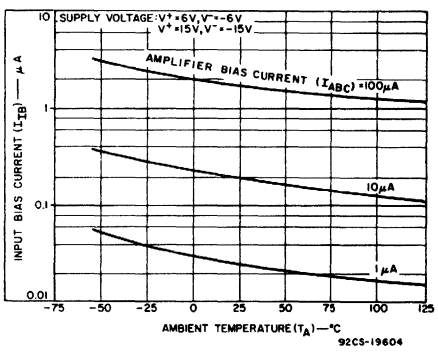


Fig. 5b—Input bias current vs. ambient temperature.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060D)
For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS — Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Negative	V_{OM^-}		5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	120	–	20	120	–	30	120	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —
V^+ is reduced to 5 volts for V^+ sensitivity
V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset} - \text{Voffset for +5 V and -6 V supplies}}{1 \text{ volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset} - \text{Voffset for -5 V and +6 V supplies}}{1 \text{ volt}}$

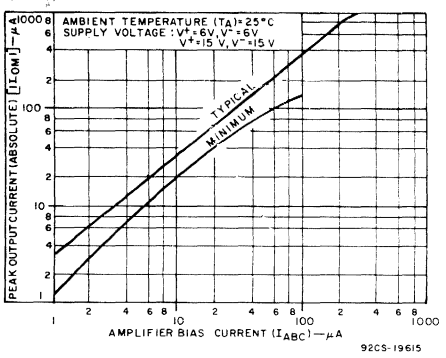


Fig.6a—Peak output current vs. amplifier bias current.

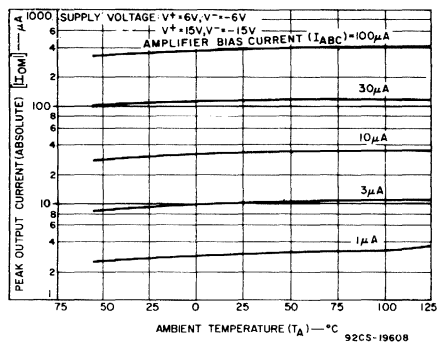


Fig.6b—Peak output current vs. ambient temperature.

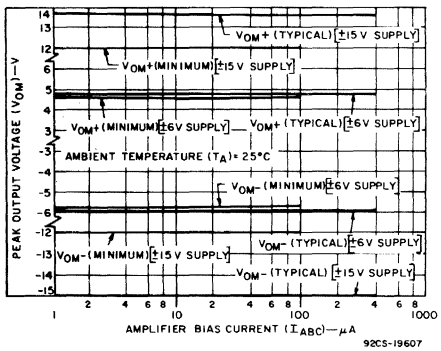


Fig.7—Peak output voltage vs. amplifier bias current.

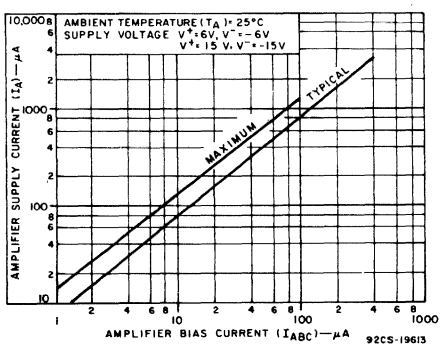


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

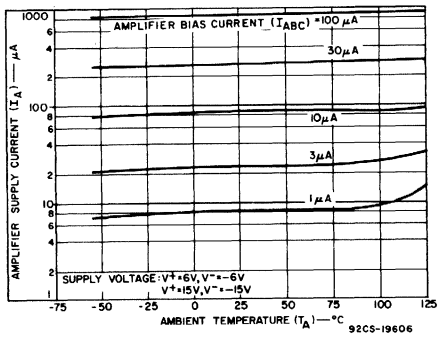


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

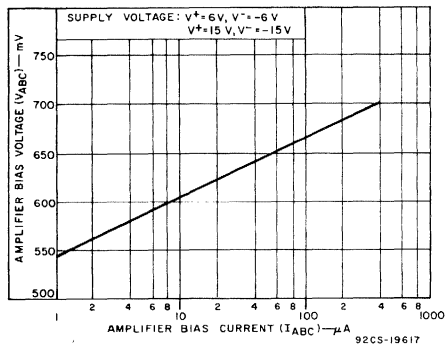


Fig.9—Amplifier bias voltage vs. amplifier bias current.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)
For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS									UNITS
			Amplifier Bias Current									
			I_{ABC} = 1 μA			I_{ABC} = 10 μA			I_{ABC} = 100 μA			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
			CA3060BD						CA3060AD CA3060BD CA3060E			
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Peak Output Voltage: Negative	V_{OM^-}	7	12	14.7	–	12	14.7	–	12	14.7	–	V
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	150	–	2	150	–	2	150	μV/V
Input Offset-Voltage Sensitivity■: Negative	$\Delta V_{IO}/\Delta V^-$	–	–	20	150	–	20	150	–	30	150	μV/V
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	–	–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Input Impedance Components: Capacitance at 1 MHz	C_I	12	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Output Impedance Components: Capacitance at 1 MHz	C_O	14	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)												
						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient: -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ···
V^+ is reduced to 13 volts for V^+ sensitivity
V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset} \cdot \text{Voffset for +13 V and −15 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset} \cdot \text{Voffset for −13 V and +15 V supplies}}{\text{1 volt}}$

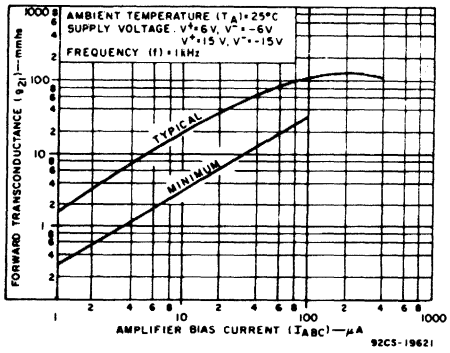


Fig.10a—Forward transconductance vs. amplifier bias current.

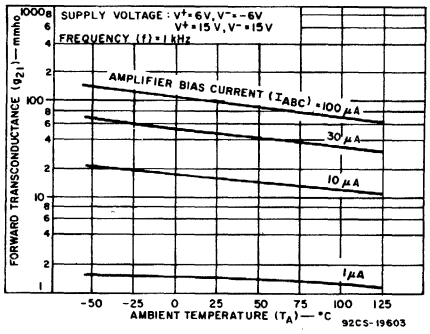


Fig.10b—Forward transconductance vs. ambient temperature.

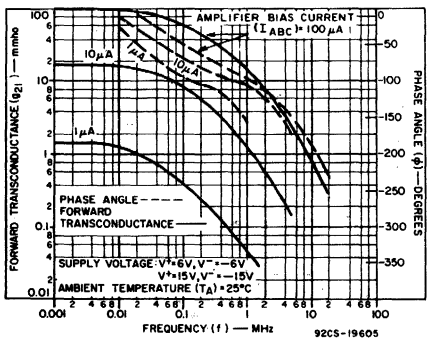


Fig.11—Forward transconductance vs. frequency.

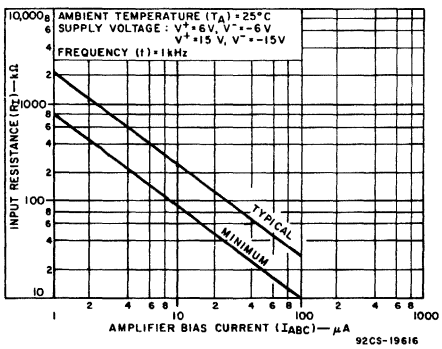
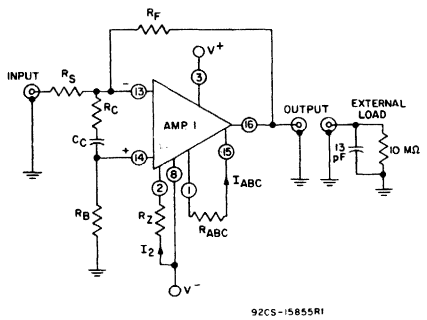


Fig.12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig.13—Slew rate test circuit for amplifier No. 1 of CA3060.

CA3060, CA3060A Types

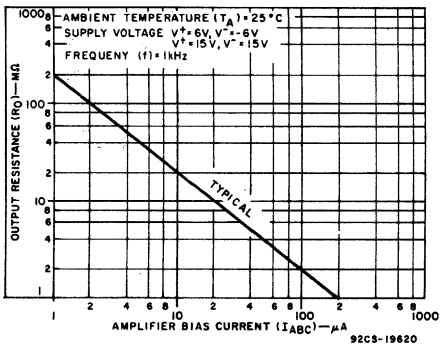


Fig.14—Output resistance vs. amplifier bias current.

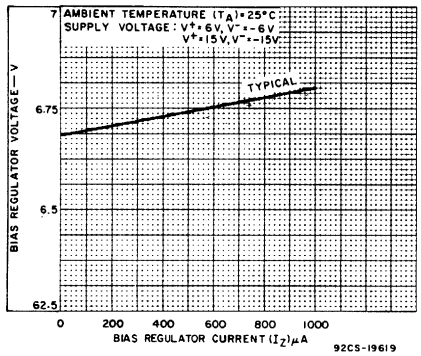


Fig.15—Bias regulator voltage vs. bias regulator current.

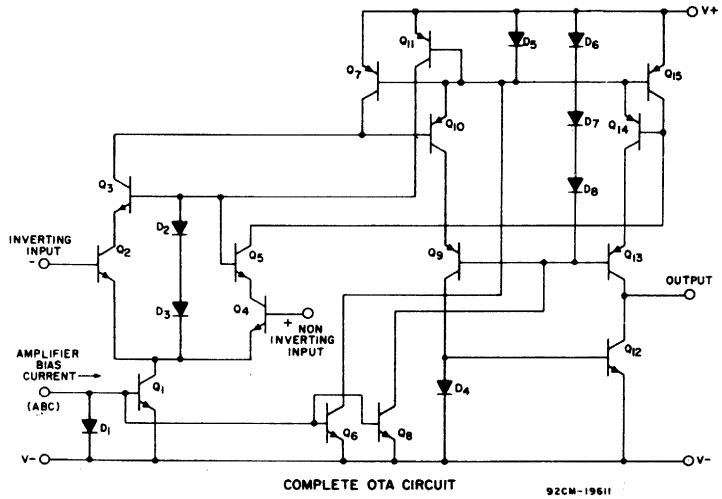


Fig.16 – Complete schematic diagram showing one of the three operational transconductance amplifiers.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

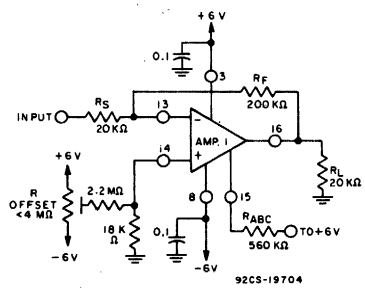


Fig.17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or} \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

$$\text{i.e. } \frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

CA3060, CA3060A Types

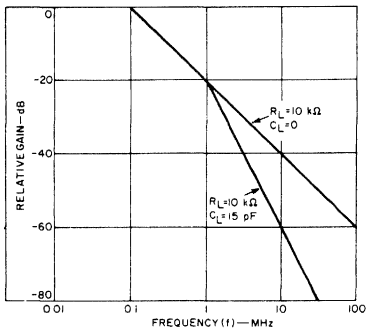


Fig.18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

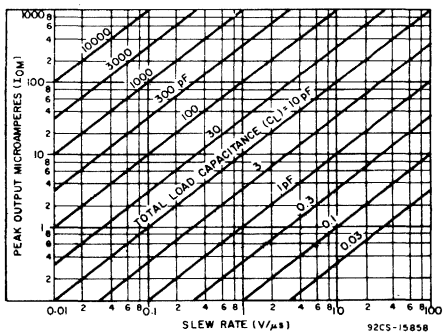


Fig.19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

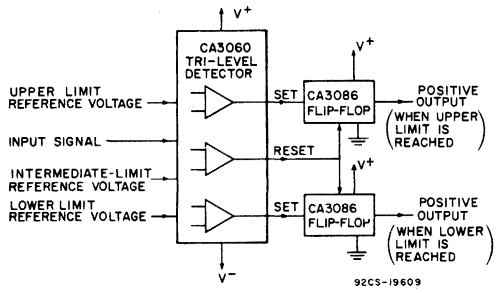


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V-, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

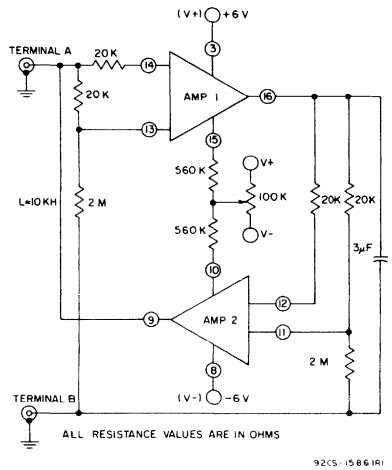


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

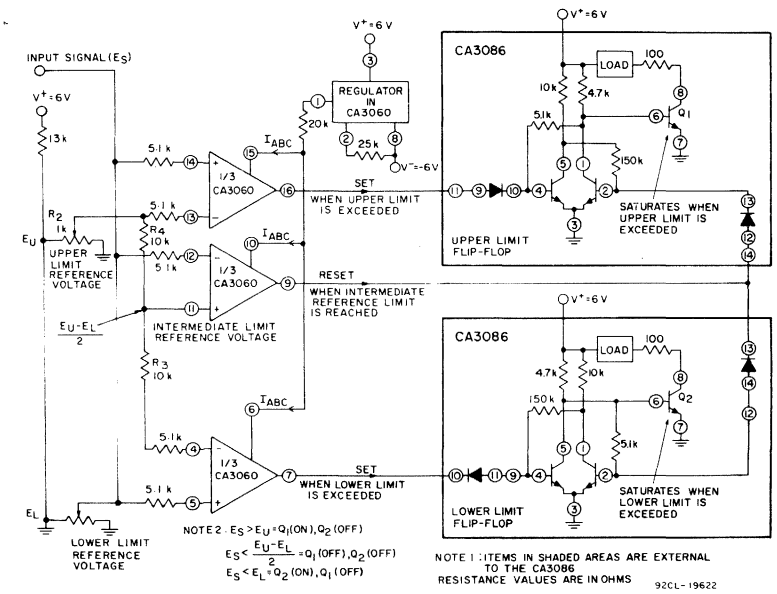


Fig.21—Tri-level comparator circuit.

CA3060, CA3060A Types

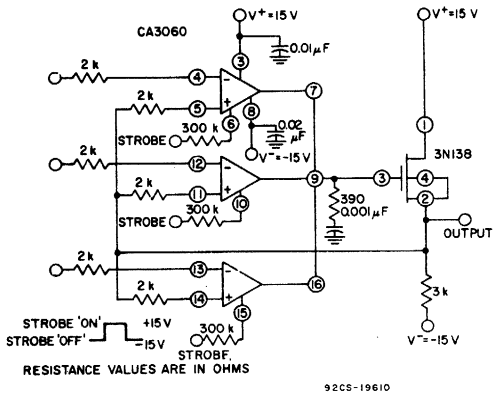


Fig.23—Three-channel multiplexer.

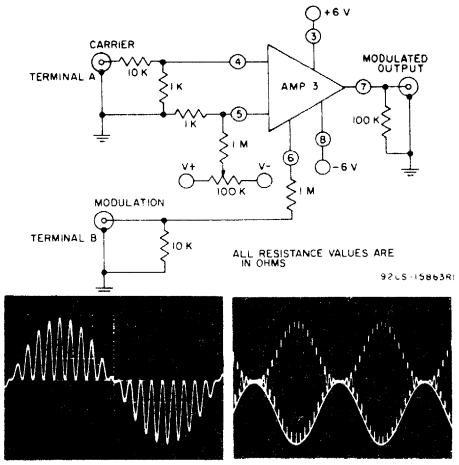


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V^-.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\,(V\text{-}) + V_Y\,]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left|[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right| \quad \text{or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

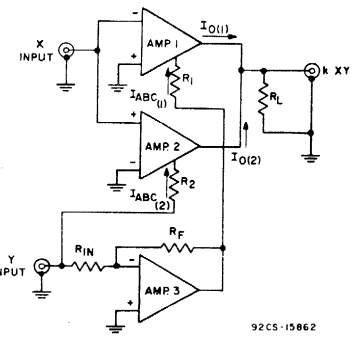


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

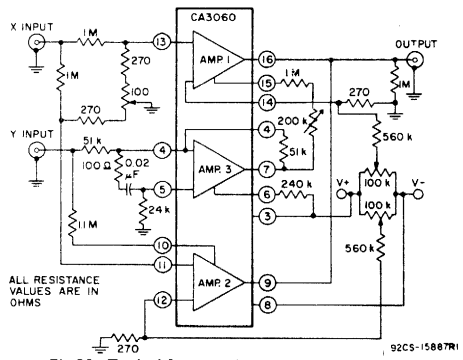


Fig.26—Typical four-quadrant multiplier circuit.

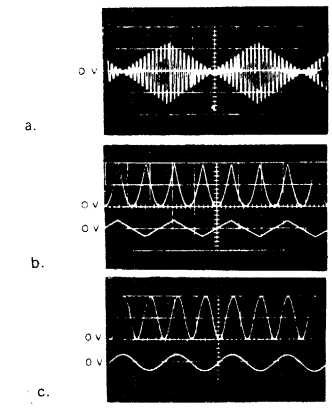


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

CA3062

Photo Detector and Power Amplifier

For Photoelectric Control Applications

Applications

- Counters
- Sorting
- Level controls
- Inspection
- Intrusion alarms
- Position sensor
- Edge monitoring
- Isolators
- **See ICAN-6538, "Applications of the RCA-CA3062 IC Photodetector and Power Amplifier in Switching Circuits"**

Features

- **100 mA output-current capability – can drive a relay or thyristor directly**
- **5 to 15 volt dc supply voltage**
- **Compact – complete system in a TO-5 style package**

The CA3062* is an integrated circuit consisting of a photosensitive section, an amplifier, and a pair of high-current output transistors on a single monolithic chip.

The photosensitive section consists of Darlington pairs and affords high sensitivity. The power amplifier has a differential configuration which provides complementing outputs in response to a light input – normally "ON" and normally "OFF". The separate photodetector, amplifier, and high-current switch provide flexibility of circuit arrangement. This feature plus the high current capability of the output section, can now provide the user with a complete system particularly useful in photoelectric control applications utilizing IR emitters and visible-light sources.

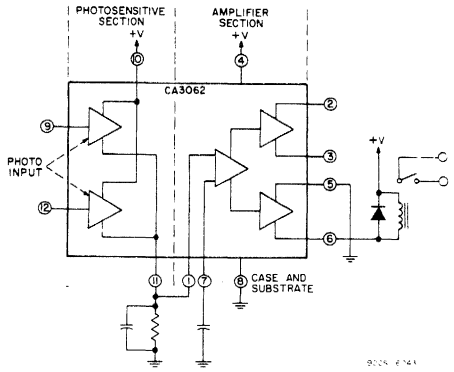


Fig. 1 - Light operated relay using CA3062.

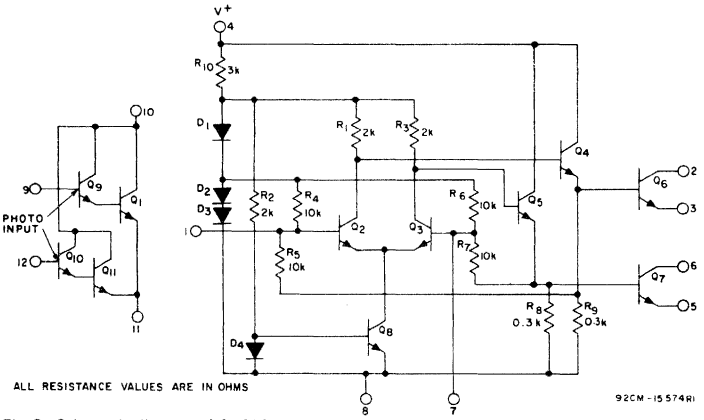


Fig. 2 - Schematic diagram of CA3062.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:
- Up to T_A = 55°C . . . . . 700 mW
- Above T_A = 55°C . . . . . Derate linearly 5.6 mW/°C
- At Case Temperature (T_C) ≤ 55°C . . . . . 1.5 W
- Above T_C = 55°C . . . . . Derate linearly 16 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . -55°C to +125°C
- Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During soldering):
- At distance ≥ 1/32 in (3.17 mm) from seating plane for 10 s max . . . . . +300°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +15 to 0 volts.

TERMINAL No.	10	11	12	1	2	3	4	5	6	7	8
9	0 -9	+2 -5	*	*	*	*	*	*	*	*	*
10		+9 0	+9 0	*	*	*	*	*	*	*	+15 0
11			+5 -2	*	*	*	*	*	*	*	*
12				*	*	*	*	*	*	*	*
1					*	*	*	*	*	+5 -5	+3 -3
2						+15 0	*	*	*	*	+15 0
3							*	*	*	*	+5 0
4								*	*	*	+9 0
5									0 -15	*	+5 0
6										*	+15 0
7											+3 -3
8	Reference Substrate and Case										

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	1	0.1
10	5	0.1
11	0.1	5
12	1	0.1
1	1	0.1
2	100	0.1
3	0.1	100
4	10	1
5	0.1	100
6	100	0.1
7	1	0.1
8	1	10

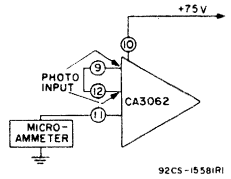


Fig. 3 - Test circuit for photocurrent and typical spectral response of photosensitive Darlington unit.

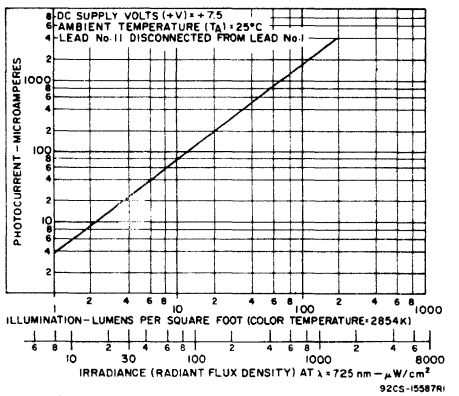


Fig. 4 - Photocurrent as a function of radiant flux.

CA3062

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MEASUREMENT TERMINAL Nos.	TEST CIRCUIT FIG.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC CHARACTERISTICS								
Photo Darlington Section: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	E = 0 lumens/ft^2, I_C = 1 mA	10-11	–	10	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 0.1 mA, E = 0	9-11, 12-11	–	10	–	–	V
Dark Current	I_{DARK}	V_{CE} = 7.5 V, E = 0	10	3	–	0.1	30	μA
Photo Current	I_P	V_{CE} = 7.5 V, E = 8 lumens/ft^2	10	3	–	60	–	μA
Wavelength of Max. Sensitivity	λ max.			3	–	725	–	Note 2 nm
Relative Angular Sensitivity				–	–	–	–	–
Area of Each Photo Transistor				–	1.3 x 10^{-4} cm^2			
Amplifier Section Output Transistor: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO\,6}$ $V_{(BR)CEO\,7}$	I_C = 1 mA	2-3, 6-5	–	15	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO\,6}$ $V_{(BR)EBO\,7}$	I_E = 1 mA	3-8, 6-8	–	5	–	–	V
DC Supply Current	I_{SUPPLY}	V_4 = 7.5 V	4	–	–	5.5	10	mA
Sensitivity: Illumination, For Normal "OFF" Output	E_{ON}	Set light input for I_6 = 70 mA	6	7, 15, 17	–	8	70	Notes 1, 3 lumens per ft^2
For Normal "ON" Output	E_{OFF}	Set light input for I_2 = 5 mA	2	17	–	10	–	Notes 1, 3 lumens per ft^2
DYNAMIC CHARACTERISTICS								
Overall Response Time: Turn-On Time	t_{on}	E = 700 μW/cm^2 at λ = 930 nm	—	12	–	38	–	μs
Rise Time	t_r				–	125	–	μs
Turn-Off Time	t_{off}				–	43	–	μs
Fall Time	t_f				–	20	–	μs

NOTES

(1) Tungsten filament light source at a color temperature of 2854K.
(2) One (1) nanometer = 10 Angstrom units.
(3) A radiant flux density of 7.5 μW/cm^2 at 725 nm produces the same photocurrent as 1 lumen/ft^2 from a tungsten filament lamp at a color temperature of 2854K.

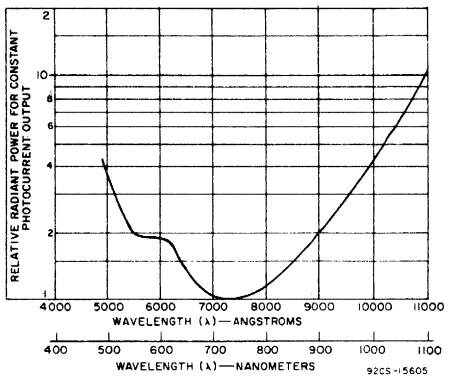


Fig. 5 - Typical spectral response of photosensitive Darlington unit.

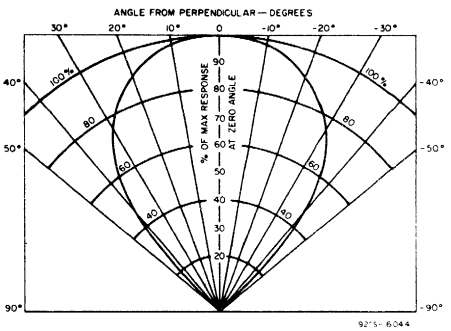


Fig. 6 - Relative angular sensitivity.

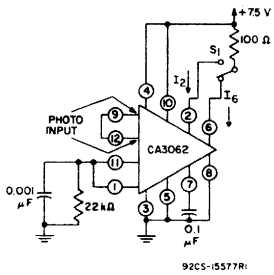


Fig. 7 - Test circuit for sensitivity and dc current measurement.

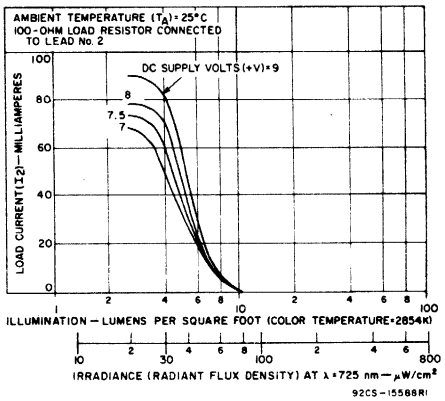


Fig. 8 - Load current (I_2) vs. illumination as a function of supply volts.

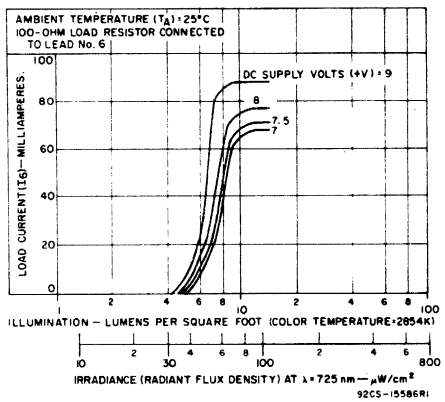


Fig. 9 - Load current (I_6) vs. illumination as a function of supply volts.

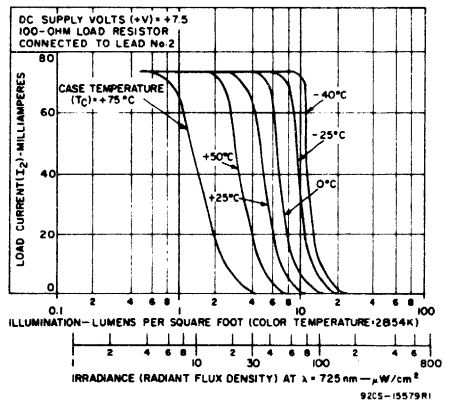


Fig. 10 - Load current (I_2) vs. illumination as a function of case temperature.

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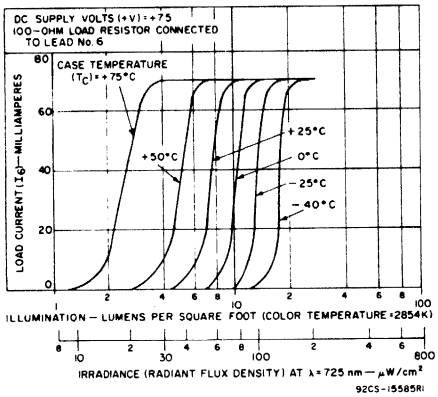


Fig. 11 - Load current (I_G) vs. illumination as a function of case temperature.

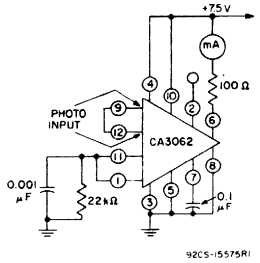


Fig. 12 - Response time test circuit.

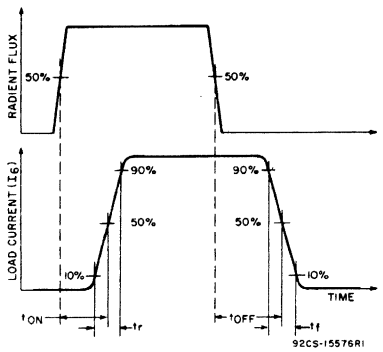


Fig. 13 - Waveforms for measurement of response time.

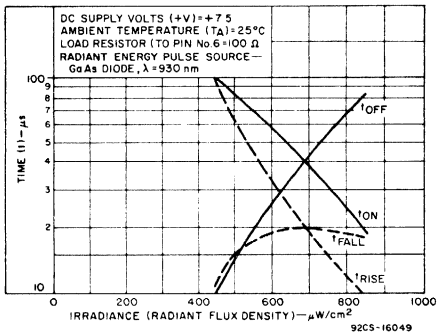


Fig. 14 - Response time as a function of radiant flux density.

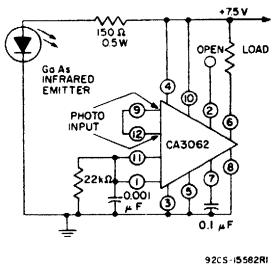


Fig. 15 - Circuit diagram for "ON-OFF" photoelectric control applications.

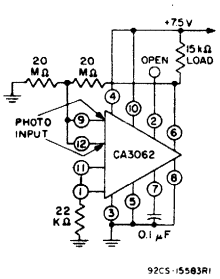


Fig. 16 - Circuit diagram for linear output photoelectric applications.

OPERATING CONSIDERATIONS

Switching Service

The CA3062 is primarily intended to provide "ON-OFF" output in response to a light signal. Optimum performance of this device is achieved when the output transistors are operated at values of load current sufficient to saturate the device in the "ON" state. Operation of the CA3062 at values of load current between the condition of no load current and saturation will cause substantial power to be dissipated in the silicon chip. This condition of operation is therefore not recommended because the heat rise in the silicon chip induced by the increased power dissipation causes the load current to shift in the same direction as though additional illumination were applied to the CA3062, a condition which will substantially alter the switching characteristics of the device.

The signal voltages at the input terminals (terminal No. 1 and No. 7) must not exceed 3 volts, because any increase in the signal voltage beyond the value specified will cause both output transistors to be turned "ON". In the circuit shown in Fig. 7, this condition will occur for values of illumination greater than 60 lumens/ft ^{2}. This adverse operating condition can be avoided by either limiting the maximum illumination or by clamping the input so that the voltage does not exceed 3 volts.

Linear Service

The CA3062 can be connected as shown in Fig. 16 to give a linear output. The value of the load resistor should be greater than 1000 ohms in order to limit the power dissipation and thus minimize the heating effects. Because of the many possible variations in circuit configurations, the CA3062 has not been characterized for linear service applications. A guide-line circuit for this class of service is shown in Fig. 16.

Specific inquiries for use of the CA3062 in this type of service should be addressed to your local RCA Field Technical Representative.

Precautions

Because of the high amplification of the CA3062, care should be taken, when wiring, to keep all lead lengths as short as possible. A recommended breadboard layout is shown in Fig. 17.

If the CA3062 is operated with an inductive load impedance, such as a relay, it is recommended that a diode be connected across the load to absorb the energy of the pulse voltages generated during switching.

Many of the graphs are shown with two sets of abscissa values for light energy input, one expressed in illumination values (lumens/sq. ft.) and the other in irradiance values (μW/sq. cm.)

Correlation between these two sets of abscissa values is accomplished by having the light source operating at the maximum sensitivity wavelength of the CA3062. See Notes on page three.

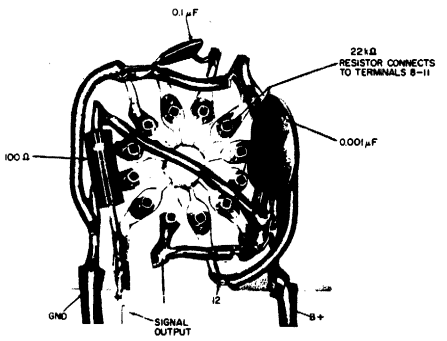


Fig. 17 - Breadboard layout of test circuit, shown in Fig. 7 for the CA3062.

CA3064, CA3064E

TV Automatic Fine Tuning Circuit

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

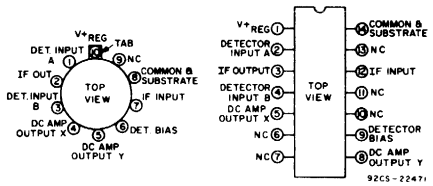
Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

Features:

- **Cascode type high-gain amplifier (18 mV input for rated output)**
- **Internal voltage regulator**
- **Differential detector**
- **For use with either color or monochrome**
- **Differential amplifier**
- **Bipolar outputs**
- **Wide operating-temperature range; −55 to +125°C**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DEVICE DISSIPATION:
Up to T_A = 25°C . . . . . 700 mW
Above T_A = 25°C . . . . . derate linearly 5.6 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . . −55 to +125°C
Storage . . . . . −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max.. . . . . 265°C



(a) CA3064 *(b) CA3064E*

Fig.2 – Terminal assignment diagrams.

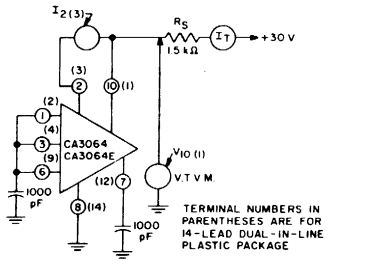


Fig. 3 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).

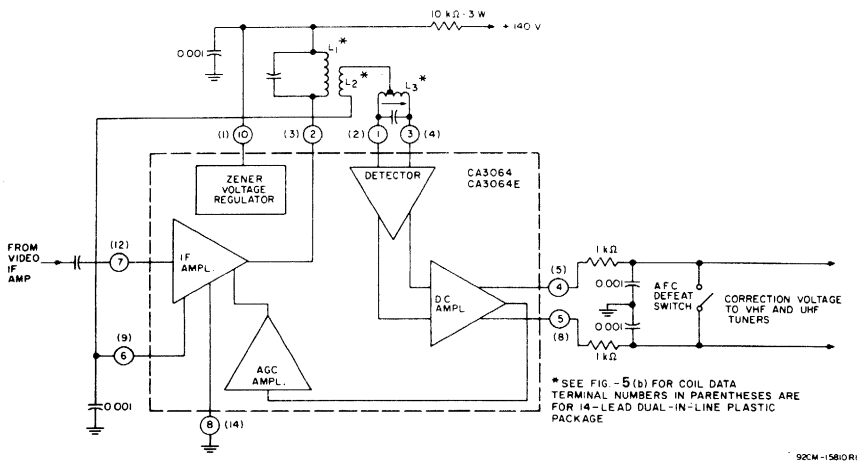


Fig.1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS		LIMITS CA3064, CA3064E MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS									
Device Dissipation	P_D	3	V^+ = 30V, R_S = 1.5kΩ	T_A = −25°C	-	135	150	mW	-
				T_A = +25°C	130	140	150		-
				T_A = +85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	3	$V_{10(1)}$ = 10.5 V		4	6.5	9.5	mA	-
Zener Regulated Voltage – DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	3			10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	3			1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-	V^+ = 30 V, R_S = 1.5 kΩ		5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-			5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-			-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)									
Input Voltage Sensitivity	V_I sensitivity	5	V^+ = +30 V, V_I = 18 mV		Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz, V^+ = 30 V, R_S = 1.5 kΩ		-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-			-	0 +j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-			-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-			-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC									
Correction-Control Voltage at Terminal 4(5)	$V_{corr.\ 4(5)}$	5	V^+ = +30 V, V_I = 18 mV RMS, f_0 = MHz as indicated	45.750 - 0.030	85	-	-	V	6,7
				45.750 + 0.030	-	-	25	V	
				45.750 - 0.900	80	-	-	V	7
				45.750 + 0.900	-	-	35	V	
				45.750 - 1.500		-	80	V	
				45.750 + 1.500	35	-		V	
Correction-Control Voltage at Terminal 5(8)	$V_{corr.\ 5(8)}$	5		45.750 - 0.030	-	-	25	V	6,7
				45.750 + 0.030	85	-	-	V	
				45.750 - 0.900	-	-	35	V	7
				45.750 + 0.900	80	-	-	V	
				45.750 - 1.500	35	-	-	V	
				45.750 + 1.500	-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

CA3064, CA3064E

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 (3) and horizontal terminal 6 (9) is +20 to 0 volts. Terminal nos. in parentheses are for the 14-lead dual-in-line plastic package.

TERMINAL No.	9(6,7, 10,11, 13)	10 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (8)	6 (9)	7 (12)	8 (14)
9(6,7,♦ 10,11, 13)	← NO INTERNAL CONNECTION →									
10 (1)			+12 0	+10 -10	+12 0	+12 0	+12 0	+10 0	+20 0	▲
1 (2)				*	+10 - 10	*	*	+5 - 5	*	+5 - 6
2 (3)					*	*	*	+20 0	*	+20 0
3 (4)						*	*	+5 - 6	*	+5 - 6
4 (5)							*	*	*	+12 0
5 (8)								*	*	+12 0
6 (9)									+5 - 2	+2 0
7 (12)										+2 - 10
8 (14)										REF. SUBSTRATE & CASE■

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9(6,7, 10,11, 13)	-	-
10 (1)	50	50
1 (2)	1	0.1
2 (3)	20	20
3 (4)	1	0.1
4 (5)	5	5
5 (8)	5	5
6 (9)	5	5
7 (12)	1	1
8 (14)	50	50

▲ Terminal number 10 (1) may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor — provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♦ It is recommended that unused terminals 6,7,10,11, and 13 on the 14-lead dual-in-line-plastic package and terminal 9 on the TO-5 package be grounded to act as shields.

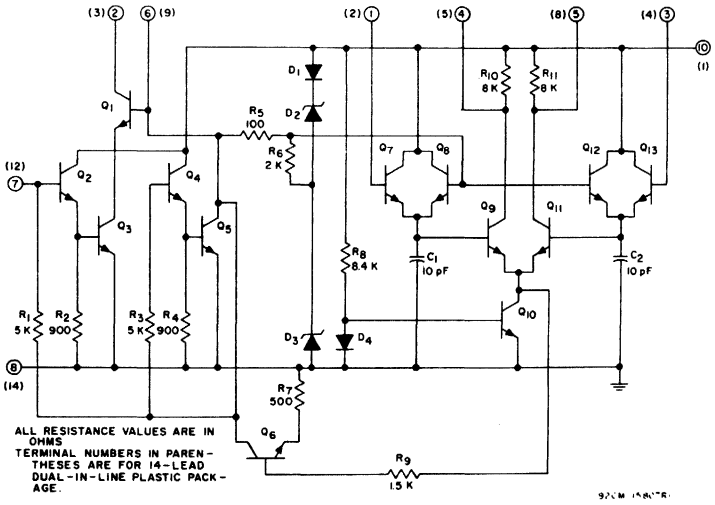
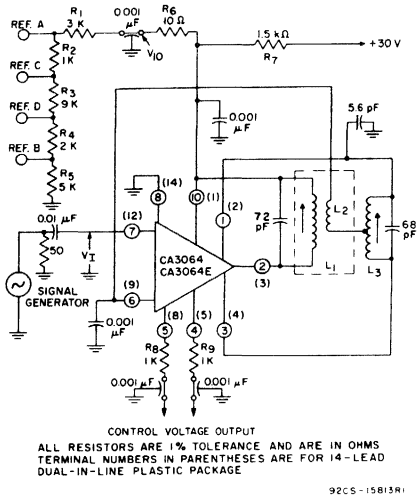


Fig.4 — Schematic diagram for CA3064 and CA3064E.



REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of $V_{10(1)}$
Ref. B	25% of $V_{10(1)}$
Ref. C	80% of $V_{10(1)}$
Ref. D	35% of $V_{10(1)}$

Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

Fig.5 (a) — Correction voltage test circuit for CA3064 and CA3064E.

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 — Discriminator Primary: 3-1/6 turns; #20 Enamel-covered wire — close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at terminal #6; finish at Terminal #1. See Notes below.

L_2 — Tertiary Windings: 2-1/6 turns; #20 Enamel-covered wire — close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 — Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5; connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; —0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

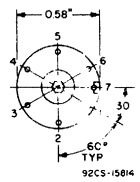


Fig.5 (b) Coil form base terminal diagram.

CA3065

IF AMPLIFIER-LIMITER, FM DETECTOR, ELECTRONIC ATTENUATOR, AUDIO DRIVER

For Television Sound-System Applications

The RCA CA3065 Television Sound System is a monolithic integrated circuit which combines a multistage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an npn power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device into suitably punched printed-circuit boards.

FEATURES:

- Electronic attenuator - replaces conventional volume control
- Differential peak detector - requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection - 50 dB typ. at 4.5 MHz
- Low harmonic distortion
- High sensitivity - 200 μV limiting (knee) at 4.5 MHz
- Audio drive capability - 6 mA p-p
- Undistorted audio output voltage - 7 V p-p

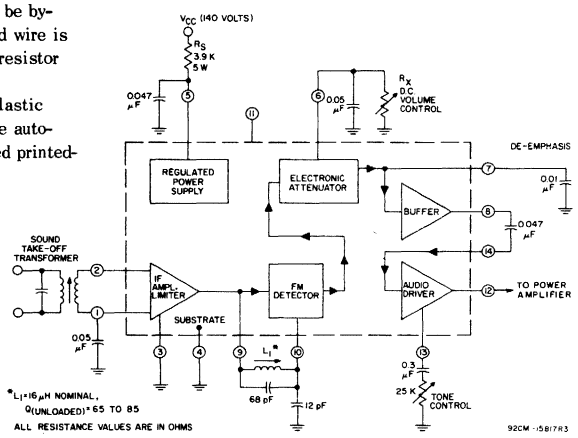


Fig. 1 - Block diagram of CA3065 in a typical circuit application.

MAXIMUM RATINGS, *Absolute Maximum Values*, at T_A = 25°C

Input Signal Voltage (between Terminals 1 and 2)	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25°C	850	mW
Above T_A = 25°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 -5
7					+1 -4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 -5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 -1	*	*	*	*
13											*	*	*	*
14												*	*	+3 -5
1													+5 -5	+5 -5
2														+4 -5
3														

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
4	SUBSTRATE: CONNECT TO TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.

CA3065

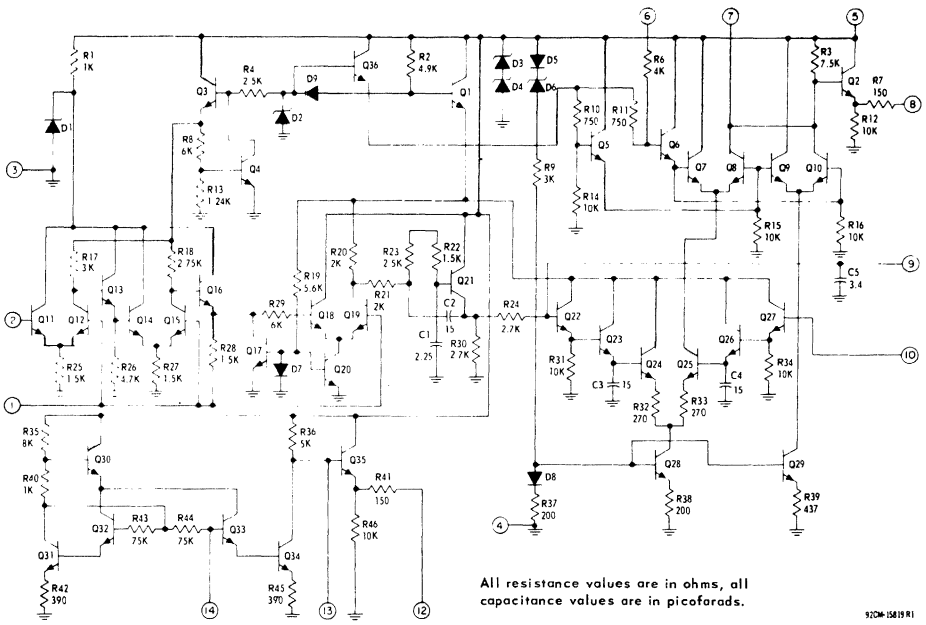


Fig. 2 - Schematic diagram of CA3065

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

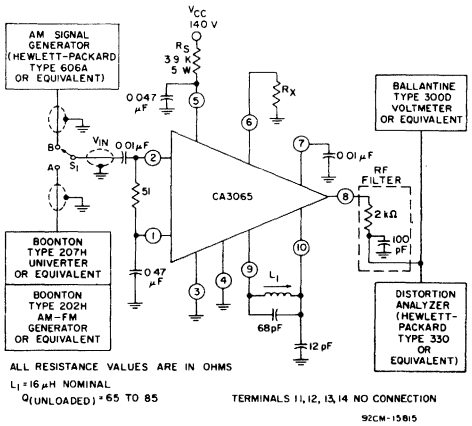


Fig. 3 - Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.

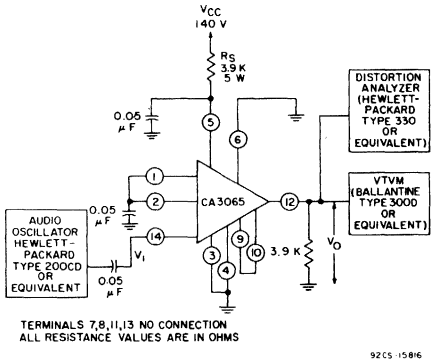
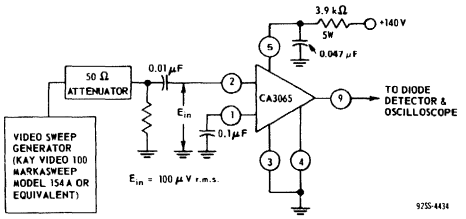
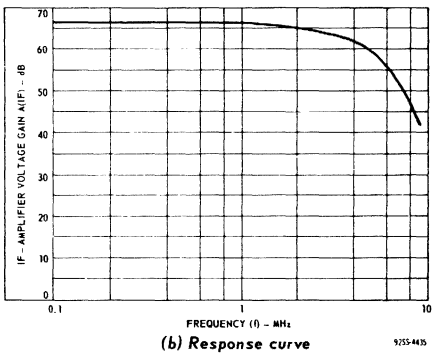


Fig. 4 - Audio voltage gain (undistorted output) test circuit.



(a) Test circuit



(b) Response curve

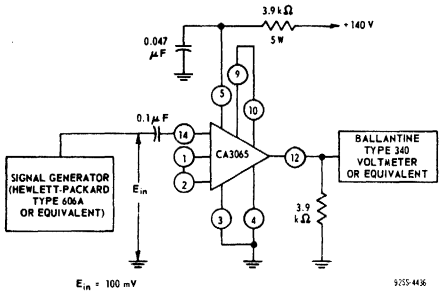
Fig. 5 - Frequency response of IF-amplifier section of CA3065

ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V_{CC} = +140 V applied to Terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_x) = 0 unless otherwise indicated.*

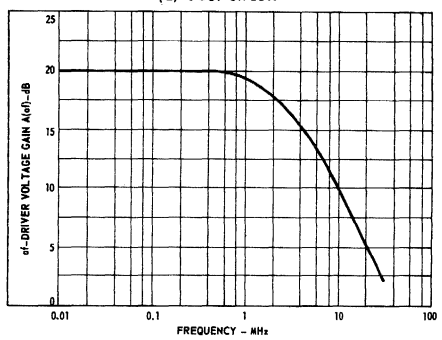
CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics						
Zener Regulating Voltage Terminal No. 5	V_5		10.3	11.2	12.2	V
Current into Terminal 5	I_5	Connect Terminal 5 to +9 V	10	16	24	mA
Total Device Dissipation	P_T		343	370	400	mW
Terminal Voltages: 1	V_1		–	2	–	V
6	V_6		–	4.8	–	
7	V_7		–	6.1	–	
9	V_9		–	3.7	–	
12	V_{12}		4	5.1	5.8	
Dynamic Characteristics						
IF AMPLIFIER Input Limiting Voltage (at −3 dB point)	$V_{i(lim)}$	f_0 = 4.5 MHz, f_m = 400 Hz, Deviation = ±25 kHz,	–	200	400	μV
AM Rejection	AMR	Amplitude Modulation 30% f = 4.5 MHz	40	50	–	dB
Transconductance Magnitude	$\|G_m\|(IF)$	f = 4.5 MHz IF Input Terminals: 2, 1	–	500	–	mmho
Phase Angle	$\theta(IF)$	IF Output Terminals: 9, 3	–	46	–	degrees
Feedback Capacitance	C_{fb}	f = 1 MHz; Terminals 2 and 9	–	0.02	–	pF
Input Impedance Components: Parallel Input Resistance	$R_i(IF)$	Measured between Terminal Nos. 1 and 2	–	17	–	kΩ
Parallel Input Capacitance	$C_i(IF)$	f = 4.5 MHz	–	4	–	pF
Output Impedance Components: Parallel Output Resistance	$R_o(IF)$	Measured between Terminal No. 9 and gnd	–	3.25	–	kΩ
Parallel Output Capacitance	$C_o(IF)$	f = 4.5 MHz	–	7.5	–	pF
DETECTOR Recovered AF Voltage	$V_o(af)$	f = 4.5 MHz; V_i = 100 mV f = ±25 kHz	0.5	0.75	–	V(rms)
Total Harmonic Distortion	THD	fm = 400 Hz	–	0.9	2	%
Output Resistance: Terminal 7	R_o		–	7.5	–	kΩ
Terminal 8			–	300	–	Ω
ATTENUATOR		See Fig. 7				
Max. Attenuation	–	R_X = ∞	60	80	–	dB
Max. "Play-through" Voltage*	–	R_X = ∞	–	0.075	1	mV
AUDIO AMPLIFIER Voltage Gain	A(af)	V_i = 0.1 V(rms), f = 400 Hz	17.5	20	–	dB
Total Harmonic Distortion	THD	V_O = 2 V(rms), f = 400 Hz	–	1.5	–	%
Undistorted Output Voltage	–	THD = 5%, f = 400 Hz	2	2.5	–	V(rms)
Input Resistance	$R_i(af)$	f = 400 Hz	–	70	–	kΩ
Output Resistance	$R_o(af)$	f = 400 Hz	–	270	–	Ω

*"Playthrough" voltage is the unwanted signal, measured at Terminal 8, when the volume control is set for minimum output.

CA3065



(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

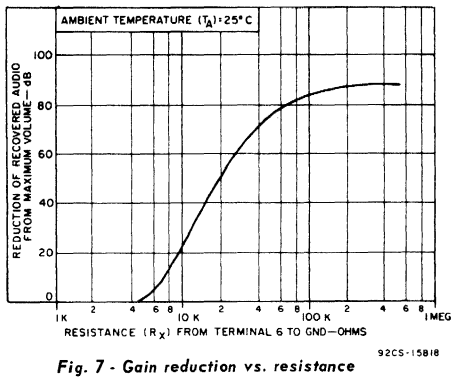


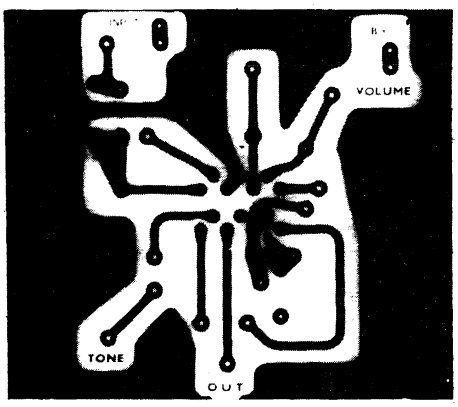
Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)

OPERATING CONSIDERATIONS

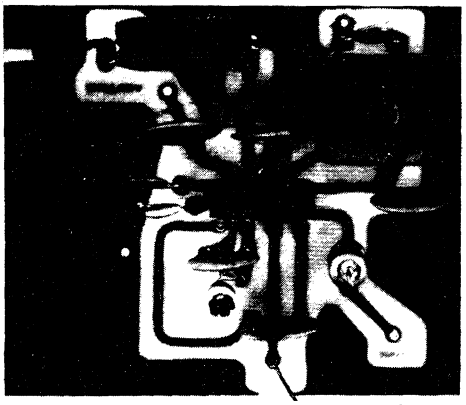
The CA3065 may be used to drive a video output transistor or a high-transconductance output tube.

As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150 k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.



*(a) Printed circuit board – bottom view**



*(b) Parts layout – top view**

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

CA3066, CA3067

Television Chroma System

The RCA CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

CA3066 CHROMA SIGNAL PROCESSOR

The CA3066 contains substantially all the color processing circuitry exclusive of the tint control and demodulating circuits. The chroma amplifier sections of the CA3066 consist of the chroma and bandpass amplifiers. The chroma amplifier receives the chroma input signal at terminal No. 1. This amplifier is gain controlled by the automatic chroma control (ACC) detector-amplifier. The chroma signal is internally coupled from the output of the chroma amplifier to the input of the chroma bandpass amplifier and burst separator amplifier. The horizontal keying pulse (+8V) is used to gate the burst portion of the chroma signal from the input of the bandpass amplifier to the input of the burst separator amplifier. The bandpass amplifier is gain controlled by the dc chroma gain control and can also be controlled by the killer detector-amplifier. The bandpass amplifier output is internally coupled to the chroma output amplifier stage of the CA3066. The coils of the chroma amplifier and the bandpass amplifier are stagger-tuned to provide a combined typical bandpass of 3.08 to 4.08 MHz. The burst separator amplifier injects the burst signal into the 3.58 MHz oscillator. The oscillator amplitude is dependent on the terminal No. 9 impedance to ground and is also responsive to the burst signal amplitude at terminal No. 11. The ACC detector and killer detector sense the burst level or absence of burst, respectively, by monitoring the oscillators response to the burst injection level. The thresholds for the ACC and killer are independently adjusted by resistors R2 and R1 at terminals No. 9 and No. 4, respectively. The chroma output is at terminal No. 14 and the oscillator output is at terminal No. 8. Terminal No. 6 is a zener diode for use as a regulated voltage reference at 11.9 volts. When the zener reference element is not used, the power supply voltage should be maintained at 11.2 ± 0.5 volts.

System Features

CA3066
CHROMA SIGNAL PROCESSOR

- Complete Color Sync Circuit
- Blanked Chroma Amplifier
- Chroma Band-Pass Amplifier
- Low Output Impedance Chroma Driver
- ACC Detector-Amplifier
- Killer Detector-Amplifier
- DC Chroma Gain Control
- Zener Diode for Regulated Voltage Reference
- Short-Circuit Protection on All Terminals

CA3067
CHROMA DEMODULATOR

- Balanced Chroma Demodulators
- Color Difference Matrix
- DC Tint Control
- Three Low Output Impedance Drivers for Direct Coupling
- Reference Subcarrier Limiter
- Zener Diode for Regulated Voltage Reference
- Internal RF Filtering

CA3066

ELECTRICAL CHARACTERISTICS at T_A = 25°C and V^+ = 11.2 V

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
ACC Reference	V_2		–	0.5	–		
Burst-Chroma Ampl. Bias Current Term.	V_3		–	2.9	–		
Killer Reference	V_4		–	1.0	–		
Zener Reg. Reference	V_6		10.6	11.9	12.6	V	2
Oscillator Input	V_7		–	1.4	–		
Oscillator Output	V_8		–	2.35	–		
Balance (ACC Control)	V_9		–	1.65	–		
Chroma Output	V_{14}		–	4.6	–		
Currents:							
Total Supply	I_5		14	24	33		
Burst Separator Output	I_{11}	S_1 Closed	–	6.5	–	mA	
Band-Pass Ampl. Output	I_{13}		–	4.8	–		
Chroma Ampl. Output	I_{16}		–	1.27	–		
Dynamic Characteristics							
Oscillator Output	v_8	v_1 = 0 v_{p-p} v_1 = 1.25 v_{p-p}	0.8 –	1.2 2.5	– 3.5	v_{p-p}	4
Chroma Output:							
100%	v_{14}	v_1 = 1.25 v_{p-p}	0.5	1.0	–	v_{p-p}	3, 4
Killed		v_1 = 0.025 v_{p-p}	–	–	12		
ACC Detector Output	v_2	v_1 = 1.25 v_{p-p}	–	0.9	–	V	4
Small-Signal Input Resistance (Term. No.1)	r_i		–	50	–	kΩ	–
Small-Signal Input Capacitance (Term. No.1)	c_i		–	2.4	–	pF	
Small-Signal Output Impedance (Term. No.14)	r_o		–	250	–	Ω	

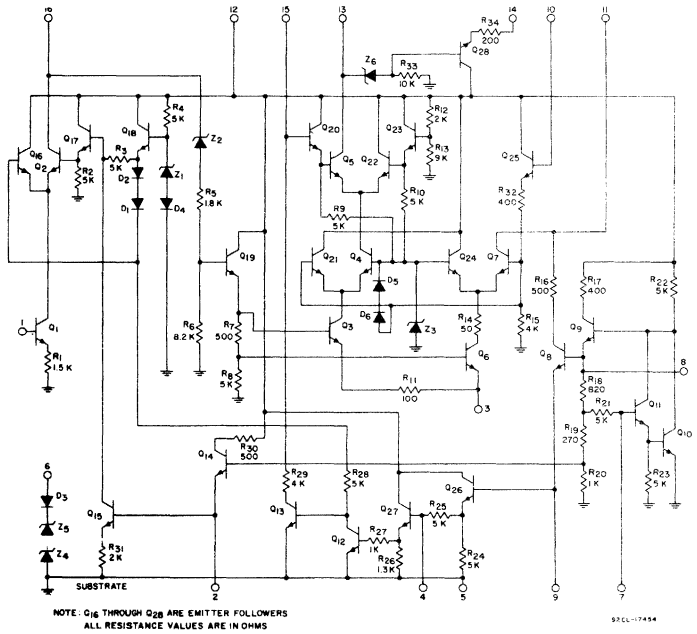


Fig. 1 - CA3066 schematic diagram.

CA3066

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Supply Voltages and Currents (see charts below)

Device Dissipation:
Up to T_A = 70°C . . . . . 600 mW
Above T_A = 70°C . . . . derate linearly 7.7 mW/°C

Ambient Temperature Range:
Operating . . . . . −40 to +85 °C
Storage . . . . . −65 to +150 °C

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 °C

Voltage with respect to Terminal No. 5.

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	See Note N1	
7	–	–
8	–	–
9	—	–
10	−5.0	N2
11	0.0	18.0
12	0.0	12.0
13	0.0	15.0
14	–	–
15	0.0	N2
16	0.0	15.0
1	−5.0	5.0
2	–	–
3	–	–
4	–	–

Current

Terminal No.	I_I mA	I_O mA
6	20	0.1
7	5	0.1
8	1	2
9	0.1	2
10	1	0.1
11	10	1
12	50	1
13	10	1
14	0.1	6
15	3	1
16	6	1
1	1	0.1
2	0.1	2
3	0.1	20
4	1	1

N1 Terminal No. 6 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 6.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 12.

CA3066, CA3067

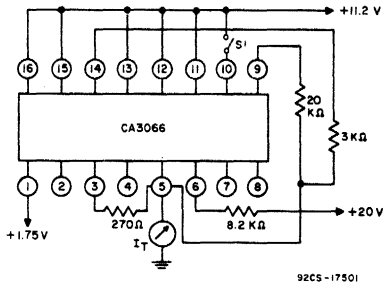


Fig. 2 - Static characteristics test circuit for CA3066.

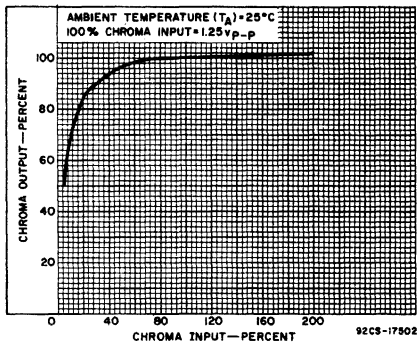


Fig. 3 - Typical ACC characteristic of chroma output vs chroma input for CA3066.

CA3067 CHROMA DEMODULATOR

The CA3067 contains the separate functional systems of a dc tint control and a demodulator. The phase shift of the tint amplifier system is accomplished by functional control of the fixed phase signal from the CA3066 oscillator output. This regenerated reference subcarrier is applied to terminal No. 3 and driven differentially into phase shift circuits. The tint adjustment controls the vector addition of phase shifted signals after which a limiting amplifier removes any remaining amplitude modulation. The output of the tint amplifier at terminal No. 1 is phase separated for the required reference subcarrier phase at terminal No. 6 and No. 12 (terminal No. 12 lags terminal No. 6 by approximately 76°). These terminals are inputs to the demodulator drive amplifiers. The demodulators consist of two sets of balanced detectors which receive their reference subcarrier from the demodulator drive amplifiers. The chroma signal input from the CA3066 is applied to terminal No. 14. The chroma signal differentially drives the demodulators. The demodulation components are matrixed and dc-shifted in voltage to give R–Y, G–Y, and B–Y color difference components with close dc balance and proper amplitude ratios. The output amplifiers of the CA3067 are specially designed to meet the low-impedance driving source requirements of the high-level color output amplifiers. A special feature of the CA3067 is R–C filtering of high frequency demodulation components. Terminal No. 4 is a zener diode for use as a regulated voltage reference at 11.9V. When the zener reference element is not used, the power supply should be maintained at +11.2 ±0.5 volts.

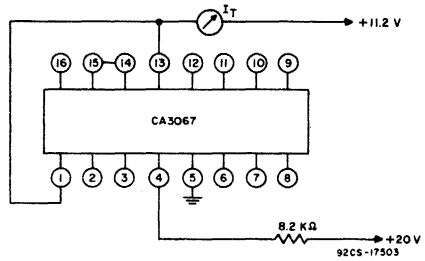


Fig. 5 - Static characteristics test circuit for CA3067.

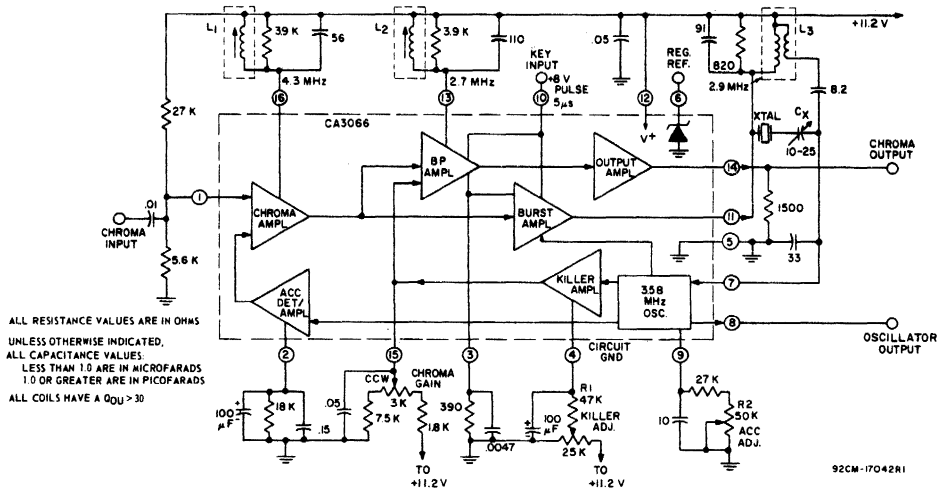


Fig. 4 - Dynamic characteristics test circuit for CA3066.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input ($v_1 = 0$)

1. Adjust ACC potentiometer for $V_2 = +0.65V$.
2. Adjust Killer potentiometer for $V_4 = +1.2V$.
3. Adjust capacitor C_X (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μs "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (v_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (v_{14}) is the same as the chroma input (v_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (v_8) is the CW output at terminal No. 8 and is in peak-to-peak volts. Some modulation of oscillation dampening between burst injection is visible.

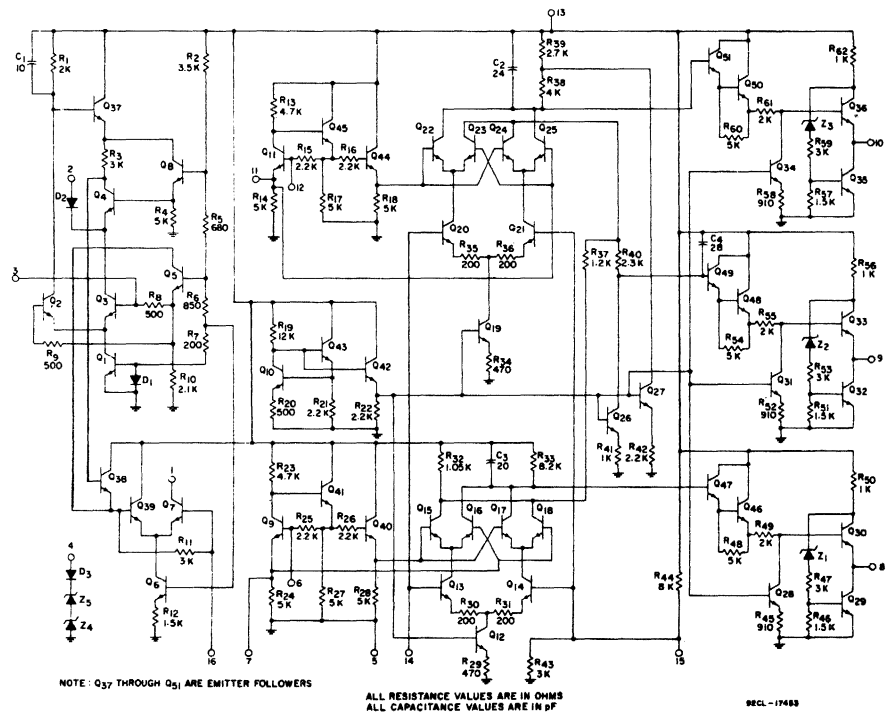


Fig. 6 - CA3067 schematic diagram.

CA3066, CA3067

ELECTRICAL CHARACTERISTICS at T_A = 25°C and V^+ = 11.2 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
Tint Control Input	V_2	I_2 = 0.25 mA	–	3.5	–		
Reference Subcarrier	V_3		–	2.1	–		
Zener Regulator Ref.	V_4		10.6	11.9	12.6	V	9
B–Y, R–Y Oscillator Ref. Inputs	V_6, V_{12}		–	5.7	–		
Balance (B–Y, R–Y)	V_7, V_{11}		–	5.0	–		
B–Y, G–Y, R–Y Outputs	$V_{8, 9, 10}$		4.2	5.0	5.8		9, 11, 12
Difference Outputs*	ΔV_8, ΔV_9, ΔV_{10}		–0.3	–	0.3		9
Chroma Inputs	V_{14}, V_{15}		–	3.0	–		
Tint Ampl. Balance	V_{16}		–	4.7	–		
Currents:							
Tint Ampl. Output (min.)	I_1(min.)	V_{16} = 8 V	0.16	0.37	–	mA	
Total Supply	$I_1 + I_{13}$		15	24	33		
Dynamic Characteristics							
Tint Amplifier Output							
Sensitivity	V_1	V_3 = 7 mV (RMS)	160	250	–	mV (RMS)	
Limiting Knee		V_3 = 35mV (RMS)	–	300	–		
Limiting		V_3 = 350mV (RMS)	–	–	380		
Tint Ampl. Phase Ref.▲	ϕ_6	V_3 = 70mV (RMS)	185	220	235	deg.	
Tint Ampl. Phase Shift‡	$\Delta\phi_6$	V_3 = 70mV (RMS)	90	105	–	deg.	
Demodulated Chroma Output:							
R–Y	V_{10}	V_3 = 70mV (RMS) V_{14} = 35mV (RMS)	150	250	–	V(RMS)	10
Ratio of G–Y to R–Y	V_9/V_{10}		0.28	0.36	0.44		
Ratio of B–Y to R–Y	V_8/V_{10}		1.0	1.2	1.4		
Color Difference Output BW at 3.3 dB	$BW_{Diff.}$		450	550	–	kHz	
Color Difference Outputs (max. input signals):							
R–Y	v_{10}	V_3 = 70mV (RMS) V_{14} = 212mV (RMS)	–	3.0	–	$v_{p\text{-}p}$	
G–Y	v_9		–	1.1	–		
B–Y	v_8		–	3.6	–		
Small Signal Input Resistance							
Terminal No. 3	r_i		–	550	–	Ω	
Terminal Nos. 6 & 12			–	22	–		
Small Signal Output Resistance							
Terminal Nos. 8, 9, & 10	r_o		–	5	–		

*$\Delta V_8 = V_8 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$, $\Delta V_9 = V_9 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$, $\Delta V_{10} = V_{10} - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$

▲ Terminal No. 3 is phase reference

‡ read phase shift as tint control is varied

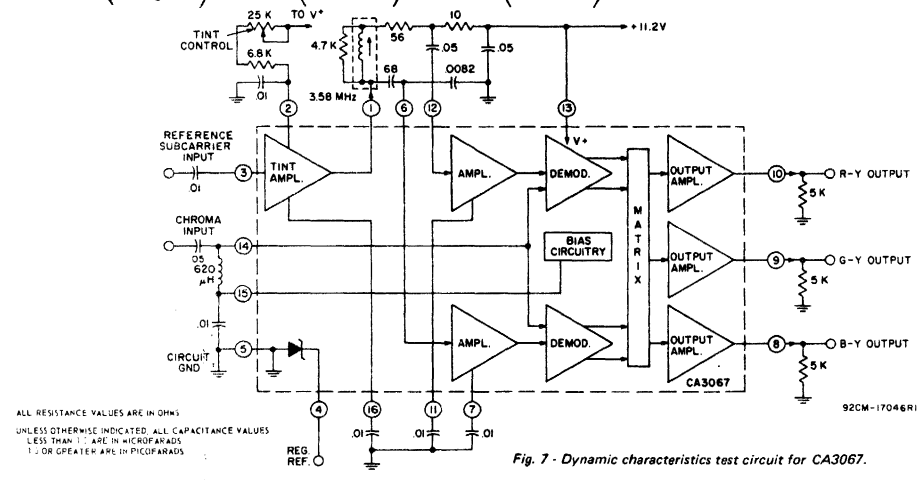


Fig. 7 - Dynamic characteristics test circuit for CA3067.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

1. The reference subcarrier input (v_3) is a 3.58 MHz CW signal from a 50Ω source.
2. The chroma input (v_{14}) is a 3.53 MHz CW signal from a 50Ω source.
3. Phase and amplitude at terminal Nos. 1, 3, 6 and 12 are measured with a vector voltmeter (HP8405A or equivalent).
4. Signals at terminal Nos. 8, 9, and 10 are measured with an ac voltmeter (HP400E or equivalent) or an oscilloscope.
5. Unless otherwise noted the Tint control is at maximum resistance.

CA3067

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Supply Voltages and Currents (see charts below)

Device Dissipation:

Up to T_A = 70°C . . . . . 600 mW

Above T_A = 70°C . . . . derate linearly 7.7 mW/°C

Ambient Temperature Range:

Operating . . . . . –40 to +85 °C

Storage . . . . . –65 to +150 °C

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 °C

Voltage with respect to Terminal No. 5

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	0	N2
7	0	N2
8	0	N2
9	0	N2
10	0	N2
11	0	N2
12	0	N2
13	0	12
14	–3	N2
15	0	N2
16	N3	N3
1	0	15
2	0	N2
3	0	5
4	N1	

Current

Terminal No.	I_i (mA)	I_o (mA)
6	3	3
7	3	3
8	20	20
9	20	20
10	20	20
11	3	3
12	3	3
13	50	1
14	1	0.1
15	6	2
16	N3	N3
1	3	3
2	3	0.1
3	3	3
4	20	0.1

N1 Terminal No. 4 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 4.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 13.

N3 Terminal No. 16 should be bypassed for normal operation.

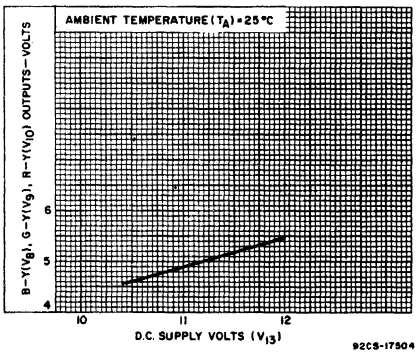


Fig. 8 - DC voltage at color-difference outputs vs supply voltage for CA3067.

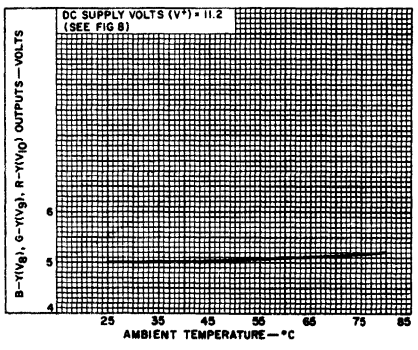


Fig. 9 - Temperature drift of DC voltage at color-difference outputs for CA3067.

CA3068

Television Video IF System

RCA-CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

FEATURES:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 M
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply
- See ICAN-6303, "A Single IC for the Complete PIX-IF System in TV Receivers" for Schematic Diagram

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25°C$*

DC Supply Voltage:		
Between Terminals 15 and 5*	14.3	V
Terminal 7 (Collector to ground)	20	V
Terminal 9 (Collector to ground)	20	V
DC Current (into Terminal 18)	2	mA
Device Dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	− 65 to +150	°C
Lead Temperature (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

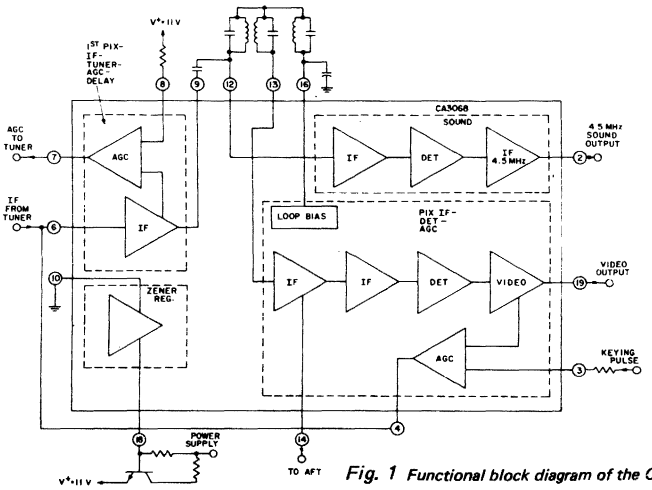


Fig. 1 Functional block diagram of the CA3068.

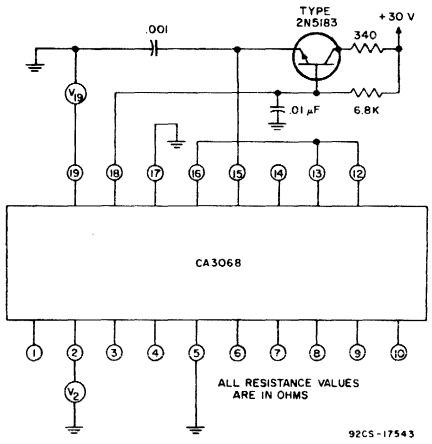
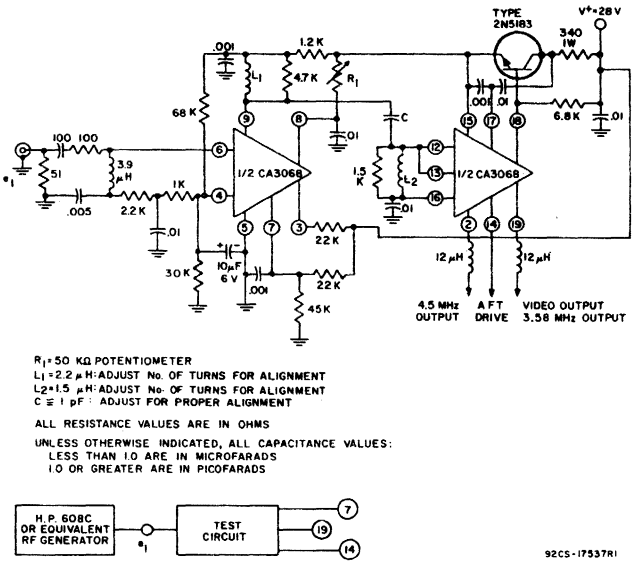
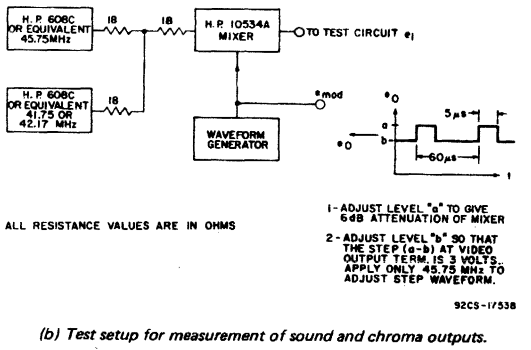


Fig. 2 – Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



(b) Test setup for measurement of sound and chroma outputs.

Fig. 3 – Typical dynamic test circuit diagrams.

CA3068

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	I_{15}	–	15	–	45	mA
DC Voltages:						
Terminal 2 (Sound)	V_2	–	–	6	–	V
Terminal 3 (Keying Input)	V_3	–	6.4	–	10	V
Terminal 7 (1) (AGC)	V_7	–	16	–	21	V
Terminal 7 (2) (AGC)	V_7	–	–	1	–	V
Terminal 8 (AGC Delay)	V_8	–	–	4	–	V
Terminal 9 (Cascode Collector)	V_9	–	–	8.5	–	V
Terminal 16 (Bias)	V_{16}	–	1.1	–	2.3	V
Terminal 18 (Zener)	V_{18}	$V_5 = V_{17} = 0$ V, $I_{18} = 1$ mA	10.6	11.9	13.2	V
Terminal 19 (White Level)	V_{19}	–	6	–	10	V
Dynamic Characteristics						
Video Sensitivity	e_i	f_o = 45.75 MHz, Mod. (AM) = 85% at 400 Hz; Adjust e_i for 4 $V_{p\text{-}p}$ at Term. 19	40	100	200	μV
Sync. Tip Level Voltage	V_{19}	f_o = 45.75 MHz, e_i(CW) = 10 mV	0.4	0.8	1.6	V
Automatic Fine Tuning (AFT) Drive Level Voltage	V_{14}		–	15	–	mV
Delay Bias Voltage:	V_7					
At e_i = 10 mV		f_o = 45.75 MHz, e_i(CW) = 20 mV;	16	–	–	V
At e_i = 30 mV		Adjust R_1 for V_7 = 14 V	0.5	–	2	V
3.58 MHz Chroma Output Voltage	V_{19}	f_o = 45.75 MHz, e_i(step mod.) = 10 mV; f_1 = 42.17 MHz, e_i(step mod.) = 3.33 mV	0.5	0.8	–	V
4.5-MHz Sound Output Voltage	V_2	f_o = 45.75 MHz, e_i(step mod.) = 10 mV; f_2 = 41.25 MHz, e_i(step mod.) = 2.5 mV	50	200	–	mV
Parallel Input Impedance:						
Resistance at Term. 6	R_{I-6}		4	–	–	kΩ
Capacitance at Term. 6	C_{I-6}		–	2	–	pF
Resistance at Term. 12	R_{I-12}	f_o = 45.75 MHz	–	4.5	–	kΩ
Capacitance at Term. 12	C_{I-12}	Impedance and Admittance measured at bias conditions as developed by circuit shown in Fig. 7	–	4	–	pF
Resistance at Term. 13	R_{I-13}		–	5	–	kΩ
Capacitance at Term. 13	C_{I-13}		–	4	–	pF
Parallel Output Impedance:						
Resistance at Term. 9	R_{O-9}		30	–	–	kΩ
Capacitance at Term. 9	C_{O-9}		–	3	–	pF
Cascode Transfer Characteristics: Magnitude of Forward Transadmittance	$\lvert Y_f \rvert$		–	50	–	mmho
Reverse Transfer Capacitance	C_r		–	0.001	–	pF

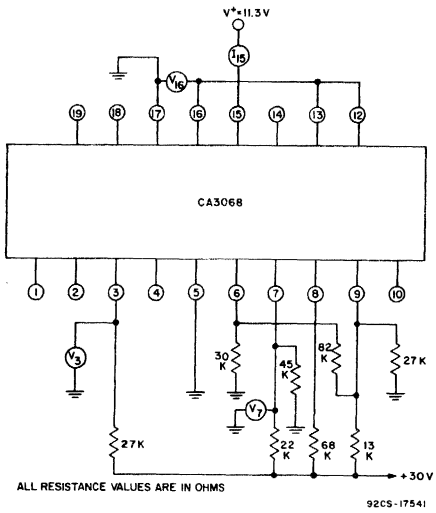


Fig. 4 – Test circuit for measurement of quiescent current (I_{15}), keying terminal voltage (V_3), bias voltage (V_{16}), AGC terminal voltage 1 (V_7), and cascode collector voltage (V_9).

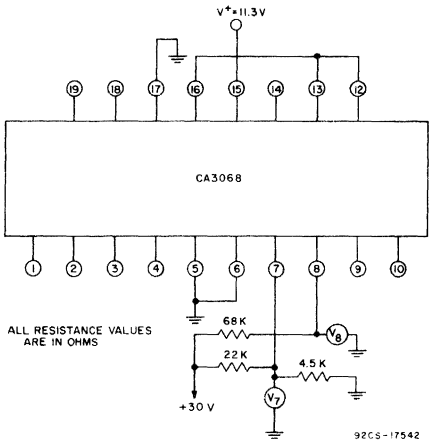


Fig. 5 – Test circuit for measurement of AGC terminal voltage 2 (V_7) and terminal 8 voltage (V_8).

CA3070, CA3071, CA3072

Television Chroma System

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

SYSTEM FEATURES

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

CA3070 Chroma Signal Processor

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage▲			Current		
Terminal No.	Min. Volts	Max. Volts	Terminal No.	I_I mA	I_O mA
1	0	*	1	20	1
2	0	+16	2	–	–
3	0	+16	3	–	–
4	–5	N2	4	20	1
6	–	–	10	N3	1
7	–	–	11	–	–
8	–	–	12	–	–
10	0	N3	13	20	1
11	0	N1	14	20	1
12	0	N1			
13	0	N1			
14	0	N1			
15	0	+16			
16	0	+16			

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.

N1 Regulated voltage at terminal No. 10.

N2 Controlled by max. input current.

N3 Limited by dissipation.

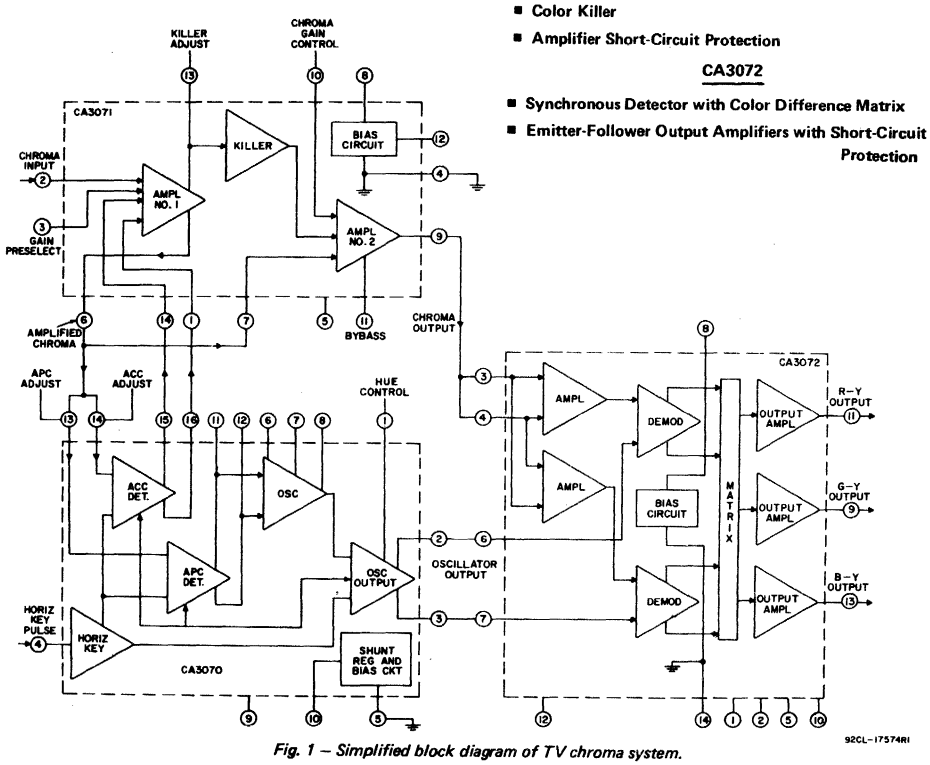


Fig. 1 – Simplified block diagram of TV chroma system.

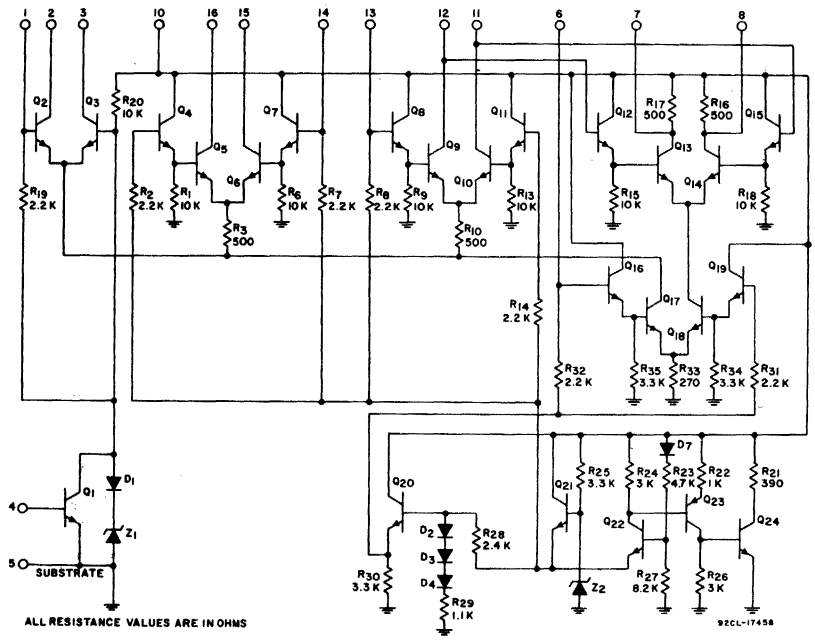


Fig. 2 – Schematic diagram CA3070.

CA3070, CA3071, CA3072

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

Device Dissipation:
- Up to T_A = +70°C ..... 530 mW
- Above T_A = +70°C ... Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
- Operating ..... −40 to +85 °C
- Storage ..... −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/32 in. (3.17 mm) from seating plane for 10 s max. ..... +265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage:							
Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	3c
Oscillator Input	V_6		–	2.8	–	V	3a
APC Input	V_{13}		–	6.5	–	V	3a
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5	V	3a
Regulator Change	V_{10}	V^+ = 27 V	−0.2	–	+0.2	V	3a
Horizontal Key Input	V_4	I_4 = −10 μA	5	—	—	V	3a
Currents:							
Oscillator Output	I_2		–	5.8	–	mA	3c
APC Output	I_{11}, I_{12}		–	1.45	–	mA	3b
ACC Output	I_{15}, I_{16}		–	1.45	–	mA	3b
Dynamic Characteristics							
Oscillator Outputs:							
Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	4
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}	4
ACC Detected Output	$V_{16}-V_{15}$	S_1 in position 1	115	150	–	mV	4
Oscillator Pull-In Range	–		–	±400	–	Hz	4

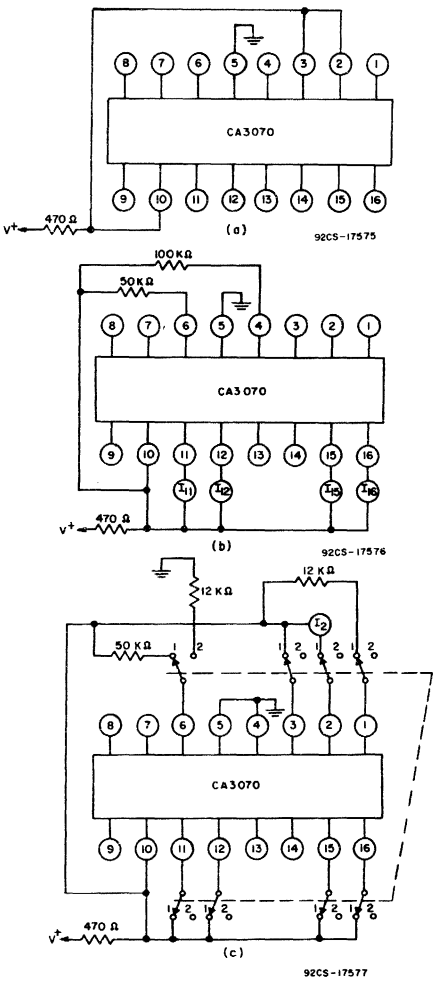


Fig. 3 – Static characteristics test circuits.

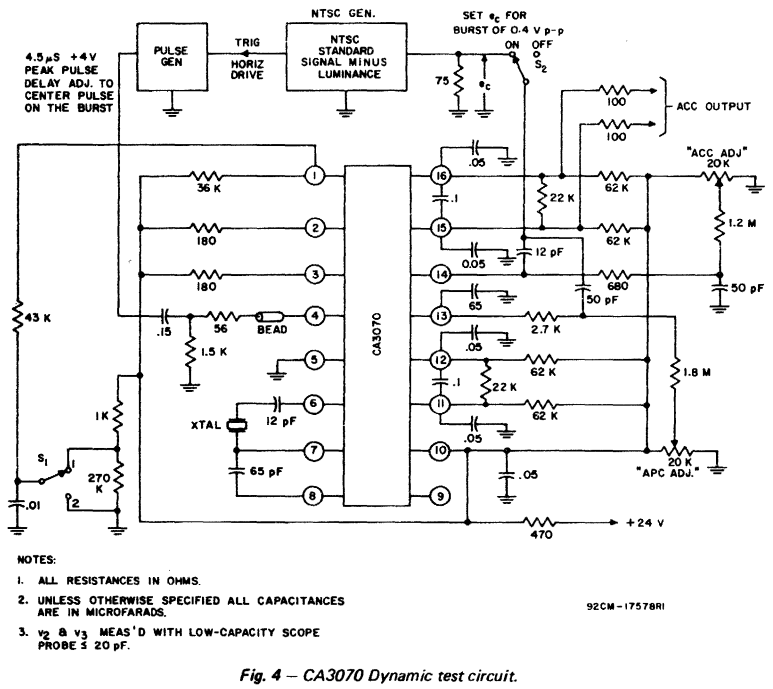


Fig. 4 – CA3070 Dynamic test circuit.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 – 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

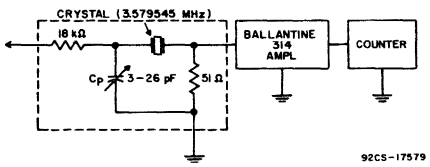


Fig. 5 – Crystal probe for frequency measurements.

CA3070, CA3071, CA3072

CA3071 Chroma Amplifier

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

DC Supply Voltage (Terminal 8 to Terminal 4)	30	VDC
Device Dissipation:		
Up to T_A = +70°C	530	mW
Above T_A = +70°C	Derate Linearly at 6.7	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max.	+265	°C

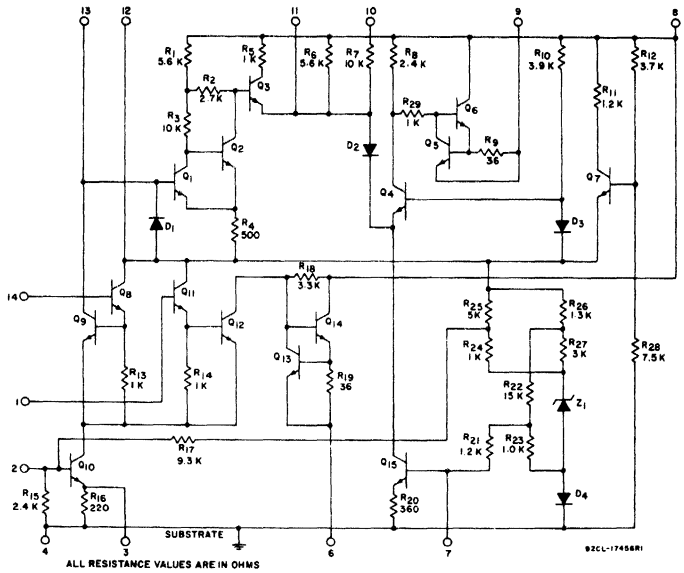


Fig. 6 -Schematic diagram for CA3071.

Maximum Voltage and Current Ratings @ T_A = +25°C

Current			Voltage*		
Terminal No.	I_I mA	I_O mA	Terminal No.	MIN VOLTS	MAX VOLTS
1	5	1.0	1	−5	+15
2	5	1.0	2	−5	+5
3	10	10	3	0	+2
6	1.0	20	6	0	+24
7	5	1.0	7	−5	+5
9	1.0	20	8	0	+30
12	1.0	5	9	0	+24
14	5	1.0	10	0	+24
			11	0	+24
			12	0	+20
			13	0	+20
			14	−5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	TYP.	MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages							
Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	7
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g = 30 mV_{RMS} Measure v_6	14	–	–	dB	8
Amplifier No. 2 Voltage Gain	A_{V2}	V_g = 1.0 V (RMS) Measure v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	11
10% Chroma Gain Control Reference Voltage	V_8-V_{10}	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	8
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9	..	–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	9, 10
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_{i1}		–	2	–	kΩ	8
	c_{i1}		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_{o1}		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_{i2}		–	2.1	–	kΩ	
	c_{i2}		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_{o2}		–	85	–	Ω	

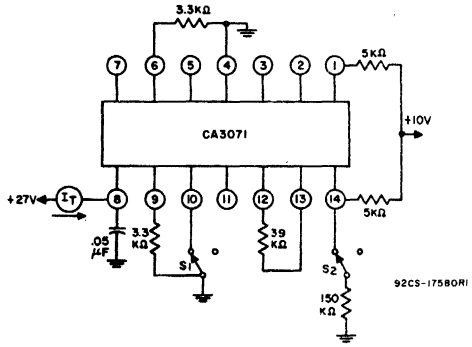


Fig. 7 - Static characteristics test circuit–CA3071.

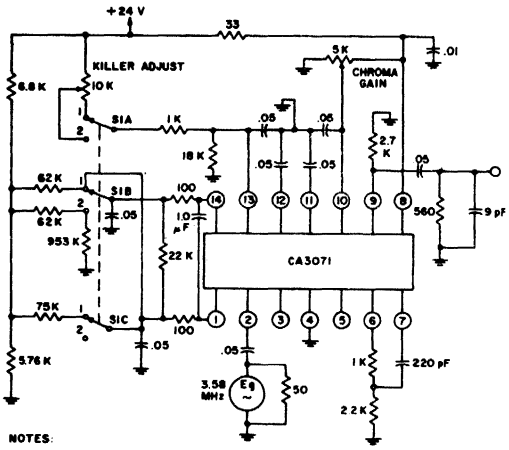


Fig. 8 – Dynamic characteristics circuit-CA3071.

CA3070, CA3071, CA3072

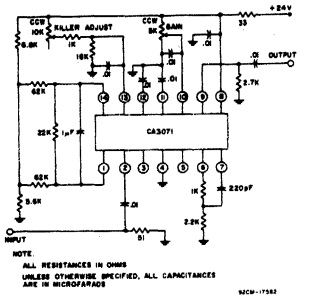


Fig. 9 – CA3071 Wideband amplifier circuit.

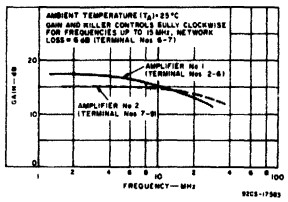


Fig. 10– Frequency response for wideband amplifier CA3071.

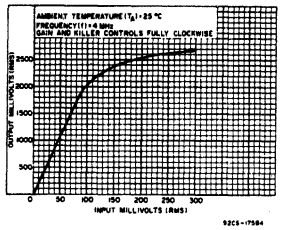


Fig. 11 – Typical CA3071 wideband amplifier linearity

CA3072 Chroma Demodulator

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14)	27 V
Reference Input Voltage	5 V_{p-p}
Chroma Input Voltage	5 V_{p-p}
Device Dissipation:	
Up to T_A = +70°C	530 mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265°C

Maximum Voltage and Current Ratings at T_A = +25°C

	Voltage*		Current		
Terminal No.	MIN VOLTS	MAX VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

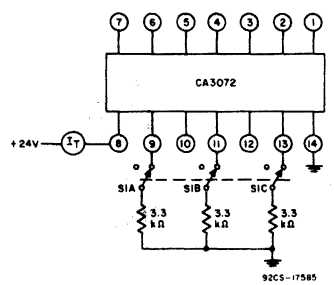


Fig. 13 – Static characteristics test circuit–CA3072.

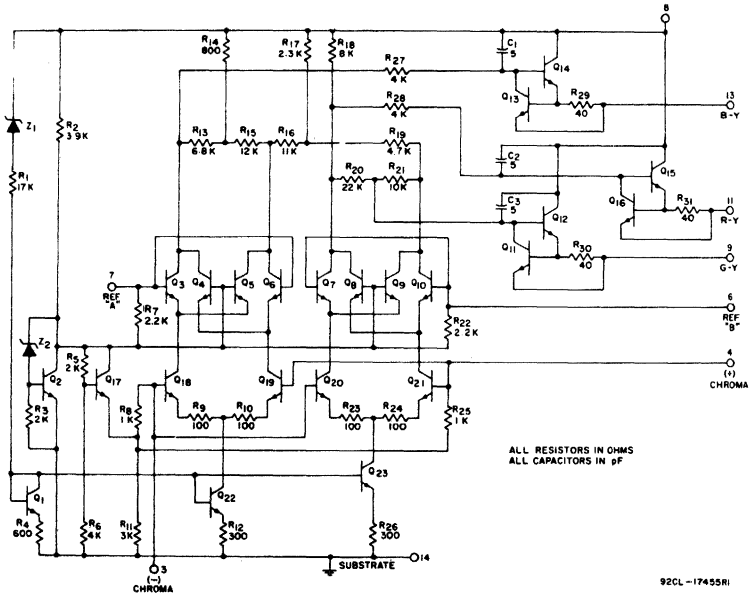


Fig. 12 – Schematic diagram for CA3072.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072 MIN.	TYP.	MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	13
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	V_9, V_{11}, V_{13}	$V_3 = V_4 = 0$	–	–	0.8	V_{p-p}	14
Maximum Color Difference Output Voltage	V_{13}	$V_3 = V_4$ = 0.6 Vp-p	8.0	–	–	V_{p-p}	
	V_{11}		5.5	–	–		
	V_9		1.2	–	–		
Chroma Input Sensitivity	V_3	Adjust e_c for 5.0 V_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35		
Relative R-Y Output	V_{11}		3.5	–	4.2		
Relative G-Y Output	V_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9\rvert - \lvert V_{11}\rvert$ $\lvert V_9\rvert - \lvert V_{13}\rvert$ $\lvert V_{11}\rvert - \lvert V_{13}\rvert$	e_c = 0	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	r_i 6, 7		–	1.7	–	kΩ	
	c_i 6, 7		–	6	–	pF	
Input Impedance at Chroma Inputs	r_i 3, 4		–	0.95	–	kΩ	
	c_i 3, 4		–	6	–	pF	
Output Resistance	r_o 9, r_o 11, r_o 13		–	180	–	Ω	

CA3070, CA3071, CA3072

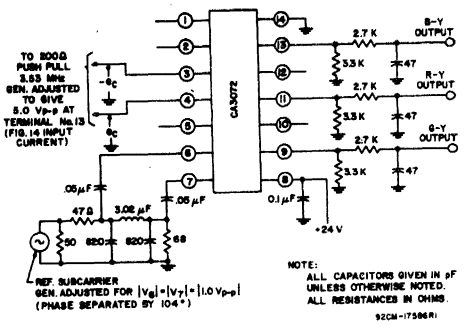


Fig. 14 - Dynamic characteristics test circuit for CA3072.

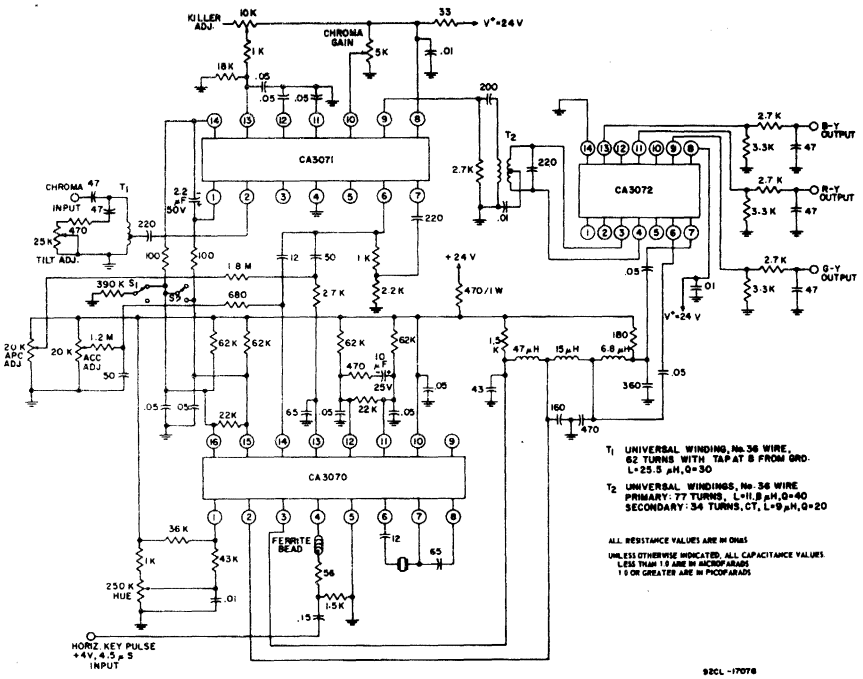


Fig. 15 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of *Fig.15* is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 2, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 2, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig.16. The effect of the keying pulse is shown in Fig.16a, and the cutoff of the oscillator output amplifier is shown in Fig.16(b) and 16c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 15, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 15 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

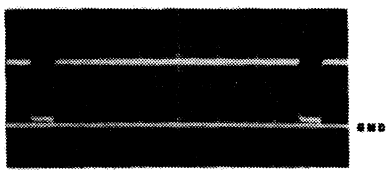


Fig. 16(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

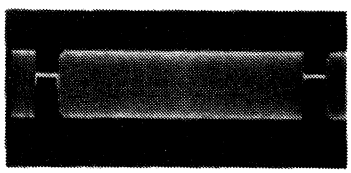


Fig. 16(b) - CA3070 terminal No. 2, 3.5 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

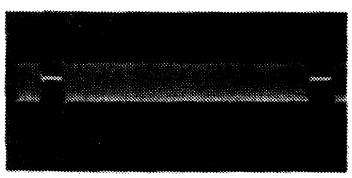


Fig. 16(c) - CA3070 terminal No. 3, 2.0 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

CA3070, CA3071, CA3072

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 17.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 10 & 11 for the wideband circuits shown in Fig. 9. This is the same basic amplifier as the one in the system shown in Fig. 15 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz, and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 V_{p-p}, even with the typical load coupling as shown in Fig. 15. Fig. 18 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 19.

CA3071 operation is as follows (Refer to Figs. 6 & 15). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12} and the output is an emitter follower, Q_{14} (Terminal No. 6.) The signal is divided in the Q_9 & Q_{12} differential amplifier, depending on the applied ACC error signal amplitude at terminal Nos. 1 & 14. The ACC error signal is derived from terminal Nos. 15 & 16 of the CA3070 and after filtering, is applied to terminal Nos. 1 & 14 of the CA3071.

At low signal drive, the 390 kilohm resistor at switch S1 (normally closed) unbalances the differential amplifier for high signal gain through Q_{12}. As the burst level at the chroma input increases, the ACC drive changes differentially in a positive direction at terminal No. 14 and a negative direction at terminal No. 14 and a negative direction at terminal No. 1. At strong signal levels the gain is reduced by diverting the balance of ac current in the differential amplifier from Q_{12} to Q_9, which is shunted to ac ground at terminal Nos. 12 and 13. The ACC loop is completed through the chroma signal at terminal No. 6 of the CA3071 to terminal No. 14 (input) of the CA3070. A typical ACC characteristic is shown in Fig. 23.

The chroma signal is buffer connected from terminal No. 6 to terminal No. 7 of the CA3071 and is amplified in the 2nd stage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 15 circuit are shown in the oscilloscope trace photographs of Fig. 21. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA3072 chroma system in the Fig. 18 circuit. Table I lists the dc terminal voltages for the system. The chroma gain and hue controls, as well as the switches S1 and S2 are removed. The template circuit board layout is also shown for duplication purposes. It should be noted that a few component values are modified in Fig. 18 from the dynamic circuit values of the data sheet. These are necessary for system matching and overall filter requirements.

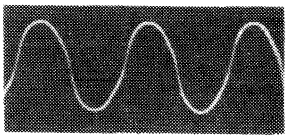


Fig. 17(a) - CA3070 terminal No. 6, oscillator waveform 1.1 V_{p-p} 3.58 MHz.

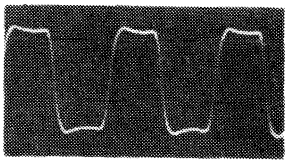


Fig. 17(b) - CA3070 terminal No. 7, oscillator waveform 1.4 V_{p-p} 3.58 MHz.

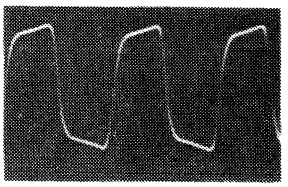


Fig. 17(c) - CA3070 terminal No. 8, oscillator waveform 1.6 V_{p-p} 3.58 MHz.

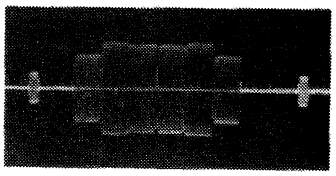


Fig. 18(a) - CA3071 chroma input 1.25 V_{p-p}; one horizontal line of NTSC input signal.

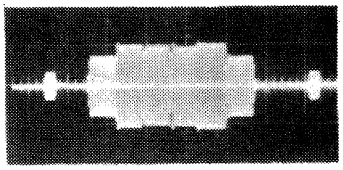


Fig. 18(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

Fig. 18(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 V_{p-p}; one horizontal line for 1.25V_{p-p} chroma input

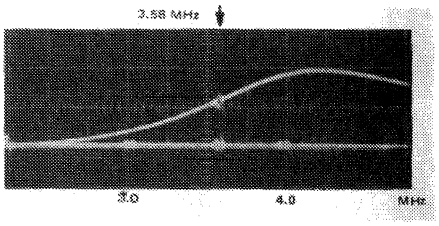


Fig. 19(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

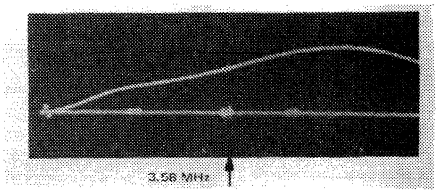


Fig. 19(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

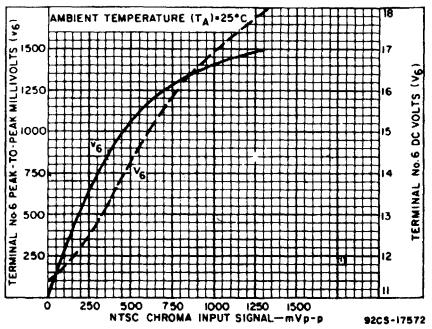


Fig. 20 - Typical ACC characteristics for chroma system of Fig. 18

CA3070, CA3071, CA3072

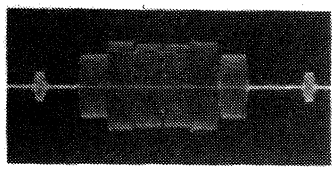


Fig. 21(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

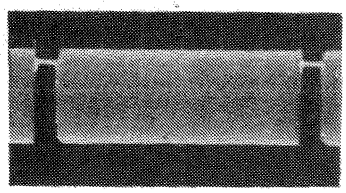


Fig. 21(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

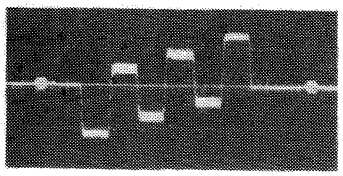


Fig. 21(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

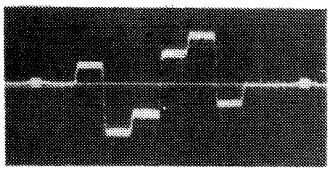


Fig. 21(d) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

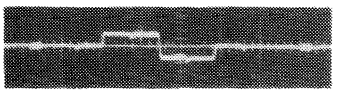


Fig. 21(e) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

CA3075

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

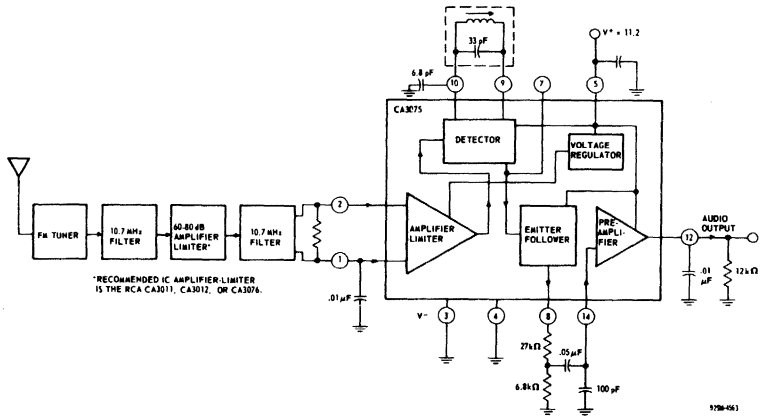


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+265	°C

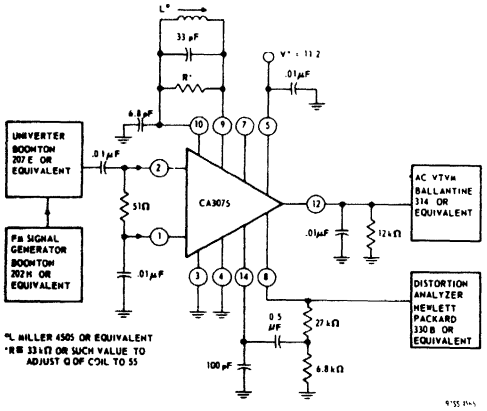


Fig. 2 - **Test Circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion**

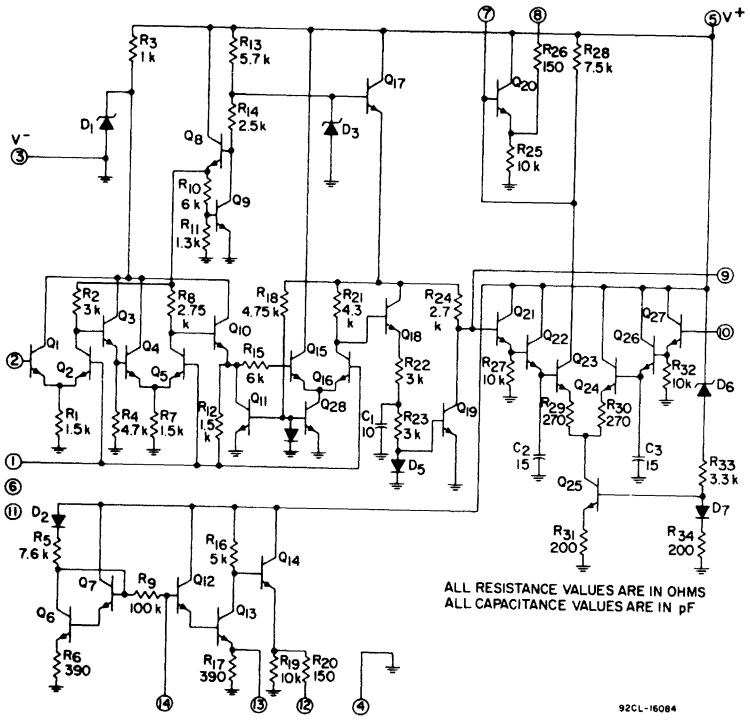


Fig.3 – Schematic diagram of CA3075

CA3075

ELECTRICAL CHARACTERISTICS at T_A = 25° C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5		8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, – 3dB point)	V_I(lim)	f_O = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_O = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							
Parallel Resistance	R_I	f_O = 10.7 MHz	–	4.5	–	kΩ	–
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_O = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	3
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER Voltage Gain	A(AF)	V_{IN} = 100 mV, f_O = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_O = 400 Hz	–	1.5	5	%	4

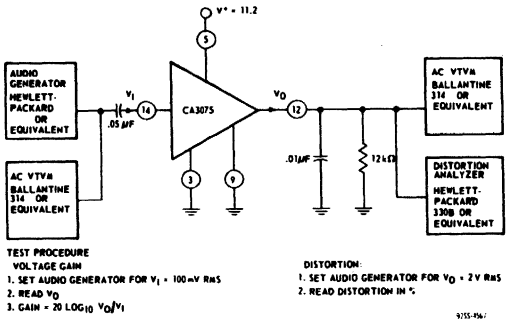


Fig.4 – Test circuit for audio preamplifier voltage gain and total harmonic distortion

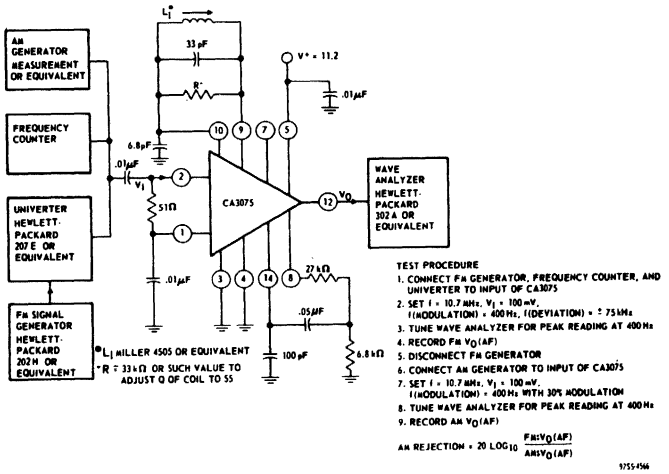


Fig.5 – Test circuit for AM rejection

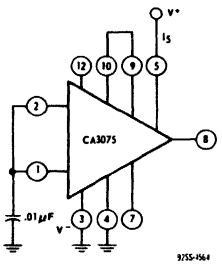


Fig. 6- Test circuit for static characteristics

CA3076
High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications in Communications Receivers

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO-5 package.

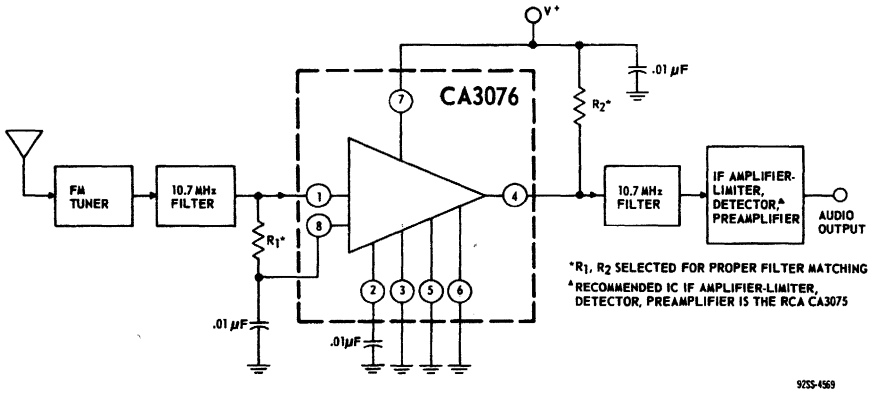


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 μV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

MAXIMUM RATINGS, ***Absolute Maximum-Values at*** T_A = 25°C

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to T_A = 50°C	500	mW
Above T_A = 50°C	derate linearly 5 mW/°C	
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static Characteristics – V^+ = 8.5 V						
DC Current (into Term. 7)	I_7	–	10	15	24	mA
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA
Dynamic Characteristics – V^+ = 8.5 V, f_0 = 10.7 MHz						
Input Limiting Voltage (knee, −3 dB point)	V_I (lim.)	–	–	50	200	μV
Output Voltage	V_O	V_I = 20 μV	4	12	–	mV
Output Noise Voltage	V_N	V_I = 0	–	1	–	mV
Forward Transfer Admittance:						
Magnitude	$\lvert Y_{21}\rvert$	V_I =	–	6	–	mho
Phase	θ_{21}	10 μV	–	80	–	degrees
Reverse Transfer Admittance:						
Magnitude	$\lvert Y_{12}\rvert$	–	–	0.1	–	μmho
Phase	θ_{12}		–	−90	–	degrees
Input-Impedance Components:						
Parallel Resistance	R_I	–	–	7.5	–	kΩ
Parallel Capacitance	C_I		–	4	–	pF
Output-Impedance Components:						
Parallel Resistance	R_O	–	50	–	–	kΩ
Parallel Capacitance	C_O		–	1.7	–	pF

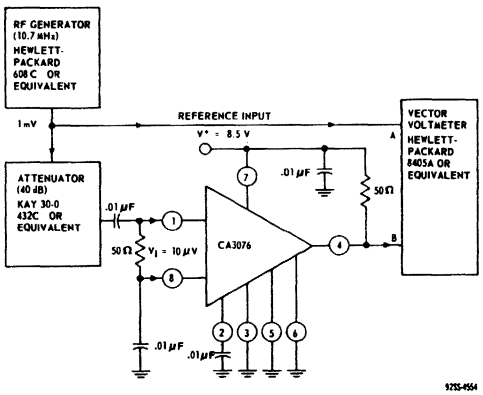


Fig. 2 - Forward transfer admittance (Y_{21}) test circuit

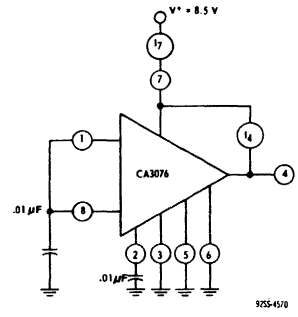
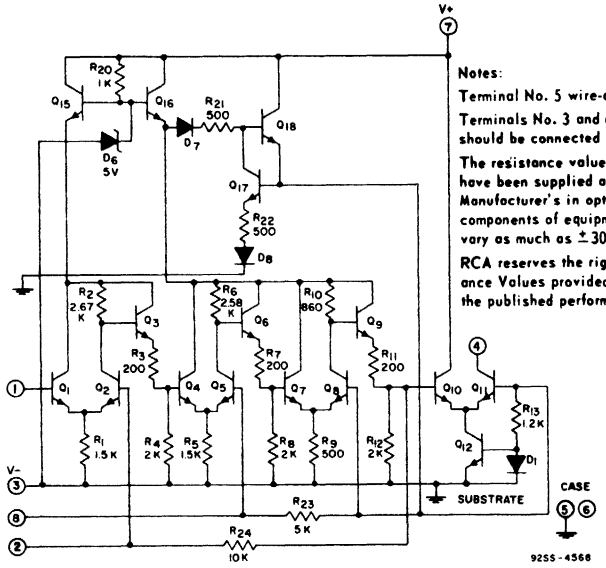


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).

CA3076



Notes:

Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 4 - Schematic diagram of CA3076.

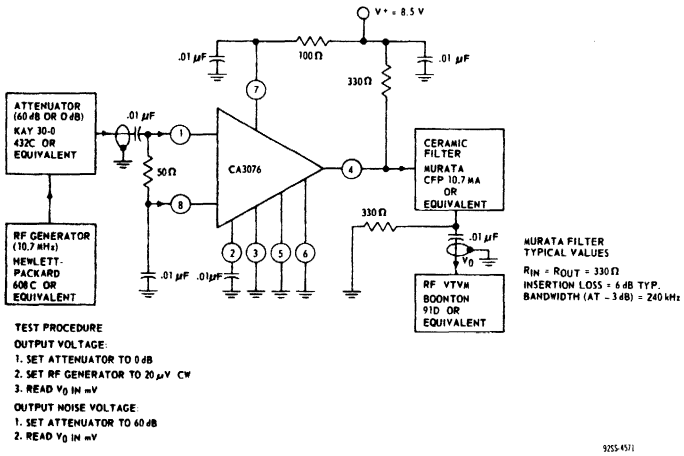


Fig. 5 - 10.7 MHz voltage gain and noise test circuit

CA3078, CA3078A Types

Amplifier

The RCA CA3078T and CA3078AT are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078T and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078AT is a premium device having a supply voltage range of $V^{\pm}$ = 0.75V to $V^{\pm}$ = 15V and an operating temperature range of -55°C to +125°C. The CA3078T has the same lower supply voltage limit but the upper limit is V^{+} = +6V and V^{-}=-6V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

Features:

- **Low standby power: as low as 700 nW**
- **Wide supply voltage range: ±0.75 to ±15 V**
- **High peak output current: 6.5 mA min.**
- **Adjustable quiescent current**
- **Output short-circuit protection**

Applications:

- **Portable electronics**
- **Medical electronics**
- **Instrumentation**
- **Telemetry**

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

	CA3078AT	CA3078T
DC Supply Voltage (between V^{+} and V^{-} terminal	36V	14V
Differential Input Voltage	±6V	±6V
DC Input Voltage	V^{+} to V^{-}	V^{+} to V^{-}
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	50 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	-55 to +125°C	0 to +70°C ▲
Storage	-65 to +150°C	-65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

*Short circuit may be applied to ground or to either supply.

▲ Types CA3078S and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			CA3078T LIMITS R_{SET} = 1 MΩ, I_Q = 100 μA					CA3078AT LIMITS R_{SET} = 5.1 MΩ, I_Q = 20 μA					UNITS
		V^{+} & V^{-}	R_S KΩ	R_L KΩ	T_A = 25°C			T_A = 0 to 70°C		T_A = 25°C			T_A = -55 to 125°C		
					MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	6	≤10		–	1.3	4.5	–	5	–	0.70	3.5	–	4.5	mV
Input Offset Current	I_{IO}				–	6	32	–	40	–	0.50	2.5	–	5.0	nA
Input Bias Current	I_{IB}				–	60	170	–	200	–	7	12	–	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}			≥10	88	92	–	86	–	92	100	–	90	–	dB
Total Quiescent Current	I_Q				–	100	130	–	150	–	20	25	–	45	μA
Device Dissipation	P_D				–	1200	1560	–	1800	–	240	300	–	540	μW
Maximum Output Voltage	V_{OM}			≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10		–	-5.5 to +5.8		-5 to +5	–	–	-5.5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10		80	110	–	–	–	80	115	–	–	–	dB
Maximum Output Current	I_{OM}^{+} or I_{OM}^{-}				–	12	–	6.5	30	–	12	–	6.5	30	mA
Input Offset Voltage Sensitivity Positive	$\Delta V_{IO}/\Delta V^{+}$		≤10			22	150	–	–		6	150	–	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^{-}$					22	150	–	–		6	150	–	–	
										R_{SET} = 13 MΩ, I_Q = 20 μA					
Input Offset Voltage	V_{IO}	15	≤10			–	–	–	–	–	1.4	3.5	–	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10		–	–	–	–	92	100	–	88	–	dB
Total Quiescent Current	I_Q					–	–	–	–	–	20	30	–	50	μA
Device Dissipation	P_D					–	–	–	–	–	600	750	–	1350	μW
Maximum Output Voltage	V_{OM}			≥10		–	–	–	–	±13.7	±14.1		±13.5	–	V
Common-Mode Rejection Ratio	CMRR		≤10			–	–	–	–	80	106	–	–	–	dB
Input Bias Current	I_{IB}					–	–	–	–	–	7	14	–	55	nA
Input Offset Current	I_{IO}					–	–	–	–	–	0.50	2.7	–	5.5	nA

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078AT and CA3078T can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 20 μA and 100 μA, respectively, for a transient response with 10% overshoot. Figs. 21 and 22 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 μA and 100 μA.

Single Supply Operation

The CA3078AT and CA3078T can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078AT or CA3078T in inverting and non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

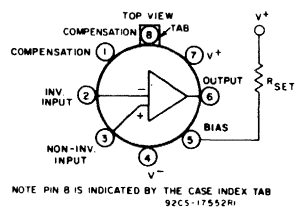


Fig. 1 – Functional diagram of the CA3078T and CA3078AT.

CA3078, CA3078A Types

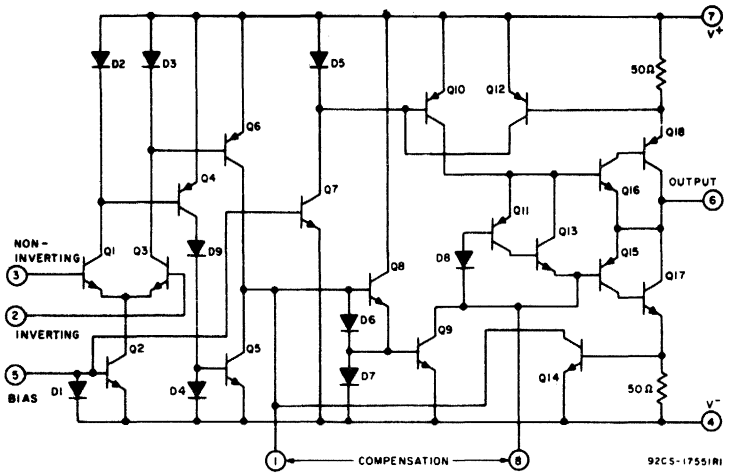


Fig.2-Schematic diagram of the CA3078T and CA3078AT.

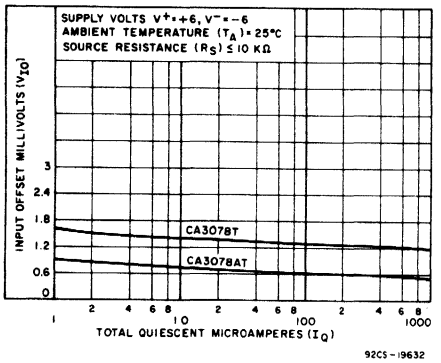


Fig.3 – Input offset voltage vs. total quiescent current.

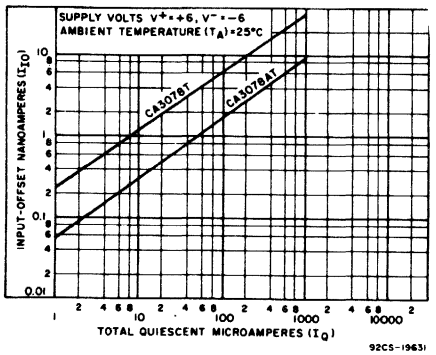


Fig.4 – Input offset current vs. total quiescent current.

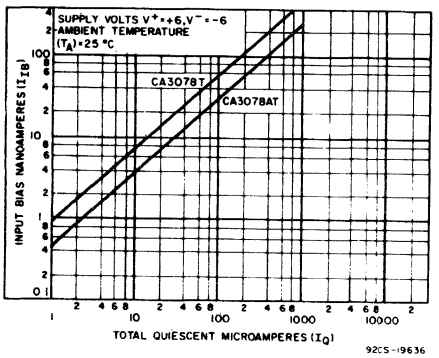


Fig.5 – Input bias current vs. total quiescent current.

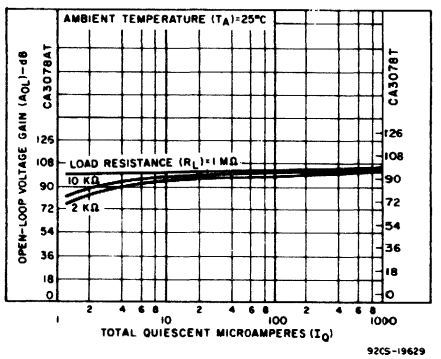


Fig.6 – Open-loop voltage gain vs. total quiescent current.

Typical Values Intended Only for Design Guidance at T_A = 25°C and V^+ = +6 V, V^- = 6 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3078AT		CA3078T	UNITS
			R_{SET} = 5.1 MΩ, I_Q = 20 μA	R_{SET} = 1 MΩ, I_Q = 100 μA	R_{SET} = 1 MΩ, I_Q = 100 μA	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	5	6	6	μV/°C
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	6.3	70	70	pA/°C
Open-Loop Bandwidth	BW_{OL}	3dB pt	0.3	2	2	kHz
Slew Rate: Unity Gain	SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
Slew Rate: Comparator	SR	See Figs. 20, 21	0.5	1.5	1.5	V/μs
Transient Response		10% to 90% Rise Time	3	2.5	2.5	μs
Input Resistance	R_I		7.4	1.7	0.87	MΩ
Output Resistance	R_O		1	0.8	0.8	KΩ
Equiv. Input Noise Voltage	e_N(10Hz)	R_S = 0	40	–	25	nV/√Hz
Equiv. Input Noise Current	i_N(10Hz)	R_S = 1 MΩ	0.25	–	1	pA/√Hz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078AT		CA3078T		
	V^+ = +1.3V, V^- = −1.3V, R_{SET} = 2 MΩ, I_Q = 10 μA	V^+ = +0.75V, V^- = −0.75V, R_{SET} = 10 MΩ, I_Q = 1 μA	V^+ = +1.3V, V^- = −1.3V, R_{SET} = 2 MΩ, I_Q = 10 μA	V^+ = 0.75V, V^- = −0.75V, R_{SET} = 10 MΩ, I_Q = 1 μA	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

CA3078, CA3078A Types

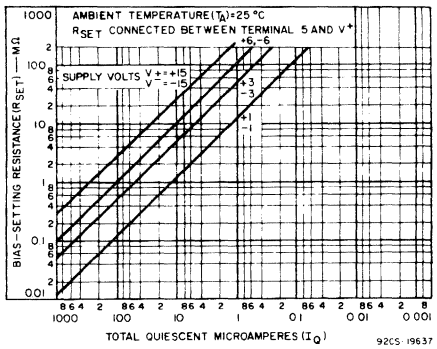


Fig. 7 – Bias-setting resistance vs. total quiescent current.

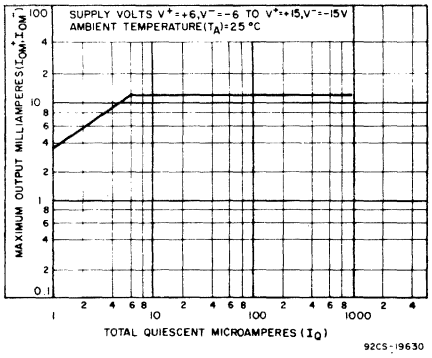


Fig. 8 – Maximum output current vs. total quiescent current.

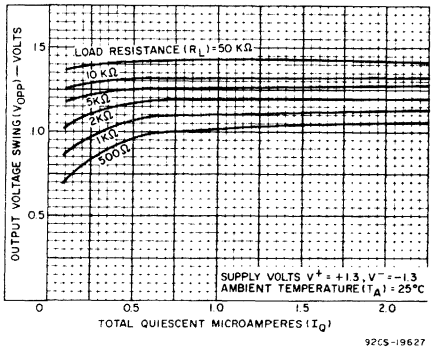


Fig. 9 – Output voltage swing vs. total quiescent current.

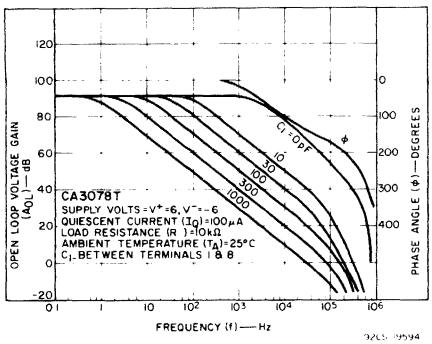


Fig. 10 – Open-loop voltage gain vs. frequency for I_Q = 100 μA – CA3078T.

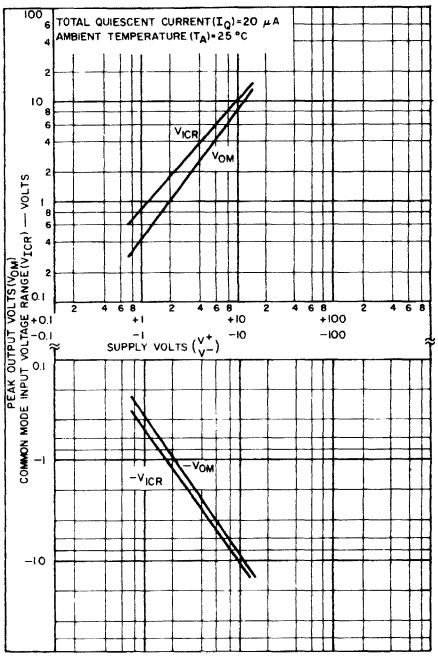


Fig. 11 – Output and common-mode voltage vs. supply voltage.

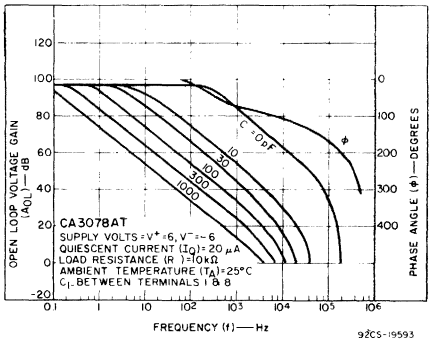


Fig. 12 – Open-loop voltage gain vs. frequency for I_Q = 20 μA – CA3078AT.

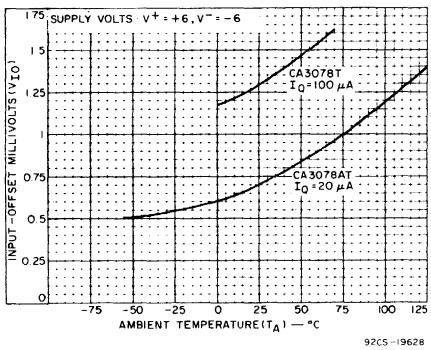


Fig. 13 – Input offset voltage vs. temperature.

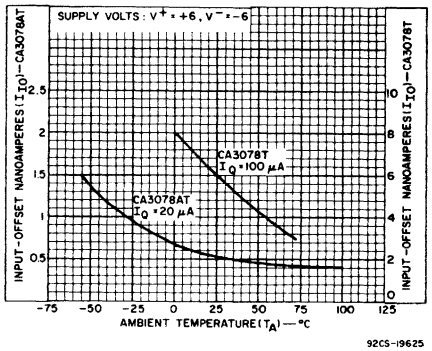


Fig. 14 – Input offset current vs. temperature.

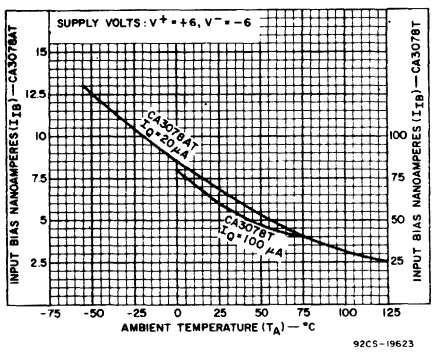


Fig. 15 – Input bias current vs. temperature.

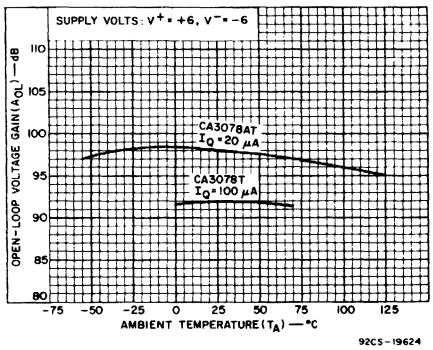


Fig. 16 – Open-loop voltage gain vs. temperature.

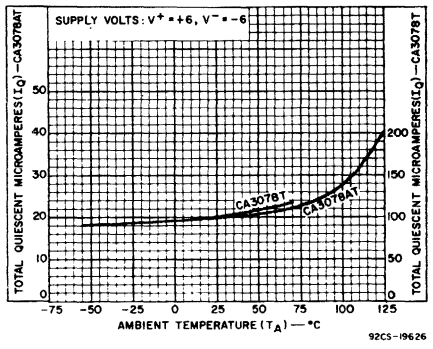


Fig. 17 – Total quiescent current vs. temperature.

CA3078, CA3078A Types

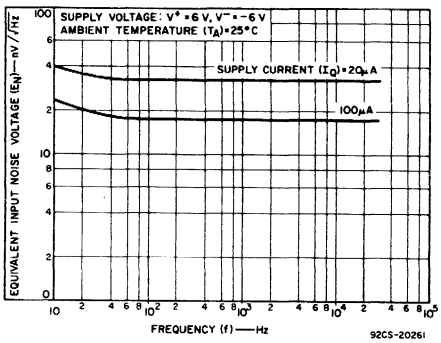


Fig.18 – Equivalent input noise voltage vs. frequency.

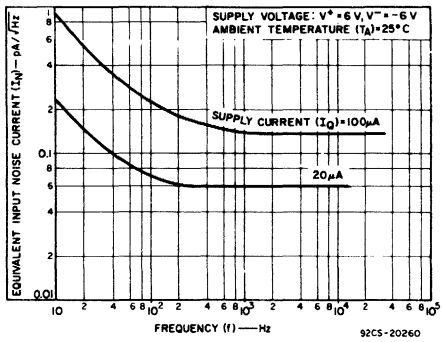


Fig.19 – Equivalent input noise current vs. frequency.

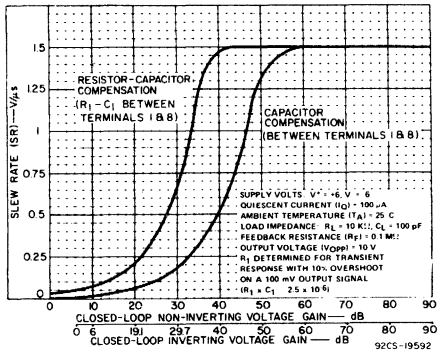


Fig.20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078T.

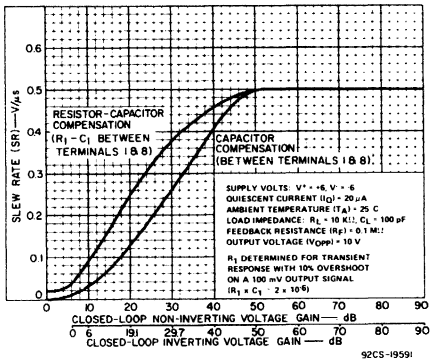


Fig.21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078AT.

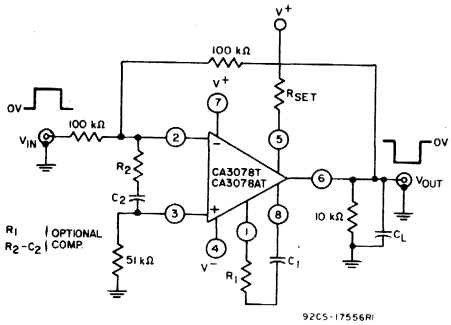


Fig.22 – Transient response and slew-rate, unity gain (inverting) test circuit.

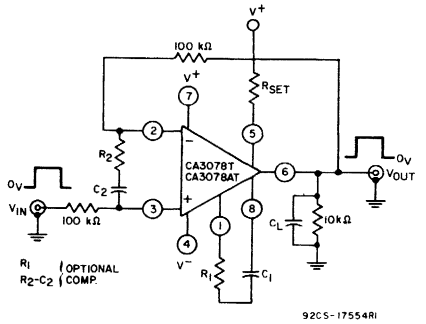


Fig.23 – Slew, rate, unity gain (non-inverting) test circuit.

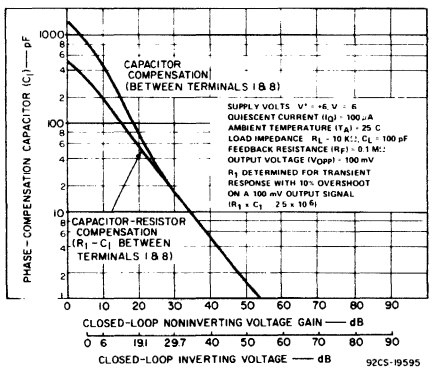


Fig.24 – Phase compensation capacitance vs. closed-loop gain – CA3078T.

Table I - Unity-gain slew rate vs. compensation – CA3078T and CA3078AT

SUPPLY VOLTS: V^+ = 6, V^- = -6 OUTPUT VOLTAGE (V_O) = ±5V LOAD RESISTANCE (R_L) = 10 kΩ						TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE of 100 mV AMBIENT TEMPERATURE (T_A) = 25°C				
COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078T – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078AT – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

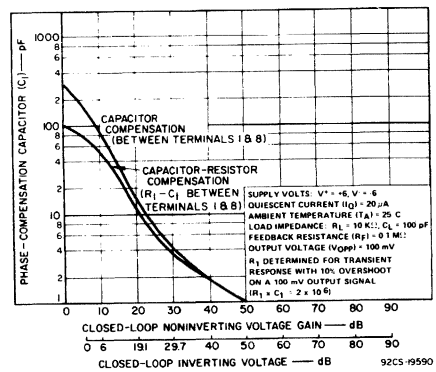


Fig.25 – Phase compensation capacitance vs. closed-loop gain – CA3078AT.

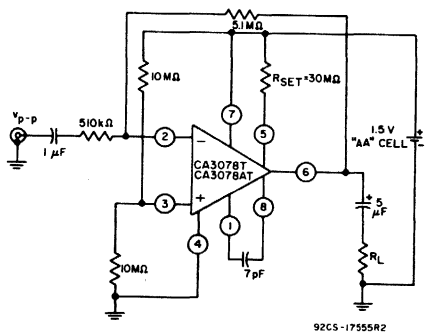


Fig.27 – Inverting 20-dB amplifier circuit.

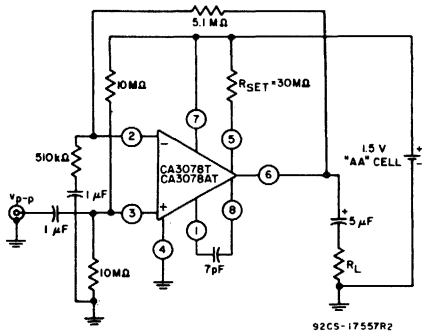


Fig.28 – Non-inverting 20-dB amplifier circuit.

CA3080, CA3080A Types

Operational Transconductance Amplifiers (OTA's)

Gateable-Gain Blocks

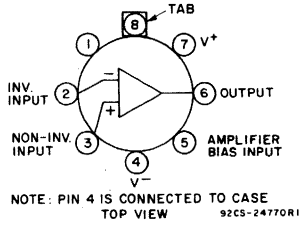
The RCA-CA3080 and CA3080A are Gateable-Gain Blocks which utilize the unique Operational Transconductance Amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5 style package (CA3080, CA3080A), and in the 8-lead TO-5 style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080E is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E), and in chip form (CA3080H).



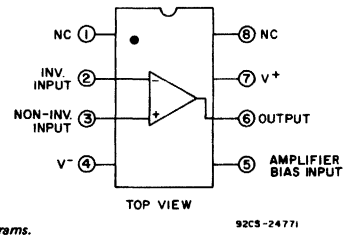


Fig. 1—Functional diagrams.

Plastic Package (CA3080E)

Features:

- Slew rate (unity gain, compensated): 50 V/μs
- Adjustable power consumption: 10μW to 30 mW
- Flexible supply voltage range: ± 2 V to ± 15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades

Applications:

- Sample and hold
- Multiplex
- Voltage follower
- Multiplier
- Comparator

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC SUPPLY VOLTAGE (between V+ and V− terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V+ to V−
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080	0 to + 70 °C
CA3080A	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

* Short circuit may be applied to ground or to either supply.

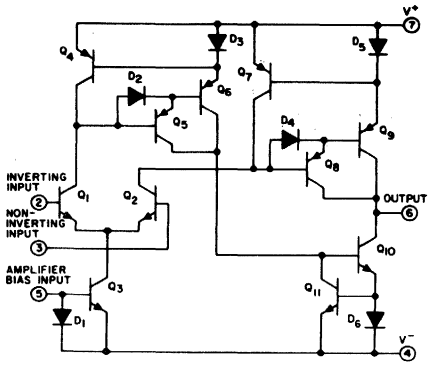


Fig.2 – Schematic diagram for CA3080 and CA3080A.

▲ Type CA3080 can be operated over the temperature of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

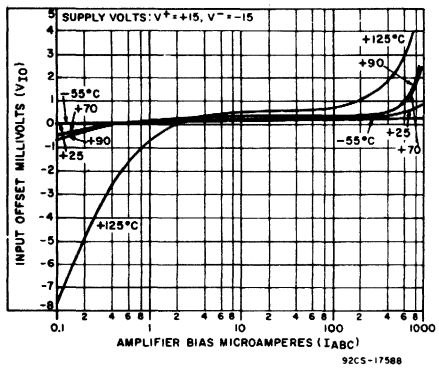


Fig.3 – Input offset voltage vs. amplifier bias current.

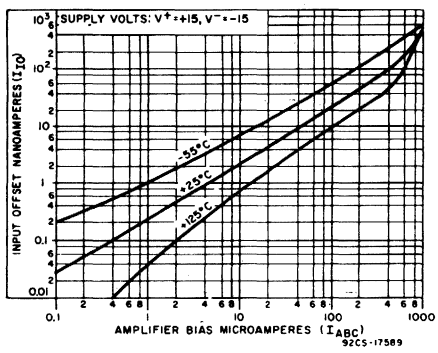


Fig.4 – Input offset current vs. amplifier bias current.

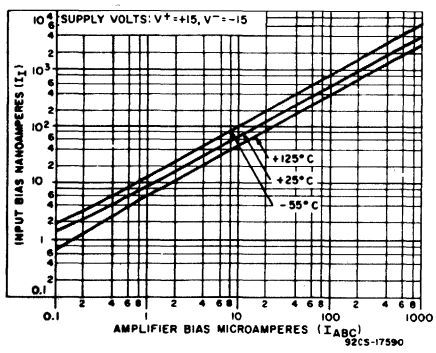


Fig.5 – Input bias current vs. amplifier bias current.

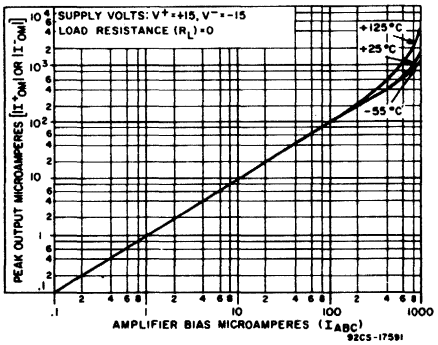


Fig.6 – Peak output current vs. amplifier bias current.

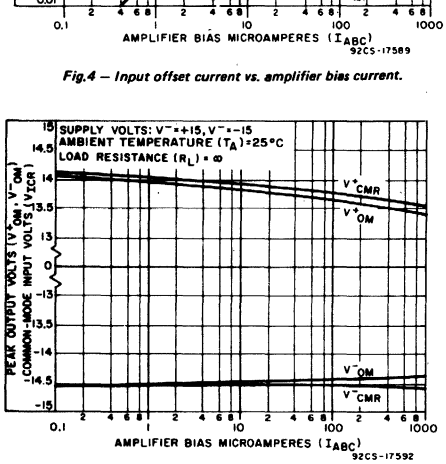


Fig.7 – Peak output voltage vs. amplifier bias current.

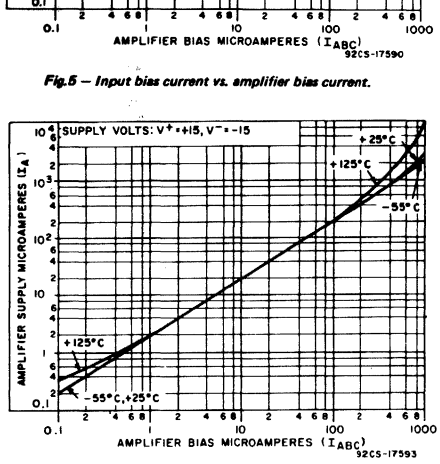


Fig.8 – Amplifier supply current vs. amplifier bias current.

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		Typical Characteristics Curves	CA3080 LIMITS			UNITS
		Circuit Fig.	$V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Fig.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	–		3	–	0.4	5	mV
			T_A = 0 to 70°C		–	–	6	
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			T_A = 0 to 70°C		–	–	7	
Forward Transconductance (large signal)	g_m	–		14	6700	9600	13000	μmho
			T_A = 0 to 70°C		5400	–	–	
Peak Output Current	$\|I_{OM}\|$	–	$R_L = 0$	6	350	500	650	μA
			$R_L = 0$, T_A = 0 to 70°C		300	–	–	
Peak Output Voltage: Positive	V^+_{OM}	–	$R_L = \infty$	7	12	13.5	–	V
Negative	V^-_{OM}				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$	–		–	–	–	150	
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

					CA3080	
Input Offset Voltage	V_{IO}	–	$I_{ABC} = 5\ \mu A$	3	0.3	mV
Input Offset Voltage Change	$\|\Delta V_{IO}\|$	–	Change in V_{IO} between $I_{ABC} = 500\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	0.2	mV
Peak Output Current	I_{OM}	–	$I_{ABC} = 5\ \mu A$	6	5	μA
Peak Output Voltage: Positive	V^+_{OM}	–	$I_{ABC} = 5\ \mu A$	7	13.8	V
Negative	V^-_{OM}				−14.5	
Magnitude of Leakage Current		10	$I_{ABC} = 0$, $V_{TP} = 0$	11	0.08	nA
			$I_{ABC} = 0$, $V_{TP} = 36$ V		0.3	
Differential Input Current		12	$I_{ABC} = 0$, $V_{DIFF} = 4$ V	13	0.008	nA
Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate: Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–		–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	19	f = 1 MHz	20	0.024	pF

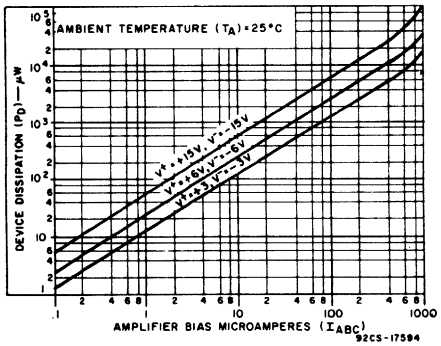


Fig.9 – Total power dissipation vs. amplifier bias current.

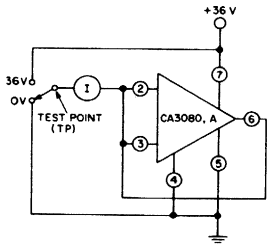


Fig.10 – Leakage current test circuit.

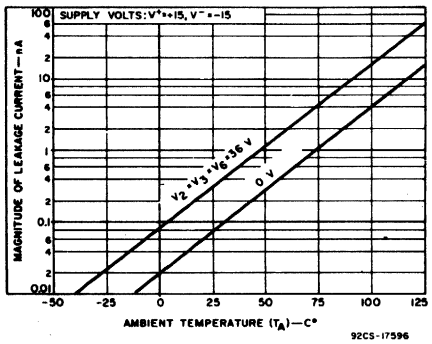


Fig.11 – Leakage current vs. temperature.

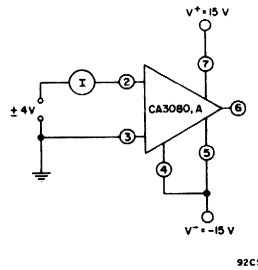


Fig.12 – Differential input current test circuit.

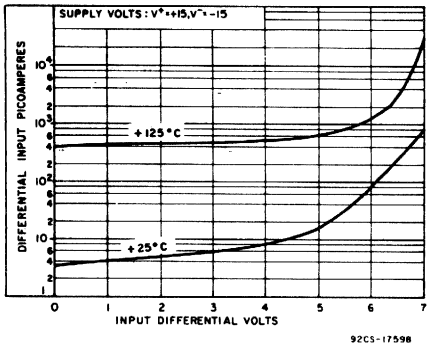


Fig.13 – Input current vs. input differential voltage.

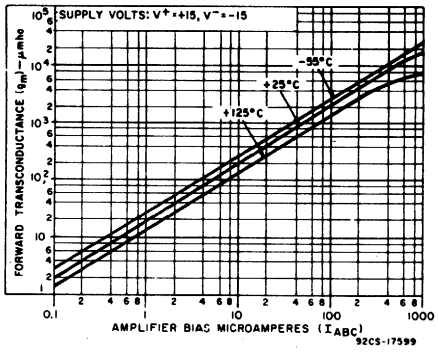


Fig.14 – Transconductance vs. amplifier bias current.

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	Circuit Fig.	TEST CONDITIONS (V^+ = 15 V, V^- = −15 V, I_{ABC} = 500 μA, T_A = 25°C (unless indicated otherwise))	Typical Characteristics Curves Fig.	CA3080A LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	–	I_{ABC} = 5 μA	3	–	0.3	2	mV
					–	0.4	2	
			T_A = −55 to +125°C		–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	–	Change in V_{IO} between I_{ABC} = 500 μA and I_{ABC} = 5 μA	3	–	0.1	3	mV
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			T_A = −55 to +125		–	–	8	
Forward Transconductance (large signal)	g_m	–		14	7700	9600	12000	μmho
			T_A = −55 to + 125°C		4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$		I_{ABC} = 5 μA, R_L = 0	6	3	5	7	μA
			R_L = 0		350	500	650	
			R_L = 0, T_A = −55 to +125°C		300	–	–	
Peak Output Voltage: Positive	V^+_{OM}	–	I_{ABC} = 5 μA, R_L = ∞	7	12	13.8	–	V
Negative	V^-_{OM}				−12	−14.5	–	
Positive	V^+_{OM}	–	R_L = ∞		12	13.5	–	
Negative	V^-_{OM}				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$				–	–	150	
Magnitude of Leakage Current		10	I_{ABC} = 0, V_{TP} = 0	11	–	0.08	5	nA
			I_{ABC} = 0, V_{TP} = 36 V		–	0.3	5	
Differential Input Current		12	I_{ABC} = 0, V_{DIFF} = 4 V	13	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

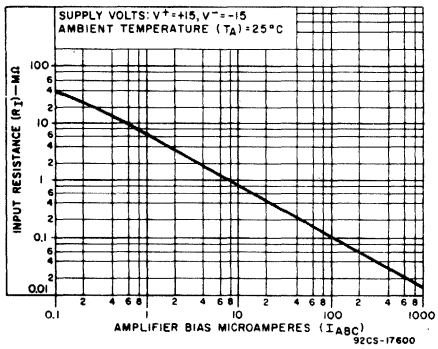


Fig.15 – Input resistance vs. amplifier bias current.

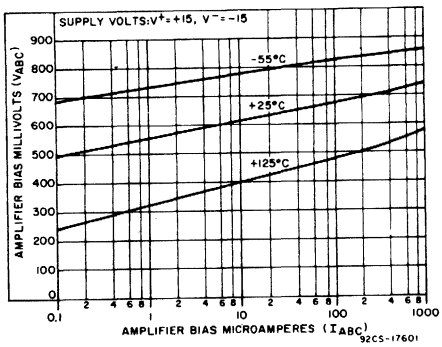


Fig.16 – Amplifier bias voltage vs. amplifier bias current.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance

					CA3080A	
Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate: Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–	–	–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	19	f = 1 MHz	20	0.024	pF

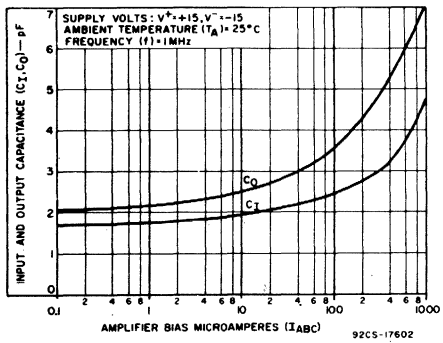


Fig.17 – Input and output capacitance vs. amplifier bias current.

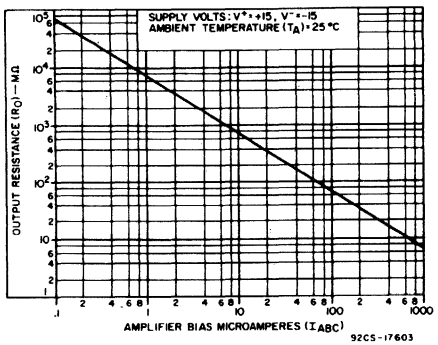


Fig.18 – Output resistance vs. amplifier bias current.

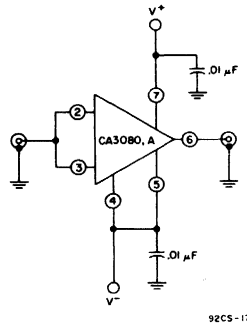


Fig.19 – Input-to-output capacitance test circuit.

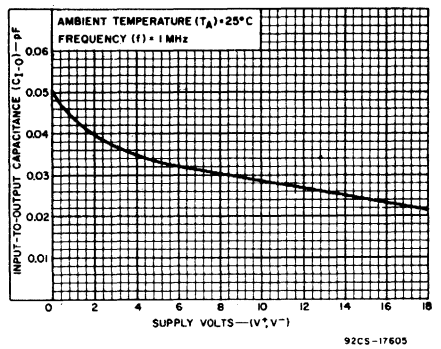


Fig.20 – Input-to-output capacitance vs. supply voltage.

CA3081, CA3082 Types

General-Purpose High-Current N-P-N Transistor Arrays

CA3081–Common-Emitter Array **CA3082–Common-Collector Array**

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features

- **7 transistors permit a wide range of applications in either a common-emitter (CA3081) or common-collector (CA3082) configuration**
- **High I_C: 100 mA max.** ■ **Low $V_{CE\ sat}$ (at 50 mA): 0.4 V typ.**

Applications

- **Drivers for:**
  - **Incandescent display devices (e.g. RCA NUMITRON DR2000 Series and lamps)**
  - **LED (e.g. RCA-SG1002 GaAs High-Efficiency Emitting Diode)**
  - **Relay control** – **Thyristor firing**

RCA-CA3081* and CA3082* consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other driver applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design.

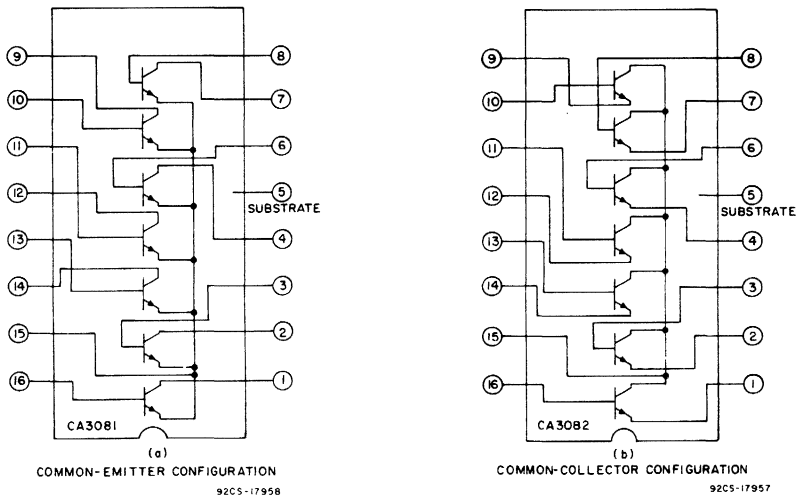


Fig.1–Functional diagrams of types CA3081 and CA3082.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

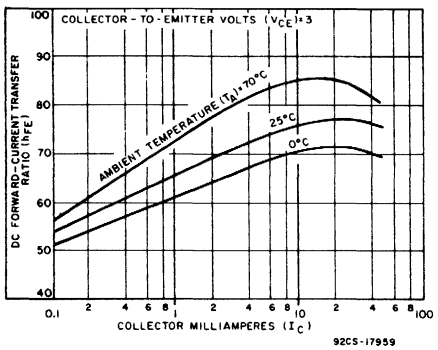


Fig.2–h_{FE} vs. I_C

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

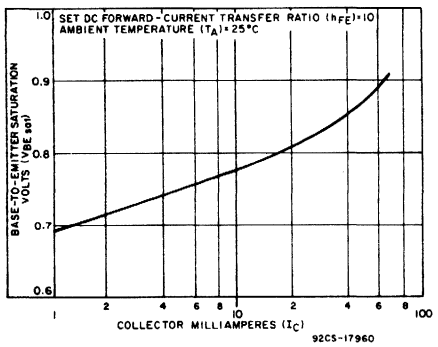


Fig.3–V_{BEsat} vs. I_C

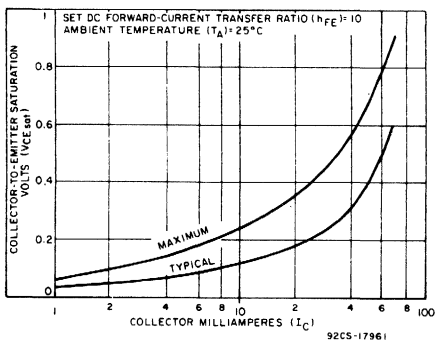


Fig.4–V_{CEsat} vs. I_C at T_A = 25°C.

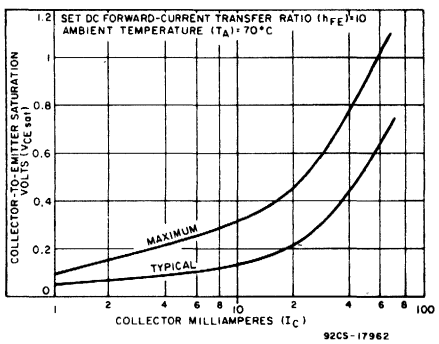


Fig.5–V_{CEsat} vs. I_C at T_A = 70°C.

CA3081, CA3082 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL READ-OUT DRIVER APPLICATIONS

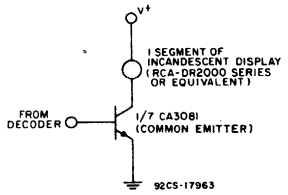


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.

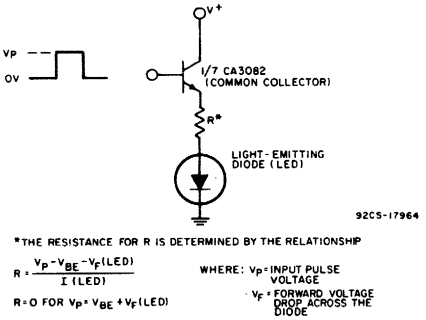


Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

CA3083

General-Purpose High-Current N-P-N Transistor Array

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

Features

- **High I_C: 100mA max.**
- **Low V_{CEsat} (at 50mA): 0.7V max.**
- **Matched pair (Q1 and Q2)—**
  V_{IO} (V_{BE} matched): ± 5 mV max.
  I_{IO} (at 1mA): 2.5 μA max.
- **5 independent transistors plus separate substrate connection**
- **The CA3083 is available in a sealed-junction Beam-Lead version (CA3083L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

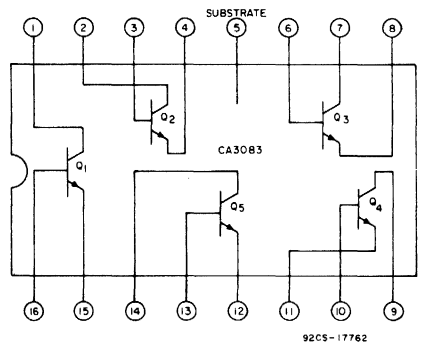


Fig.1—Functional diagram of the CA3083.

Applications

- **Signal processing and switching systems operating from DC to VHF**
- **Lamp and relay driver**
- **Differential amplifier**
- **Temperature-compensated amplifier**
- **Thyristor firing**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications**

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16" +1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

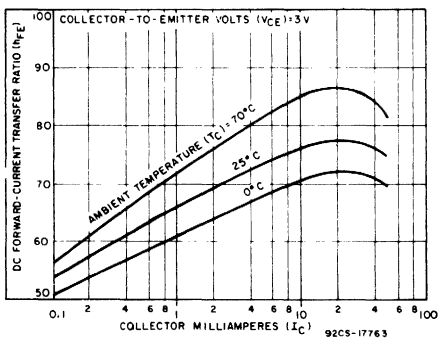


Fig.2 – h_{FE} vs I_C

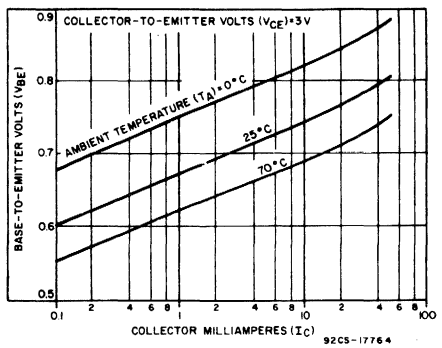


Fig.3 – V_{BE} vs I_C

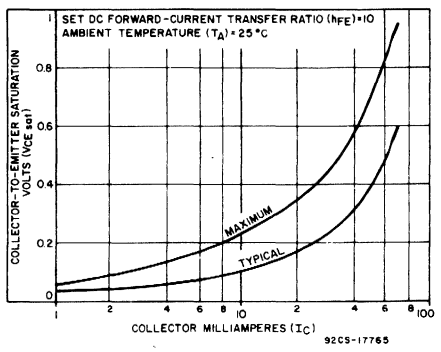


Fig.4 – V_{CEsat} vs I_C at 25°C

CA3083

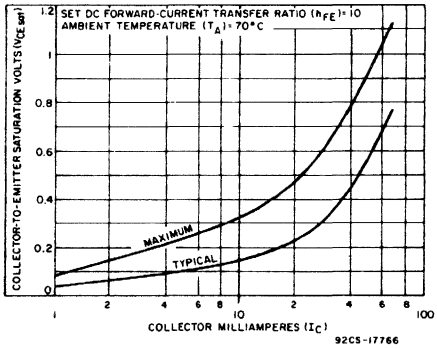


Fig.5 – V_{CEsat} vs I_C at 70°C

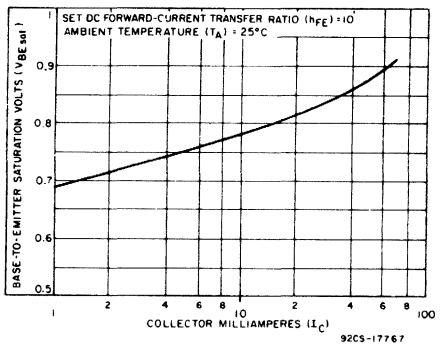


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

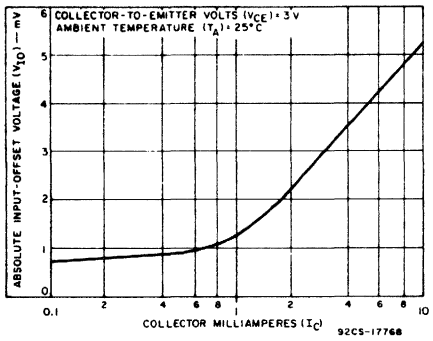


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

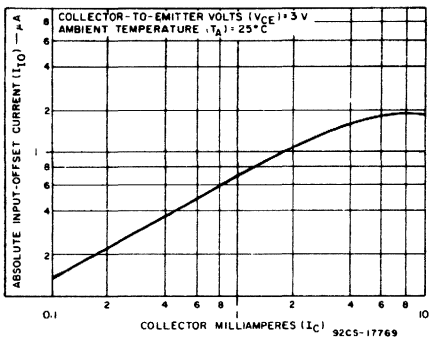


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

CA3084

General-Purpose P-N-P Transistor Array

RCA-CA3084 is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

FEATURES

- **Matched transistor pair (Q1 and Q2)**
  V_{IO} (V_{BE} matched): ± 6mV max.
  I_{IO} (at 100 μA): ± 0.6 μA
- **Wide operating current range**
- **Low noise figure - - 3.2 dB typ. at 1 kHz**
- **The CA3084 is available in a sealed-junction Beam-Lead version (CA3084L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

APPLICATIONS

- **General use in signal processing systems having low-power and low-frequency requirements**
- **Differential amplifiers**
- **Temperature compensated amplifiers**
- **Active loads for differential amplifiers using n-p-n transistors**
- **Complementary uses with RCA n-p-n transistor arrays**

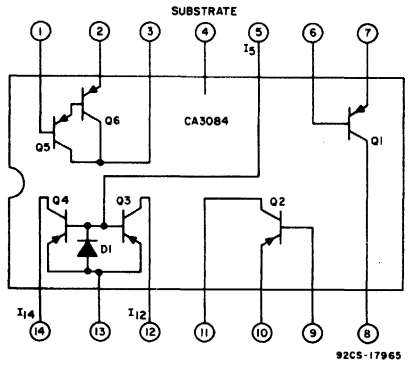


Fig.1 – Functional diagram of the CA3084.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	−40	V
Collector-to-Base Voltage (V_{CBO})	−40	V
Base-to-Substrate Voltage (V_{BIO})*	40	V
Emitter-to-Base Voltage (V_{EBO})	−40	V
Collector Current (I_C)	−10	mA

The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

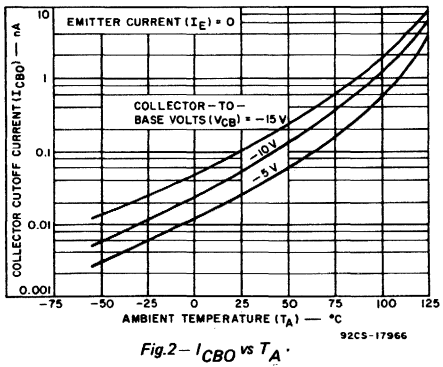


Fig.2 – I_{CBO} vs T_A.

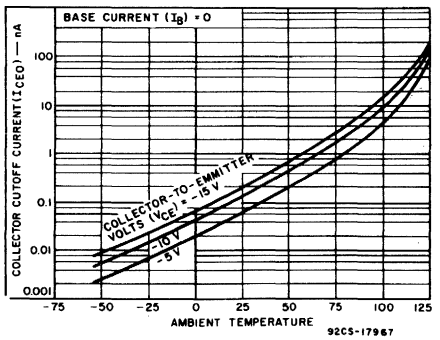


Fig.3 – I_{CEO} vs T_A.

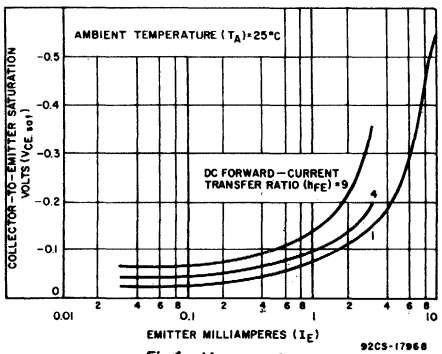


Fig.4 – V_{CEsat} vs I_E.

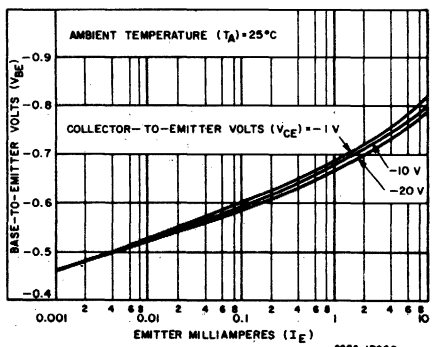


Fig.5 – V_{BE} vs I_E.

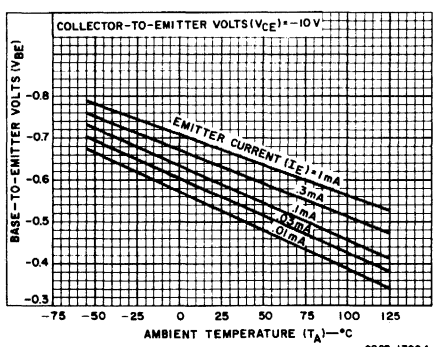


Fig.6 – V_{BE} vs T_A.

CA3084

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	40	100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}	I_E = 100μA, V_{CE} = −10V	–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current (Normalized)	I_C/I_5	V_{CE} = −5V, V_{CIO} = −5V, Term. 13 = Gnd. I_5 = −100μA,	10	0.85	1.00	1.15	
Magnitude of Collector Current Ratio	$\lvert I_C(Q3)/I_C(Q4) \rvert$	V_{CE} = −5V, V_{CIO} = −5V, Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistance	R_I	f = 1kHz, V_{CE} = −10V,	19		9		kΩ
Output Resistance	R_O	I_C = −100μA	20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

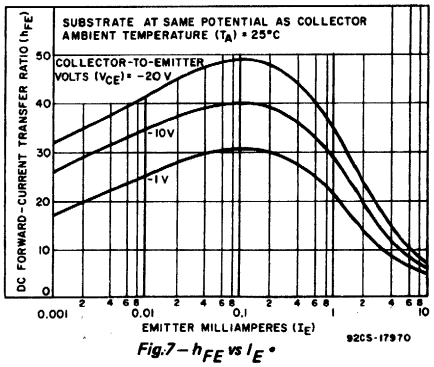


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

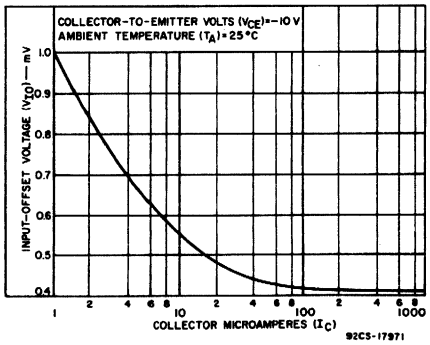


Fig.8–V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

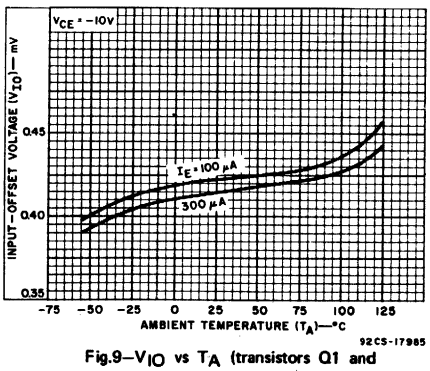


Fig.9–V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

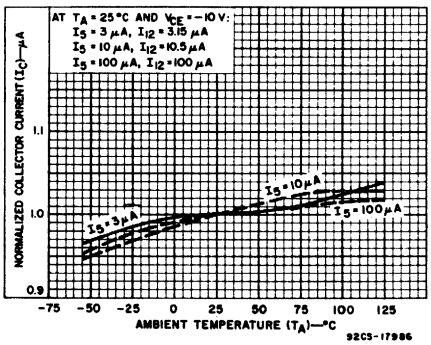


Fig.10–Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

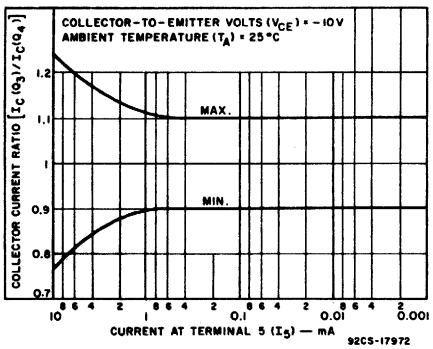


Fig.11–I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

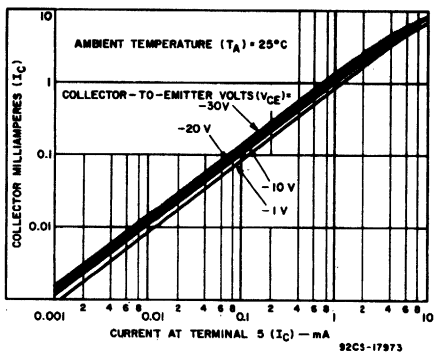


Fig.12 – I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

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STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

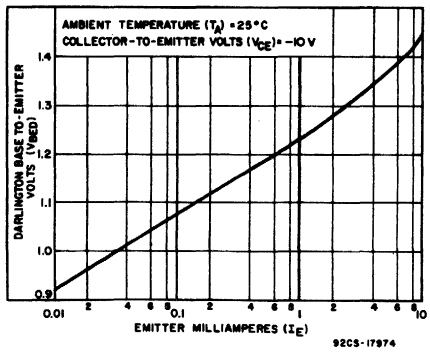


Fig.13 – V_{BE} vs I_E (transistors Q5 and Q6 in a darlingtron configuration).

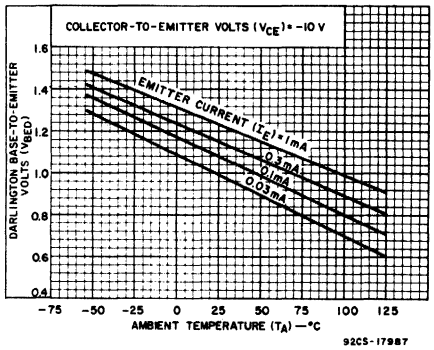


Fig.14 – V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

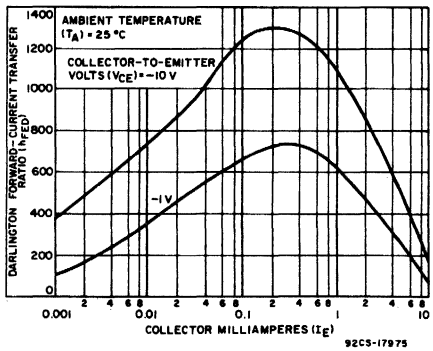


Fig.15 – h_{FE} vs. I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

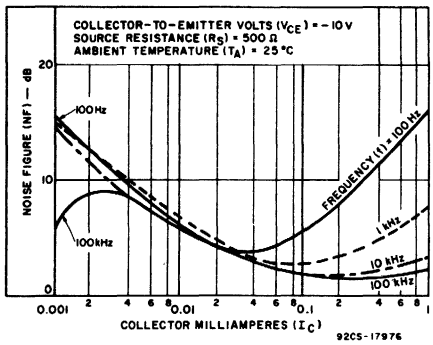


Fig.16 – NF vs I_C at R_S = 500 Ω

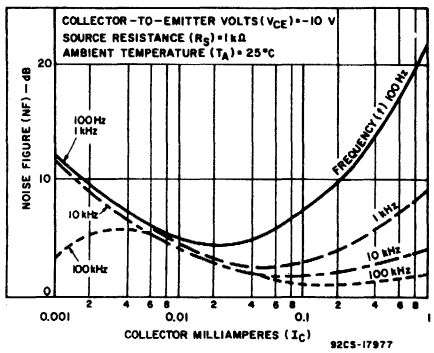


Fig.17 – NF bs I_C at R_S = 1 kΩ

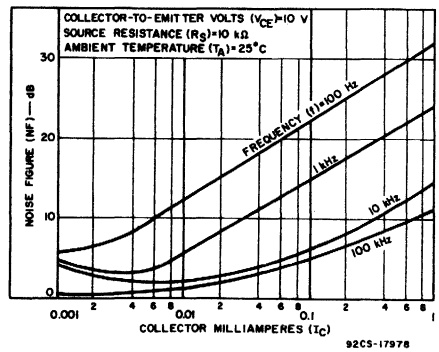


Fig.18 – NF vs I_C at R_S = 10kΩ

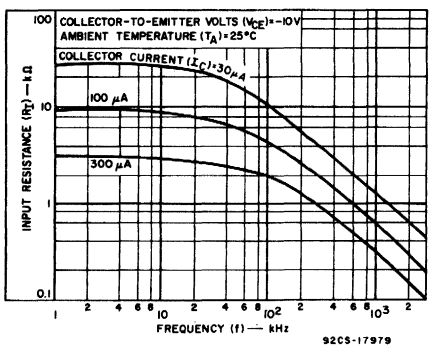


Fig.19 – R_I vs f

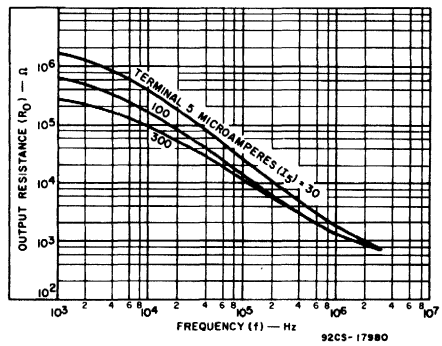


Fig.20 – R_O vs f

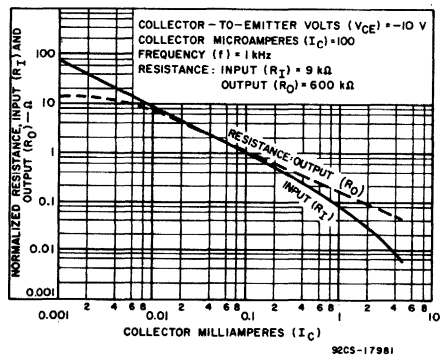


Fig.21 – Normalized R_I and R_O vs I_C

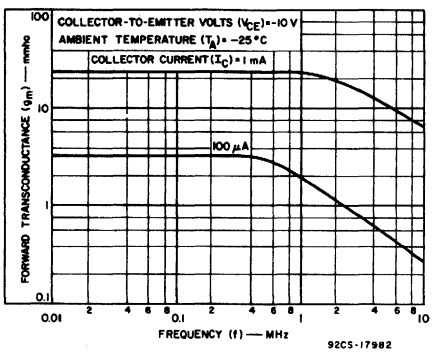


Fig.22 – g_m vs f

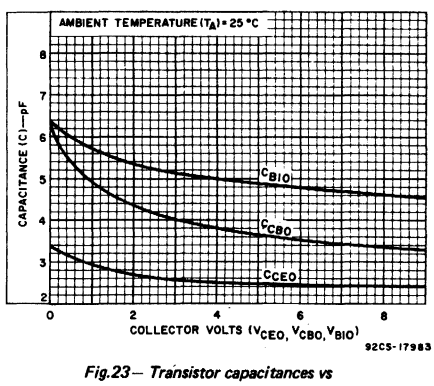


Fig.23 – Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

CA3085, CA3085A, CA3085B Types

Positive Voltage Regulators

For Regulated Voltages from 1.7V to 46V at Currents up to 100mA

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

The CA3085 is available in a sealed-junction Beam-Lead version (CA3085L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**
- Low noise

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**
- See Application Note ICAN-6157 "Applications of the CA3085-Series Monolithic IC Voltage Regulators".

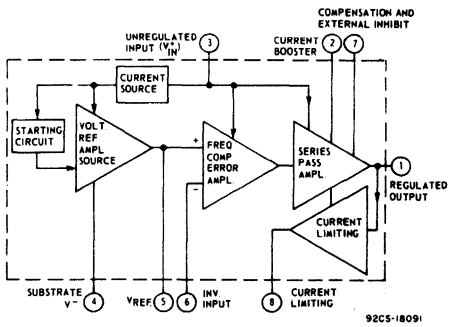


Fig.1–Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:
CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	·	·	·	·	·	+10 0
6	–	–	·	·	·	·	·	·
7	–	–	–	+3 −10	+3 −10	·	·	+† 0
8	–	–	–	–	+5 −1	·	·	·
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

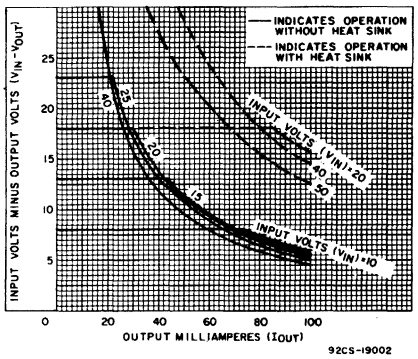


Fig.3–Dissipation limitation (V_{IN}–V_{OUT} vs. I_{OUT}).

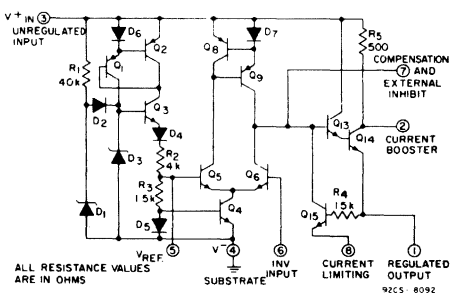


Fig.2–Schematic diagram of CA3085 Series.

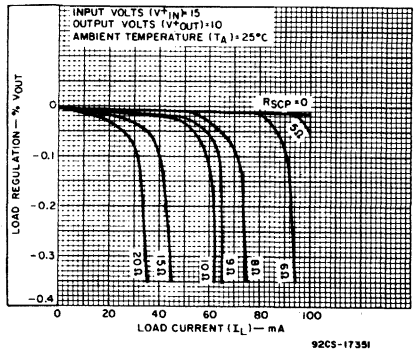


Fig.4–Load regulation characteristics.

CA3085, CA3085A, CA3085B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]		CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	15	V^+_{IN} = 15V		1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	15	V^+_{IN} = 30V		–	3.3	4.5	–	–	–	–	–	–	mA
			V^+_{IN} = 40V		–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V		–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–		7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	15	V^+_{IN} = 30,40,50V#; R_L = 365Ω; Term. No. 6 to Gnd.		26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	15	V^+_{IN} = 30V		–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–		4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	16	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6Ω		–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0		–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0		–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1mA, R_{SCP} = 0		–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage■	V_{NOISE}	12	V^+_{IN} = 25V	C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
				C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	13	V^+_{IN} = 25V f = 1kHz	C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
				C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	13	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	$\Delta V_{REF}/\Delta V_o$	–	I_L = 0, V_{REF} = 1.6V		–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	14	V^+_{IN} = 25V, +50mA Step		–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step		–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step		–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–			–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* R_{SCP}: Short-circuit protection resistance

■ Bandwidth DC to 10 MHz.

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{(V_{OUT(initial)})\ (\Delta V_{IN})} \times 100\%$

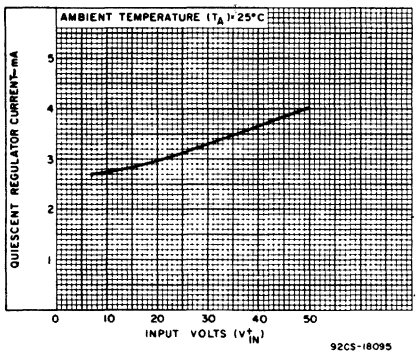


Fig.5–$I_{quiescent}$ vs. V^+_{IN}.

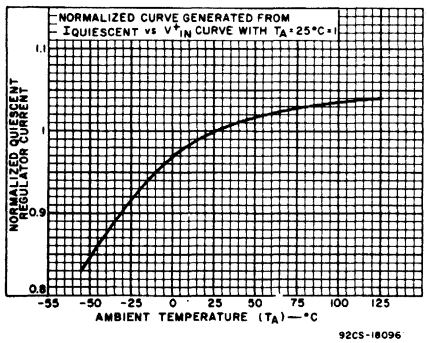


Fig.6–Normalized $I_{quiescent}$ vs. T_A.

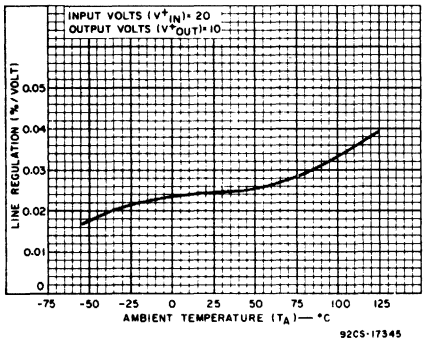


Fig.7–Line regulation temperature characteristics.

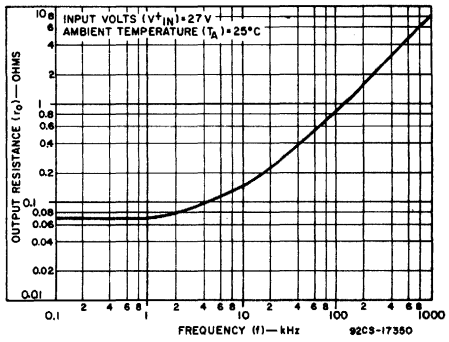


Fig.8–r_o vs. f.

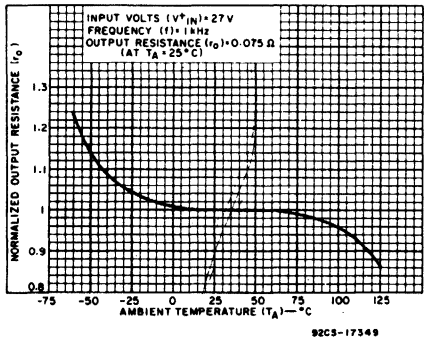


Fig.9–Normalized r_o vs. T_A.

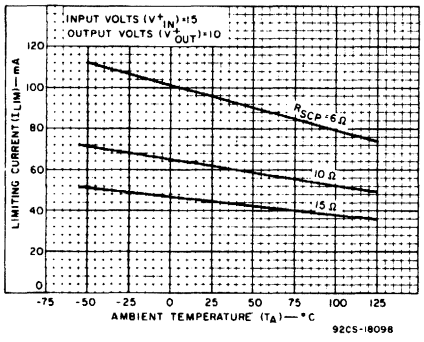


Fig.10–I_{LIM} vs. T_A.

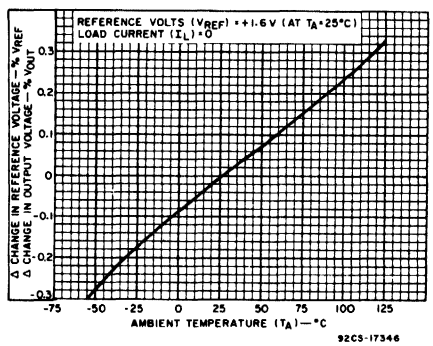


Fig.11–Temperature coefficient of V_{REF} and V_{OUT}.

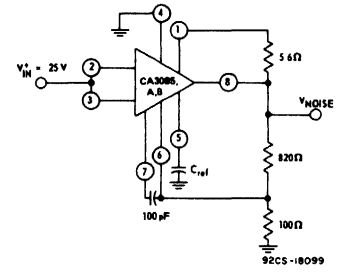


Fig.12–Test circuit for noise voltage.

CA3085, CA3085A, CA3085B Types

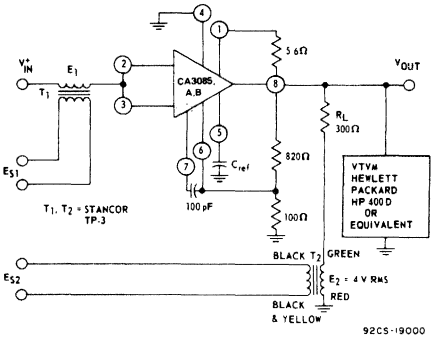


Fig.13– Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25 V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection – I

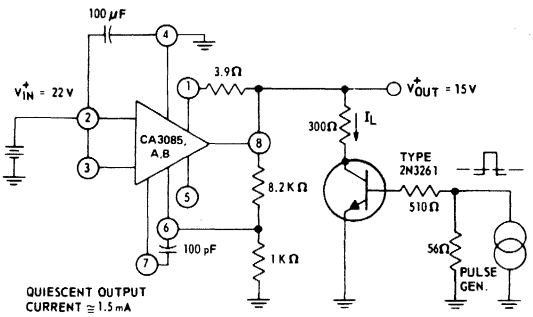
Conditions:

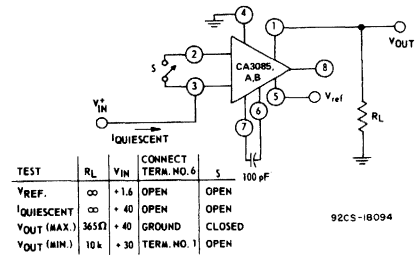
1. V_{IN} = +25 V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection – II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF





TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
V_{REF}	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10 k	+30	TERM. NO. 1	OPEN

Fig.15– Test circuit for V_{REF}, $I_{quiescent}$, V_{OUT}(max.), V_{OUT}(min.).

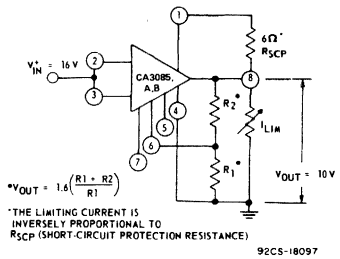


Fig.16– Test circuit for limiting current

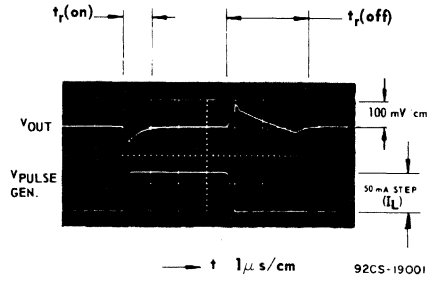


Fig.14– Turn-on and turn-off recovery time test circuit with associated waveforms.

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

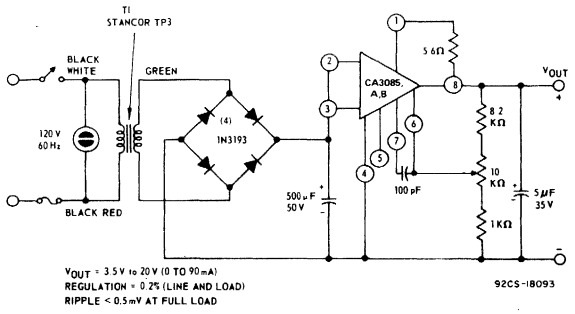
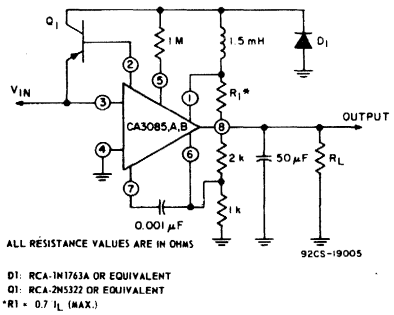
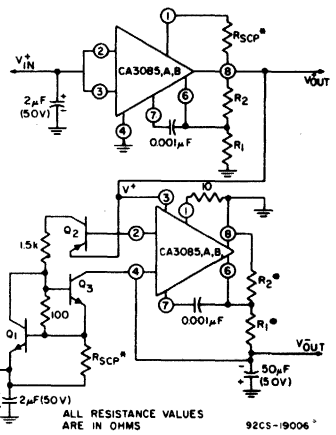


Fig.17– Application of the CA3085 Series in a typical power supply.



D1: RCA-1N1763A OR EQUIVALENT
Q1: RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.18– Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1 RCA-2N2102 OR EQUIVALENT
Q2 ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

*$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$
*R_{SCP} SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21– Combination positive and negative voltage regulator circuit.

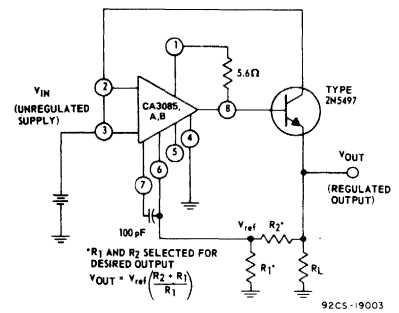


Fig.19– Typical high-current voltage regulator circuit.

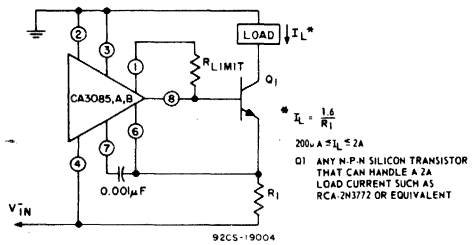


Fig.20– Typical current regulator circuit.

CA3086
General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially– Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

DISSIPATION:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to + 125	°C
Storage	–65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

* The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

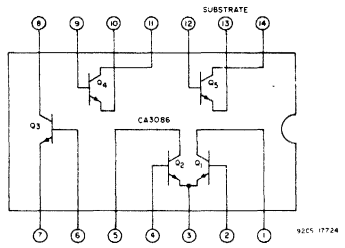


Fig.1 – Functional diagram of the CA3086.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	Typ. Characteristic Curves Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

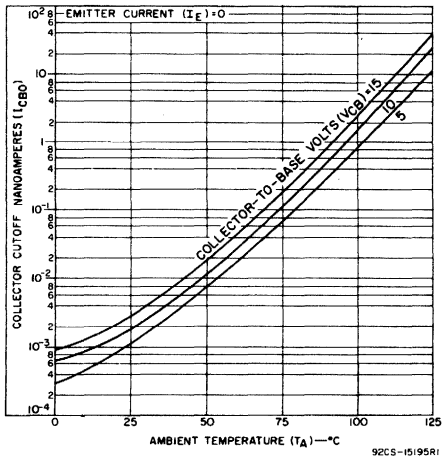


Fig.2– I_{CBO} vs T_A.

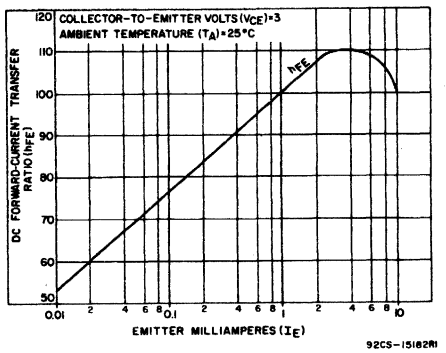


Fig.3– h_{FE} vs I_E.

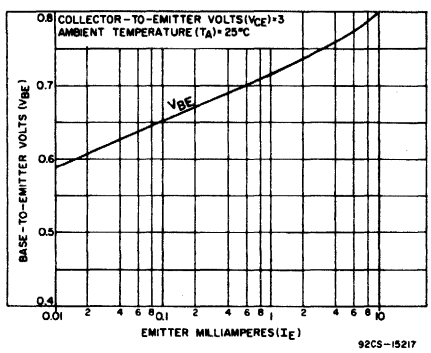


Fig.4 V_{BE} vs I_E.

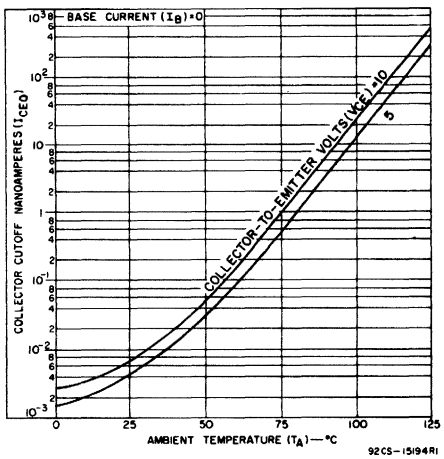


Fig.5– I_{CEO} vs T_A.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

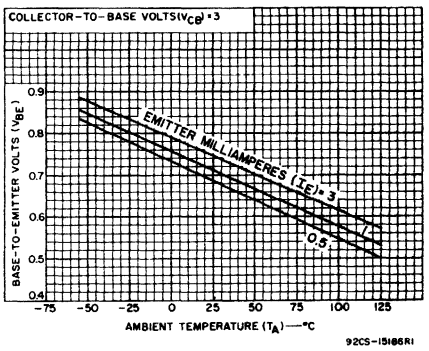


Fig.6– V_{BE} vs T_A.

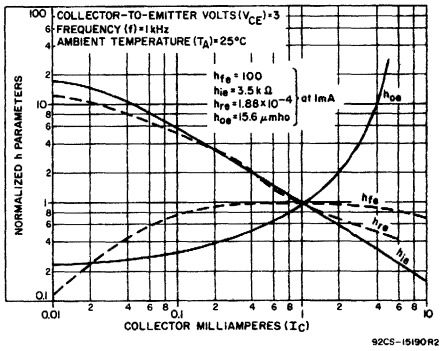


Fig.7– Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

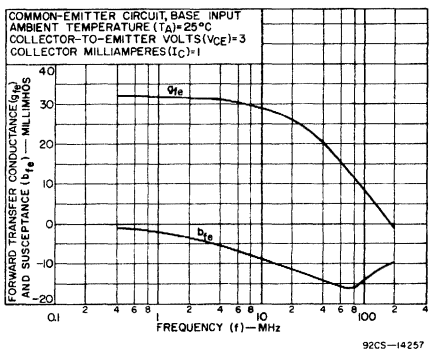


Fig.8– y_{fe} vs f.

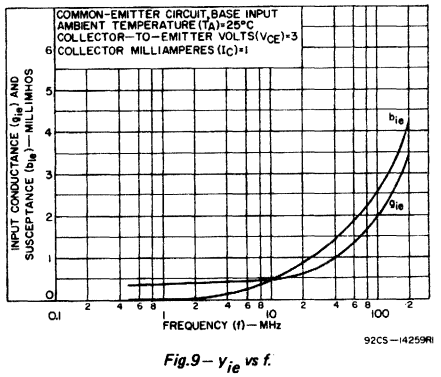


Fig.9– y_{ie} vs f.

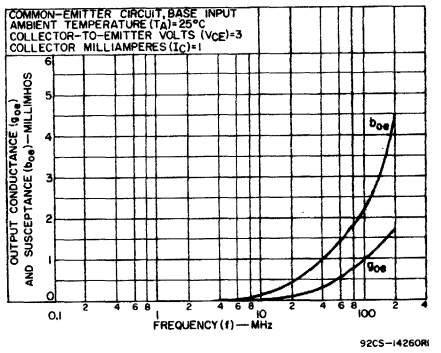


Fig.10– y_{oe} vs f.

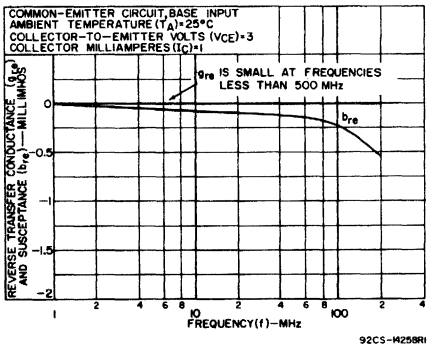


Fig.11– y_{re} vs f.

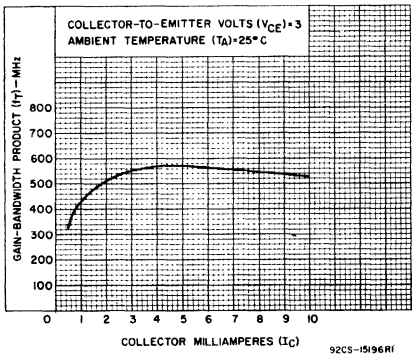


Fig.12– f_T vs I_C.

CA3088E

AM Receiver Subsystem

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- Excellent overload characteristics
- AGC for IF amplifier
- Buffered output signal for tuning meter
- Internal Zener diode provides voltage regulation
- Two IF amplifier stages
- Low-noise converter and first IF amplifier
- Low harmonic distortion (THD)
- Delayed AGC for RF amplifier
- Terminals for optional inclusion of tone control
- Operates from wide range of power supplies: V^+ = 6 to 16 volts
- Optional AC and/or DC feedback on wide-band amplifier
- Array of amplifiers for general-purpose applications
- Suitable for use with optional external RF stage, either MOS or bipolar

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

*Formerly Developmental Type TA5842.

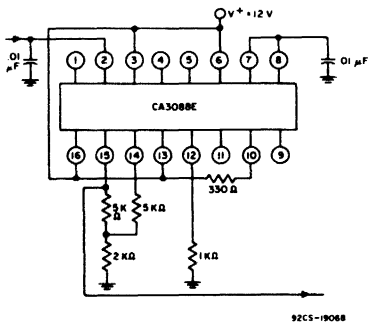


Fig.1–Test circuit for DC characteristics.

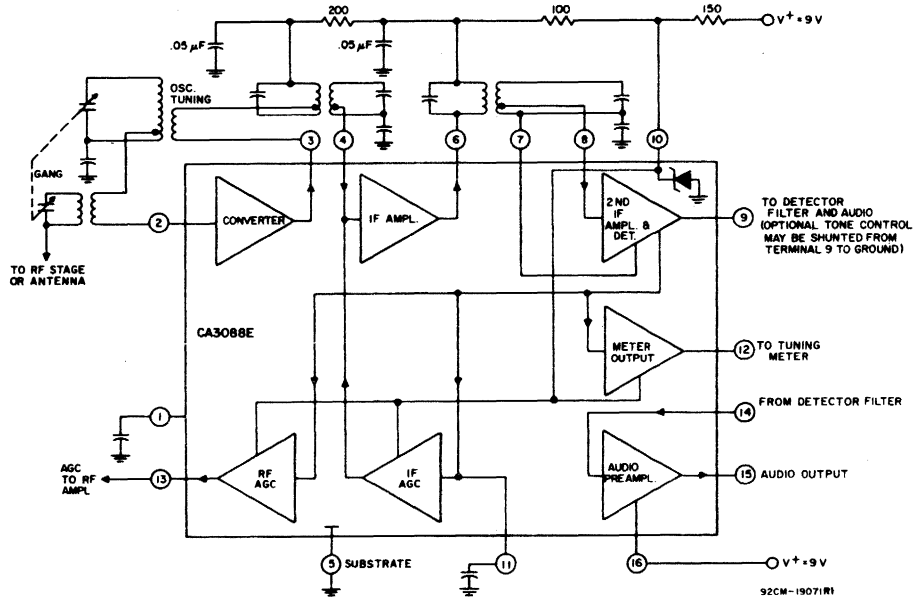


Fig.2–Functional block diagram of the CA3088E.

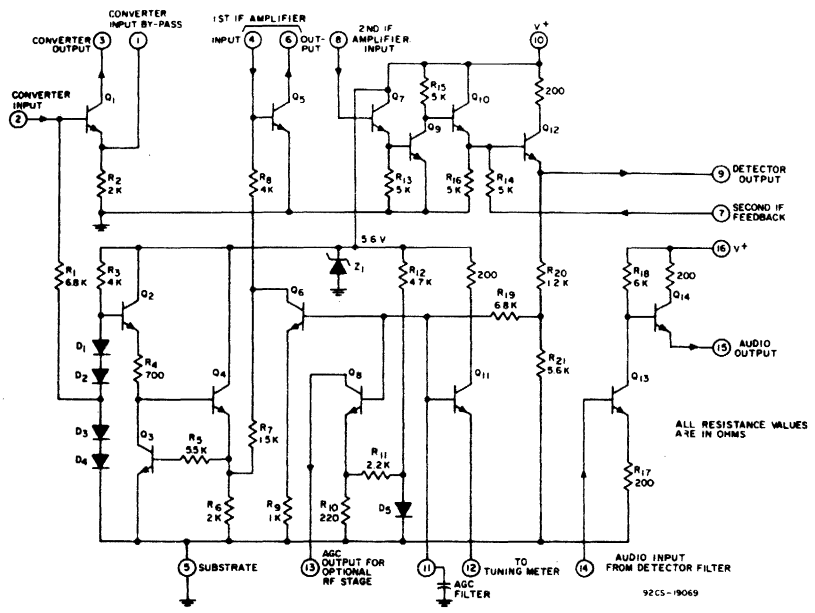


Fig.3–Schematic diagram of the CA3088E.

CA3088E

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V+ = 12 V	TEST CIRCUIT FIG. NO.	TYPICAL VALUES	UNITS
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1, 4, 9, 11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2, 7, 8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_I				
At Transistor Q1				3500	Ω
At Transistor Q5		No AGC,		2000	Ω
Input Capacitance:	C_I				
At Transistor Q1		Input signal frequency		12	pF
At Transistor Q5		(f_{IN}) = 1 MHz		17	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

The typical characteristics for the CA3088E are intended for guidance purposes in evaluating this device for equipment design.

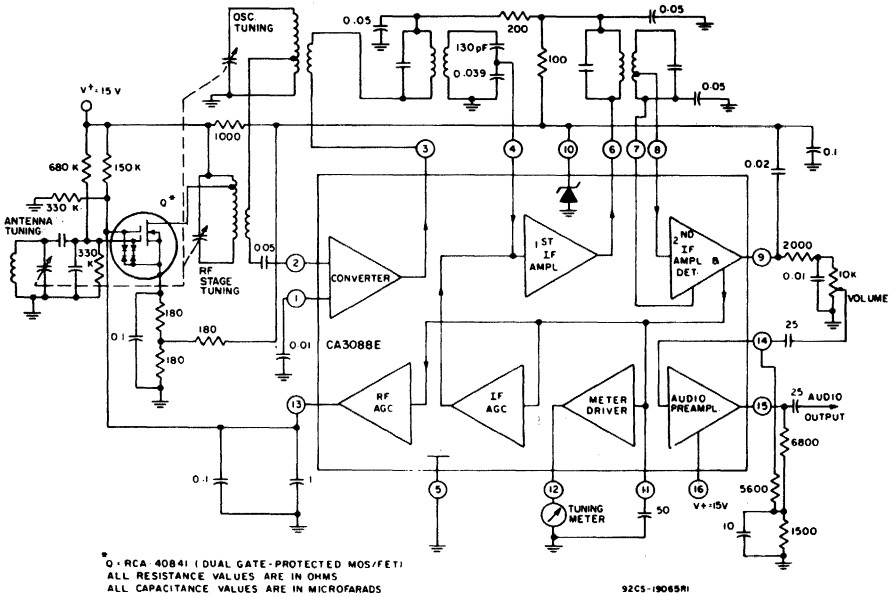


Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

CA3089E

FM IF System

Includes———IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

For FM IF Amplifier Applications in High-Fidelity Automotive, and Communications Receivers

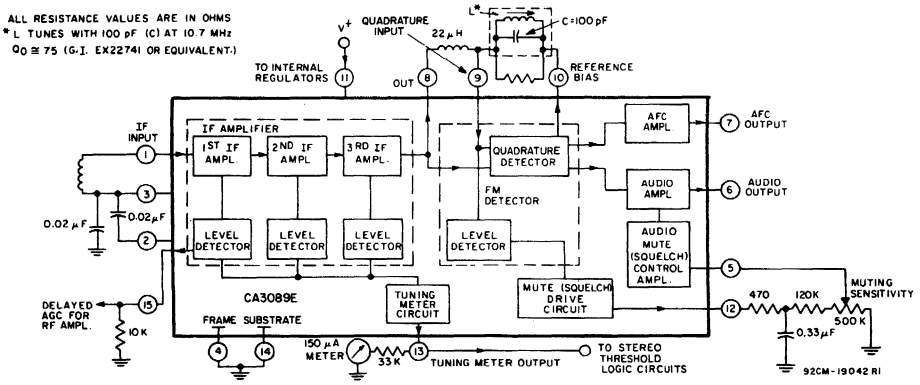


Fig.1-Block diagram of the CA3089E.

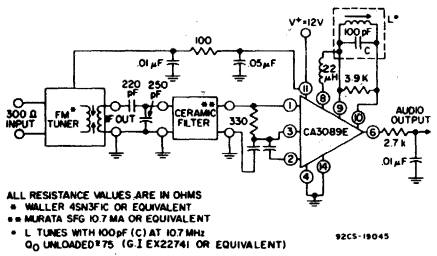
Features:

- **Exceptional limiting sensitivity: 12 μV typ. at −3 dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400 mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply-voltage regulators**

RCA-CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.



Performance data at f_0 = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity . . . . . 2μV (Antenna Level)
20dB Quieting Sensitivity . . . . . 1μV (Antenna Level)
30dB Quieting Sensitivity . . . . 1.5μV (Antenna Level)

Fig.2 - Typical FM tuner using the CA3089E with a single-tuned detector coil.

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25^oC$*

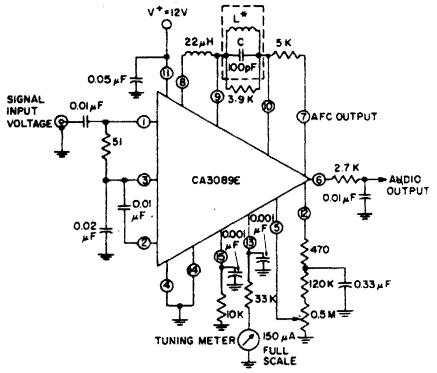
DC Supply Voltage:		
Between Terminals 11 and 4	16	V
Between Terminals 11 and 14	16	V
DC Current (out of Terminal 15)	2	mA
Device Dissipation:		
Up to $T_A = 60^oC$	600	mW
Above $T_A = 60^oC$	derate linearly 6.7 mW/^oC	
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	-65 to +150	^oC
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	^oC

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V^+ = 12$ Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		Circuit Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3, 4	16	23	30	mA
DC Voltages:								
Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 6 (Audio Output)	V_6				5.0	5.6	6.0	V
Terminal 10 (DC Reference)	V_{10}				5.0	5.6	6.0	V
Dynamic Characteristics								
Input Limiting Voltage (-3 dB point)	V_I(lim)	–		3, 4	–	12	25	μV
AM Rejection (Term. 6)	AMR	V_{IN} = 0.1 V, AM Mod. = 30%	f_0 = 10.7 MHz,		45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				300	400	500	mV
Total Harmonic Distortion: *		V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz, Deviation = ±75 kHz					
Single Tuned (Term. 6)	THD			3	–	0.5	1.0	%
Double Tuned (Term. 6)	THD			4	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3, 4	60	67	–	dB

* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

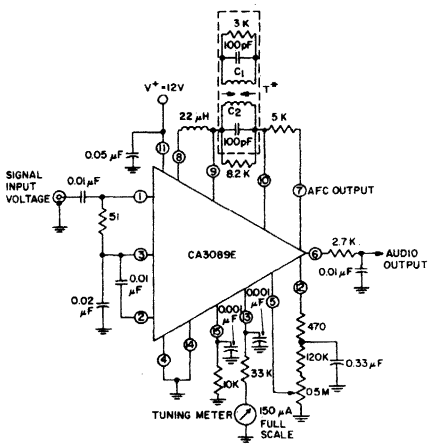
CA3089E



ALL RESISTANCE VALUES ARE IN OHMS
*L: TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19040R1

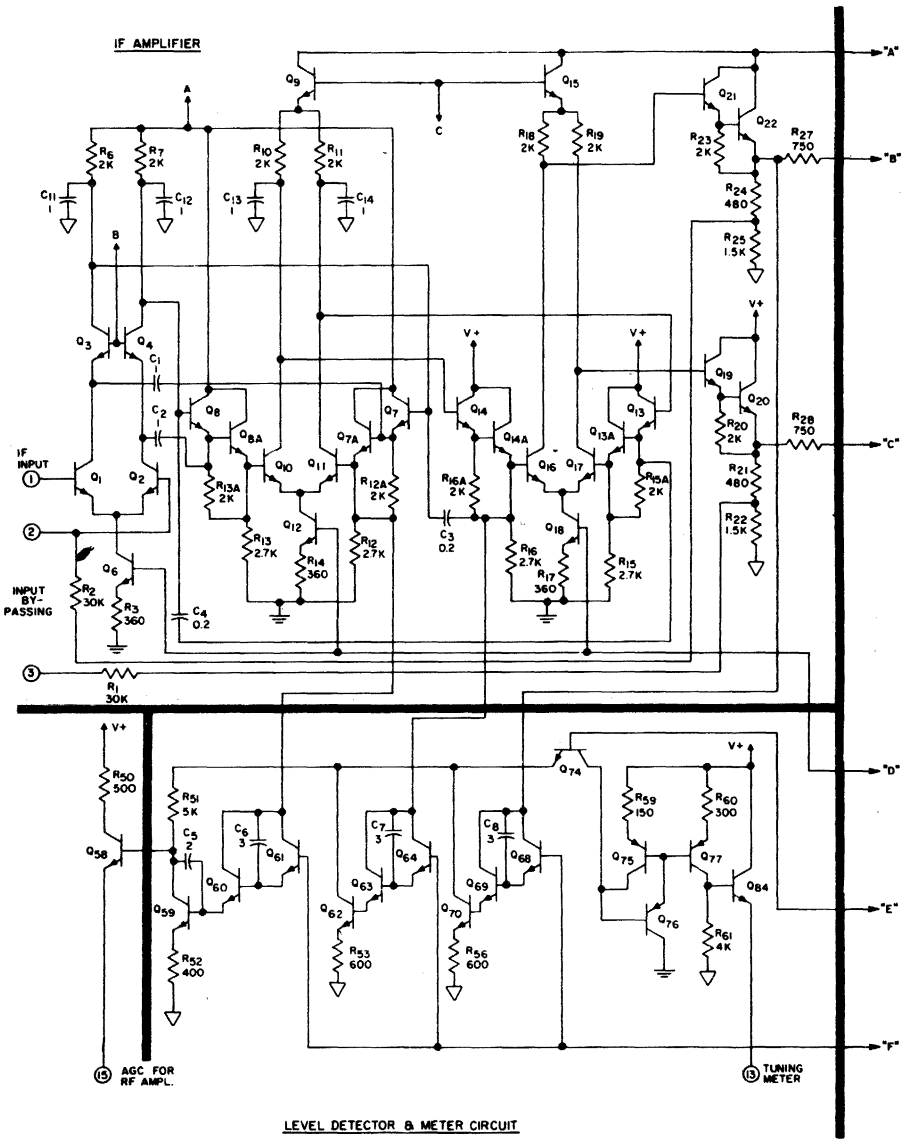
Fig.3-Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
* T: PRI. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 t OF 34ø ON 7/32" DIA. FORM
SEC. – Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 t OF 34ø ON 7/32" DIA. FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70 %
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19041R1

Fig.4-Test circuit for CA3089E using a double-tuned detector coil.



LEVEL DETECTOR & METER CIRCUIT

Fig.5-Schematic diagram of the CA3089E.

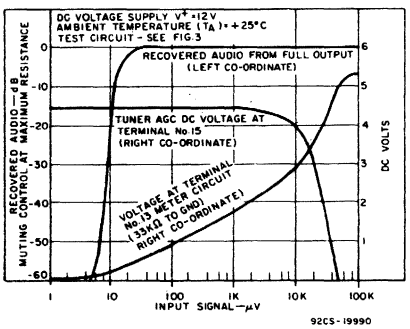


Fig.6-Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

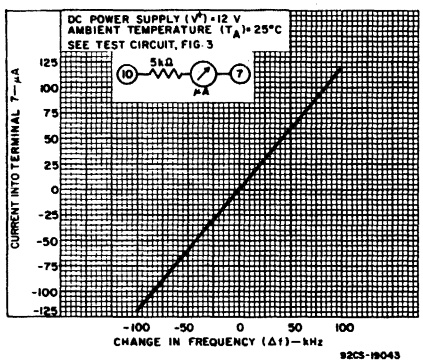


Fig.7-AFC characteristics (current at Term. 7 as a function of change in frequency).

CA3089E

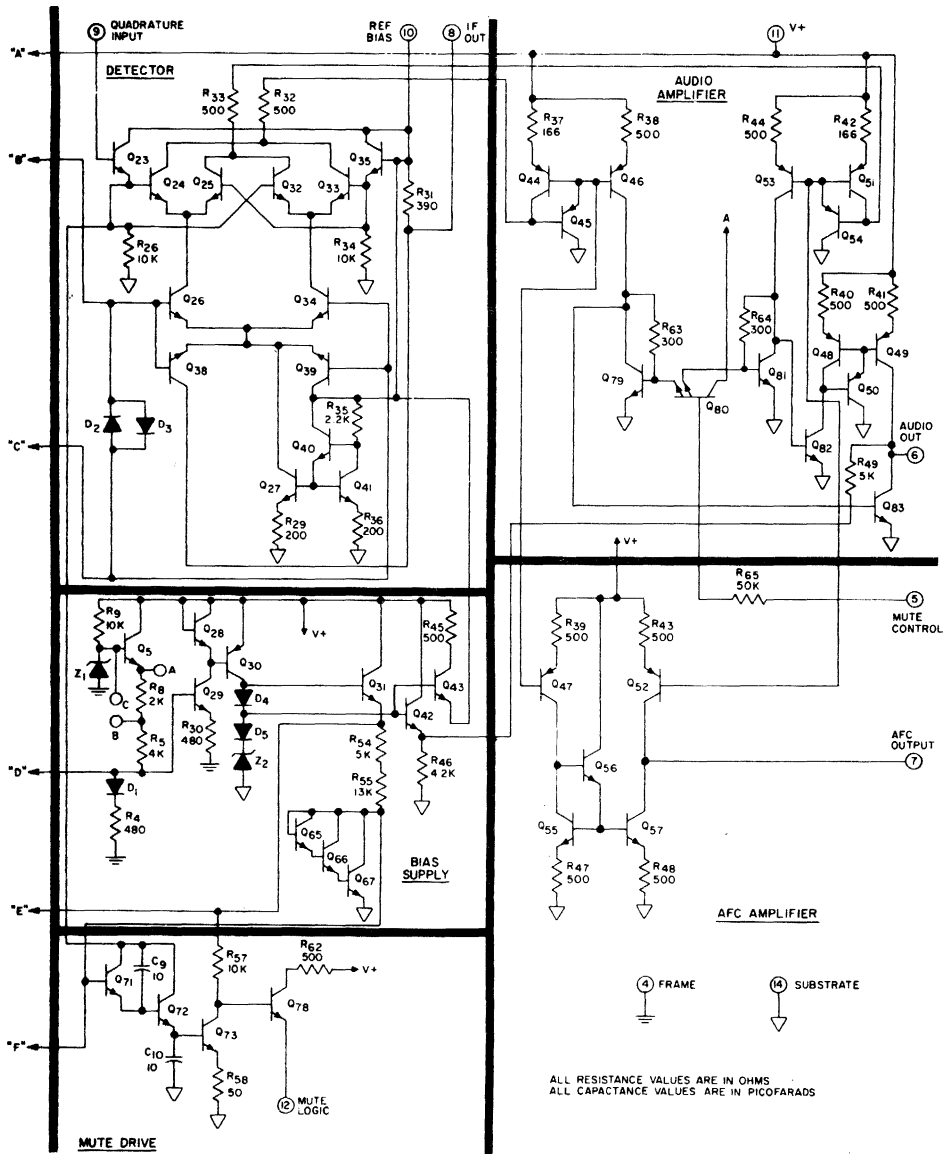
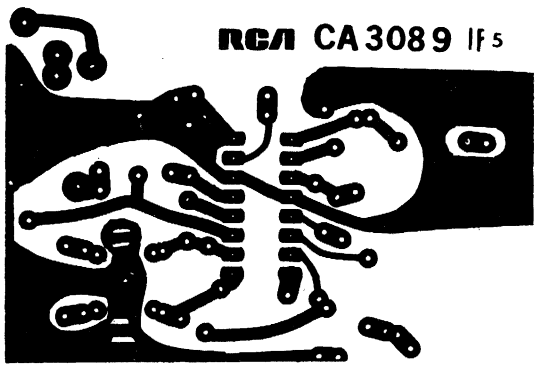


Fig.5 - Schematic diagram of the CA3089E.



a) Bottom view of printed-circuit board.

b) Component side — top view.

Fig.8-Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.

CA3090AQ

Stereo Multiplex Decoder

For FM Stereo Multiplex Systems

RCA-CA3090AQ , a monolithic silicon integrated circuit, is a stereo multiplex decoder intended for FM multiplex systems.

The CA3090AQ is the successor to the CA3090Q; it offers three major advantages over the CA3090Q as follows:

1. Can directly drive a stereo indicator lamp with a current drain of up to 100 mA.
2. Stereo Defeat/Enable control-voltage specifications.
3. Capable of operation with lower distortion.

This stereo multiplex decoder requires only one low-inductance tuning coil (requires only one adjustment for complete alignment), provides automatic stereo switching, energizes a stereo indicator lamp, and operates from a wide range of voltage supplies.

Figure 1 shows the block diagram for the CA3090AQ. The input signal from the detector is amplified by a low-distortion preamplifier and simultaneously applied to both the 19-kHz and 38-kHz synchronous detectors. A 76-kHz signal, generated by a local voltage-controlled oscillator (VCO), is counted down by two frequency dividers to a 38-kHz signal and to two 19-kHz signals in phase quadrature.

The 19-kHz pilot-tone supplied by the FM detector is compared to the locally generated 19-kHz signal in a synchronous detector. The resultant signal controls the voltage controlled oscillator (VCO) so that it produces an output signal to phase-lock the stereo decoder with the pilot tone. A second synchronous detector compares the locally generated 19-kHz signal with the 19-kHz pilot tone. If the pilot tone exceeds an externally adjustable threshold voltage, a Schmitt trigger circuit is energized. The signal from the Schmitt trigger lights the stereo indicator, enables the 38-kHz synchronous detector, and automatically switches the CA3090AQ from monaural to stereo operation. The output signal from the 38-kHz detector and the composite signal from the preamplifier are applied to a matrixing circuit from which emerge the resultant left and right channel audio signals. These signals are applied to their respective left and right post amplifiers for amplification to a level sufficient to drive most audio amplifiers.

The CA3090AQ may be used without the stereo defeat/enable function (see Fig. 6) if a control voltage for this function is not readily available. In this case, Terminal 4 should be grounded.

The CA3090AQ utilizes the 16-lead quad-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C.

Features:

- **Requires the use of only one low-inductance tuning coil**
- **Automatic stereo switching**
- **Directly drives a stereo indicator lamp up to 100 mA**
- **Includes driver for stereo-lamp indicator**
- **Operates from a wide range of power supplies: 10 to 16 volts**
- **Requires only one adjustment for alignment**
- **Switching from monaural to stereo and stereo to monaural produces no audible thumps**
- **Low distortion: under 0.22% (typ.)**
- **Separate dc input permits stereo defeat or enable**
- **High signal output: directly drives audio amplifiers**
- **Excellent SCA (storecast) rejection: 55 dB typ.**
- **High audio channel separation: 40 dB typ.**

MAXIMUM RATINGS, ***Absolute-Maximum Values at T_A = 25°C***

DC SUPPLY VOLTAGE	16 V
CURRENT AT TERM. 12	100 mA
INPUT SIGNAL VOLTAGE (COMPOSITE)■	400 mV
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

■ For stereo operation, a minimum input signal voltage (composite) of 40 mV is required.

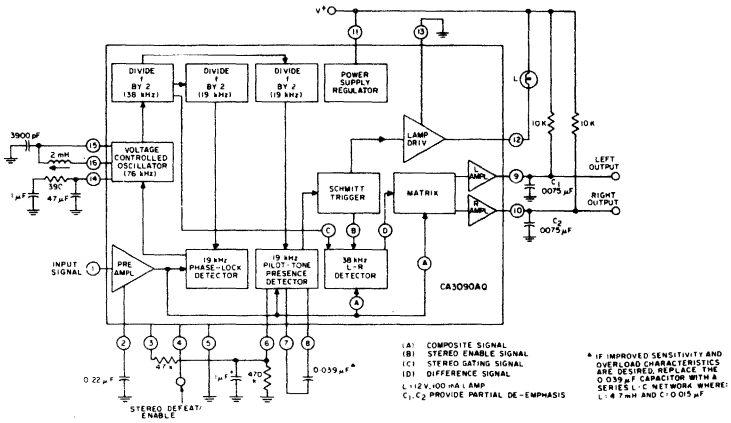


Fig. 1 – Functional block diagram of the CA3090AQ.

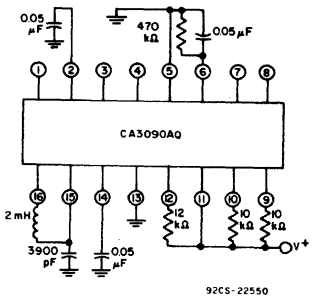


Fig. 2 – Test circuit for DC characteristics.

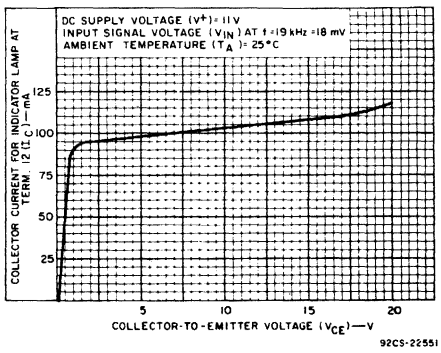


Fig. 3 – Indicator lamp characteristics (I_C vs. V_{CE}).

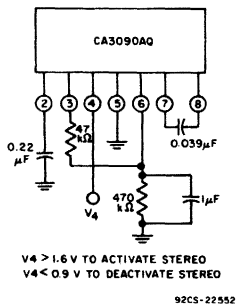


Fig. 4 – Test circuit for use with stereo defeat/enable.

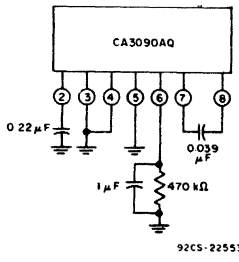


Fig. 5 – Test circuit for use without stereo defeat/enable.

CA3090AQ

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS $T_A = 25°C$, V+ = 12 V (unless specified otherwise)	LIMITS Min.	Typ.	Max.	UNITS
Static Characteristics						
Total Current (Terms. 9, 10, 11)	I_{total}	Lamp OFF	–	22	27	mA
DC Voltage: Term. 1	V_1		1.6	2.3	3.1	V
Term. 6 (Indicator Lamp OFF)	V_6		–	2.1	3.6	V
Terms. 9 and 10	$V_{9\ \&\ 10}$		4.7	6.4	8.4	V
Term. 12 (Indicator Lamp OFF)	V_{12}	$V^+ = 16$ V	12.7	–	–	V
Voltage Differential (Term. 2–Term. 1)	$V_2 - V_1$		–	0	0.1	V
Current at Term. 12 (In actual use external circuit resistance (e.g. lamp should limit Term. 12 to the maximum rated value of 100 mA.)		V_{IN} (at f = 19 kHz) = 18 mV	75	100	–	mA
Dynamic Characteristics						
Input Impedance	Z_{IN}		–	50k	–	Ω
Channel Separation (L + R Reference)*		V_{IN} = 180 mV	25	40	–	dB
Channel Balance (Monaural)			–	0.3	3	dB
Monaural Gain			3	6	9	dB
Stereo/Monaural Gain Ratio*			–	±0.3	±3	dB
Indicator Lamp – Turn-ON Voltage		19-kHz pilot-tone @ Term. 1	–	4	–	mV
Capture Range (Deviation from 76-kHz center frequency)		19-kHz pilot-tone voltage = 18 mV	±6.6	±10	–	%
Distortion (75-μs de-emphasis): 2nd Harmonic		V_{IN} = 240 mV	–	0.2	–	%
3rd, 4th, and 5th Harmonic			–	<0.1	–	%
19-kHz Rejection			–	35	–	dB
38-kHz Rejection			–	48	–	dB
SCA (storecast) Rejection			–	70	–	dB
Stereo Defeat Voltage (V_4)			–	1.2	<0.9	V
Stereo Enable Voltage (V_4)			>1.6	1.2	–	V

* For stereo operation, test conditions require a composite stereo input signal (modulated at 1 kHz) including a 19-kHz (18 mV) pilot-tone signal.

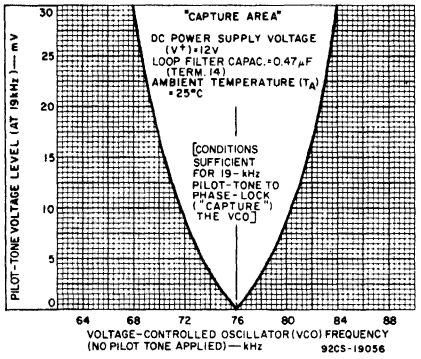


Fig. 7 – Pilot-tone voltage level vs. VCO frequency with no pilot-tone applied.

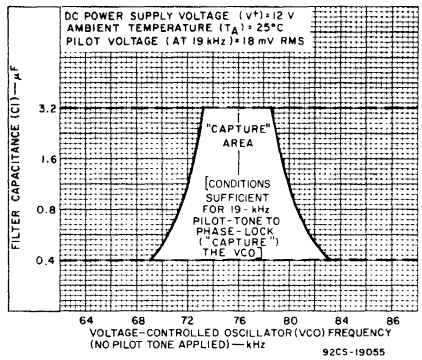


Fig. 8 – Filter capacitance vs. VCO frequency with no pilot-tone applied.

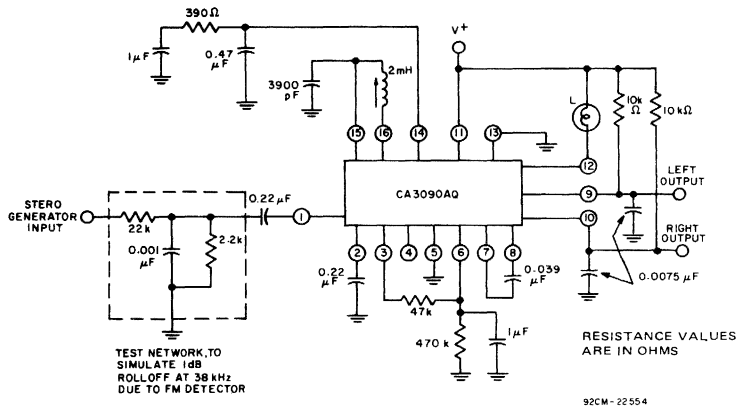
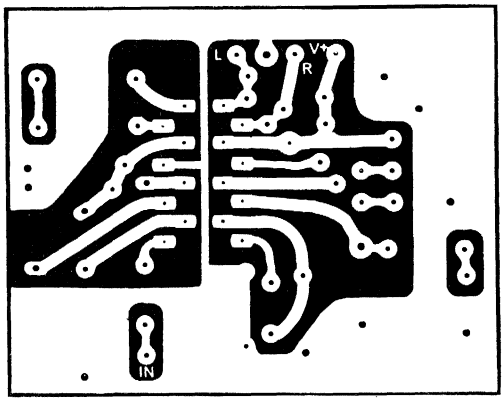
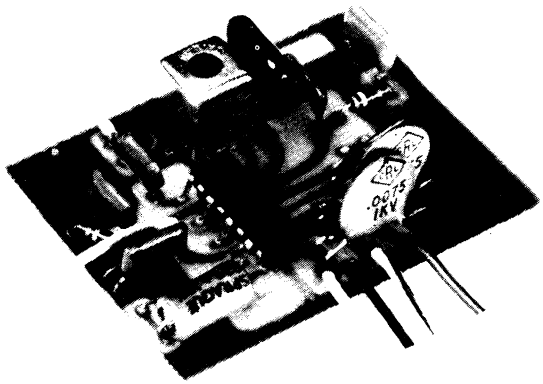


Fig. 6 – Test circuit for measurement of dynamic characteristics.



A–Foil side.



B–Component side.

Fig. 9 – Photographs of the CA3090AQ and outboard components mounted on a 2 X 2½-inch printed-circuit board to constitute a complete stereo multiplex decoder.

CA3091D

RCA-CA3091D, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage-controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

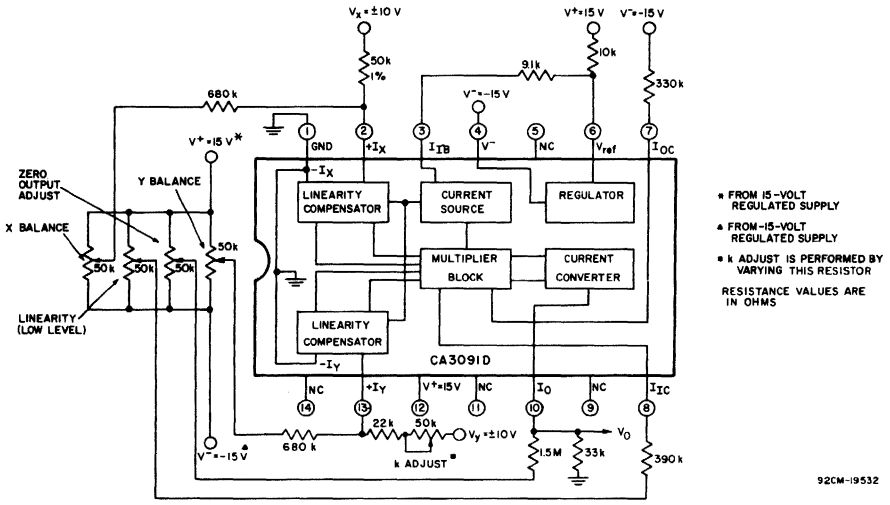


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard(peripheral)circuitry.

MAXIMUM RATINGS; *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration	No limitation	
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.

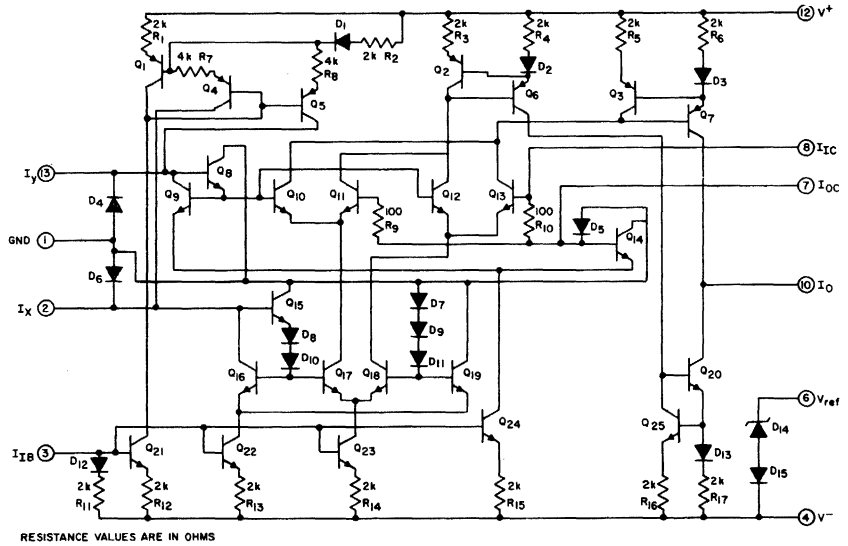


Fig.2—Schematic diagram of the CA3091D.

Features: •

- **"Accuracy": ±4% (max.)**
- **"Linearity": 3.0% (max.)**
- **Feedthrough: 9 mV p-p (typ.)**
- **3-db bandwidth: 4.4 MHz**
- **Low power operation capability: ±6.0 V, 4 mW drain**
- **Low power-supply sensitivity: 36 mV/V typ.**
- **Smooth overload characteristics — no foldback if full-scale input signal is exceeded**
- **Negligible warm-up drift**
- **Broadband operation capability (flat to 1 MHz) — both inputs have similar characteristics for reduced high-frequency phase shift between the inputs**
- **Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy**
- **All multiplication is performed with wideband circuitry — this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multiplier's bandwidth**
- **High immunity to parasitic oscillation**
- **Essentially free from excess peaking — provides improved frequency response**
- **Requires no level shifting at the output — current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier**
- **Internal bias regulator**

Applications:

- **Multiplier** ■ **Divider** ■ **Squarer** ■ **Square Rooter**
- **Power-series approximator**
- **Full-wave rectifier**
- **Automatic level controller**
- **RMS converter**
- **Frequency discriminator**
- **Voltage-controlled filters and oscillators**

CA3091D

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = -15 V	TEST CONDITIONS: Circuit and/or Char. Curve	LIMITS: Min.	LIMITS: Typ.	LIMITS: Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	-20	-2.1	+20	μA
At y Input		y = 0	–	-20	-8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	-34	-2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = 0,	–	-10	-0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	-0.330	-0.0076	+0.330	V
Output Peak Current Swing	$\|I_O\|$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\|V_O\|$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = 0			–	–	9	20	mV p-p
At x = 20V p-p, y = 0			–	–	9	20	

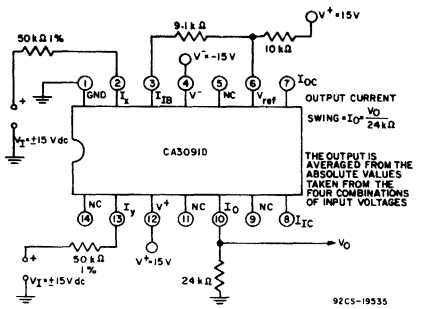


Fig.3—Test circuit for measurement of output current swing capability.

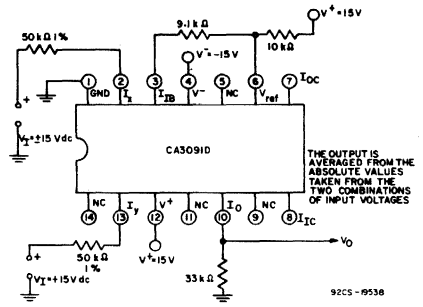


Fig.4—Test circuit for measurement of output voltage swing capability.

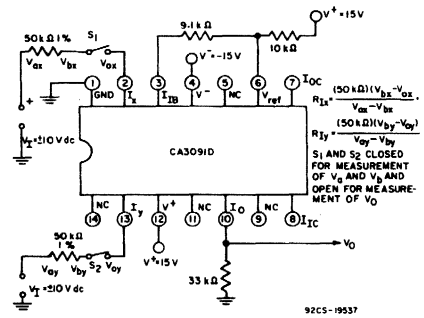


Fig.5—Test circuit for measurement of input resistance.

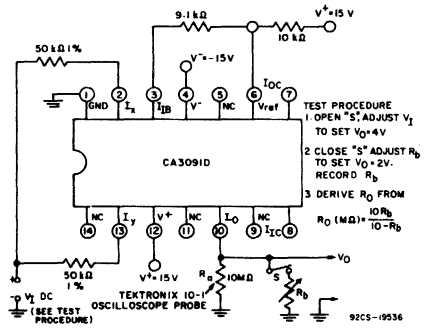


Fig.6—Test circuit for measurement of output resistance.

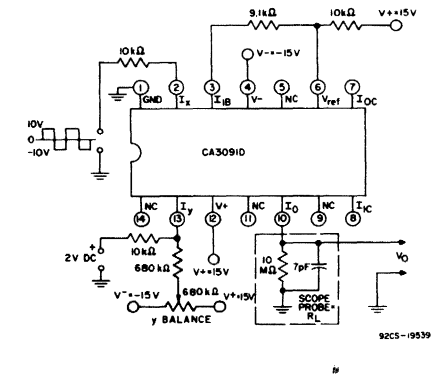


Fig.7—Test circuit for measurement of maximum slew rate.

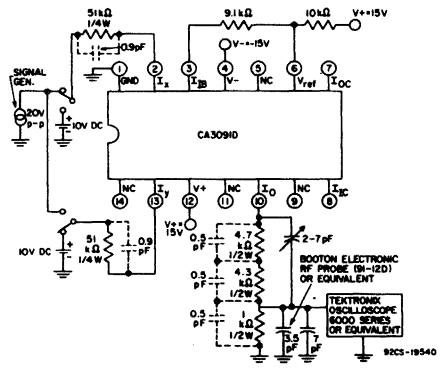


Fig.8—Test circuit for measurement of frequency response.

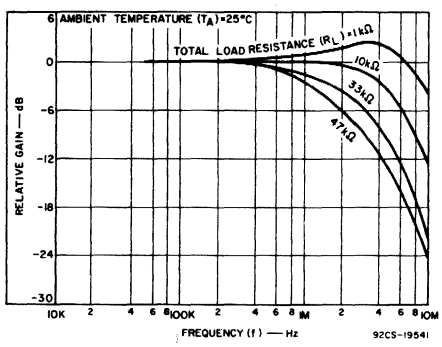
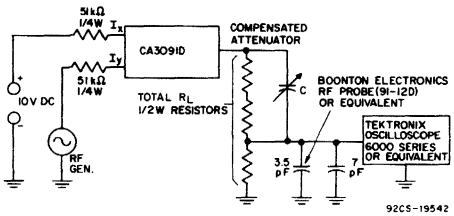


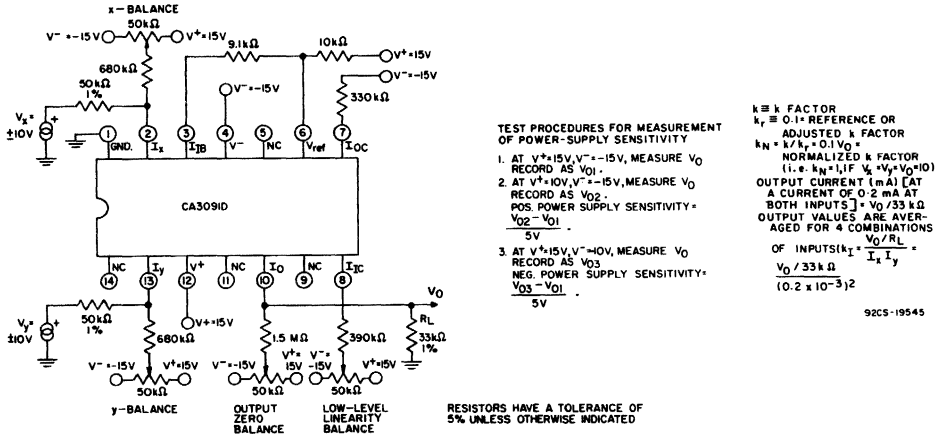
Fig.9- y-input frequency response characteristic curve with associated test circuit.



CA3091D

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = −15 V	Circuit and/or Char. Curve	TYPICAL VALUES	UNITS
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x \rvert \leq 0.2$ mA	5	1.3	kΩ
At y Input		$\lvert I_y \rvert \leq 0.2$ mA		0.5	kΩ
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	MΩ
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{IO}/\Delta T$	x & y = 0	–	−0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = 0	–	−0.063	μA/°C
y-Input Balance Current		y = 0	–	−0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	−0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = 0			–	5.6	mV/°C
At y = 0				5.7	mV/°C



TEST PROCEDURES FOR MEASUREMENT OF POWER-SUPPLY SENSITIVITY

1. AT V^+=15V, V^-=−15V, MEASURE V_O RECORD AS V_{O1}.
2. AT V^+=10V, V^-=−15V, MEASURE V_O RECORD AS V_{O2}. POS. POWER SUPPLY SENSITIVITY = $\frac{V_{O2} - V_{O1}}{5V}$.
3. AT V^+=15V, V^-=−10V, MEASURE V_O RECORD AS V_{O3}. NEG. POWER SUPPLY SENSITIVITY = $\frac{V_{O3} - V_{O1}}{5V}$.

k ≡ k FACTOR
k_r ≡ 0.1 = REFERENCE OR ADJUSTED k FACTOR
$k_N = k/k_r = 0.1\,V_O$ = NORMALIZED k FACTOR (i.e. k_N=1, IF V_x=V_y=V_O=10)
OUTPUT CURRENT (mA) [AT A CURRENT OF 0.2 mA AT BOTH INPUTS] = $V_O/33\,k\Omega$
OUTPUT VALUES ARE AVERAGED FOR 4 COMBINATIONS OF INPUTS ($k_I = \frac{V_O/R_L}{I_x I_y} = \frac{V_O/33\,k\Omega}{(0.2 \times 10^{-3})2}$)

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Fig.11—Test circuit for measurement of current gain and power-supply sensitivity.

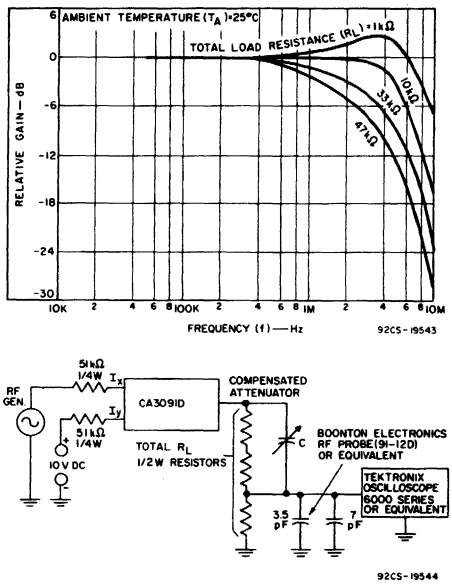

Fig.10- x–input frequency response characteristic curve with associated test circuit.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance — Converts the input voltage to an input current.

R_L
Output (Load) Resistance — Converts the output current to a voltage.

R_O
Output Resistance — See V_O and I_O for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_O = kV_xV_y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2}.$$

V_O
The output product voltage derived from the expression

$$(kV_xV_y = V_O)$$

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V_{ref}.
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_x, V_y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at V_X = 5V and V_Y = −3V indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\,\text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

i_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_I^2/R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

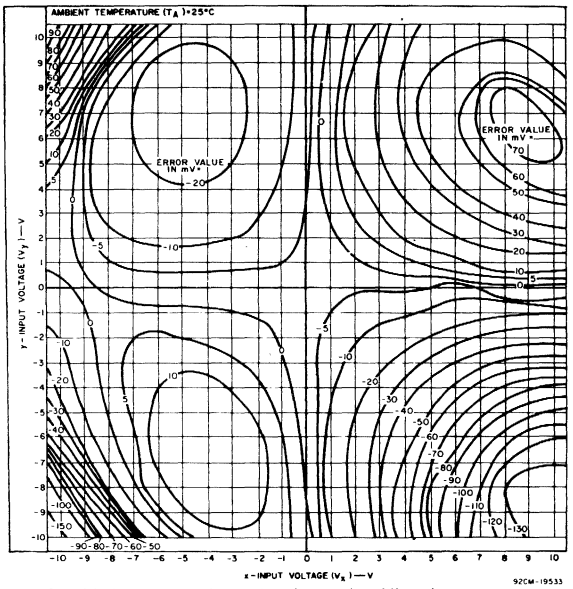
I_x, I_y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_I^2/R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_x + V_{xe})(V_y + V_{ye}) = V_o + V_{oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_x, V_y = the external inputs to be multiplied

V_o = the desired value of the product output signal

V_{xe}, V_{ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_X) with the external gain controlling signal (V_Y) to produce the resultant output (V_O). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

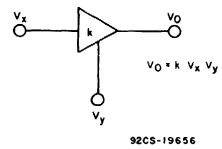
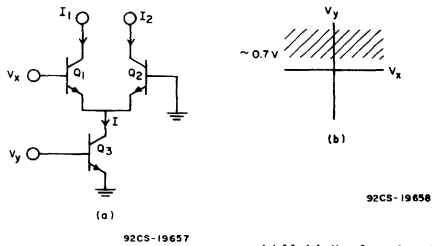


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_X) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_Y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_X) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_Y) the output current ($I_1 - I_2$), therefore, is related to both V_X and V_Y.



a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_X V_Y \qquad \text{(Eq. 1)}$$

where k' is a constant

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Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_X and V_Y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_X = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1+i_4 = i_2+i_3$.
   Since $I_1 = i_1+i_4$ and $I_2 = i_2+i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_Y
2. Now assume $V_Y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1+i_2$ and $i_6 = i_3+i_4$,
   then $i_1+i_2 = i_3+i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1+i_4 = i_3+i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_X.

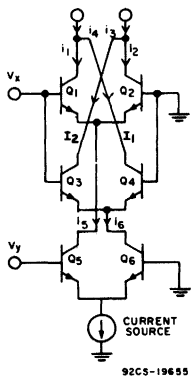


Fig.15—Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_X nor V_Y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k'V_XV_Y.$$

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_X or V_Y is 0. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that may occur between Differential Amplifiers A and B, an external potentiometer is connected to Terminals 7 and 8 (See Fig. 1). The Current Converter circuit, which consists of a set of current mirrors, supplies the output current ($I_1 - I_2$). It is important that circuit unbalances be corrected prior to operation. Table I describes the alignment procedures for correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is available for performing the four basic applications, such as, multiplying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $0 < V_Y \leqslant 10V$ and $-10V \leqslant V_Z \leqslant 10V$. Note, the range of V_Y is limited to the positive polarity; if V_Y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

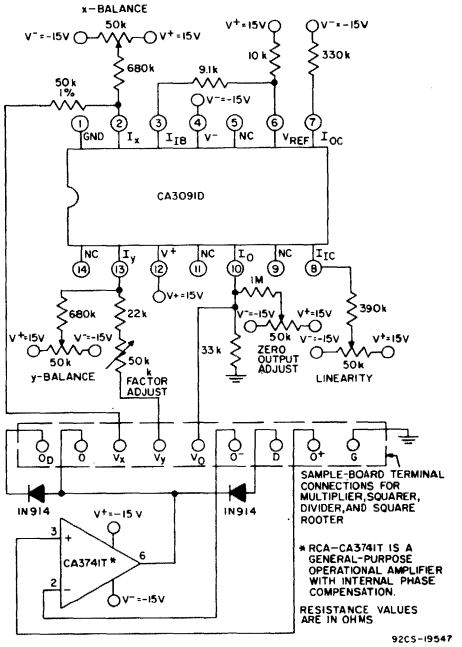
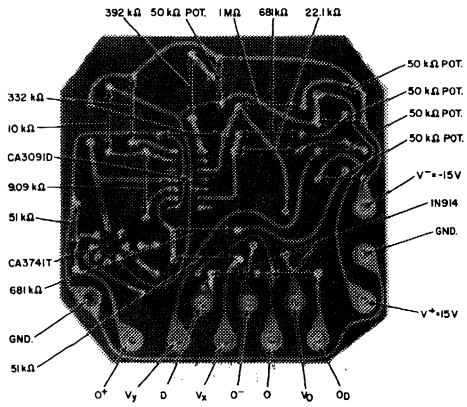
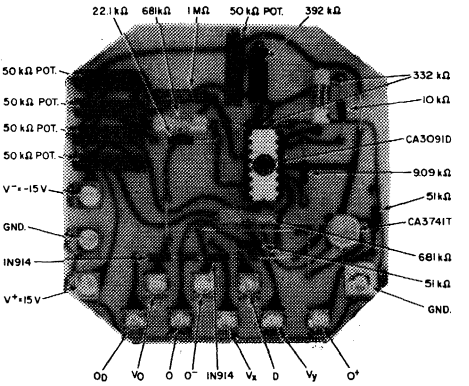


Fig.16—Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.



b) Component side.

Fig.17—Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_X	V_Y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	0	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	0	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Steps 1 and 2 until no further improvement is noted.
5	V_{IM}	0	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	0	0	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V_{MID}^2/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

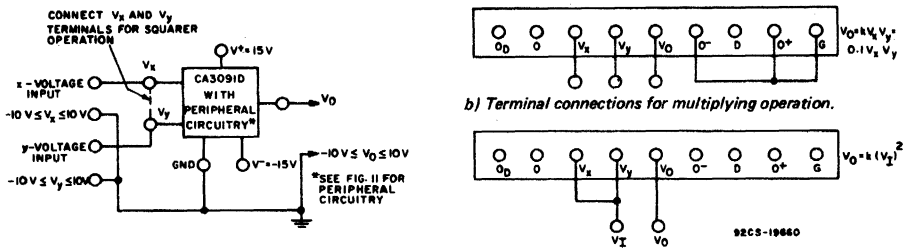
V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm resistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

CA3091D

Table II — Divider Alignment Procedure

Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	–	–	–	–	–	–	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac – VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc – VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac – VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc – VM	k_{adjust}	Adjust for 10 V dc output.



a) Circuit arrangement for multiplier or squarer operation.

b) Terminal connections for multiplying operation.

c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

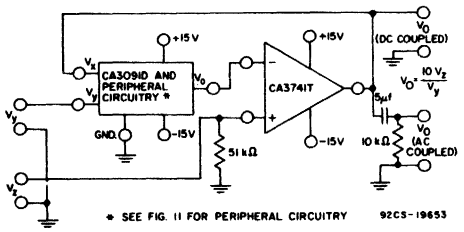


Fig.19—(a) Divider alignment circuit.

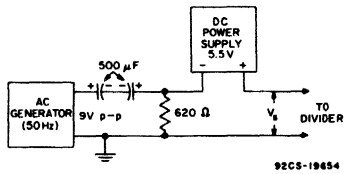
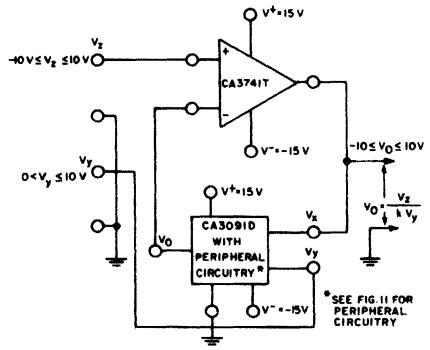
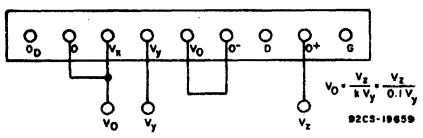


Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.

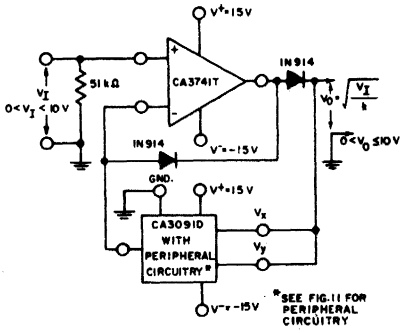


a) Circuit arrangement for divider operation.

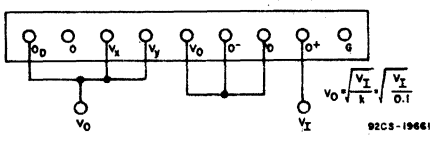


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

CA3093E

General-Purpose High-Current N-P-N Transistor-Zener Diode-Diode Array

RCA CA3093E* is a versatile array of three high-current (to 100mA) NPN transistors, two 10%-tolerance Zener diodes and one conventional diode, all on a common monolithic substrate. Two of the transistors (Q_1 and Q_2) are matched at 1 mA for applications in which offset parameters are of special importance. The combination of positive Zener voltage temperature coefficients and negative forward base-emitter voltage temperature coefficients provides a unique temperature compensation capability.

Independent connections for each transistor and diode plus a separate terminal for the substrate permit maximum flexibility in circuit design.

*Formerly developmental type TA6119

#Z_1, Z_2 and D1 are transistors internally connected as shown below.

Features:

- 6 independent devices plus separate substrate connection
- Compensating temperature coefficients – V_{BE} and V_{D1} vs. V_Z

Transistors

- High I_C (100mA max)
- Matched pair (Q1 & Q_2)
  V_{IO} = ± 5mV max
  I_{IO} = 2.5 μA max
  } at I_C = 1mA
  $\Delta V_{IO}/\Delta T$ = 5 μV/°C typ
- h_{FE} = 40 min @ I_C = 10mA
  or 50mA
- Low V_{CEsat} . . . 0.7V max @ 50mA

Zener Diodes

- Two 1/4W Zeners
- V_Z = 7V ± 10%
- z_Z = 15Ω typ

Diode

- Close forward voltage match to V_{BE}'s of Q_1 and Q_2
- V_{PIV} = 5.5V min.

Applications

- Signal processing and switching systems operating from DC to VHF
- Lamp and relay driver
- Differential amplifier
- Temperature-compensated amplifier
- Thyristor firing
- Temperature-compensated shunt regulator
- Temperature-compensated series regulator
- Level shifting
- Voltage-level clamping
- Current regulator
- Voltage clamping
- Simple off-line regulated supply
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for applications in addition to those given on pages 5 & 6 of this bulletin.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Power Dissipation:

Any one transistor	500	mW
Any one Zener Diode	250	mW
Total package	750	mW
Above 25°C . . . Derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

The following maximum ratings apply for each transistor

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5.5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	35	mA

The following maximum ratings apply for each Zener Diode or Diode

Zener Diode dc Current (I_Z)	35	mA
Zener Diode-to-Substrate Voltage (V_{ZIO})*	20	V
Diode (D1) Forward Current (I_{DF})	50	mA
Diode (D1) Reverse Voltage (V_{DR})	5.5	V
Diode (D1)-to-Substrate Voltage (V_{DIO})*	20	V

*The collector of each transistor, the cathode of each Zener diode, and the anode of the diode are isolated from the substrate by an internal diode. The substrate must be connected to a voltage which is more negative than any of these isolated terminals in order to maintain isolation between devices and provide normal transistor action. To avoid undesired coupling between devices, the substrate terminal (5) should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

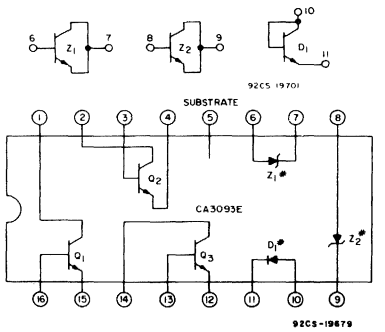


Fig. 1 – Functional diagram of the CA3093E (bottom view)

TYPICAL STATIC CHARACTERISTICS

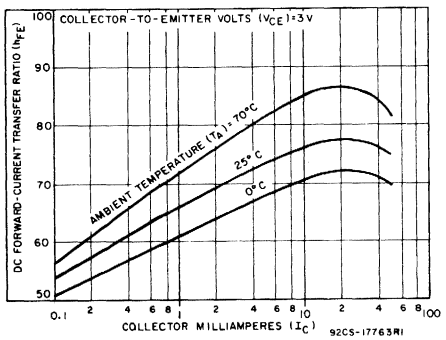


Fig. 2 – h_{FE} vs I_C

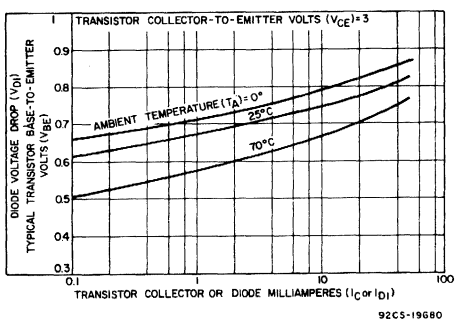


Fig. 3 – V_{BE} vs I_C and V_{D1} vs I_{D1}

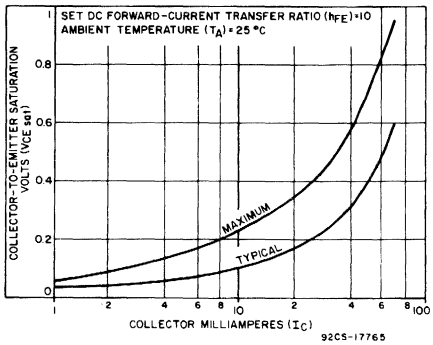


Fig. 4 – V_{CEsat} vs I_C at 25°C

CA3093E

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	μA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	–	
		V_{CE} = 3V, I_C = 50mA	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE}/\Delta T$	I_E = 10mA	–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	0.7	2.5	μA
Temp. Coefficient of Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$	–	–	5	–	μV/°C
For Each Zener Diode						
Zener Voltage	V_Z	I_Z = 10mA	6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz	–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V	–	–	1	μA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA	– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100μA (Terminals 7 & 9)	20	60	–	V
Dissipation		Refer to Example in Application "a"	–	–	250	mW
For Diode (D1)						
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V	0.65	0.74	0.85	V
Diode Forward Current	I_{DF}		–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500μA	5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100μA (Terminal 10)	20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA	–	-1.9	–	mV/°C

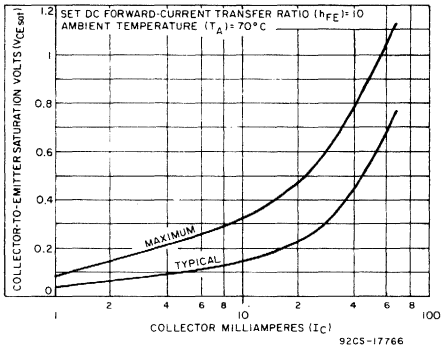


Fig. 5 – V_{CEsat} vs I_C at 70°C

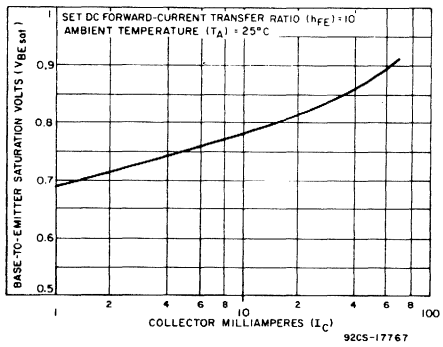


Fig. 6 – V_{BEsat} vs I_C

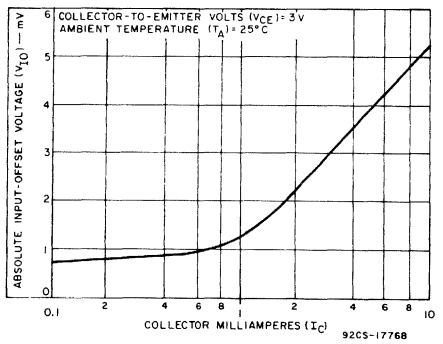


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

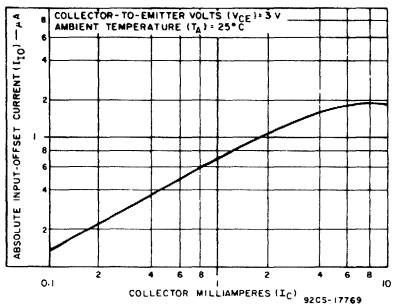


Fig. 8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

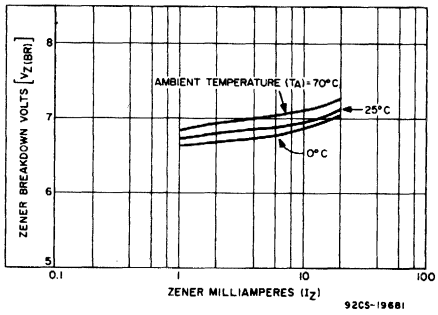


Fig. 9 – Typical Zener breakdown voltage vs current

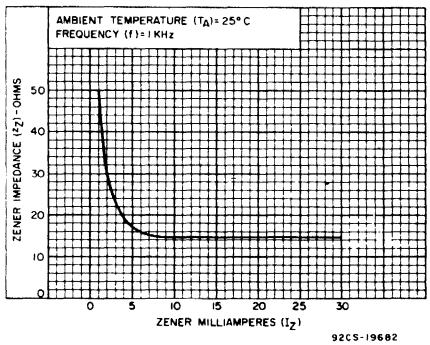
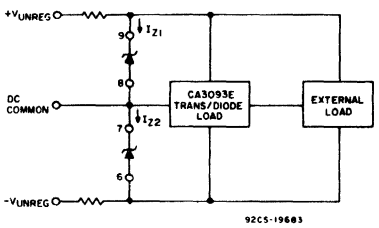


Fig. 10 – Typical Zener impedance vs current

CA3093E

TYPICAL APPLICATIONS

a) ±7V Regulator supplying CA3093E Transistors plus an external load.



Sample Computation for Determining Permissible Zener Dissipation at +25°C.

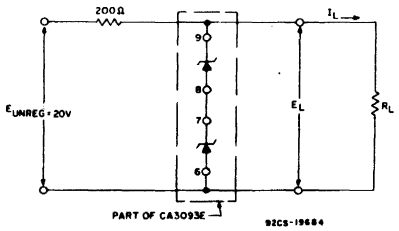
CA3093E Ratings at T_A = +25°C
Total Diss. Max = 750 mW (Derate @ 6.67 mW/°C above 25°C)
Each Zener Diss. Max = 250 mW
Max. Zener Current = 35 mA

Assume CA3093E Transistor/Diode Load Dissipation = 350 mW then max. total Zener Diss. ($P_{Z1} + P_{Z2}$) = 750 - 350 = 400 mW

$(I_{Z1} + I_{Z2})$ max = $\frac{400\ mW}{7V}$ = 57 mA

(Note: Max. current rating on each Zener is 35 mA)

b) 14V Regulator for Q1, Q2, Q3



Typical Load Regulation for I_L = 0 to 25 mA

$\Delta E_L/E_L \times 100 \approx -6\%$ (no load to full load)

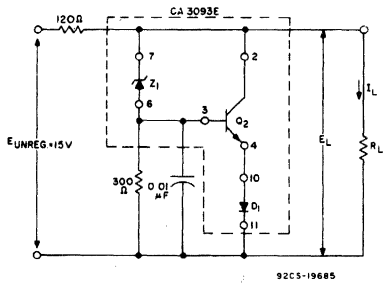
Typical Line Regulation

$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ unreg.} \approx \pm 0.9\%/V$

Typical Temperature Characteristic

$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = +0.05\%/°C$

c) 8.6V Temp.-Compensated Shunt Regulator



Typical Temperature Characteristic @ R_L = 330Ω

$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm 0.007\%/°C$

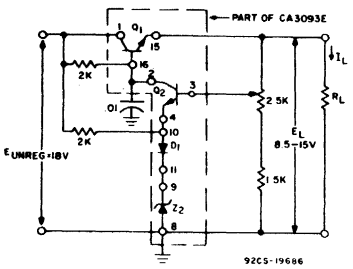
Typical Load Regulation I_L = 0 to 40 mA

$(\Delta E_L/E_L) \times 100 = -3\%$ (no load to full load)

Typical Line Regulation at R_L = 330Ω

$\frac{\Delta E_L/E_L}{\Delta E\ unreg.} \times 100 = \pm 0.55\%/V$

d) Temp.-Compensated Series Voltage Regulator



Typical Temperature Characteristic @ E_L = 12V

$\frac{\Delta E_L/E_L}{\Delta T} \times 100 = \pm\ 0.009\%/°C$

Typical Load Regulation @ E_L = 12V
I_L = 0 to 40 mA

$\frac{\Delta E_L}{E_L} \times 100 = \pm 0.4\%$ (no load to full load)

Typical Line Regulation @ E_L = 12V

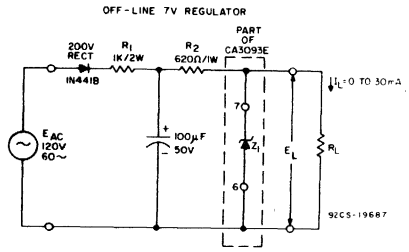
$\frac{(\Delta E_L/E_L) \times 100}{\Delta E\ unreg.} = \pm 0.45\%/V$

Typical E_L Ripple Voltage = 70 mV_{p-p}

Typical Load Regulation (I_L = 0 to 30 mA) = $\frac{\Delta E_L}{E_L} \times 100 = -8.5\%$ (no load to full load)

Typical Line Regulation = $\frac{(\Delta E_L/E_L) \times 100}{\Delta E_{AC}} = \pm .075\%/V$

e) Off-Line 7V Regulator



CA3094, CA3094A, CA3094B Types

Programmable Power Switch/ Amplifier

For Control & General-Purpose Applications

CA3094: For Operation Up to 24 Volts
CA3094A: For Operation Up to 36 Volts
CA3094B: For Operation Up to 44 Volts

APPLICATIONS:

- **Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor**
- **Over-current, over-voltage, over-temperature protectors**
- **Dual-tracking power supply with RCA-CA3085**
- **Wide-frequency-range oscillator ■ Analog timer**
- **Level detector ■ Alarm systems ■ Voltage follower**
- **Ramp-voltage generator ■ High-power comparator**
- **Ground-fault interrupter (GFI) circuits**

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

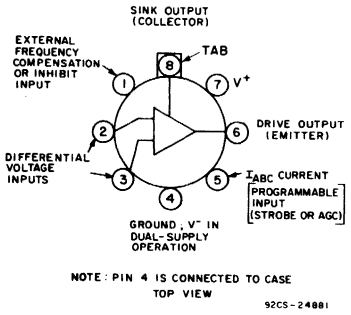
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs.27,28 and 29 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

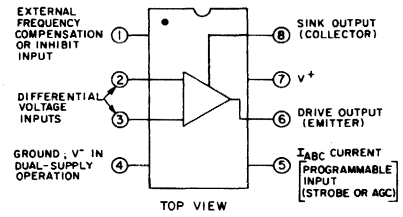
Application Note ICAN-6668 describes the rudiments of Operational Transconductance Amplifiers (OTA's).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

APPLICATION NOTE ICAN-6048 GIVES DETAILED APPLICATION INFORMATION FOR THE CA3094, CA3094A, AND CA3094B.



TO-5 Style Package



Plastic Package

Features:

- **Designed for *single* or dual power supply**
- **Programmable: strobing, gating, squelching, AGC capabilities**
- **Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)**
- **High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)**
- **Total harmonic distortion (THD) @ 0.6 W in class A operation – 1.4% typ.**
- **High current-handling capability – 100 mA (avg.), 300 mA (peak)**
- **Sensitivity controlled by varying bias current**
- **Output: "sink" or "drive" capability**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ≤ Term. 2 & 3 ≤ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	–55 to +125			°C
Storage	–65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

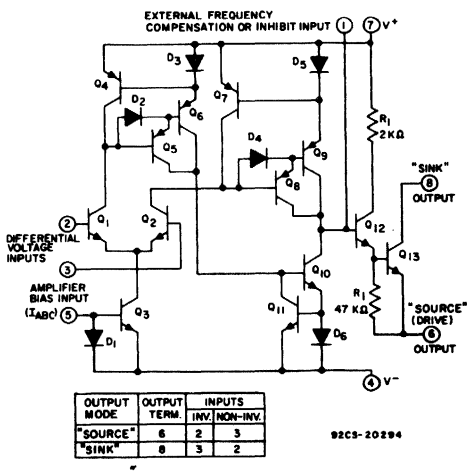


Fig. 1—Schematic diagram of CA3094.

Typical Characteristics Curves

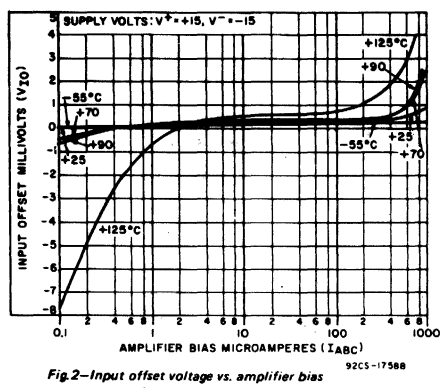


Fig.2—Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

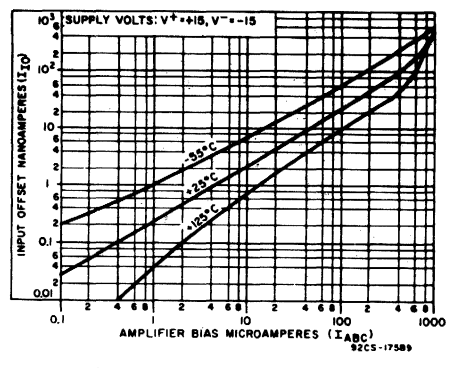


Fig.3—Input offset current vs. amplifier bias current (I_{ABC}, terminal No. 5).

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
INPUT PARAMETERS								
Input Offset Voltage	V_{IO}	17	T_A = 25°C	2	–	0.4	5	mV
			T_A = 0 to 70°C		–	–	7	mV
Input-Offset-Voltage Change	$\lvert\Delta V_{IO}\rvert$		Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA		–	1	8	mV
Input Offset Current	I_{IO}	18	T_A = 25°C	3	–	0.02	0.2	μA
			T_A = 0 to 70°C		–	–	0.3	μA
Input Bias Current	I_I	19	T_A = 25°C	4	–	0.2	0.50	μA
			T_A = 0 to 70°C		–	–	0.70	μA
Device Dissipation	P_D	18	I_{out} = 0	5, 6	8	10	12	mW
Common-Mode Rejection Ratio	C_{MRR}	20			70	110	–	dB
Common-Mode Input–Voltage Range	V_{ICR}	20	V^+ = 30 V $\frac{\text{High}}{\text{Low}}$	7	27	28.8	–	V
					1.0	0.5	–	V
			V^+ = 15 V, V^- = 15 V	7	+12	+13.8	–	V
					−14	−14.5	–	V
Unity Gain-Bandwidth			I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA		–	30	–	MHz
Open-Loop Bandwidth At −3 dB Point	BW_{OL}		I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	12	–	4	–	kHz
Total Harmonic Distortion (Class A Operation)	THD		P_D = 220 mW		–	0.4	–	%
			P_D = 600 mW		–	1.4	–	
Amplifier Bias Voltage (Terminal (No.5 to Terminal No.4)	V_{ABC}				–	0.68	–	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$				–	4	–	μV/°C
Power-Supply Rejection	$\Delta V_{IO}/\Delta V$	17			–	15	150	μV/V
1/F Noise Voltage	E_N	21	f = 10 Hz, I_{ABC} = 50 μA	8	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current	I_N	21	f = 10 Hz, I_{ABC} = 50 μA	9	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I		I_{ABC} = 20 μA		0.50	1	–	MΩ
Differential Input Capacitance	C_I		f = 1 MHz, V^+ = 30 V		–	2.6	–	pF

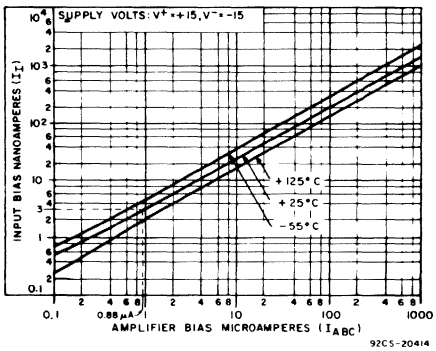


Fig.4—Input bias current vs. amplifier bias current (I_{ABC}, terminal No. 5).

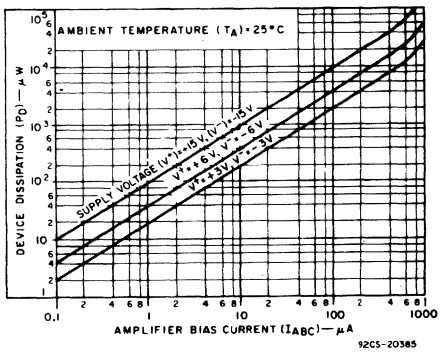


Fig.5—Device dissipation vs. amplifier bias current (I_{ABC}, terminal No. 5).

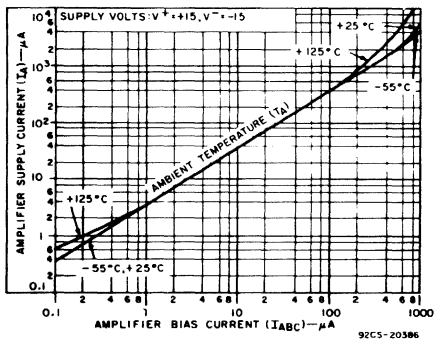


Fig.6—Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No. 5).

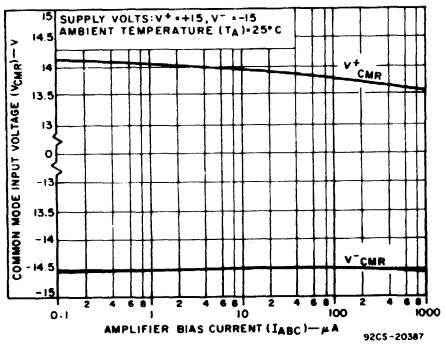


Fig.7—Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

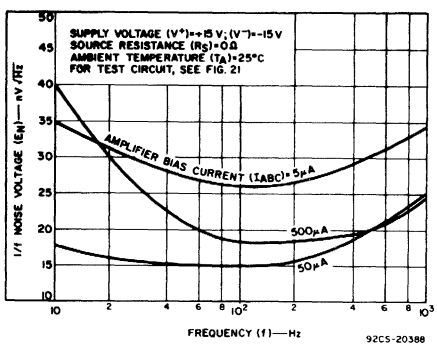


Fig.8—1/F Noise voltage vs. frequency.

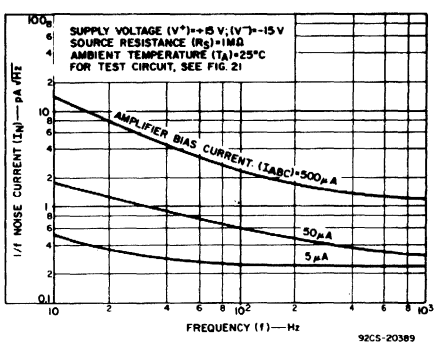


Fig.9—1/F Noise current vs. frequency.

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V, Dual Supply V^+ = 15 V, V^- = 15 V, I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)								
Peak Output Voltage: (Terminal No. 6)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to ground		26	27	–	V
With Q13 "OFF"	V_{-OM}				–	0.01	0.05	V
Peak Output Voltage: (Terminal No. 6)			V^+ = +15 V, V^- = -15 V				0.5	
Positive	V^+_{OM}		R_L = 2 kΩ to −15 V		+11	+12	–	V
Negative	V_{-OM}				–	−14.99	−14.95	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to 30 V		29.95	29.99	–	V
With Q13 "OFF"	V_{-OM}				–	0.040	–	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 15 V, V^- = − 15 V					
Positive	V^+_{OM}		R_L = 2 kΩ to + 15 V		+14.95	+14.99	–	V
Negative	V_{-OM}				–	14.96	–	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$		V^+ = 30 V, I_C = 50 mA, Terminal No.6 grounded	10	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)			V^+ = 30 V		–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13})	h_{fe}		V^+ = 30 V, V_{CE} = 5 V, I_C = 50 mA	11	16,000	100,000	–	
Output Capacitance:			f = 1 MHz					
Terminal No. 6	C_O		All Remaining Terminals Tied to Terminal No. 4		–	5.5	–	pF
Terminal No. 8					–	17	–	pF
TRANSFER PARAMETERS								
Voltage Gain	A		V^+ = 30 V, I_{ABC} = 100 μA		20,000	100,000	–	V/V
		22	ΔV_{out} = 20 V, R_L = 2 kΩ	12	86	100	–	dB
Forward Transconductance To Terminal No. 1	g_m			13	1650	2200	2750	μmhos
Slew Rate: Open Loop:								
Positive Slope		23	I_{ABC} = 500 μA, R_L = 2 kΩ	14	–	500	–	V/μs
Negative Slope					–	50	–	V/μs
Unity Gain (Non-Inverting, Compensated)		24	I_{ABC} = 500 μA, R_L = 2 kΩ	15	–	0.7	–	V/μs

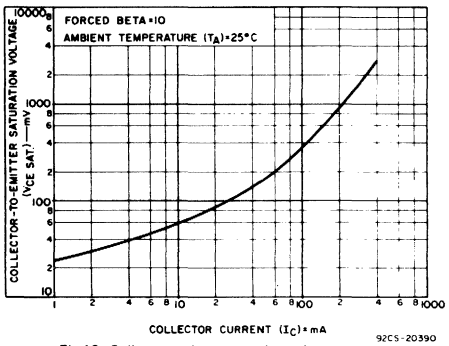
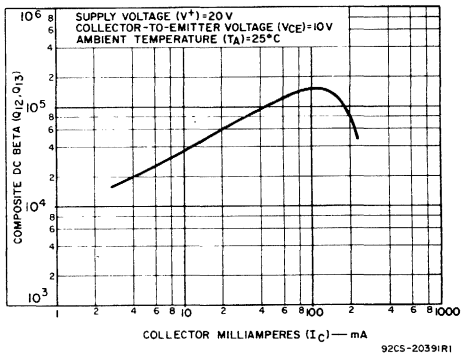


Fig.10—Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.



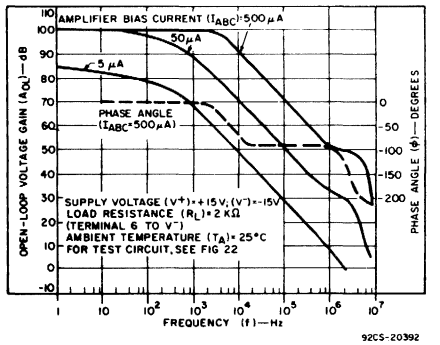


Fig.12—Open-loop voltage gain vs. frequency.

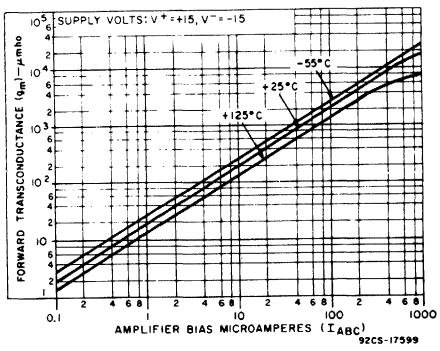


Fig.13—Forward transconductance vs. amplifier bias current.

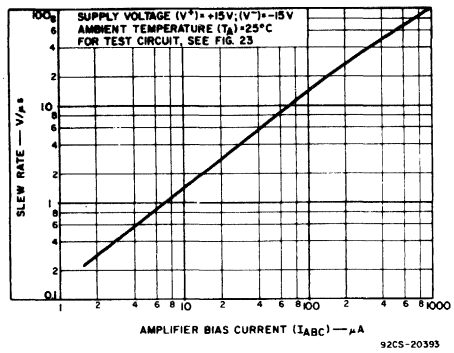


Fig.14—Slew rate vs. amplifier bias current.

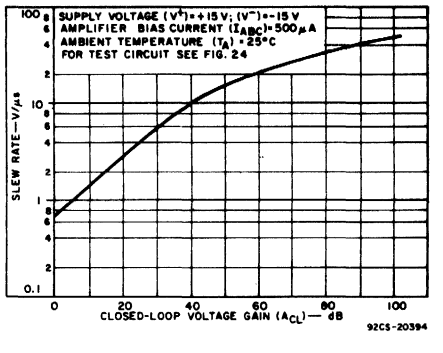


Fig.15—Slew rate vs. closed-loop voltage gain.

CA3094, CA3094A, CA3094B Types

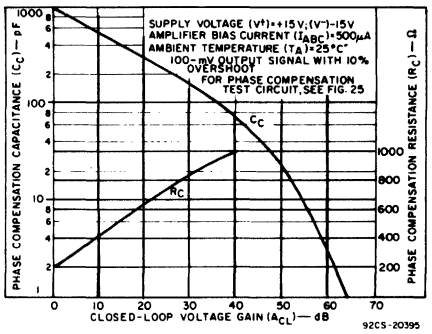


Fig. 16—Phase compensation capacitance and resistance vs. closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No. 8) and the "Drive" Output (terminal No. 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No. 6 and terminal No. 4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No. 7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No. 8 and terminal No. 7, the current-limiting resistor should be connected between terminal 6 and terminal No. 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No. 7 and the V^+ supply.

TEST CIRCUITS

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig. 21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No. 2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for ^{E} noise and ^{I} noise measurements, respectively. These measurements are made at frequencies of 10 Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are $E_n = 18\ nV/\sqrt{HZ}$ and $I_N = 1.8\ pA/\sqrt{HZ}$.

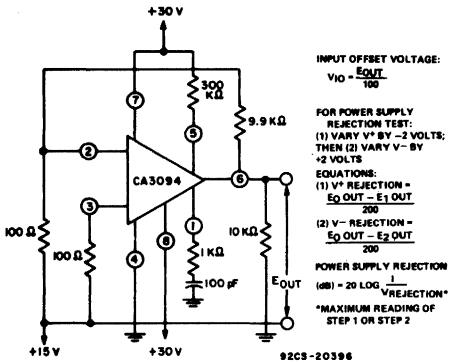


Fig. 17—Input offset voltage and power-supply rejection test circuit.

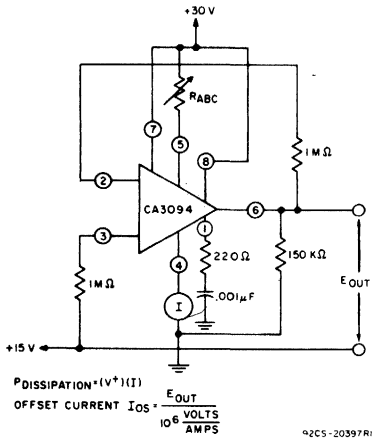


Fig. 18—Input offset current test circuit.

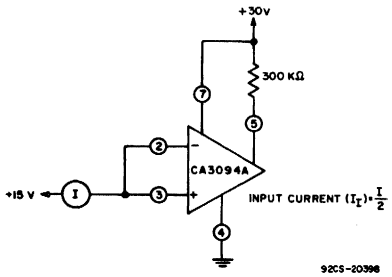


Fig. 19—Input bias current test circuit.

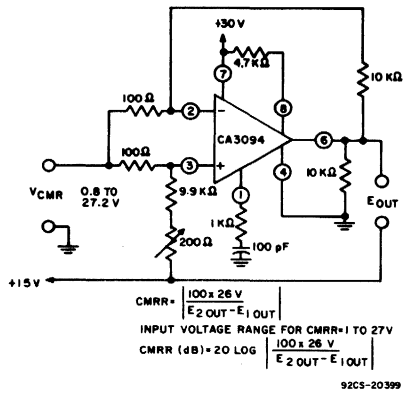


Fig. 20—Common-mode range and rejection ratio test circuit.

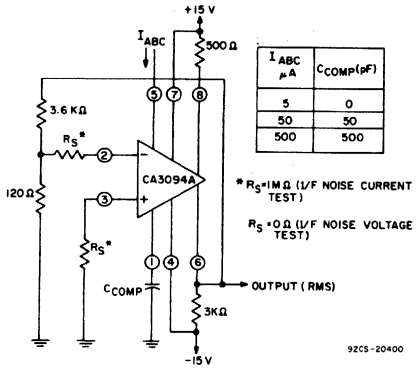


Fig. 21—1/F noise test circuit.

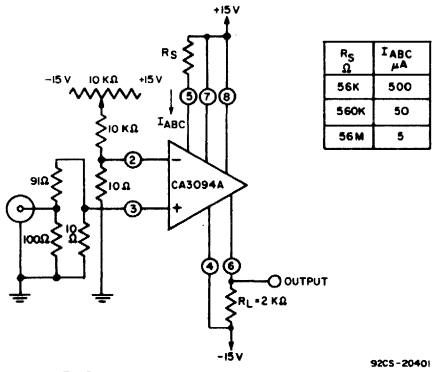


Fig. 22—Open-loop gain vs. frequency test circuit.

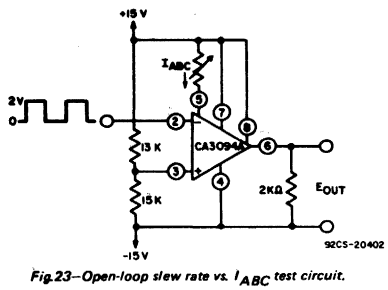


Fig. 23—Open-loop slew rate vs. I_{ABC} test circuit.

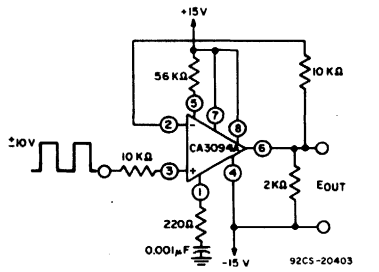


Fig. 24—Slew rate vs. non-inverting unity gain test circuit.

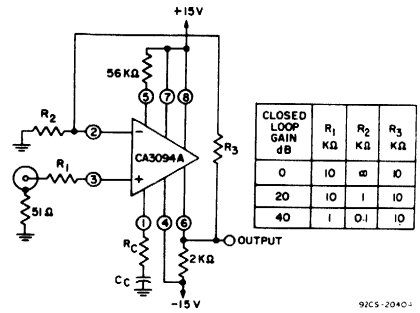


Fig. 25—Phase compensation test circuit.

CA3095E

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

RCA-CA3095E is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors. (Refer to Fig. 1 for following description.)

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of 1 μA to 2 mA. Each of these types comprises the input section of its respective cascode amplifier. The output section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors. See Operating Considerations for bias considerations of the differential cascode amplifier.

The exceptionally high-beta characteristics of Q1 and Q2, plus the large signal-voltage swing capability of Q3 and Q4, make the composite differential cascode amplifier an excellent choice for a broad range of small-signal, high-input-impedance amplifier applications including low-noise video amplifiers. This amplifier is also recommended for use in long-interval timers, oscillators, and long-duration one-shot applications.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C

Features

- Two super-beta n-p-n transistors – $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to < 1 nA
- Matched pair (Q1 and Q2) –
  V_{IO} = 5 mV max. at I_C = 100 μA dc
  I_{IO} = 20 nA max. at I_C = 100 μA dc
- Wide current range – < 1 μA to 2 mA

Independent Transistors:

- h_{FE} = 300 typ. for each transistor
- Wide current range – < 1 μA to 10 mA
- Matched general-purpose transistors
- High voltage – V_{CBO} = 45 V max.

Applications

Differential Cascode Amplifier:

- Super-beta pre-amplifier for op-amp
- High-impedance dc meter amplifier
- Low-noise video amplifier
- Piezoelectric transducer amplifier
- Long-interval timer
- Long-duration one-shot multivibrator
- Comparator with high-input impedance
- Long-time-constant integrator
- Photocell amplifier
- Low-noise amplifier—for operation from high-source impedances

Independent Transistors:

- General use in signal processing systems in dc through vhf range

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25 °C*

Power Dissipation:		
Any One Transistor	300	mW
Total Package–		
Up to 25 °C	750	mW
Above 25 °C ..... derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C
Voltage and Current Ratings Apply for Each Specified Transistor:		
Super-Beta Transistors (Q1, Q2)–		
Collector-to-Base Voltage (V_{CBO})	6	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional N-P-N Transistors (Q3, Q4, Q6, Q7, Q8)–		
Collector-to-Base Voltage (V_{CBO})	45	V
Collector-to-Emitter Voltage (V_{CEO})	35	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional P-N-P Transistor (Q5)–		
Collector-to-Base Voltage (V_{CBO})	−45	V
Collector-to-Emitter Voltage (V_{CEO})	−35	V
Limiting Circuit Current ($I_{Pin\ 11}$)	20	mA

* The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

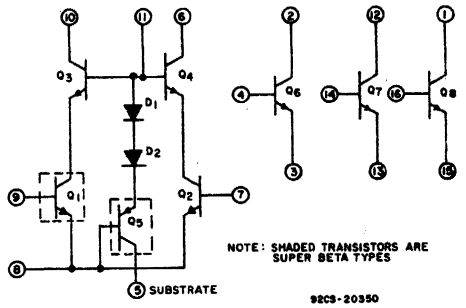


Fig. 1—Functional diagram.

STATIC CHARACTERISTICS

Characteristics	Symbol	Test Conditions (T_A = 25 °C)		Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3) and (Q2, Q4), Unless Indicated Otherwise							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0 See Note 1		6	–	–	V
Emitter-to-Base Breakdown Voltage (Applies only to Q1 & Q2)	$V_{(BR)EBO}$	I_E = 100 μA, I_C = 0	Term. 9 to 8 or Term. 7 to 8	6	8	--	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100 μA, I_B = I_E = 0		45	–	–	V
Collector Cutoff Current	I_{CER}	V_{6-8} or V_{10-8} = 10 V, I_{11} = 100 μA, R_{BE} = 100 MΩ		–	–	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{10-8} = 5 V or V_{6-8} = 5 V	I_C = 1 mA	–	1500	--	
			I_C = 100 μA	1000	2000	5000	
			I_C = 10 μA	–	1500	–	
Base-to-Emitter Voltage (Applies only to Q1 & Q2)	V_{BE}	I_C = 100 μA, V_{6-8} or V_{10-8} = 5 V		0.50	0.59	0.68	V
Saturation Voltage	V_{sat}	I_6 or I_{10} = 1 mA, I_{11} = 100 μA, I_7 or I_9 = 100 μA		–	0.22	0.7	V
For Cascode Amplifiers as a Differential Matched Pair							
Magnitude of Input-Offset Voltage	$\lvert I_{IO}\rvert$	I_C = 100 μA		–	1	5	mV
Magnitude of Input-Offset Current	$\lvert I_{IO}\rvert$	$V_{6-8} = V_{10-8}$ = 5 V		–	4	20	nA
Magnitude of Input-Offset Voltage Drift (Temp. Coeff.)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			–	3.3	–	μV/°C
Magnitude of Input-Offset Current Drift (Temp. Coeff.)	$\frac{\lvert\Delta I_{IO}\rvert}{\Delta T}$			–	0.05	–	nA/°C

Note 1: Terminal No. 9 to terminals 10 and 11 connected or terminal No. 7 to terminals 6 and 11 connected.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

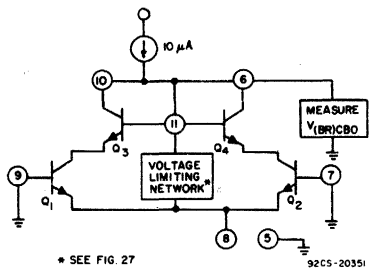


Fig. 2—$V_{(BR)CBO}$ test circuit.

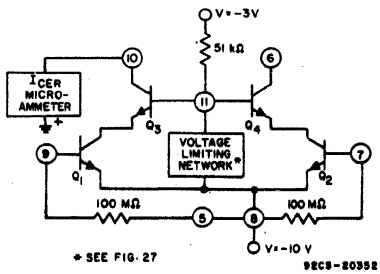


Fig. 3—I_{CER} test circuit

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STATIC CHARACTERISTICS (Cont'd)

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$		Limits Min.	Typ.	Max.	Units
For Each Conventional n-p-n Transistor (Q3, Q4, Q6, Q7, Q8)							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A$, $I_E = 0$		45	95	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		35	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 100\ \mu A$, $I_C = 0$		6	8	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_{CI} = 100\ \mu A$, $I_B = I_E = 0$		45	95	–	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$		–	–	100	nA
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		–	–	10	nA
DC Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 5$ V	$I_C = 10$ mA	–	210	–	
			$I_C = 1$ mA	150	300	500	
			$I_C = 10\ \mu A$	–	180	–	
Base-to-Emitter Voltage	V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V		0.60	0.69	0.78	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10$ mA, $I_B = 1$ mA		–	0.22	0.7	V

Dynamic Characteristics

Characteristics	Symbol	Test Conditions $T_A = 25\ ^\circ C$	Limits Min.	Typ.	Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3), Unless Indicated Otherwise						
Gain-Bandwidth Product	f_T	$I_C = 100\ \mu A$, $V_{6-8} = V_{10-8} = 5$ V,	–	78	–	MHz
Noise Voltage (Referred to Input) For Differential Amplifier Operation	E_N	$I_C = 50\ \mu A$, f = 10 Hz	–	13	–	nV/$\sqrt{Hz}$
Noise Current (Referred to Input) For Differential Amplifier Operation	I_N	$I_C = 5\ \mu A$, f = 10 Hz	–	0.12	–	pA/$\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	$V_{6-7} = V_{10-9} = 5$ V, $I_E = 0$	–	0.3		pF
Collector-to-Substrate Capacitance	C_{CIO}	$V_{6-5} = V_{10-5} = 5$ V, $I_B = 0$	–	3.0	–	pF
For Each Conventional Transistor (Q3 through Q8)						
Gain-Bandwidth Product	f_T	$I_C = 100\ \mu A$, $V_{CE} = 5$ V	–	100	–	MHz
		$I_C = 3$ mA, $V_{CE} = 5$ V	–	320	–	
Noise Voltage (Referred to Input)	E_N	$I_C = 100\ \mu A$, $V_{CE} = 5$ V, f = 10 Hz	–	5	–	nV/$\sqrt{Hz}$
Noise Current (Referred to Input)	I_N	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, f = 10 Hz	–	0.8	–	pA/$\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 5$ V, $I_E = 0$	–	0.4	–	pF
Collector-to-Substrate Capacitance	C_{CIO}	$V_{CI} = 5$ V, $I_B = 0$	–	2	–	pF

* Curve plotted for I_{CEO} characteristic.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

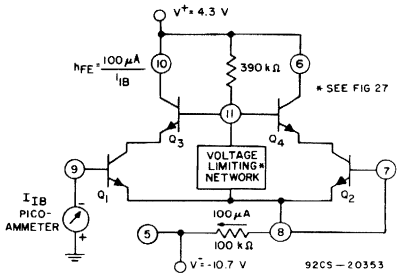

Fig.4—DC Beta (h_{FE}) test circuit.

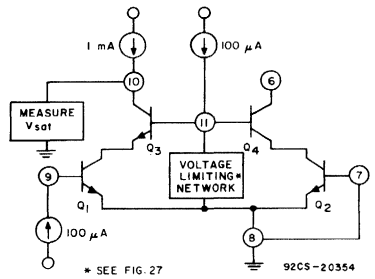

Fig.5—V_{sat} test circuit for super-beta cascode pairs.

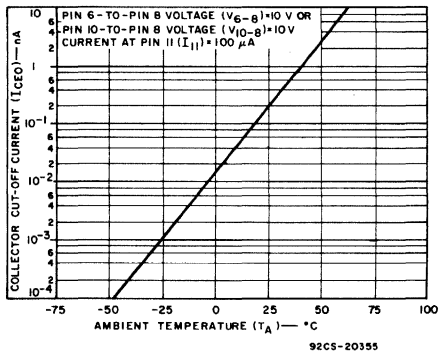

Fig.6—Collector cut-off current vs ambient temperature for super-beta cascode pairs.

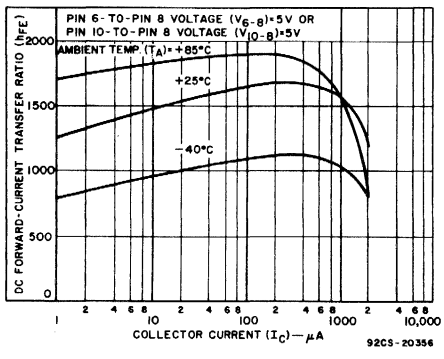

Fig.7—h_{FE} vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

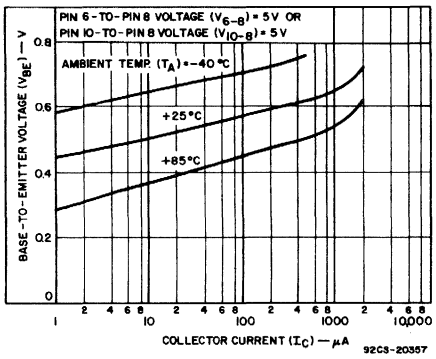

Fig.8—V_{BE} vs. I_C for each super-beta transistor (Q1 and Q2).

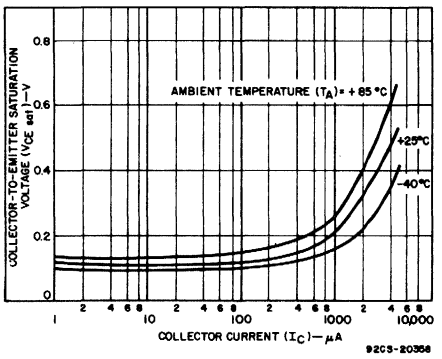

Fig.9—$V_{CE(sat)}$ vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

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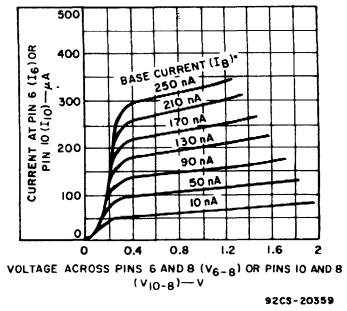


Fig.10—I-V characteristics for the super-beta cascode pairs.

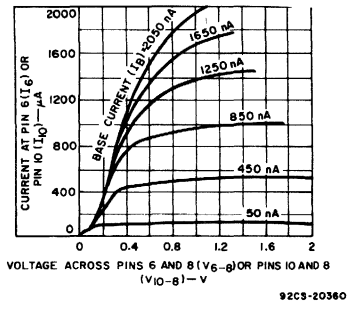


Fig.11—I-V characteristics for the super-beta cascode pairs.

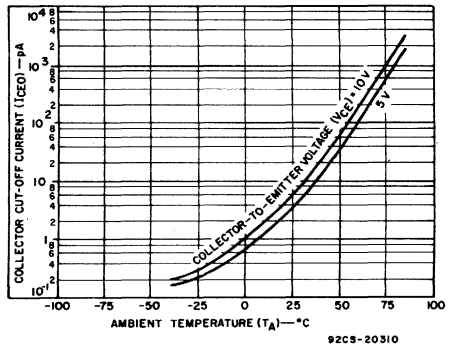


Fig.12—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CE} = 5 V, 10 V).

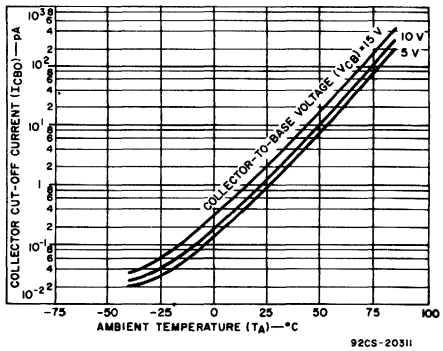


Fig.13—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CB} = 5 V, 10 V, 15 V).

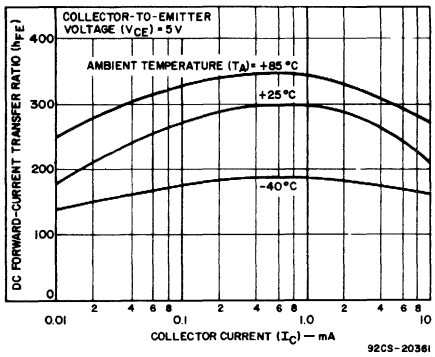


Fig.14—h_{FE} vs. I_C for each conventional transistor (Q6, Q7, Q8).

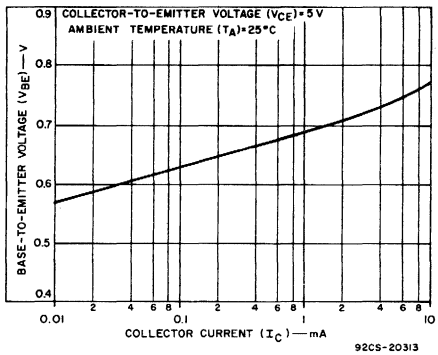


Fig.15—V_{BE} as a function of collector current for the conventional transistors.

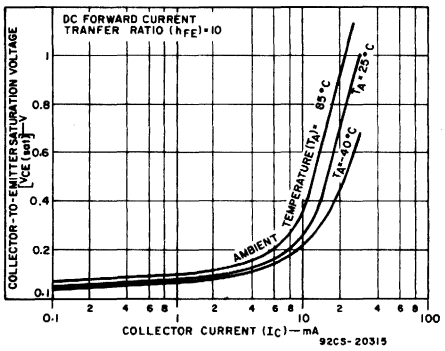


Fig.16—$V_{CE(sat)}$ as a function of collector current for the conventional transistors.

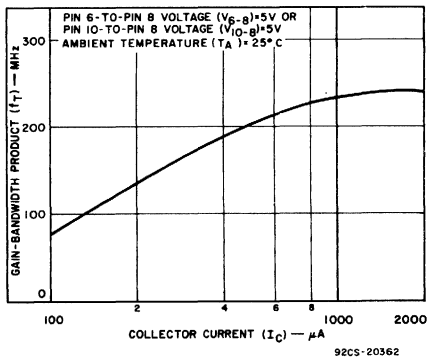


Fig.17—Gain bandwidth product vs collector current for the super-beta cascode pairs.

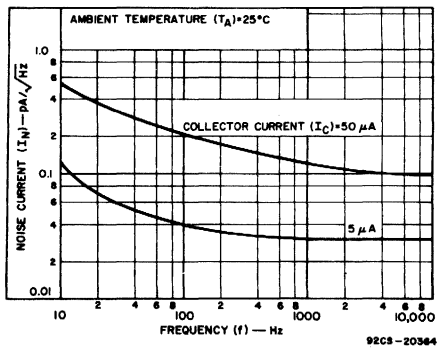


Fig.18—I_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

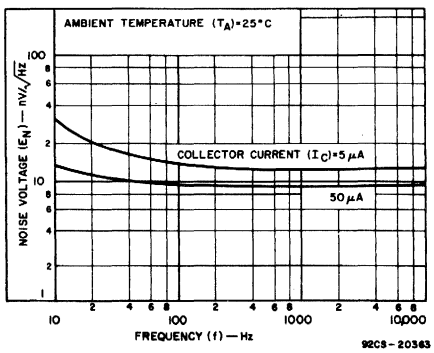


Fig.19—E_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

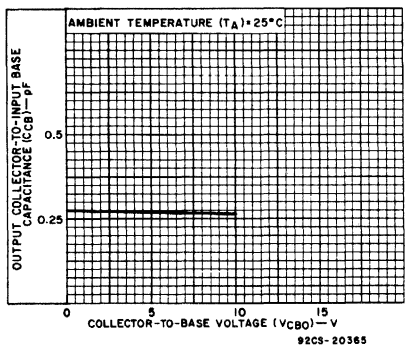


Fig.20—C_{CB} vs. V_{CBO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

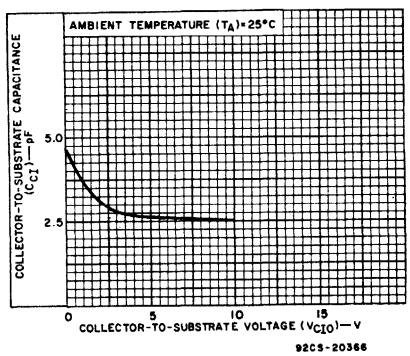


Fig.21—C_{CI} vs. V_{CIO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

CA3095E

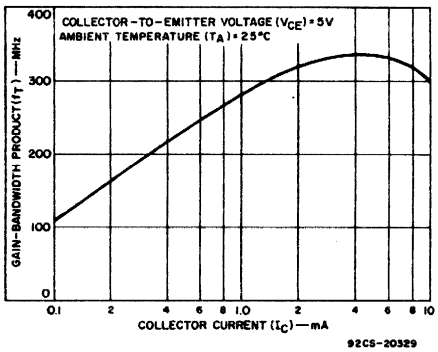


Fig.22—Gain bandwidth product vs collector current for the conventional transistors.

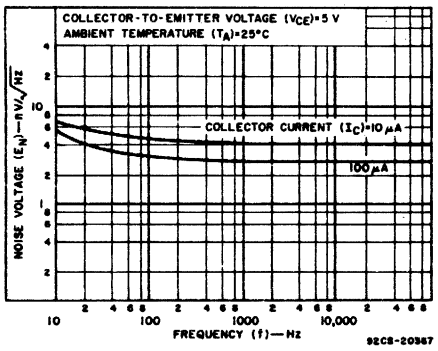


Fig.23—Noise voltage vs frequency for the conventional transistors.

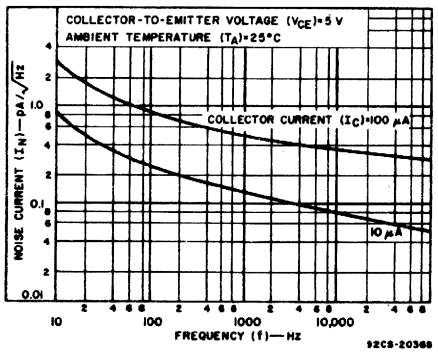


Fig.24—I_N vs. f for each conventional transistor (Q6, Q7, Q8).

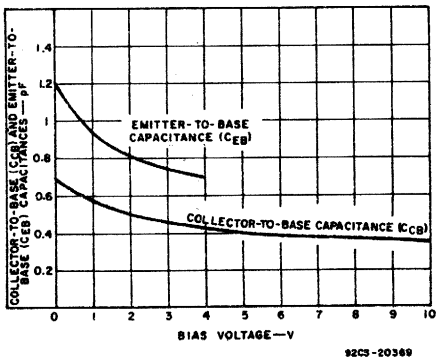


Fig.25—Collector-to-base and emitter-to-base capacitances vs bias voltage for the conventional transistors.

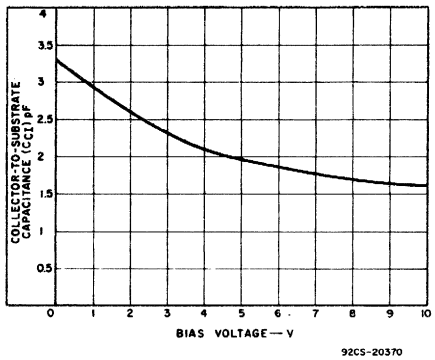


Fig.26—Collector-to-substrate capacitance vs bias voltage for the conventional transistors.

TYPICAL APPLICATIONS

Operating Considerations

Operation Considerations for the Super-Beta Differential Cascode Amplifier

An internal voltage-limiting network (diodes D1, D2 and p-n-p transistor Q5) incorporated in the differential cascode amplifier, assures that the applied collector-to-emitter voltage of each super-beta unit is maintained below two volts. Fig. 27 shows a typical bias arrangement of the super-beta differential cascode amplifier.

Bias current for this network must be supplied by an external source. This bias current can be obtained by simply connecting a resistor from Pin 11 to the positive supply of the differential amplifier. The return path for most of the bias current is through the substrate, Pin 5, rather than through the common emitter, Pin 8. This arrangement provides superior common-mode and power-supply rejection. As a general rule-of-thumb, the current supplied into Pin 11 should be approximately 0.04 to 0.1 times the value of the quiescent current of Pin 8.

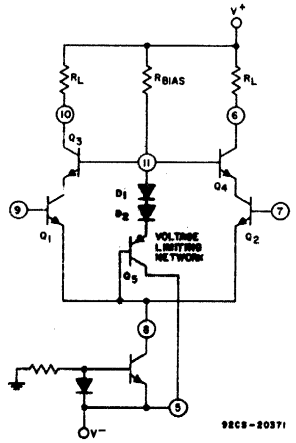


Fig.27—Bias arrangement for operation of the super-beta differential cascode amplifier.

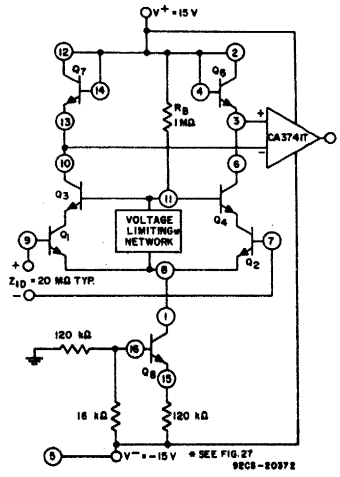


Fig.28—Super-beta Op-Amp with diode drive network.

CA3095E

TYPICAL APPLICATIONS (Cont'd)

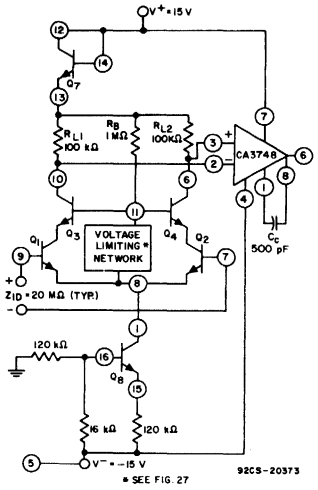


Fig.29—Super-beta Op-Amp with resistor drive network.

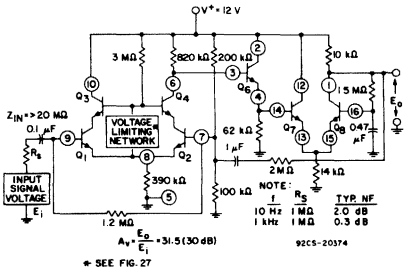


Fig.30—High-input-impedance, low-noise amplifier circuit.

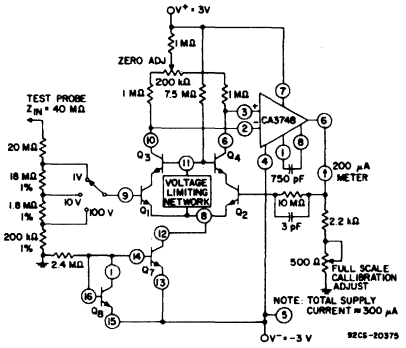


Fig.31—Typical high-input-impedance dc voltmeter circuit.

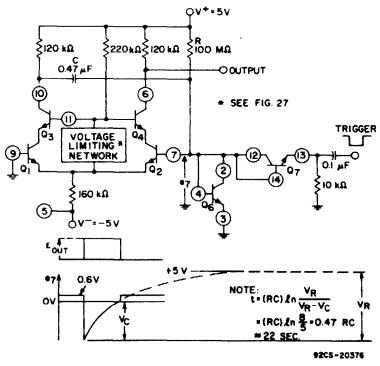


Fig.32—Long-delay monostable multivibrator circuit.

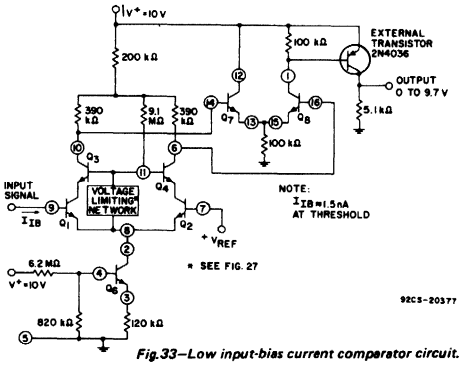


Fig.33—Low input-bias current comparator circuit.

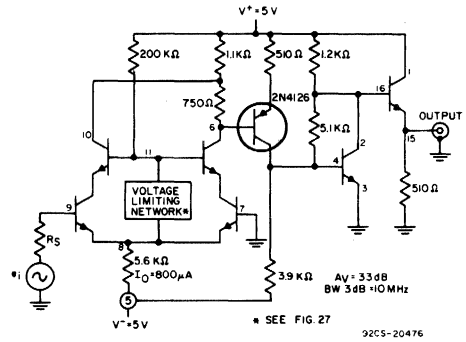


Fig.34—CA3095E wideband amplifier.

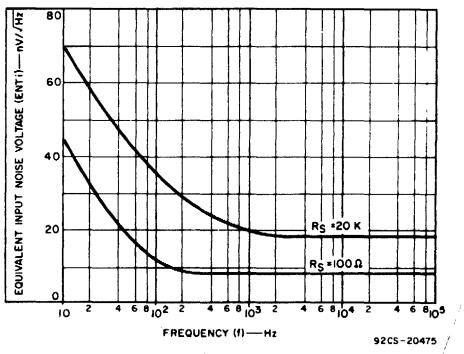


Fig.35—Equivalent input noise voltage vs. frequency for circuit of figure 34.

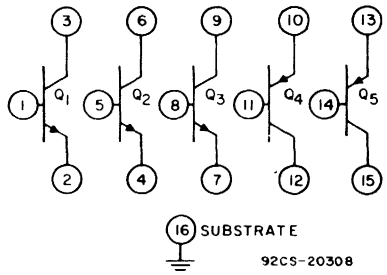
CA3096E, CA3096AE

N-P-N/P-N-P Transistor-Array IC

RCA-CA3096E and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE and CA3096E are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE(SAT)}$ (see Table I).

CA3096E and CA3096AE are supplied in 16-lead dual-in-line plastic packages.



Schematic Diagram

TABLE I—CA3096AE AND CA3096E ESSENTIAL DIFFERENCES*

RCA TYPE	I_{CBO} (nA)		I_{CEO} (nA)		$V_{CE(SAT)}$ (V)		$\lvert V_{IO}\rvert$ (mV)		$\lvert I_{IO}\rvert$ (μA)	
	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p
CA3096AE	40	-40	100	-100	0.7	0.4	5	5	0.6	0.25
CA3096E	100	-100	1000	-1000	1.0	0.7	–	–	–	–

* Maximum values.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (For Equipment Design)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	CA3096AE, CA3096E LIMITS			UNITS
			Min.	Typ.	Max.	
For Each n-p-n Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	100	nA
Collector-Cutoff Current (CA3096E)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	100	nA
Collector-Cutoff Current (CA3096E)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	1	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	35	50	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	45	100	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10 μA, I_B = I_E = 0	45	100	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	8	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	6	7.9	9.8	V
Collector-to-Emitter Saturation Voltage (CA3096AE)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.5	V
Collector-to-Emitter Saturation Voltage (CA3096E)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.7	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 5 V	0.6	0.69	0.78	V
DC Forward-Current Transfer Ratio	h_{FE}		150	390	500	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = 1 mA, V_{CE} = 5 V	–	−1.9	–	mV/°C
For Each p-n-p Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	100	nA
Collector-Cutoff-Current (CA3096E)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	1	μA
Collector-Cutoff-Current (CA3096E)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = −100 μA, I_B = 0	−40	−75	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = −10 μA, I_E = 0	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = −10 μA, I_C = 0	−40	−100	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	10	16	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 10 μA, I_B = I_C = 0	40	100	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = −1 mA, I_B = −100 μA	–	−0.16	−0.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = −100 μA, V_{CE} = −5 V	−0.5	−0.6	−0.7	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −100 μA, V_{CE} = −5 V	40	85	200	
		I_C = −1 mA, V_{CE} = −5 V	20	47	150	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = −100 μA, V_{CE} = −5 V	–	−2.2	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	1.1		μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	0.54	–	μV/°C

Features:

- **Matched General-Purpose Transistors (CA3096AE Only)**
- **Input Offset Voltage ± 5 mV**
- **Input Offset Current:**
  - **p-n-p Pair ± 250 nA max. @ I_C = −100 μA**
  - **n-p-n Pair ± 0.6 μA max. @ I_C = 1 mA**
- **High h_{FE}**
  - **n-p-n transistor: 150 min. @ I_C = 1 mA**
  - **p-n-p transistor: 40 min. @ I_C = 100 μA**
- **High Breakdown Voltages:**
  - **n-p-n transistor: $V_{(BR)CEO}$ = 35 V min; $V_{(BR)CBO}$ = 45 V min.**
  - **p-n-p transistor: $V_{(BR)CEO}$ = 40 V min; $V_{(BR)CBO}$ = 40 V min.**
- **Separate Substrate Connection**
- **Low Noise Figure:**
  - **n-p-n transistor: 2.2 dB typ. at 1 kHz**
  - **p-n-p transistor: 3 dB typ. at 1 kHz**

Applications:

- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature-Compensated Amplifiers**
- **Operational Amplifiers**

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

		Each n-p-n Transistor	Each p-n-p Transistor	
Collector-to-Emitter Voltage	V_{CEO}	35	−40	V
Collector-to-Base Voltage	V_{CBO}	45	−40	V
Collector-to-Substrate Voltage	V_{CIO}	45	45	V
Emitter-to-Base Voltage	V_{EBO}	6	−40	V
Collector Current	I_C	50	−10	mA
Dissipation P_D:				
Up to T_A = 55 °C:				
Device (Total)		750		mW
Each Transistor		200		mW
Above T_A = 55 °C		Derate Linearly 6.67		mW/°C
Temperature Range:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
Lead Temperature (During Soldering) At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.		265		°C

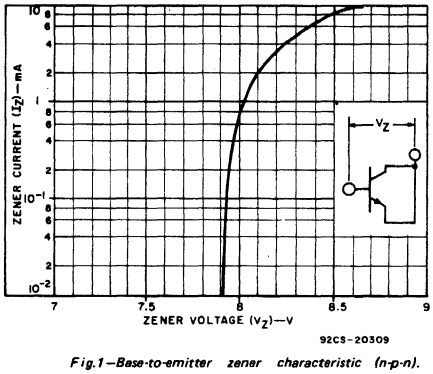


Fig. 1—Base-to-emitter zener characteristic (n-p-n).

CA3096E, CA3096AE

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance	R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_o		80	kΩ
Admittance Characteristics:		f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance	$\|y_{fe}\| \frac{g_{fe}}{b_{fe}}$		7.5 −j13	mmho
Input Admittance	$\|y_{ie}\| \frac{g_{ie}}{b_{ie}}$		2.2 j3.1	mmho
Output Admittance	$\|y_{oe}\| \frac{g_{oe}}{b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
		V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance	R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance	R_o		680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance	C_{BI}	V_{BI} = 3 V	3.05	pF

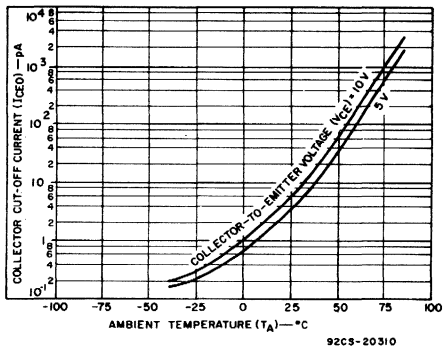


Fig.2—Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

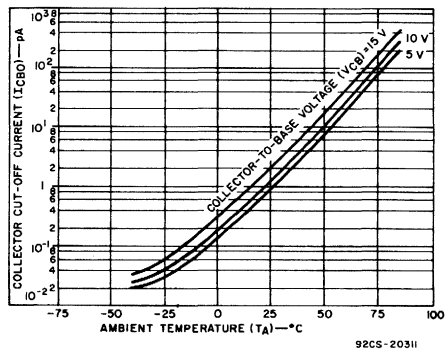


Fig.3—Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

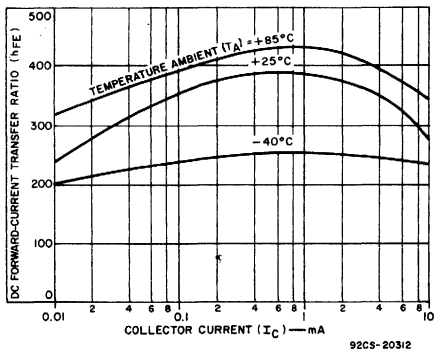


Fig.4—Transistor (n-p-n) h_{FE} as a function of collector current.

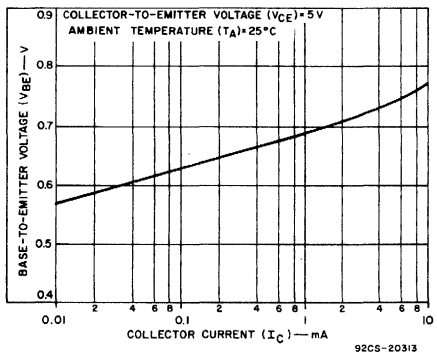


Fig.5—V_{BE} (n-p-n) as a function of collector current.

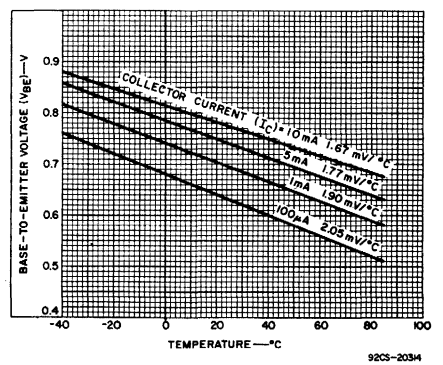


Fig.6—V_{BE} (n-p-n) as a function of temperature.

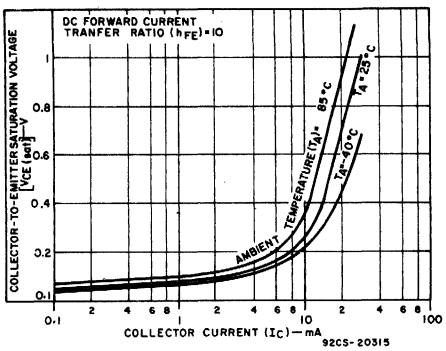


Fig.7—$V_{CE(SAT)}$ (n-p-n) as a function of collector current.

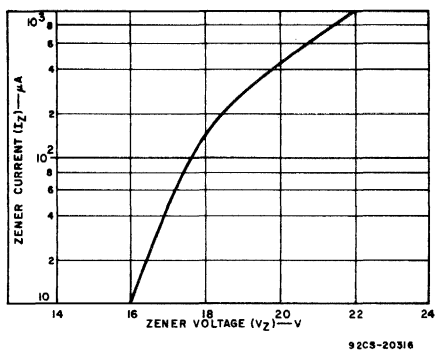


Fig.8—Base-to-emitter zener characteristic (p-n-p).

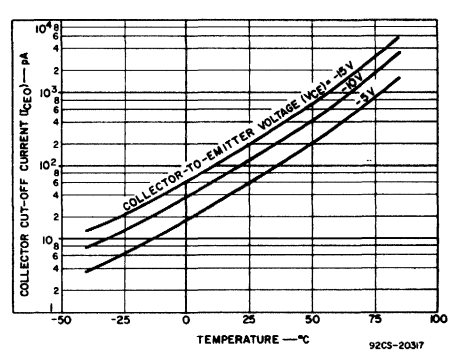


Fig.9—Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

CA3096E, CA3096AE

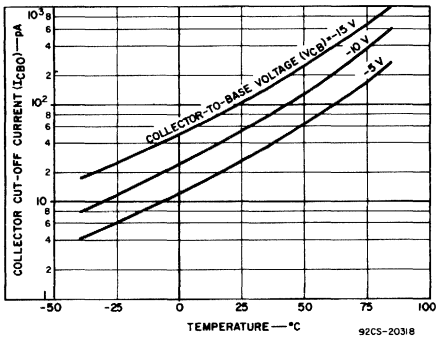


Fig.10—Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

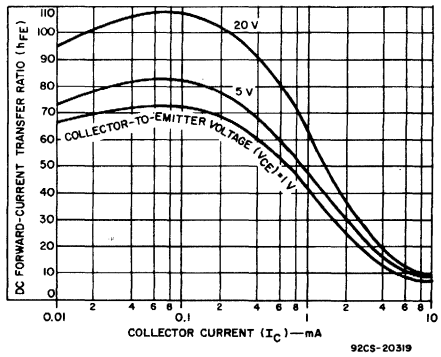


Fig.11—Transistor (p-n-p) h_{FE} as a function of collector current.

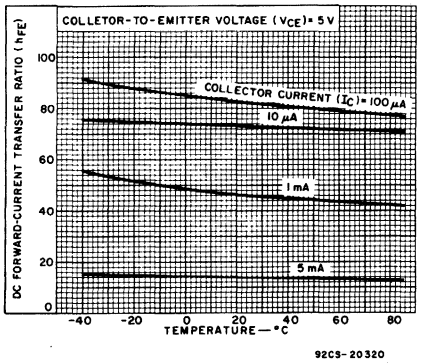


Fig.12—Transistor (p-n-p) h_{FE} as a function of temperature.

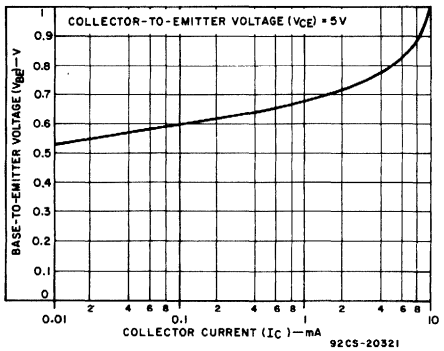


Fig.13—V_{BE} (p-n-p) as a function of collector current.

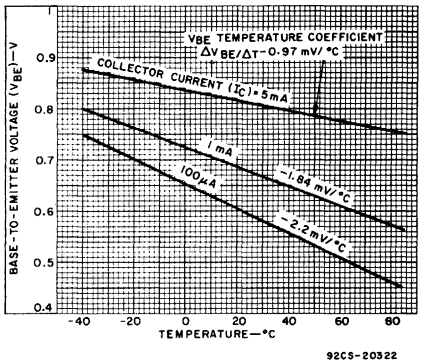


Fig.14—V_{BE} (p-n-p) as a function of temperature.

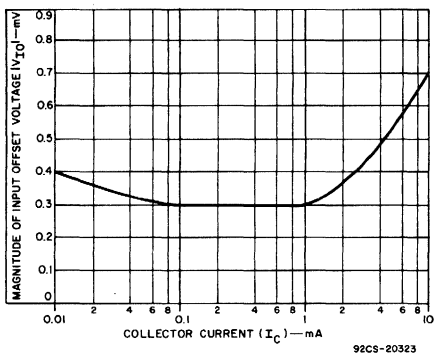


Fig.15—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

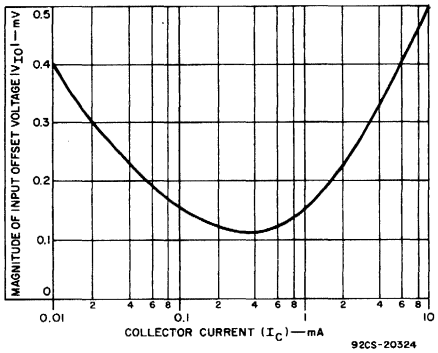


Fig.16—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistors Q_4–Q_5.

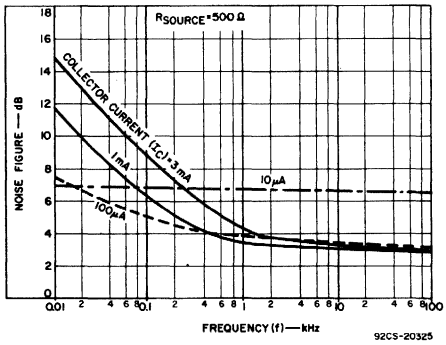


Fig.17—Noise figure as a function of frequency for n-p-n transistors.

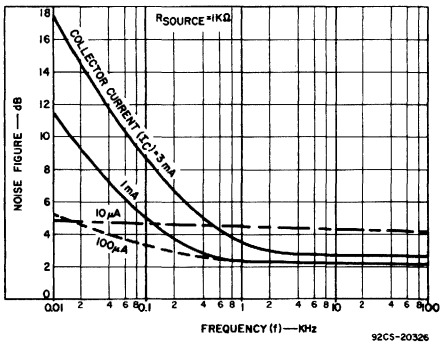


Fig.18—Noise figure as a function of frequency for n-p-n transistors.

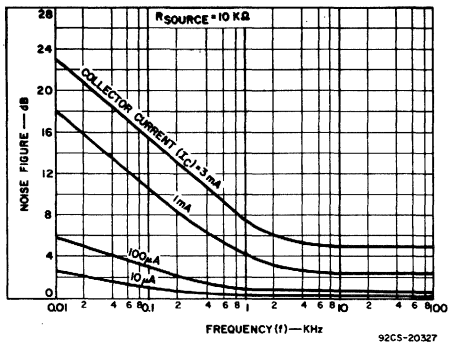


Fig.19—Noise as a function of frequency for n-p-n transistors.

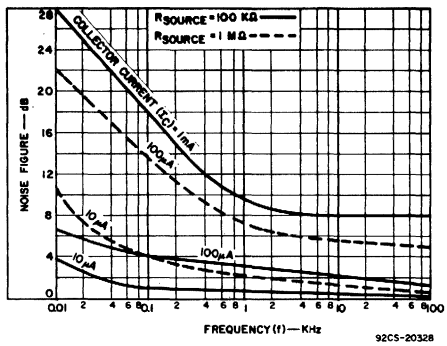


Fig.20—Noise figure as a function of frequency for n-p-n transistors.

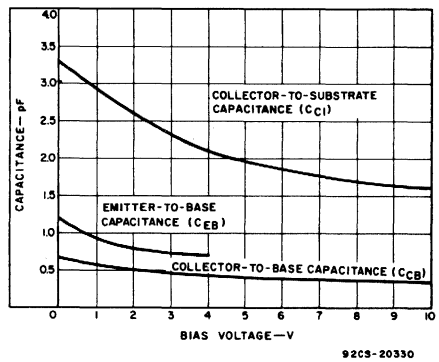


Fig.21—Gain-bandwidth product as a function of collector current (n-p-n).

CA3096E, CA3096AE

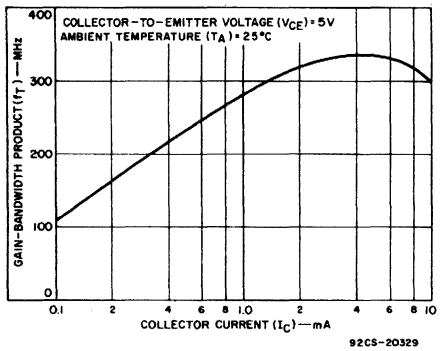


Fig.22—Capacitance as a function of bias voltage (n-p-n).

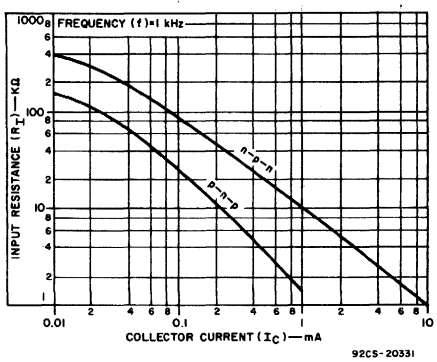


Fig.23—Input resistance as a function of collector current.

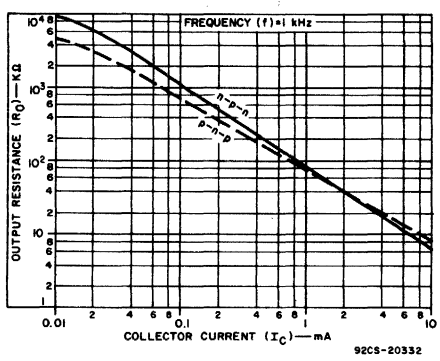


Fig.24—Output resistance as a function of collector current.

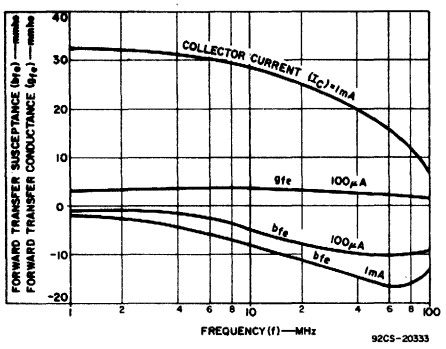


Fig.25—Forward transconductance as a function of frequency.

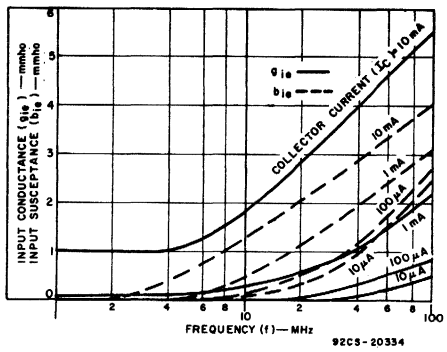


Fig.26—Input admittance as a function of frequency.

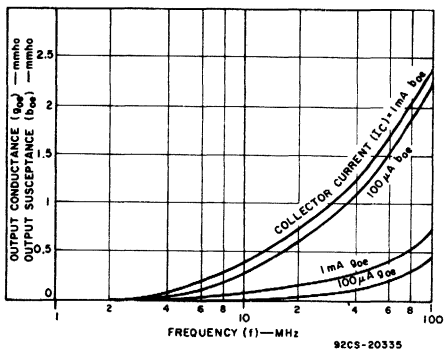


Fig.27—Output admittance as a function of frequency.

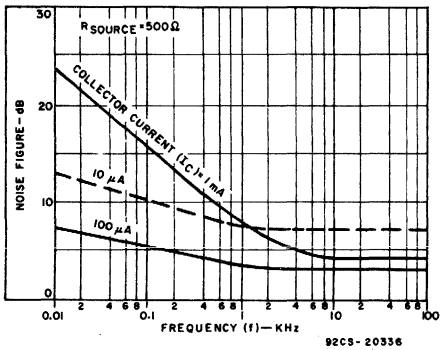


Fig.28—Noise figure as a function of frequency (p-n-p).

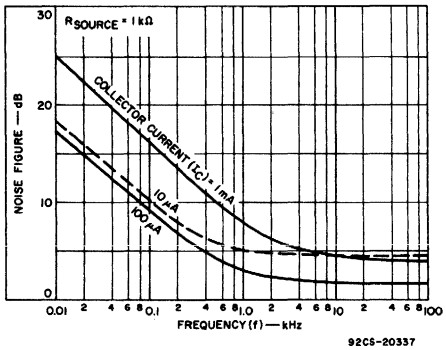


Fig.29—Noise figure as a function of frequency (p-n-p).

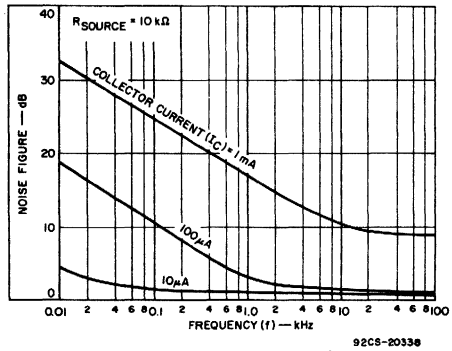


Fig.30—Noise figure as a function of frequency (p-n-p).

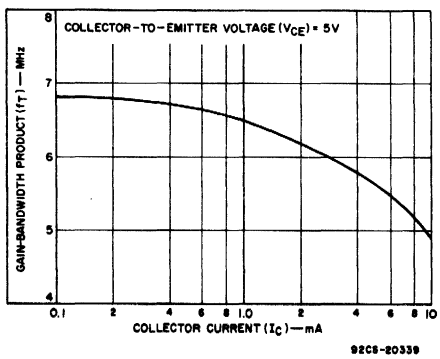


Fig.31—Gain-bandwidth product as a function of collector current (p-n-p).

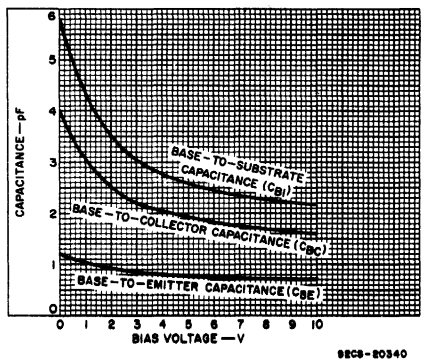


Fig.32—Capacitance as a function of bias voltage (p-n-p).

For application information, see Data Bulletin File No. 595.

CA3097E

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

RCA-CA3097E Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125°C.

Includes:

- **Uncommitted n-p-n Transistor**
- **Sensitive-Gate Silicon Controlled Rectifier**
- **Programmable Unijunction Transistor (PUT)**
- **p-n-p/n-p-n Transistor Pair**
- **Zener Diode**
- **Separate Substrate Connection**

Features:

- **Complete isolation between elements**
- **n-p-n transistor — V_{CEO} = 30 V (min.) I_C = 100 mA (max.)**
- **p-n-p/n-p-n transistor pair — beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation**
- **Programmable unijunction transistor (PUT) — peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ±30 V**
- **(PUT) Extremely long RC time constants with low value of external capacitor**
- **Sensitive-gate silicon controlled rectifier (SCR) — 150 mA forward current (max.)**
- **Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA**

Applications:

- **Timers**
- **Light dimmers/motor controls**
- **Oscillators**
- **"One-shot" multivibrators**
- **Voltage regulators**
- **Comparators, Schmitt triggers**
- **Constant-current sources**
- **Amplifiers**
- **Logic circuits**
- **SCR triggering**
- **Pulse Circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

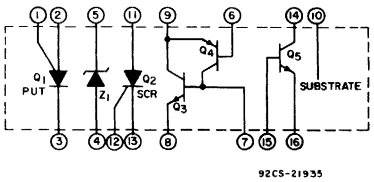


Fig. 1 — Schematic diagram of CA3097E.

TYPICAL CHARACTERISTICS

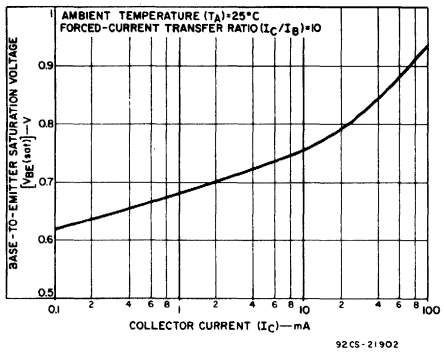


Fig.2 — Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

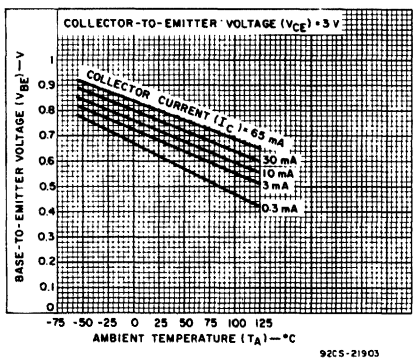


Fig.3 — Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

CA3097E

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = -1mA, I_B = –100μA-	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

TYPICAL CHARACTERISTICS (CONT'D)

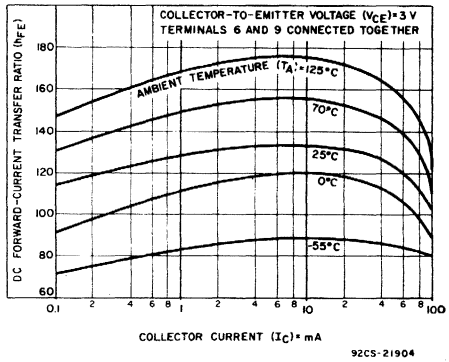


Fig.4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

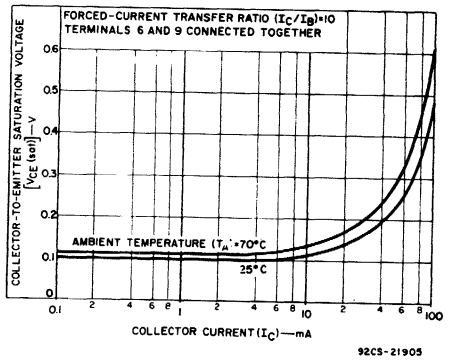


Fig.5 – Collector-to-emitter saturation voltage vs. collector for n-p-n- transistors Q3 & Q5.

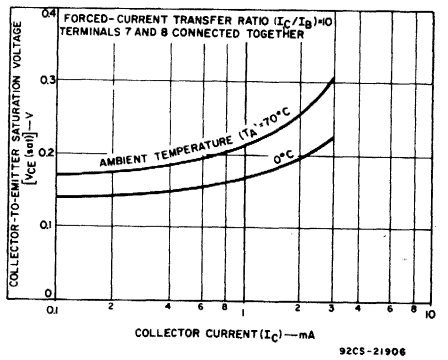


Fig.6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

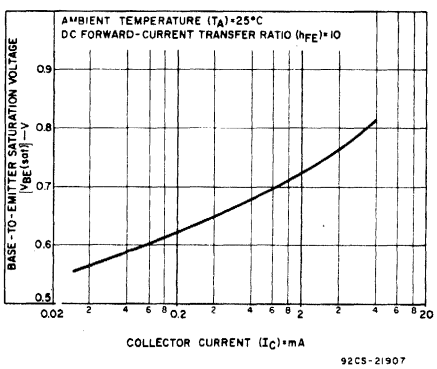


Fig.7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

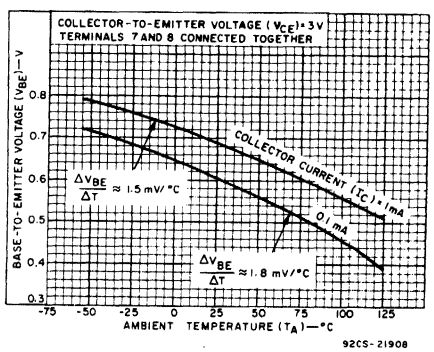


Fig.8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

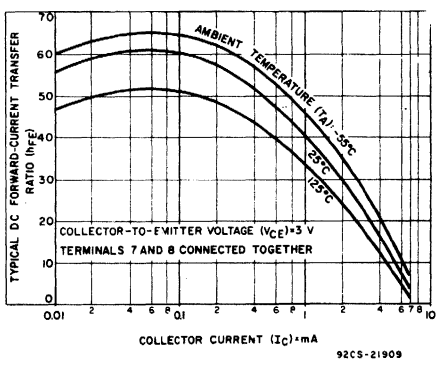


Fig.9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

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ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	Typ.	Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF, Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V, C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA, TERM. 5 TO SUBSTRATE		50	80	–	V

* $V_T = V_P - V_S$ (Fig. 22)

TYPICAL CHARACTERISTICS (CONT'D)

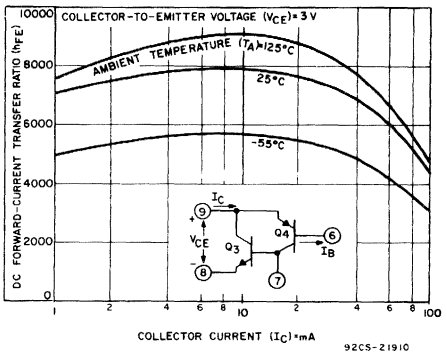

Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

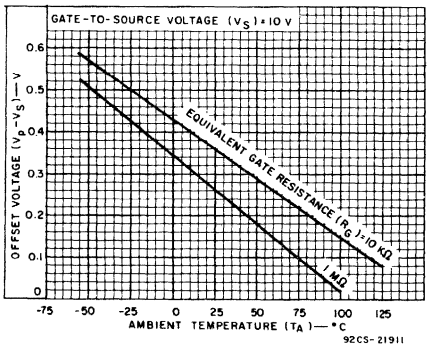

Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

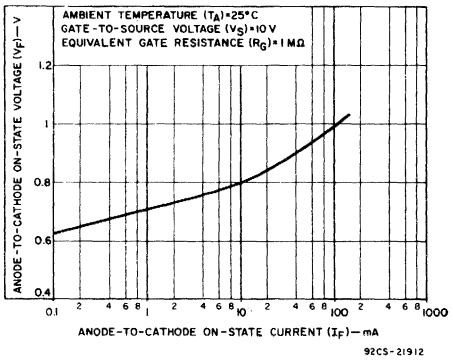

Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

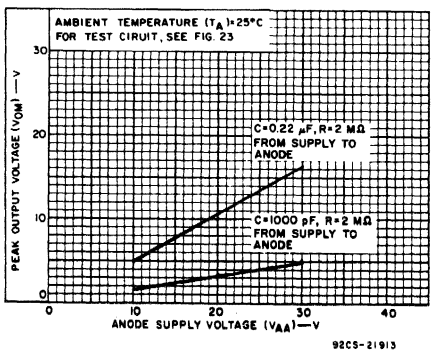

Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

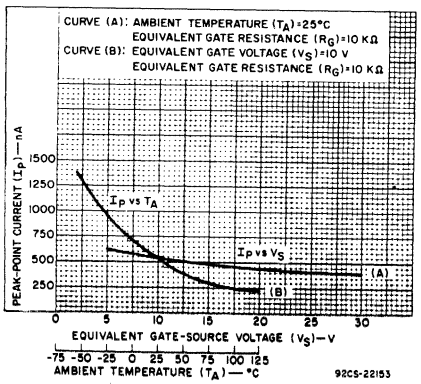

Fig. 14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

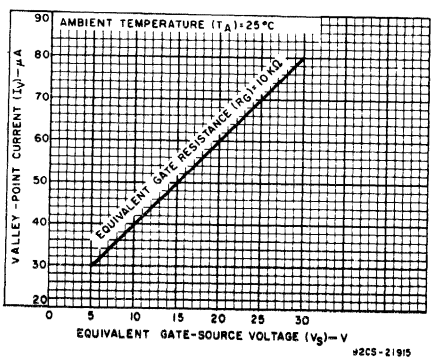

Fig. 15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

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TYPICAL CHARACTERISTICS (CONT'D)

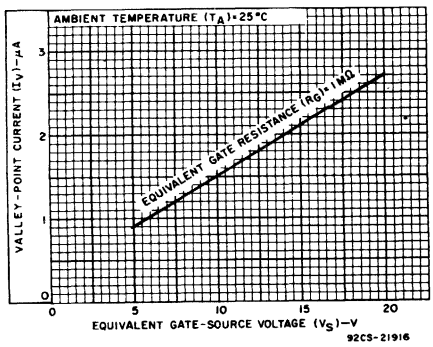

Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

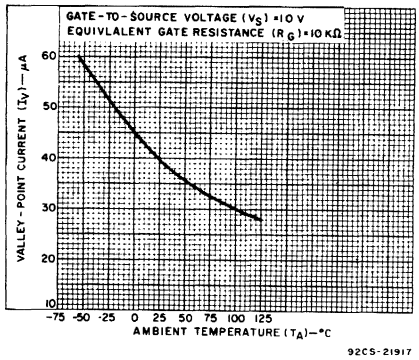

Fig.17 – Valley-point current vs. ambient temperature for Q1 (PUT).

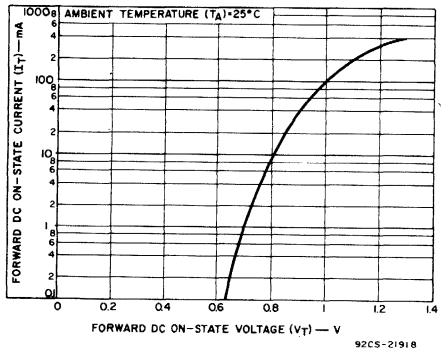

Fig.18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

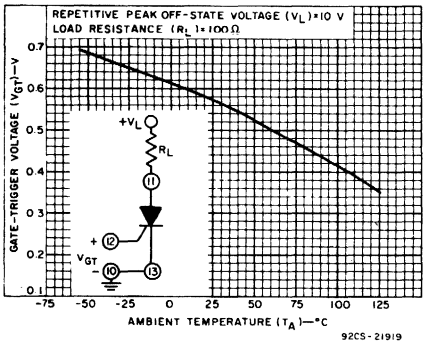

Fig.19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

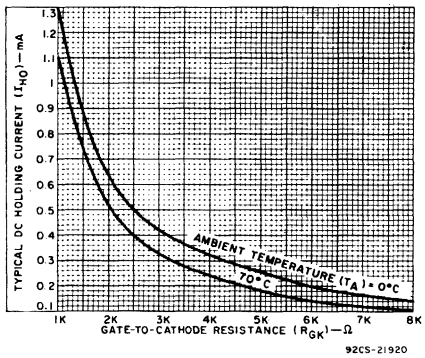

Fig.20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

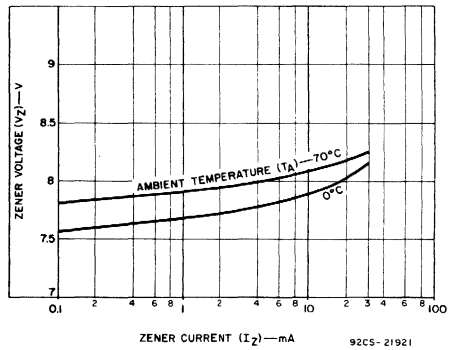

Fig.21 – Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097E

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal is greater than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

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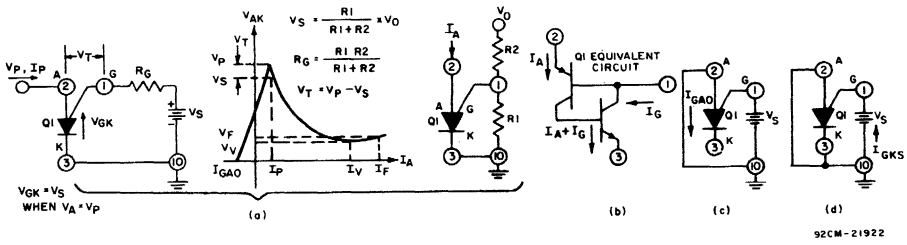

Fig. 22 – General anode characteristics for Q1 (PUT).

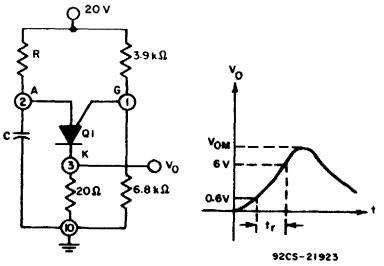

Fig. 23 – Output pulse characteristics for Q1 (PUT).

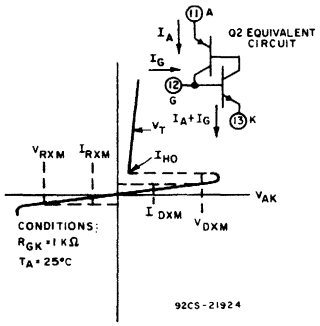

Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

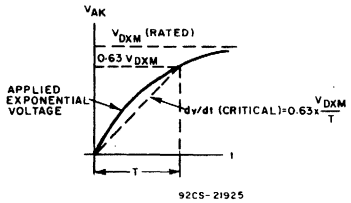

Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).

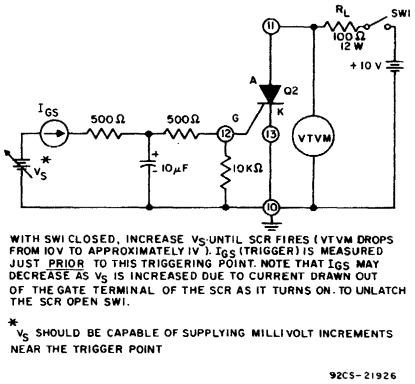

Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

APPLICATIONS CIRCUITS

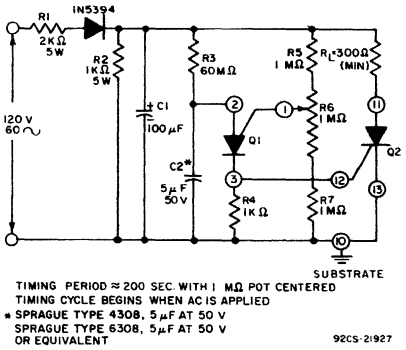

Fig. 27 – AC line-operated one-shot timer.

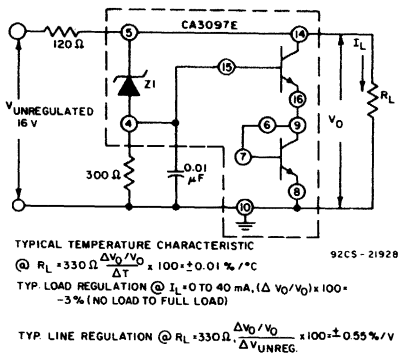

Fig. 28 – Temperature-compensated shunt regulator.

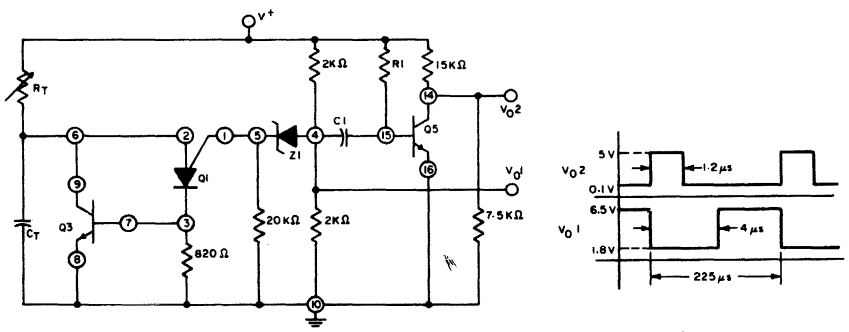

Fig. 29 – Pulse generator.

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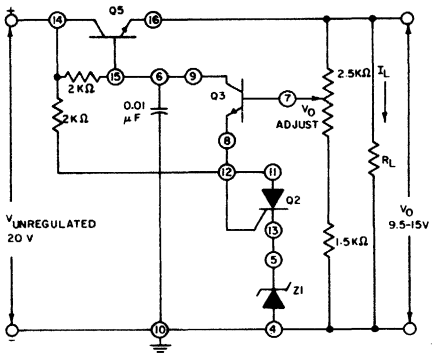
APPLICATIONS CIRCUITS (CONT'D)



TYPICAL LOAD REGULATION @ V_O=12 V, I_L=0 TO 40 mA

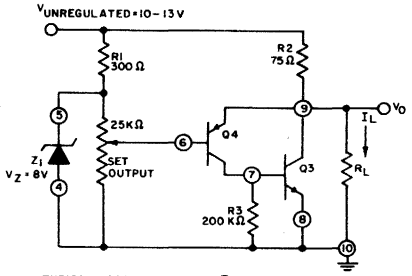
$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\ \%$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O=12 V

$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\ \%/V$

92CS-21930

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O=7 V, I_L=0 TO 40 mA

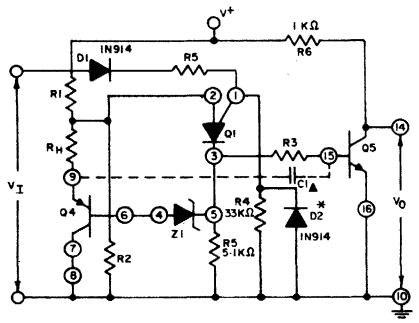
$\frac{\Delta V_O}{V_O} \times 100 = -1.1\ \%$

TYPICAL LINE REGULATION @ V_O=7 V, I_L=20 mA

$\frac{\Delta V_O}{V_O} / \Delta V_{UNREGULATED} = \pm 0.85\ \%/VOLT$

92CS-21931

Fig. 31 – 5 to 7.5 V shunt regulator.



▲ OPTIONAL SPEED-UP CAPACITOR

* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:

FREQUENCY IN = 0-10 KHz

SUPPLY VOLTAGE (V^+) = 15 V

R1, R2, R_H = 5.1 KΩ

R3 = 6.2 KΩ, R_S = 300Ω

C_1 = 820 pF

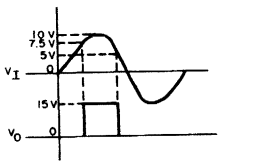
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V

HYSTERESIS VOLTAGE = 2.5 V

UPPER THRESHOLD VOLTAGE $(V_{TH}U) \approx V^+ \frac{R2}{R1+R2}$

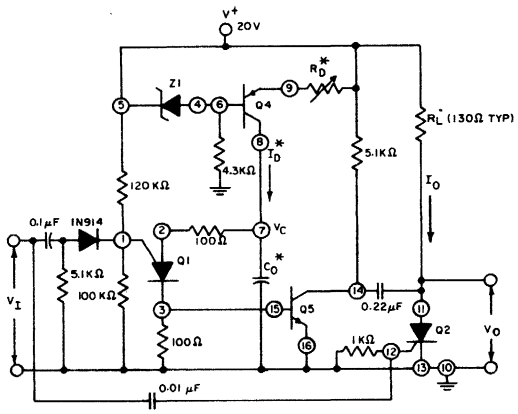
LOWER THRESHOLD VOLTAGE $(V_{TH}L) \approx \frac{(V^+)\left(\frac{R2\ R_H}{R2+R_H}\right)}{\frac{R2\ R_H}{R2+R_H} + R1}$

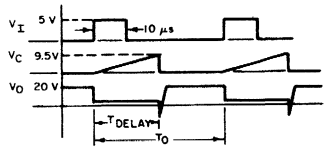
HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 – Schmitt trigger.





*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY C_D. I_D MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

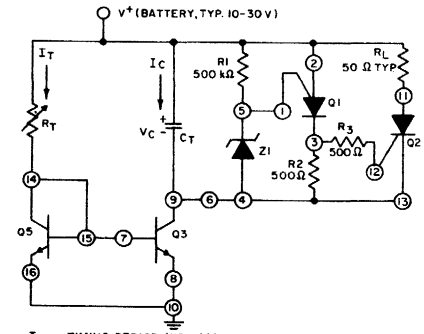
Q2 (SCR) SWITCHING TIMES:

GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP.)

CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP.)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)

PUT FIRES WHEN $V_C \approx 8$ V

$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

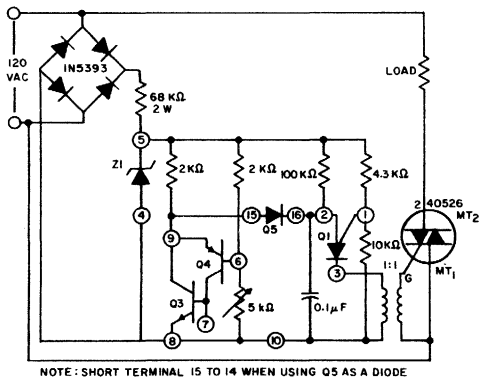
EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN

C_T = 1000 μF, I_T = 16 μA

$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx 1$ MΩ)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.

CA3098 Types

Programmable Schmitt Trigger

— With Memory

—Dual-Input Precision Level Detectors

Applications:

- **Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.**
- **Signal reconditioning**
- **Phase and frequency modulators**
- **On/off motor switching**
- **Schmitt triggers, level detectors**
- **Time delays**
- **Overvoltage, overcurrent, overtemperature protection**
- **Battery-operated equipment**
- **Square and triangular-wave generators**

Features:

- **Programmable operating current**
- **Micropower standby dissipation**
- **Direct control of currents up to 150 mA**
- **Low input on/off current of less than 1 nA for programmable bias current of 1 μA**
- **Built-in hysteresis: 20 mV max.**
- **Programmable hysteresis: 20 mV to V^+**
- **Dual reference input**
- **High sensor range: 100 Ω to 100 MΩ**
- **Stable predictable switching levels**
- **Temperature-compensated reference voltage**
- **Power can be strobed off via term. 2**

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

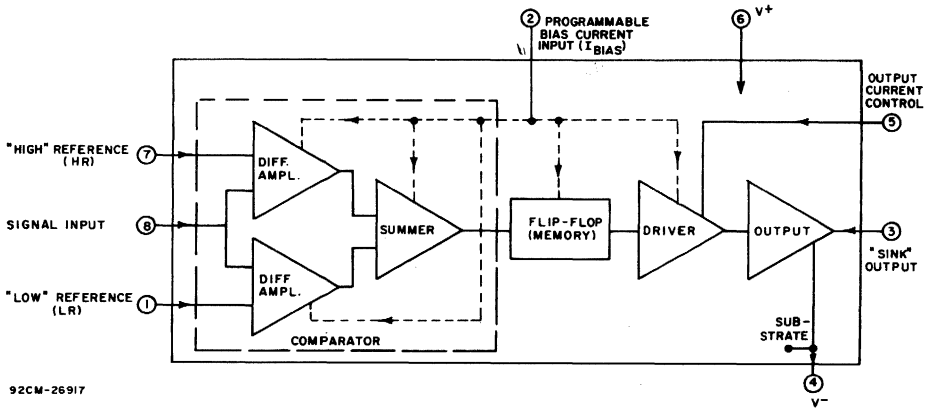


Fig. 1 — Block diagram of CA3098 programmable Schmitt trigger.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above $T_A = 55°C$ Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to $T_A = 55°C$		
CA3098S, CA3098T	1.6	W
Above $T_A = 55°C$		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

CA3098 Types

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs. 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

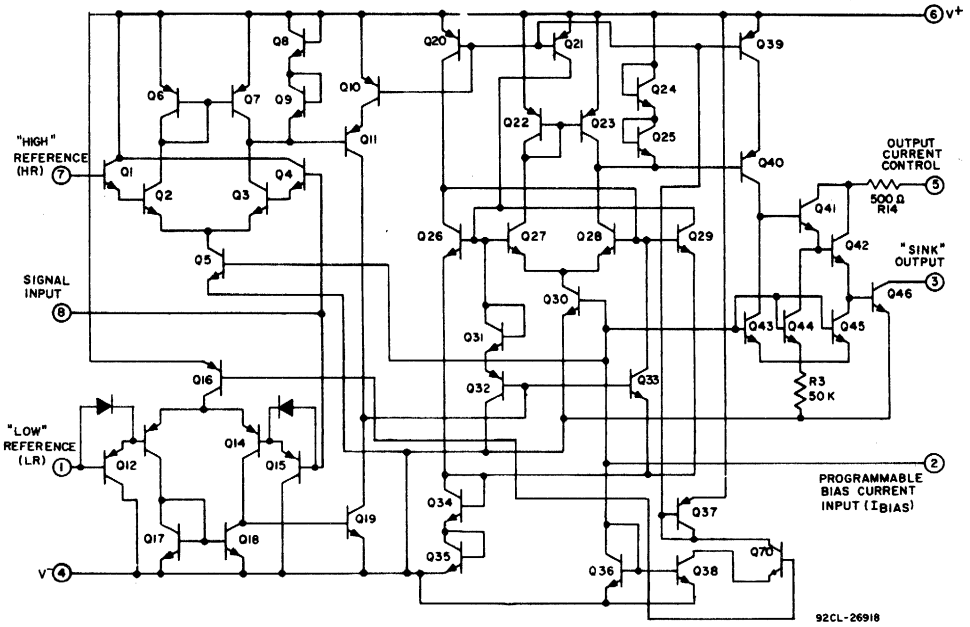


Fig. 2 – Schematic Diagram of CA3098.

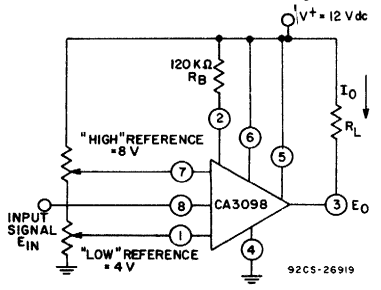


Fig. 3 – Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 – Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

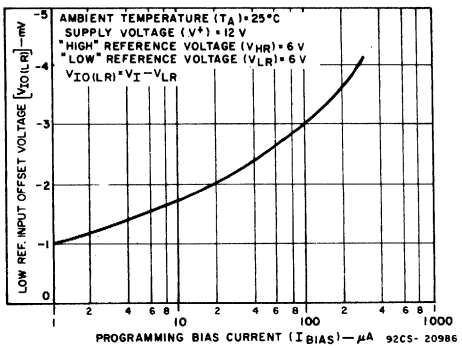


Fig. 5 – Input-offset voltage ("low" reference) vs. programming bias current.

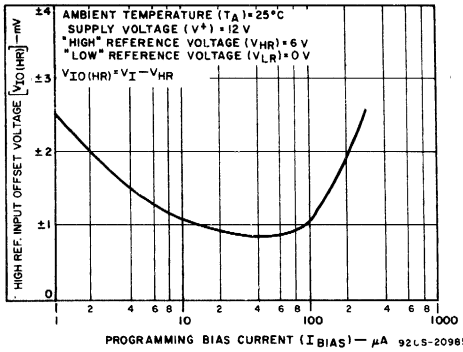


Fig. 6 – Input-offset voltage ("high" reference) vs. programming bias current.

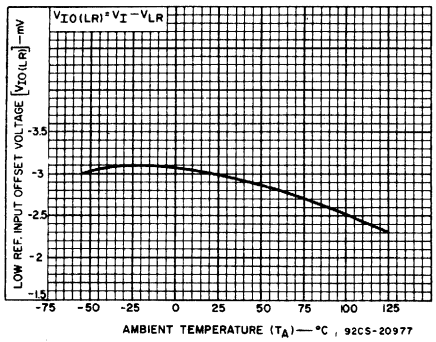


Fig. 7 – Input-offset voltage ("low reference) vs. ambient temperature.

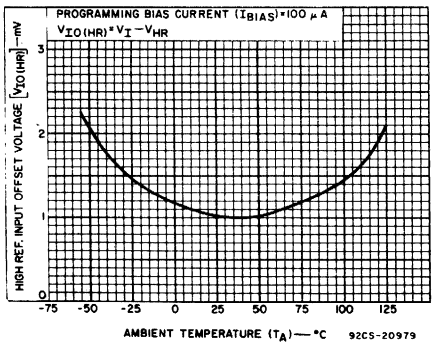


Fig. 8 – Input-offset voltage ("high reference) vs. ambient temperature.

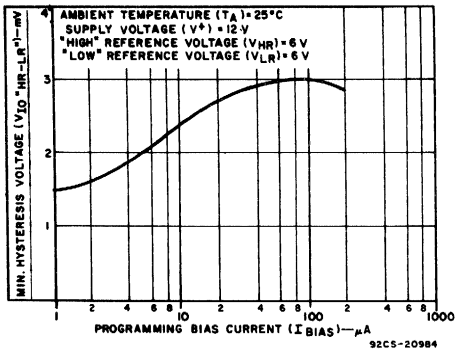


Fig. 9 – Min. hysteresis voltage vs. programming bias current.

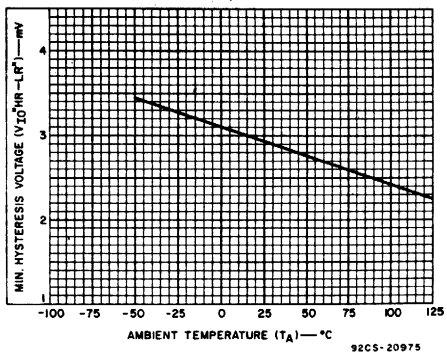


Fig. 10 – Min. hysteresis voltage vs. ambient temperature.

CA3098 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	—	4.5	—	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	—	±8.2	—	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	—	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	—	6.7	—	μV/°C
Output Saturation Voltage, $V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	—	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	15	—	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		—	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	—	—	—	10	μA
Switching Times: Delay, t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	18	—	600	—	ns
Fall, t_f			—	50	—	ns
Rise, t_r			—	500	—	ns
Storage, t_s			—	4.5	—	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	—	100	—	—	mA

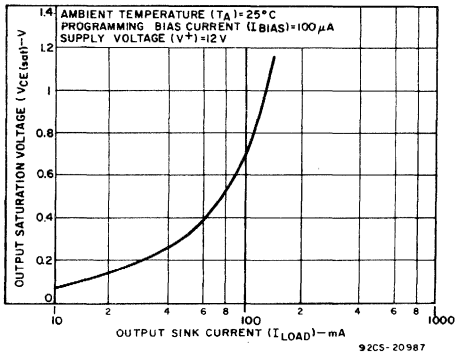


Fig. 11 — Output saturation voltage vs. output sink current.

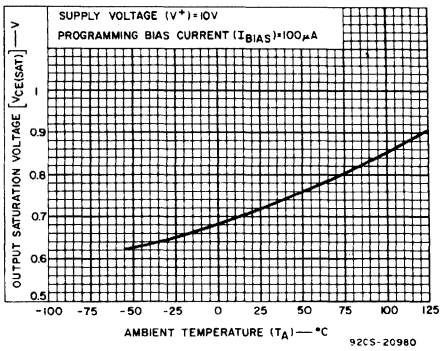


Fig. 12 — Output saturation voltage vs. ambient temperature.

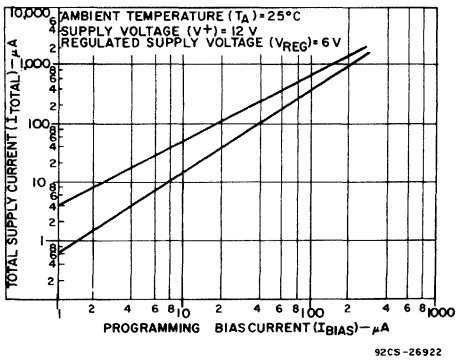


Fig. 13 — Total supply current vs. programming bias current.

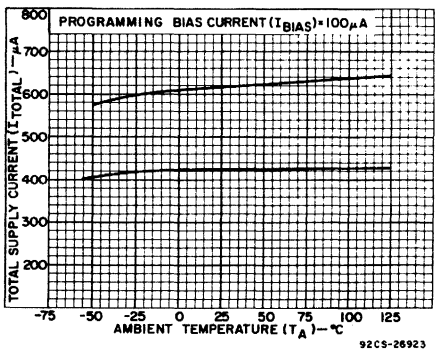


Fig. 14 — Total supply current vs. ambient temperature.

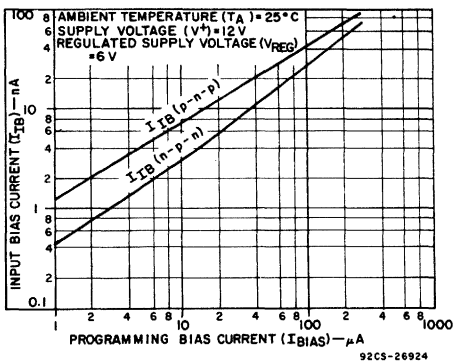


Fig. 15 — Input bias current vs. programming bias current.

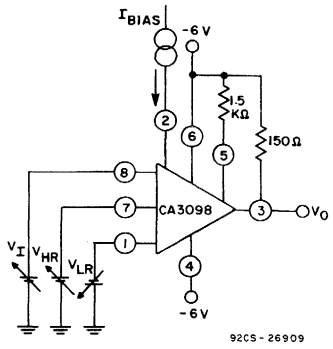


Fig. 16 — Input-offset voltage test circuit.

CA3098 Types

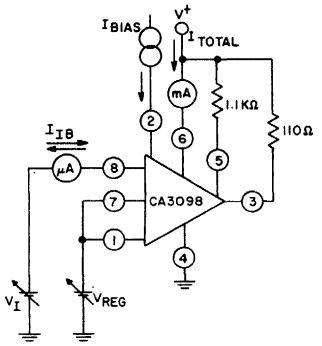


Fig. 17 – Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

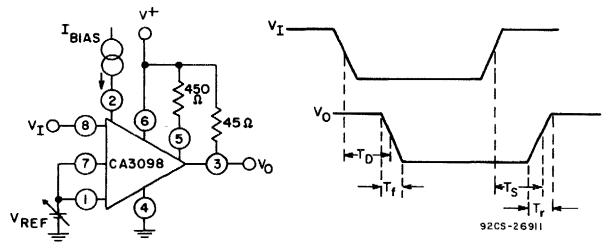


Fig. 18 – Switching time test circuit.

TYPICAL APPLICATIONS

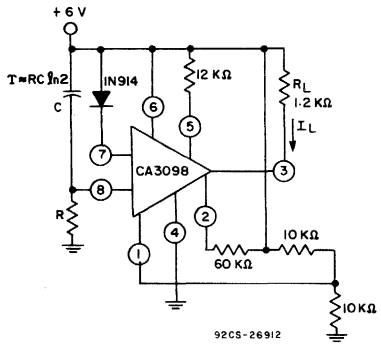


Fig. 19 – Time delay circuit: Terminal 3 "sinks" after τ seconds.

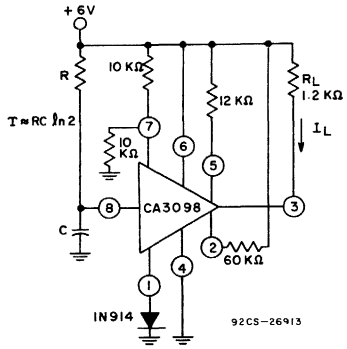


Fig. 20 – Time delay circuit: "sink" current interrupted after τ seconds.

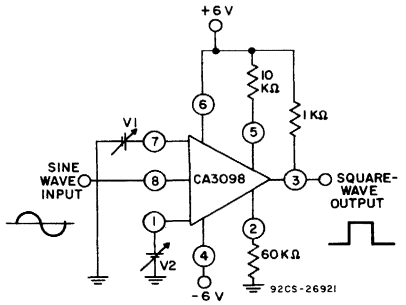
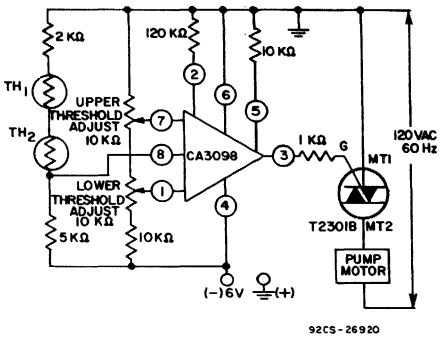


Fig. 21 – Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.
(b) Motor pump remains "ON" until water level falls below thermistor TH_1.
(c) Thermistors, operate in self-heating mode.

Fig. 22(a) – Water-level control.

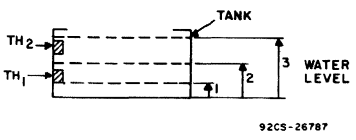


Fig. 22(b) – Water level diagram for circuit of Fig. 22(a).

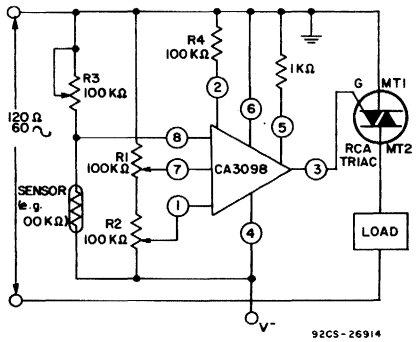


Fig. 23 – OFF/ON control of triac with programmable hysteresis.

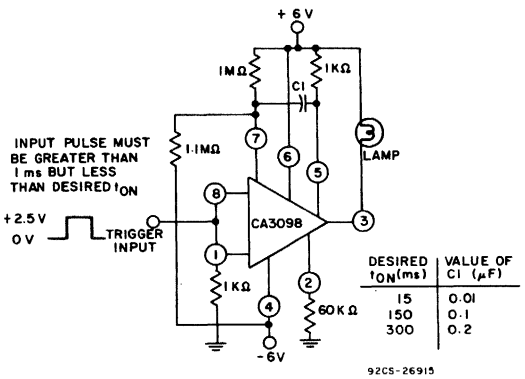


Fig. 24 – One-shot multivibrator.

CA3099E

Programmable Comparator - - With Memory

RCA-CA3099E Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

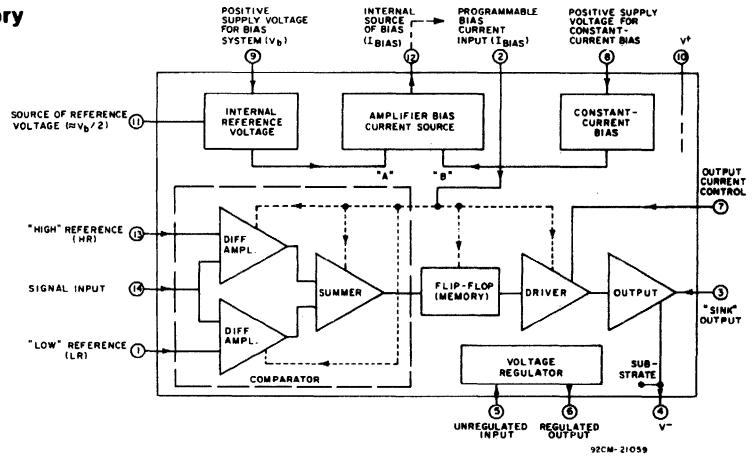


Fig.1–Block diagram of CA3099E programmable comparator.
(See page 3 for general description of circuit operation.)

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V^+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V^+	
Term. 13	2.0 V to V^+	
Term. 1	0 V to V^+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C, Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Termperature (During Soldering): At distance not less than 1/32 inch (0.79 mm) from seating plane for 10 s maximum	+265	°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	$V_{IO\ (LR)}$	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	–8	–3	2	mV
"High" Reference	$V_{IO\ (HR)}$	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	–5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/°C
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times: Delay	t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	22	–	600	–	ns
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	μs

CA3099E

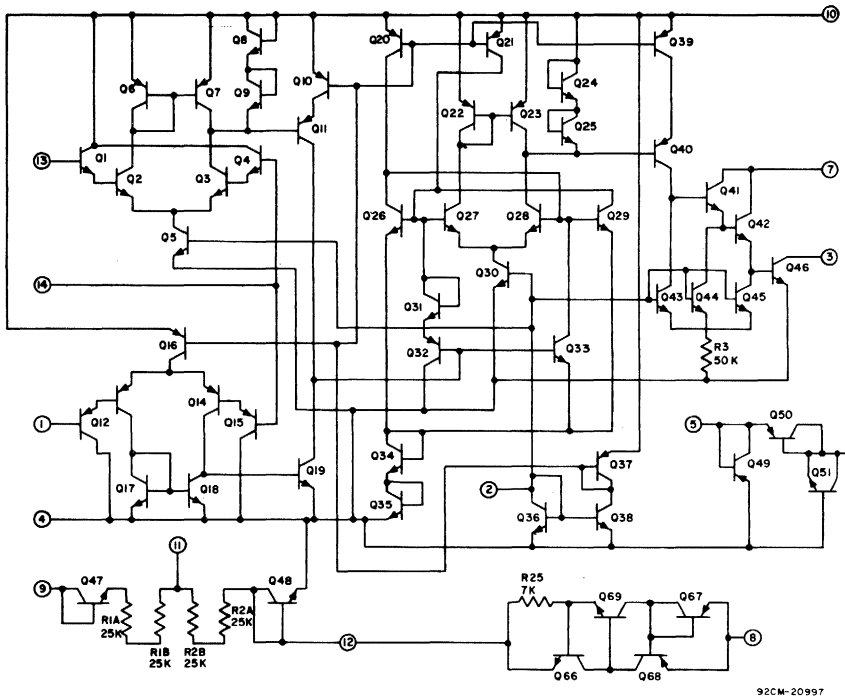


Fig.2–Schematic diagram of CA3099E.

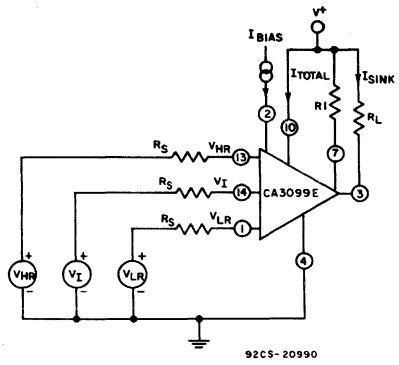


Fig. 3 – Functional diagram.

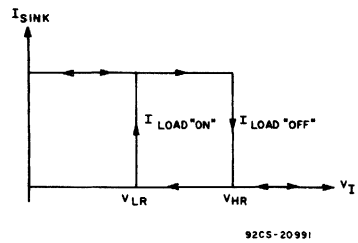


Fig. 4 – Logic diagram.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

TYPICAL CHARACTERISTIC CURVES

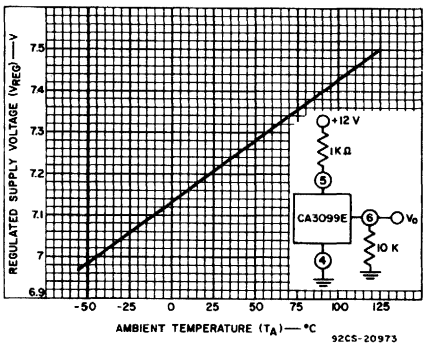


Fig. 5 – Regulated supply voltage vs. ambient temperature.

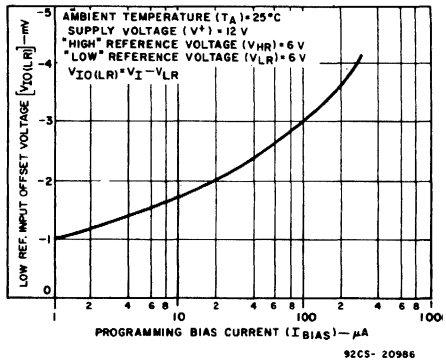


Fig. 6 – Input-offset voltage ("low" reference) vs. programming bias current.

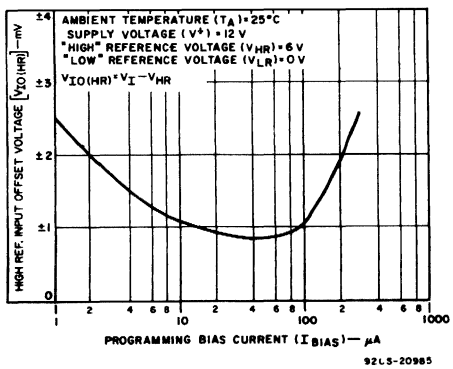


Fig. 7 – Input-offset voltage ("high" reference) vs. programming bias current.

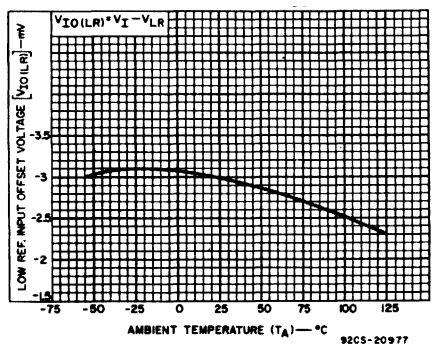


Fig. 8 – Input-offset voltage ("low" reference) vs. ambient temperature.

CA3099E

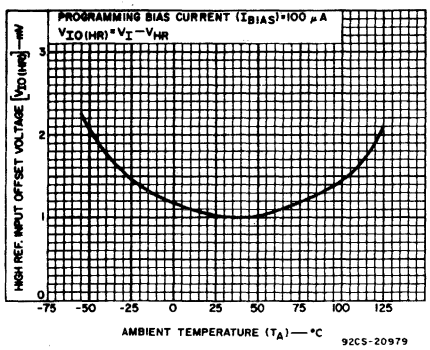


Fig. 9 – Input-offset voltage ("high" reference) vs. ambient temperature.

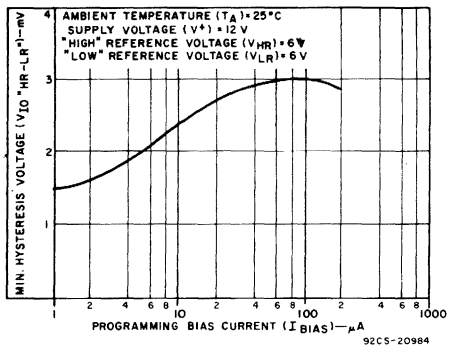


Fig. 10 – Min. hysteresis voltage vs. programming bias current.

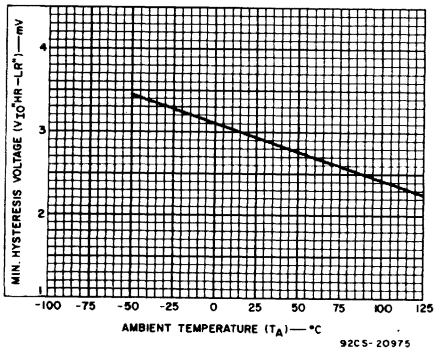


Fig. 11 – Min. hysteresis voltage vs. ambient temperature.

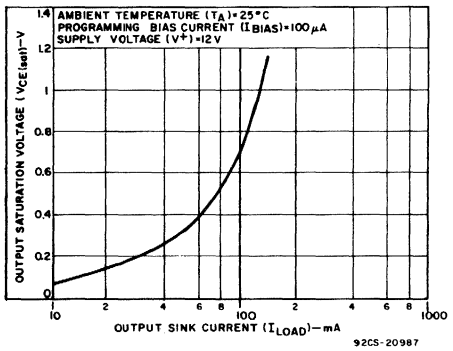


Fig. 12 – Output saturation voltage vs. output sink current.

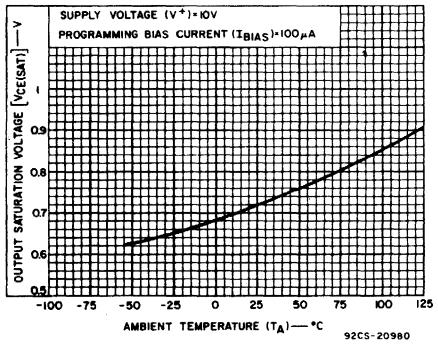


Fig. 13 – Output saturation voltage vs. ambient temperature.

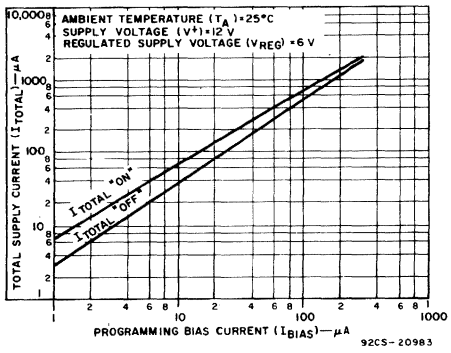


Fig. 14 – Total supply current vs. programming bias current.

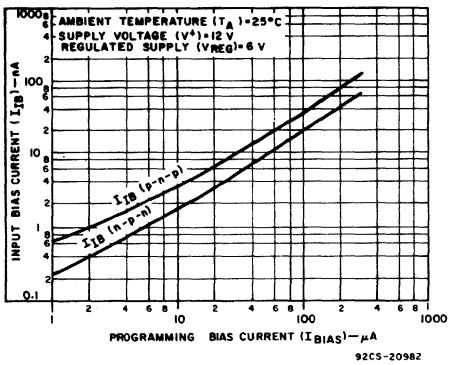


Fig. 15 - Input bias current vs. programming bias current.

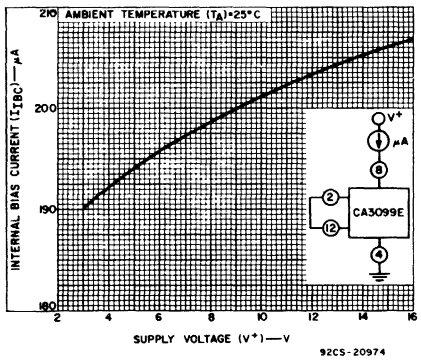


Fig. 16 – Internal bias current vs. supply voltage.

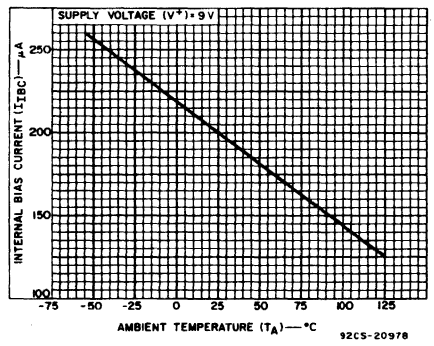


Fig. 17 – Internal bias current vs. ambient temperature.

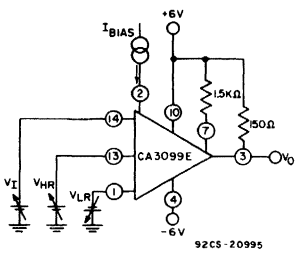


Fig. 18 – Input-offset voltage test circuit.

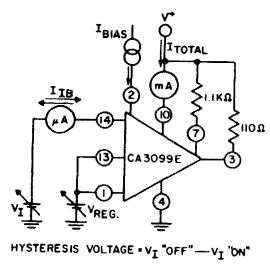


Fig. 19 – Min. hysteresis voltage, total supply current, and input bias current test circuit.

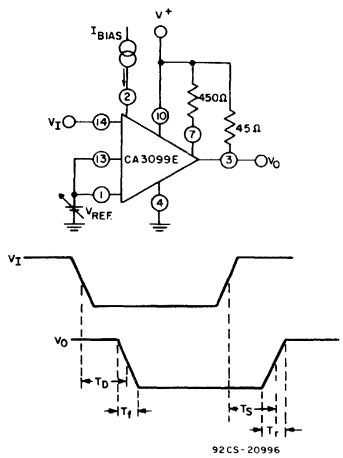


Fig. 20 – Switching time test circuit.

For application information, see Data Bulletin File No. 620.

CA3100
Wideband Operational Amplifier

RCA-CA3100S, CA3100T is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 V p-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

Applications:

- **Video amplifiers**
- **Fast peak detectors**
- **Meter-driver amplifiers**
- **High-frequency feedback amplifiers**
- **Video pre-drivers**
- **Oscillators**
- **Multivibrators**
- **Voltage-controlled oscillator**
- **Fast comparators**

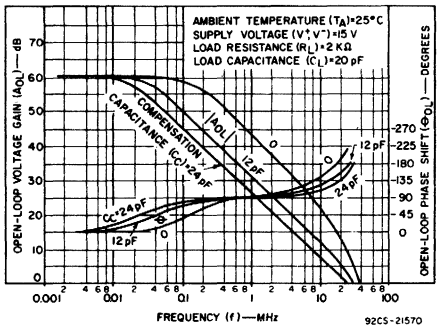


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

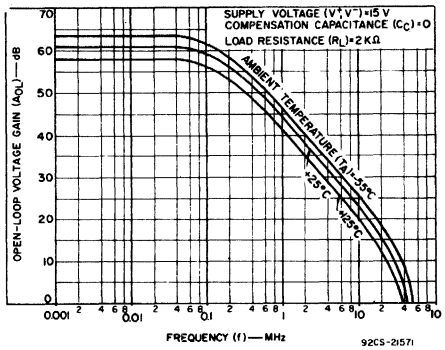


Fig. 3 – Open-loop gain vs. frequency and temperature.

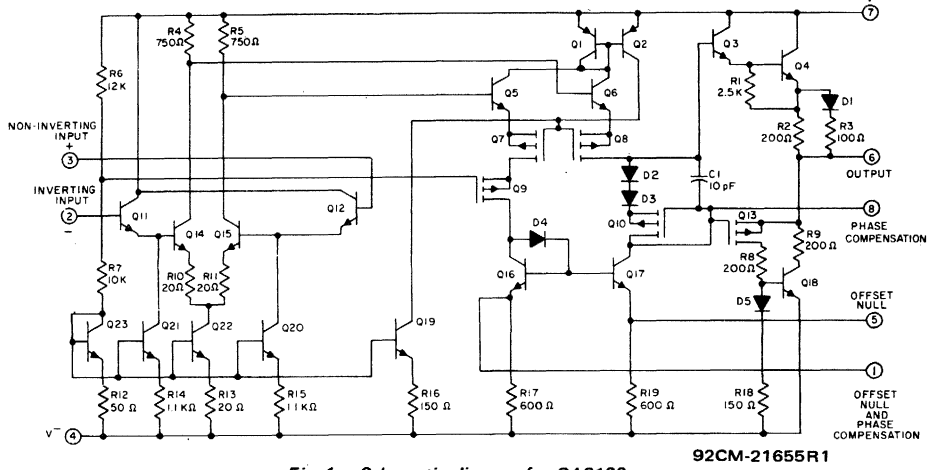


Fig. 1 – Schematic diagram for CA3100.

Features:

- **High open-loop gain at video frequencies – 42 dB typ. at 1 MHz**
- **High unity-gain crossover frequency (f_T) – 38 MHz typ.**
- **Wide power bandwidth – V_O = 18 V p-p typ. at 1.2 MHz**
- **High slew rate – 70 V/μs (typ.) in 20 dB amplifier**
  25 V/μs (typ.) in unity-gain amplifier
- **Fast settling time – 0.6 μs typ.**
- **High output current – ±15 mA min.**
- **LM118, 748/LM101 pin compatibility**
- **Single capacitor compensation**
- **Offset null terminals**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage (between V+ and V− terminals) ..	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V−		
Terminal Voltage	±0.5	V
Output Current	50	mA●
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature		
Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..	300	°C

*If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

●CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

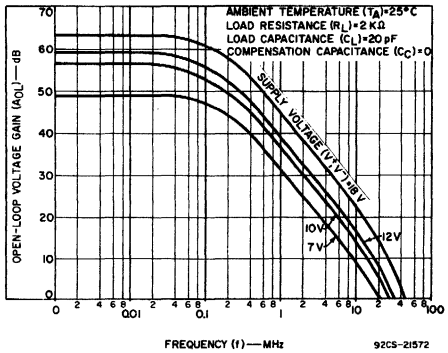


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

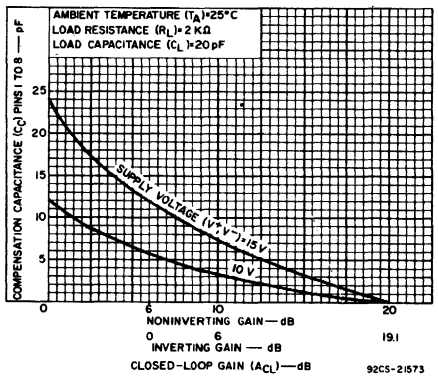


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

CA3100

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	±1	±5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}	V_O = 0 ± 1 V	–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}•	V_O = ± 1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ± 12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	+9	+11	–	V
Maximum Output Voltage: Negative, V_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	−9	−11	–	V
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	+15	+30	–	mA
Maximum Output Current: Negative, I_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	−15	−30	–	mA
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Slew Rate, SR: Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	V/μs
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Power Bandwidth, PBW▲: Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	MHz
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s [To Within ± 50 mV of 9 V Output Swing]	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ • Low-frequency dynamic characteristic

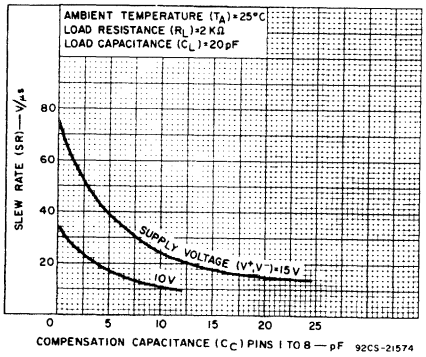


Fig. 6 – Slew rate vs. compensation capacitance.

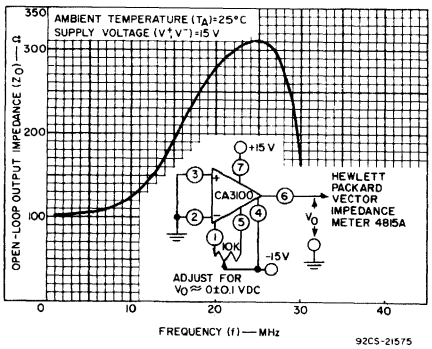


Fig. 7 – Typical open-loop output impedance vs. frequency.

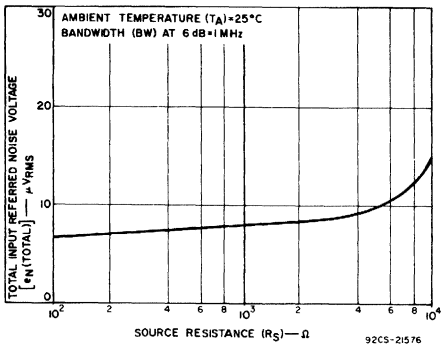


Fig. 8 – Wideband input noise voltage vs. source resistance.

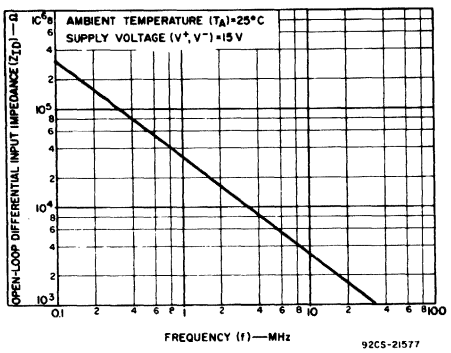


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

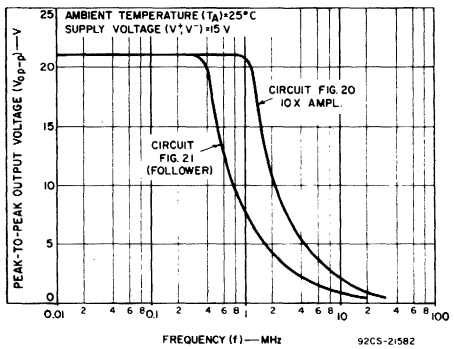


Fig. 10 – Maximum output voltage swing vs. frequency.

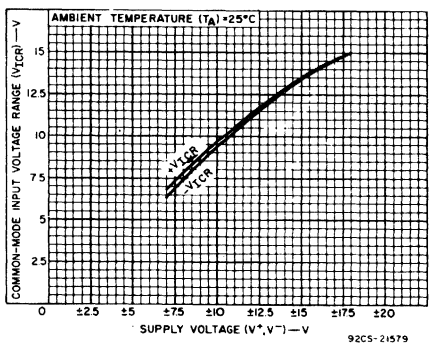


Fig. 11 – Common-mode input voltage range vs. supply voltage.

CA3100

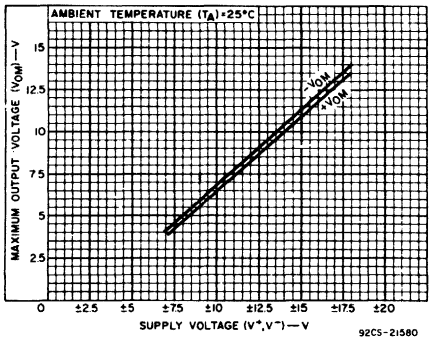


Fig. 12 – Maximum output voltage vs. supply voltage.

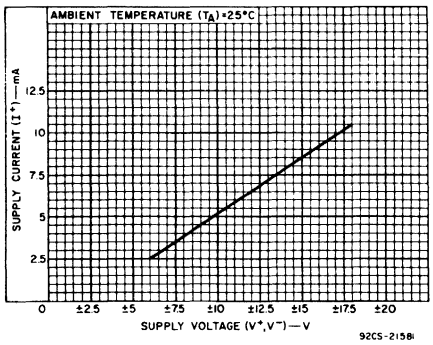


Fig. 13 – Supply current vs. supply voltage.

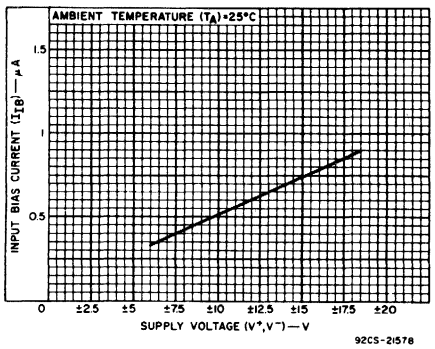


Fig. 14 – Input bias current vs. supply voltage.

TEST CIRCUITS

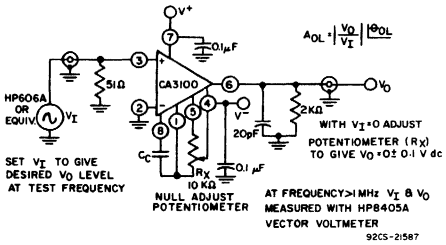


Fig. 15 – Open-loop voltage gain test circuit.

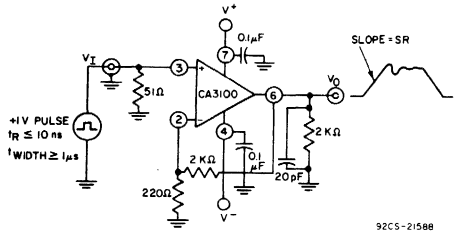


Fig. 16 – Slew rate in 10X amplifier test circuit.

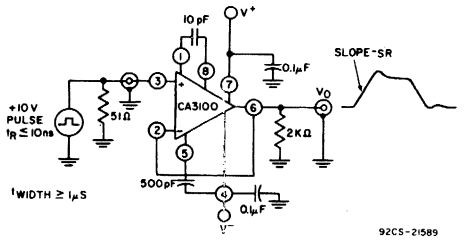


Fig. 17 – Follower slew rate test circuit.

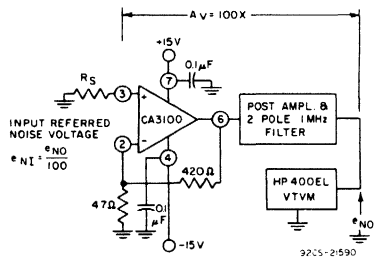


Fig. 18 – Wideband input noise voltage test circuit.

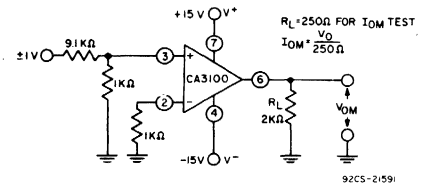


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

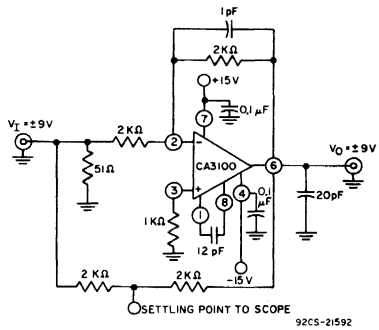


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

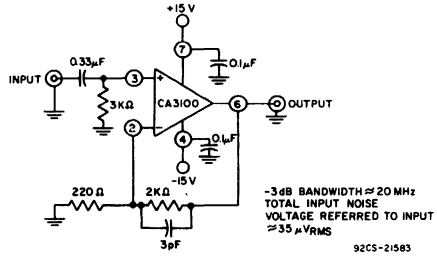


Fig. 21 – 20 dB video amplifier.

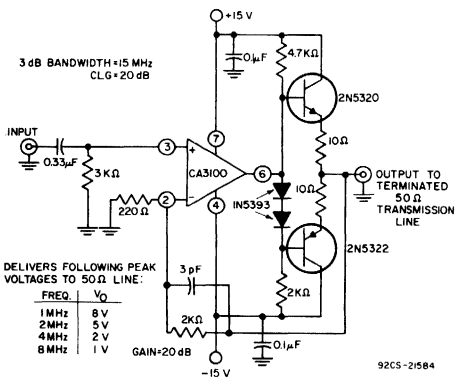


Fig. 22 – 20 dB video line driver.

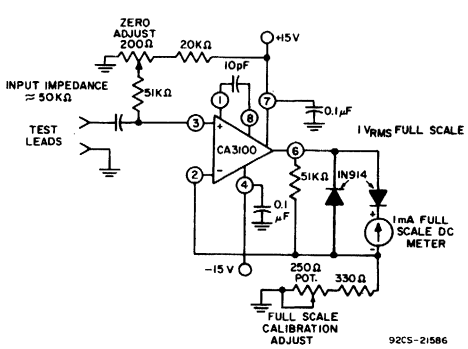


Fig. 23 – 1 MHz meter-driver amplifier.

CA3118, CA3146, CA3183 Types

High-Voltage Transistor Arrays

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA-3183AE, and CA3183E are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range.

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design.

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

Features

- Matched general-purpose transistors
- V_{BE} matched ±5mV max.
- Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)
- Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)
- High I_C: 75mA max. (CA3183AE, E)

Applications

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers (CA3183AE, E)
- Thyristor firing (CA3183AE, E)

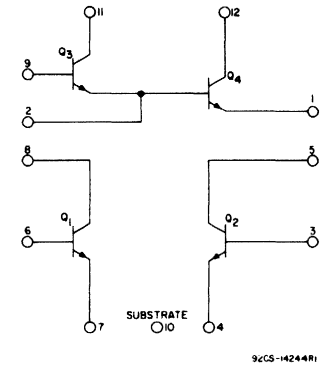
TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	V_{CE} sat. at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	Diff. Pair at 1mA V_{IO} max. mV	Diff. Pair at 1mA I_{IO} max. µA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	
CA3118T	300	50	30	40	0.33	95	±5	2	
CA3146AE	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3146E	300	50	30	40	0.33	95	±5	2	
CA3183AE	500	75	40	50	0.16	75	±5	2.5	
CA3183E	500	75	30	40	0.16	75	±5	2.5	

● Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW/°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW/°C.

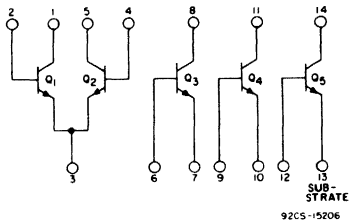
MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –	−55 to +125	°C
Storage (all types)	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

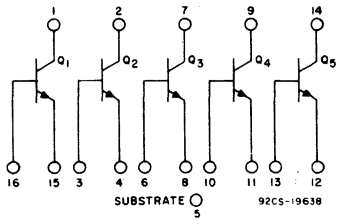
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3118AT, CA3118T.



CA3146AE, CA314E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

CA3118, CA3146, CA3183 Types

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	V_{CE} sat. typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10 mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50 mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

STATIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C		LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0, I_E = 0		50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0		–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V	I_C=10 mA	–	85	–	–	85	–	–
			I_C=1 mA	30	100	–	30	100	–	
			I_C=10μA	–	90	–	–	90	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1 mA		0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 10mA, I_B = 1 mA		–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):										
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	V_{CE} = 10V, I_B = 0		–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	V_{CE} = 5V, I_C = 1 mA		1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V	I_E = 10mA	–	1.46	–	–	1.46	–	V
			I_E = 1mA	–	1.32	–	–	1.32	–	
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1 mA		–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_E = 1 mA		–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA		0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1mA		–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA		–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO1} - I_{IO2}\rvert$ (CA3146AE and CA3146E only)	I_{IO}	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1 mA		–	0.3	2	–	0.3	2	μA

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (cont'd Fig.2 to 12)

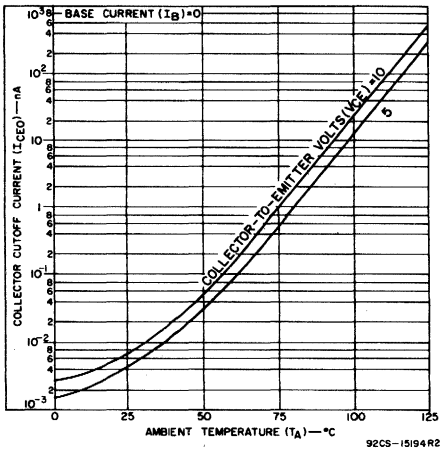


Fig. 2 – I_{CEO} vs. T_A for any transistor.

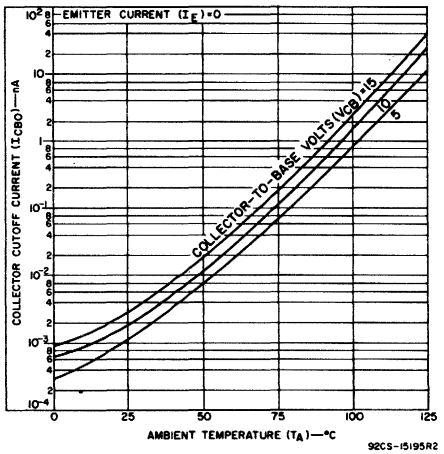


Fig. 3 – I_{CBO} vs. T_A for any transistor.

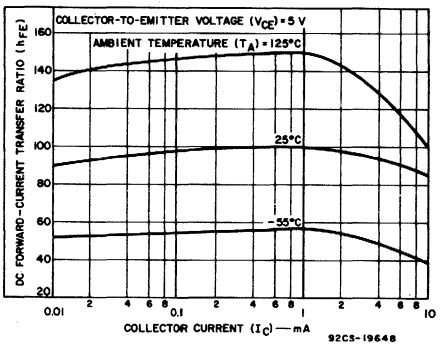


Fig. 4 – h_{FE} vs. I_C for any transistor.

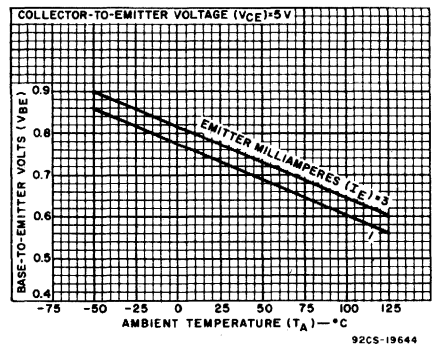


Fig. 5 – V_{BE} vs. T_A for any transistor.

CA3118, CA3146, CA3183 Types

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:									
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–
Admittance Characteristics:									
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}			See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	LIMITS CA3183AE			LIMITS CA3183E			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:									
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}= 3 V, I_C = 10mA	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):									
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = 3V, I_C = 1mA	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (cont'd Fig.2 to 12)

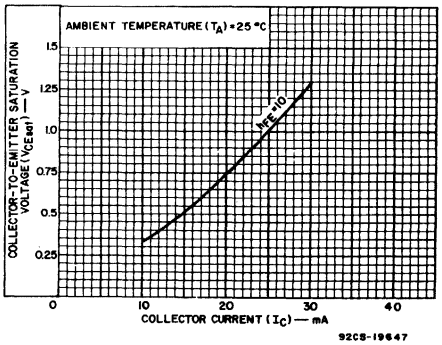


Fig. 6 – V_{CE} sat vs. I_C for any transistor.

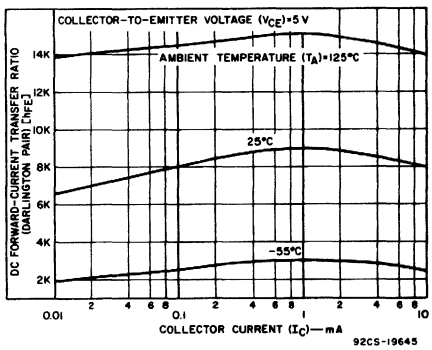


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

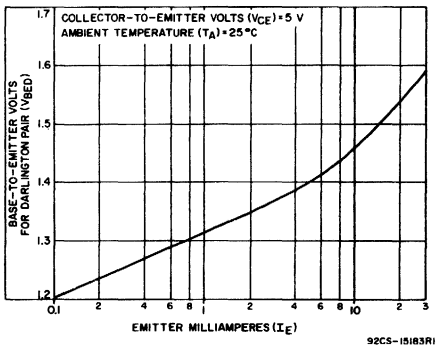


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

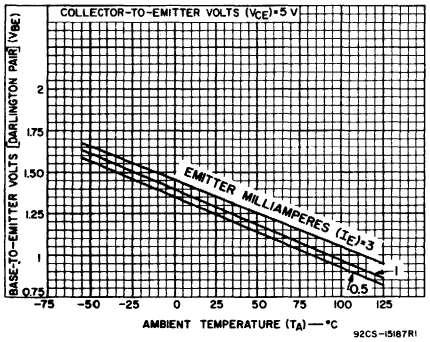


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

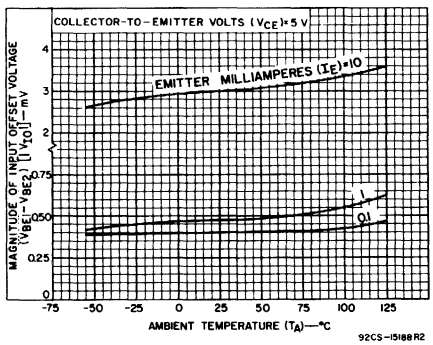


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

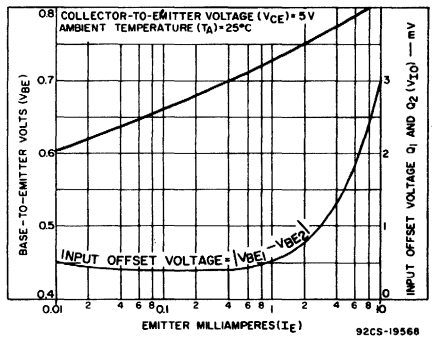


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

CA3118, CA3146, CA3183 Types

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (Fig.2 to 12)

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR)–CA3118,CA3146 SERIES (Fig. 13 to 22)

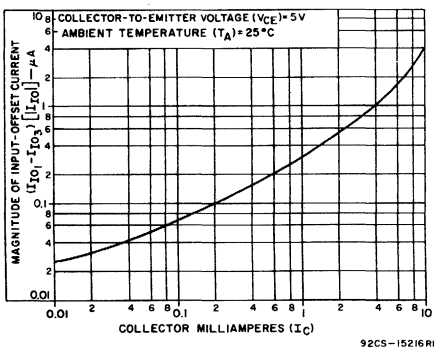


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

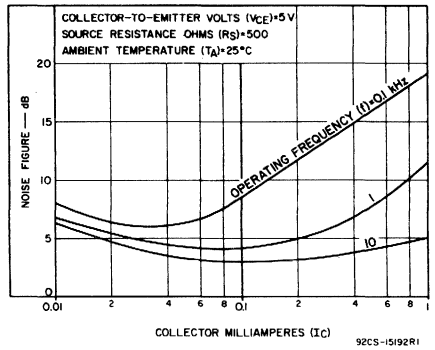


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

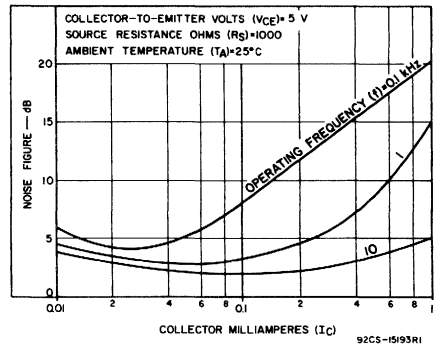


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

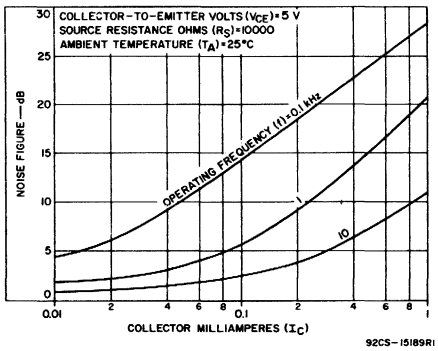


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

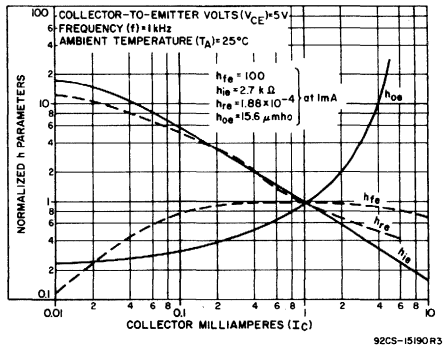


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

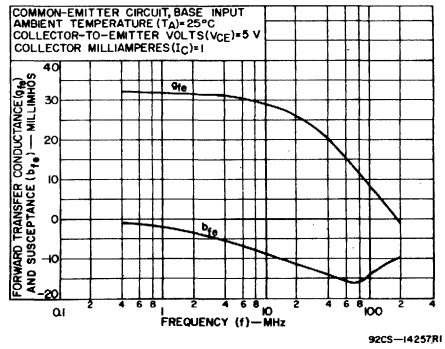


Fig. 17 – y_{fe} vs. f.

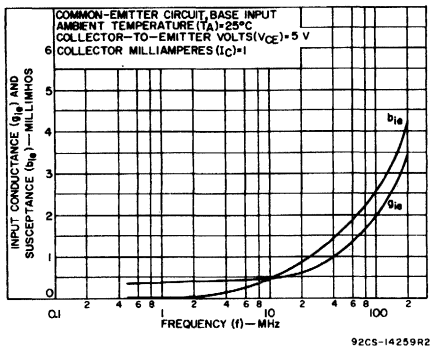


Fig. 18 – y_{ie} vs. f.

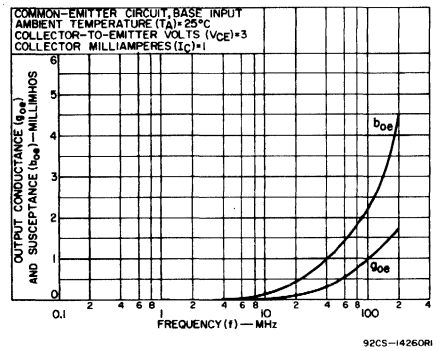


Fig. 19 – y_{oe} vs. f.

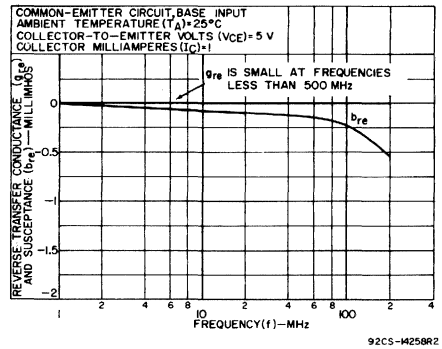


Fig. 20 – y_{re} vs. f.

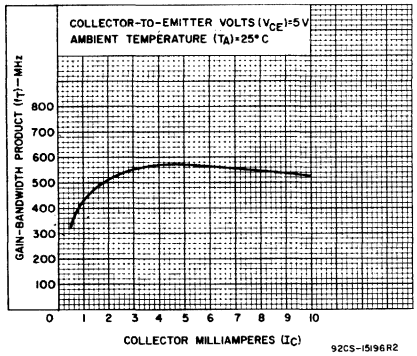


Fig. 21 – f_T vs. I_C.

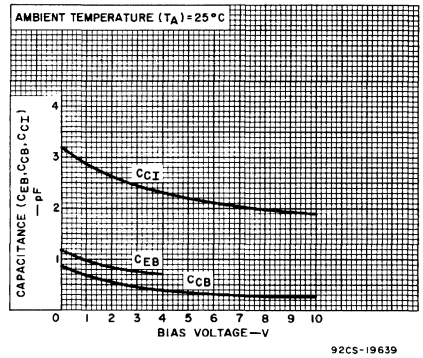


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

CA3118, CA3146, CA3183 Types

TYPICAL STATIC CHARACTERISTICS CURVES—CA3183 SERIES
(Fig. 23 to 30)

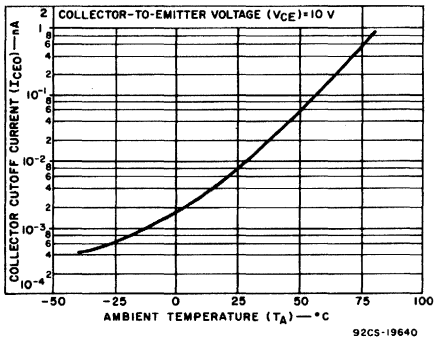


Fig. 23 – I_{CEO} vs. T_A for any transistor.

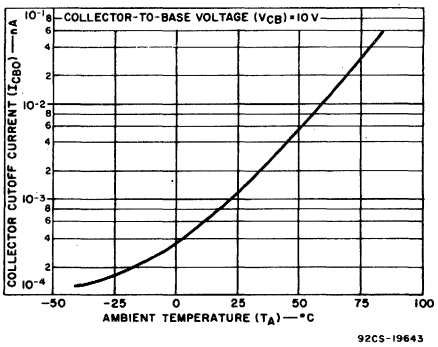


Fig. 24 – I_{CBO} vs. T_A for any transistor.

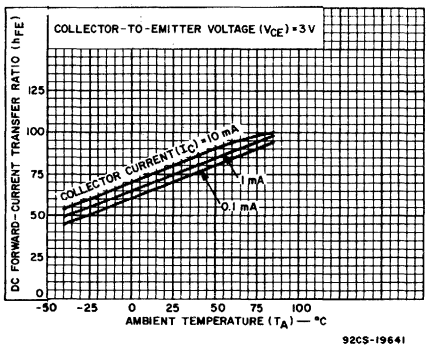


Fig. 25 – h_{FE} vs. T_A for any transistor.

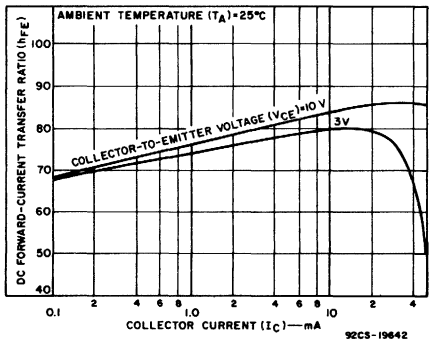


Fig. 26 – h_{FE} vs. I_C for any transistor.

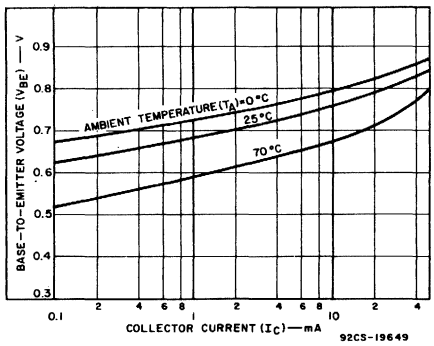


Fig. 27 – V_{BE} vs. I_C for any transistor.

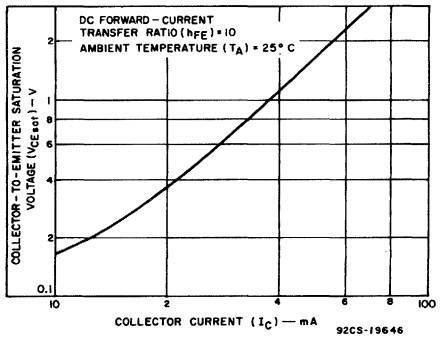


Fig. 28 – $V_{CE\,sat}$ vs. I_C for any transistor.

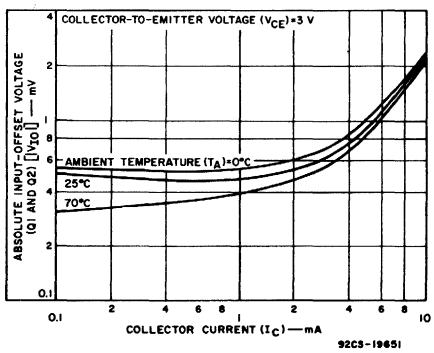


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

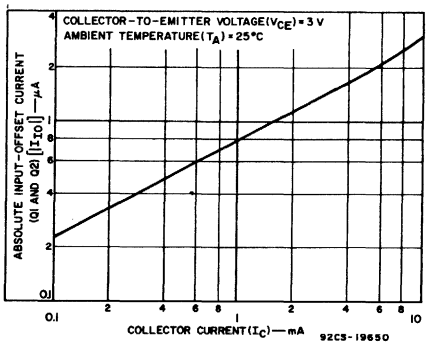


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

CA3120E, CA3142E

TV Signal Processors ("Jungle" Circuits)

For Color and Monochrome Receivers

The RCA-CA3120E and CA3142E are monolithic silicon integrated circuit TV signal processors for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit designs of the CA3120E and CA3142E feature impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques. The AGC noise lockout circuit is deleted in the CA3142E.

Features:

- **Internal impulse noise processing**
- **Sync separator – low impedance, dual polarity**
- **Strobed AGC system**
- **IF AGC output**
- **Delayed outputs for forward or reverse AGC tuners**
- **Automatic noise threshold and AGC detector level control**
- **High-impedance video input**
- **Low-impedance video output**
- **Choice of external time constants for sync separator**
- **Negative power supply not required**
- **RF AGC delay externally controlled**

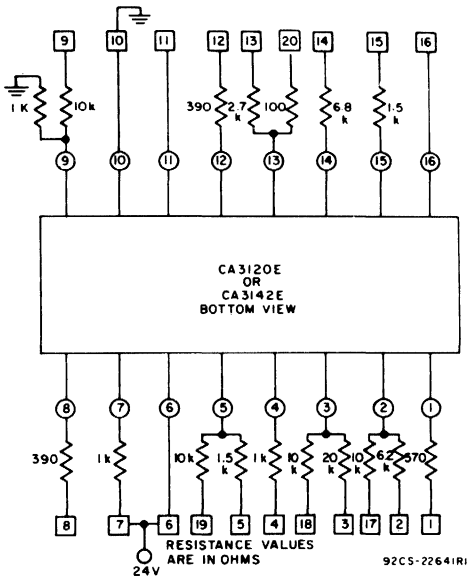


Fig.2 – Test circuit for measuring electrical characteristics of the CA3120E and CA3142E. Refer to Figs. 7 and 8 for switch selector positions.

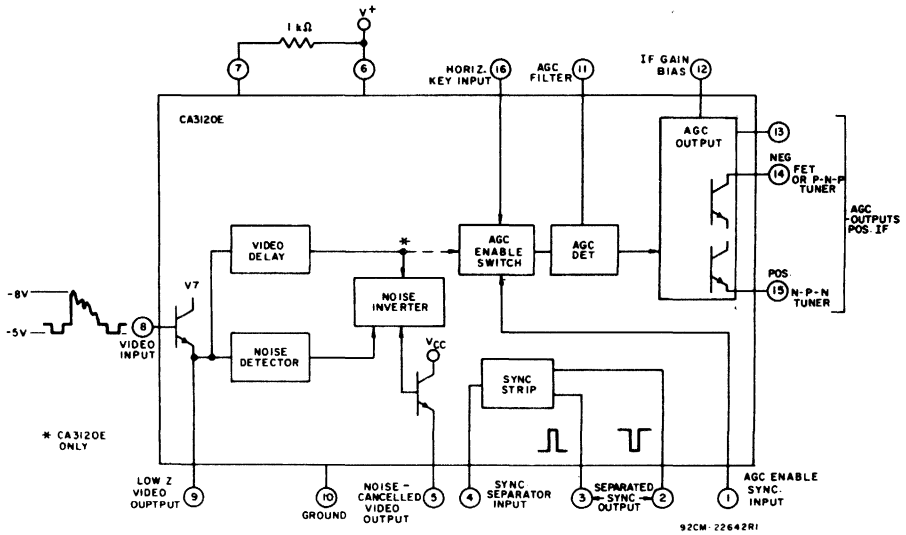


Fig.1 – Simplified block diagram of the CA3120E and CA3142E.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE	30 V
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$ . . . . . Derate linearly at 7.9	mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–40 to +85 °C
Storage	–65 to +150 °C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 °C

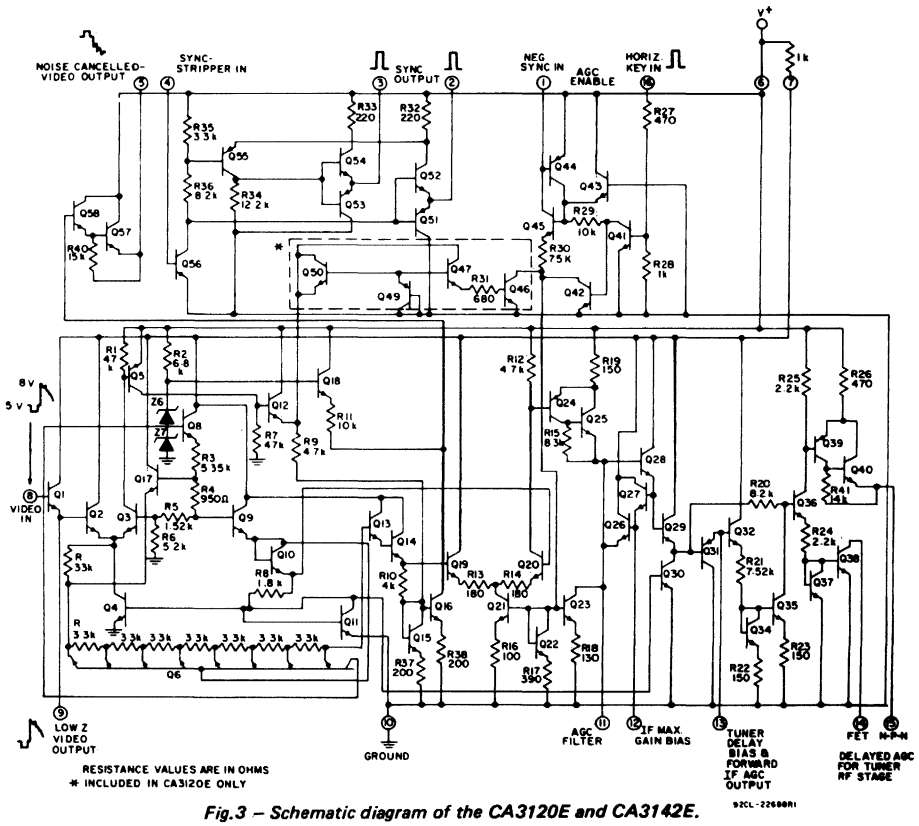


Fig.3 – Schematic diagram of the CA3120E and CA3142E.

CA3120E, CA3142E

CIRCUIT DESCRIPTION*

An AGC sample-and-hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter – The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3120E or CA3142E and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 3). The external resistor (R_{X1} in Fig.9) reduces the dissipation of Q1. The emitter-follower output of Q1 is directly coupled to a differential comparator stage (Q2, Q3). Unless a negative-going pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q12.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Figure 4) – The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage (≅ 0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video-signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 5 shows three typical coupling networks.

Fig. 6 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 6) the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 6), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

* For additional information refer to the IEEE Transactions on Broadcast and TV Receivers," August 1970, pp. 185–195, Vol. BTR No.3.

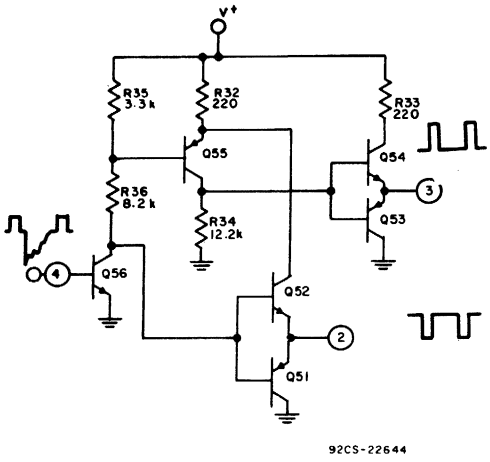


Fig. 4 – Sync separator stage.

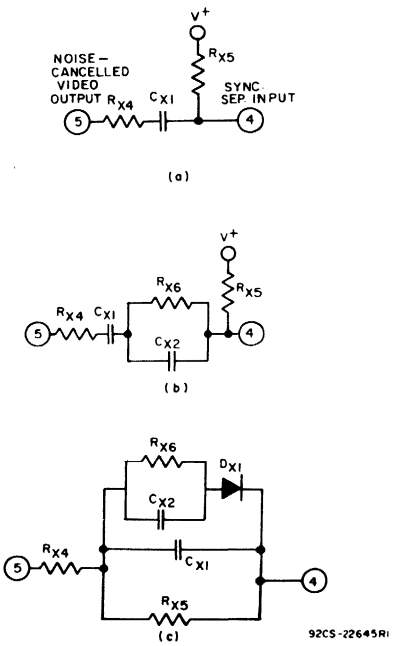


Fig. 5 – Typical coupling networks (Term. 5 to Term. 4).

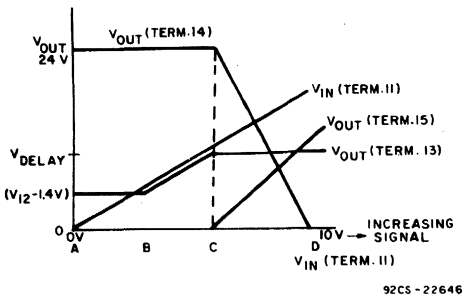


Fig. 6 – Typical operation of the AGC circuits using the CA3120E and CA3142E.

CA3120E, CA3142E

CHARACTERISTIC	TEST CONDITIONS — SWITCH NUMBERS / SWITCH POSITION																	TERMINAL MEASURED
	1	*2*	*3*	*4*	*5*	*8*	*9*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	*2 6 7 9 14*
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	*8*
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	*19*
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 2 and 8.

Fig.7 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 2 and 8 for test circuit and test-condition selector-switch arrangements.

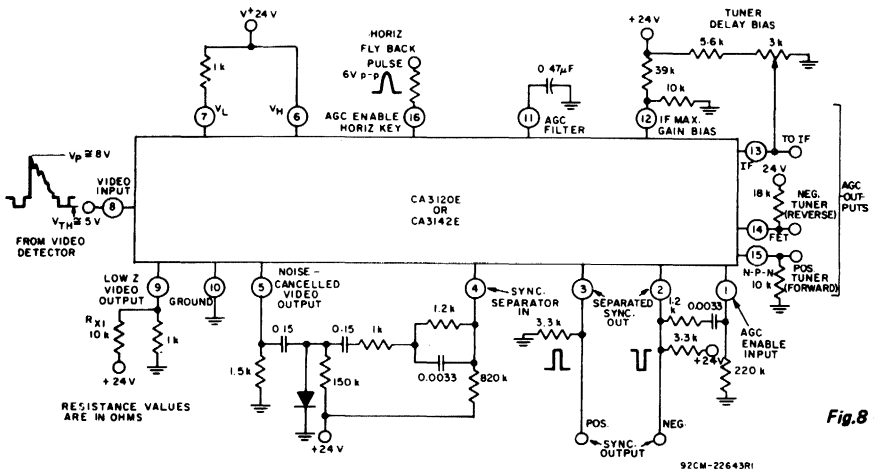
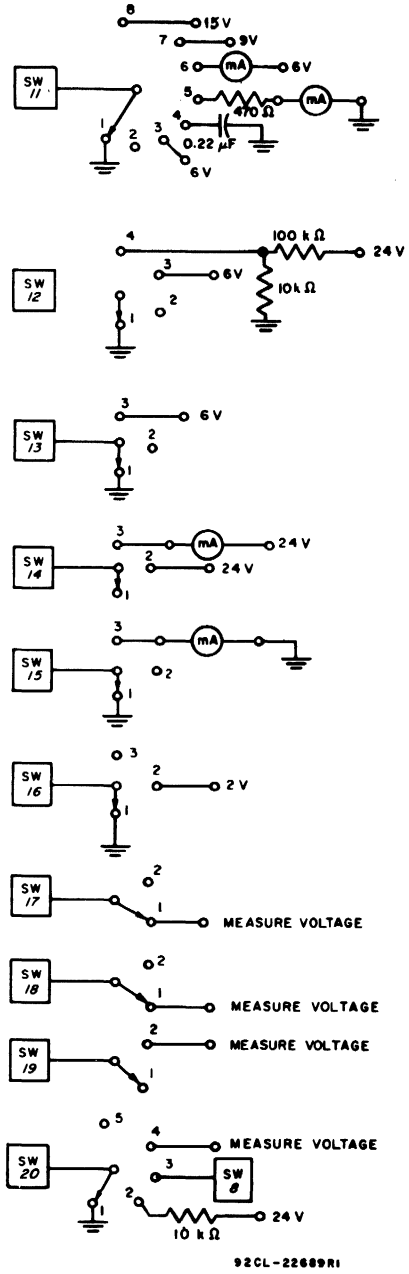


Fig.9 – Typical application using the CA3120E and CA3142E.



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

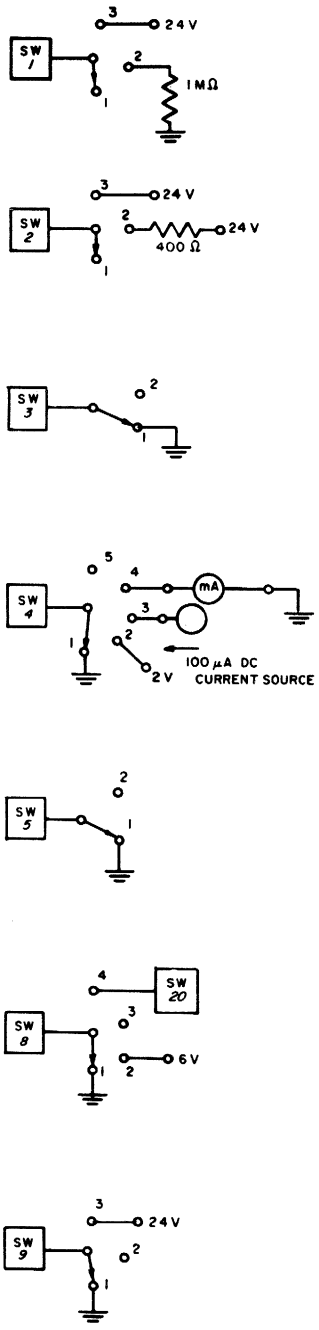
Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

(Figure 8 continued on the next page)

CA3120E, CA3142E

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 2, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3120E CA3142E LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA
Internal Noise-Lockout Time (CA3120E only)	T	1	–	63	μs



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

CA3121E

TV Chroma Amplifier/Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070

RCA-CA3121E is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC and killer control for color-TV receivers. It is designed to function compatibly with the CA3070 in a two package chroma system. Fig. 4 shows a functional block diagram and the outboard circuitry of a typical two-package chroma system incorporating the CA3121E and CA3070, respectively.

The CA3121E is supplied in a 16-lead dual-in-line plastic package.

Features

- **Excellent linearity in dc chroma gain-controlled circuit**
- **Improved filtering reduces 7.2 MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**

MAXIMUM RATINGS at $T_A = 25^\circ C$

Supply Voltage	30 V
Device Dissipation:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$	derate linearly 7.9 mW/°C
Operating Temperature Range	−40 to +85°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

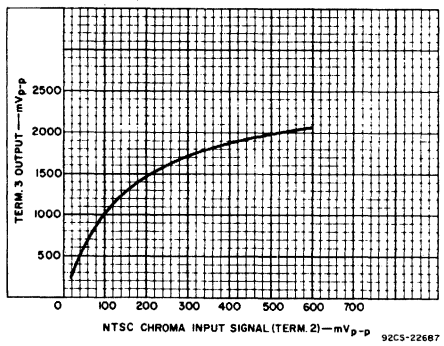


Fig. 2 – Typical ACC plot for the CA3121E when used with the CA3070.

CIRCUIT OPERATION

The CA3121E consists of three basic circuit sections: (1) amplifier No. 1, (2) amplifier No. 2, and (3) demodulator. Amplifier No. 1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No. 1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No. 2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No. 1 acts upon amplifier No. 2 to greatly reduce its gain.

The output from amplifier No. 2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the chroma signal processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121E reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

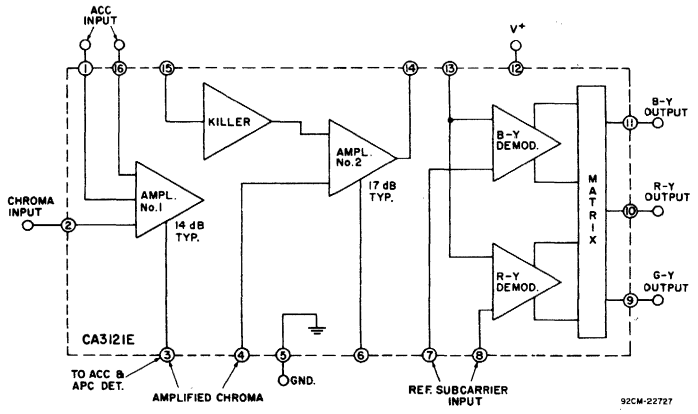


Fig. 1 – Functional block diagram of the CA3121E.

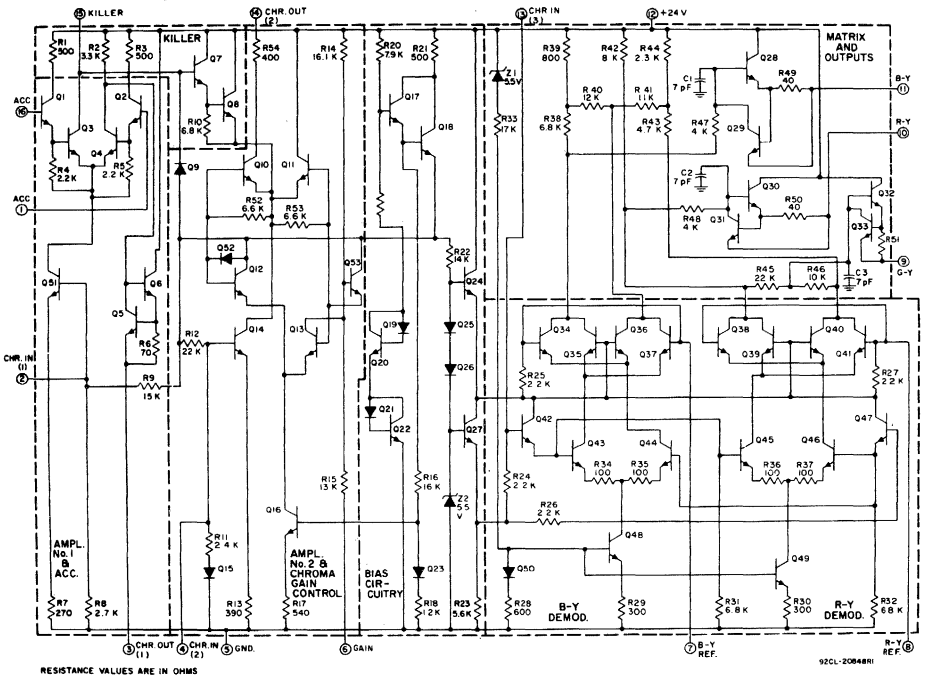


Fig. 3 – Schematic diagram of the CA3121E.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ and Referenced to Test Circuit (Fig. 5)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Supply Current	I_T	–	–	40	44	mA
Input Sensitivity	V_2	Vary Eg; set V_4 for 55 mV RMS	6	10	15	mV RMS
Second-Stage Sensitivity	V_4	Vary Eg; set V_{11} for 2 V RMS	25	55	100	mV RMS
Output Voltage (Killer off)	V_{11}	Switch Position: S1=2, S2=2, S3=2 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Demodulator Characteristics:						
Output Voltages	V_9, V_{10}, V_{11}		13	14.3	15.6	V
DC Output Balance (Between any 2 outputs)	–	–	−0.6	–	+0.6	V
Unbalance	V_9, V_{10}, V_{11}	Eg=0; Switch Position: S1=1, S2=1, S3=1	–	–	0.8	Vp-p
Relative Outputs— R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS	1.4	1.52	1.68	V RMS
G-Y	V_9		0.3	0.4	0.5	V RMS
Relative Phase— R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	−101	−106	−111	degrees
G-Y	V_9	with V_{11} as reference	112	104	96	degrees
Max. Output Voltage	V_{11}	Eg = 750 mV	2.8	–	–	V RMS

CA3121E

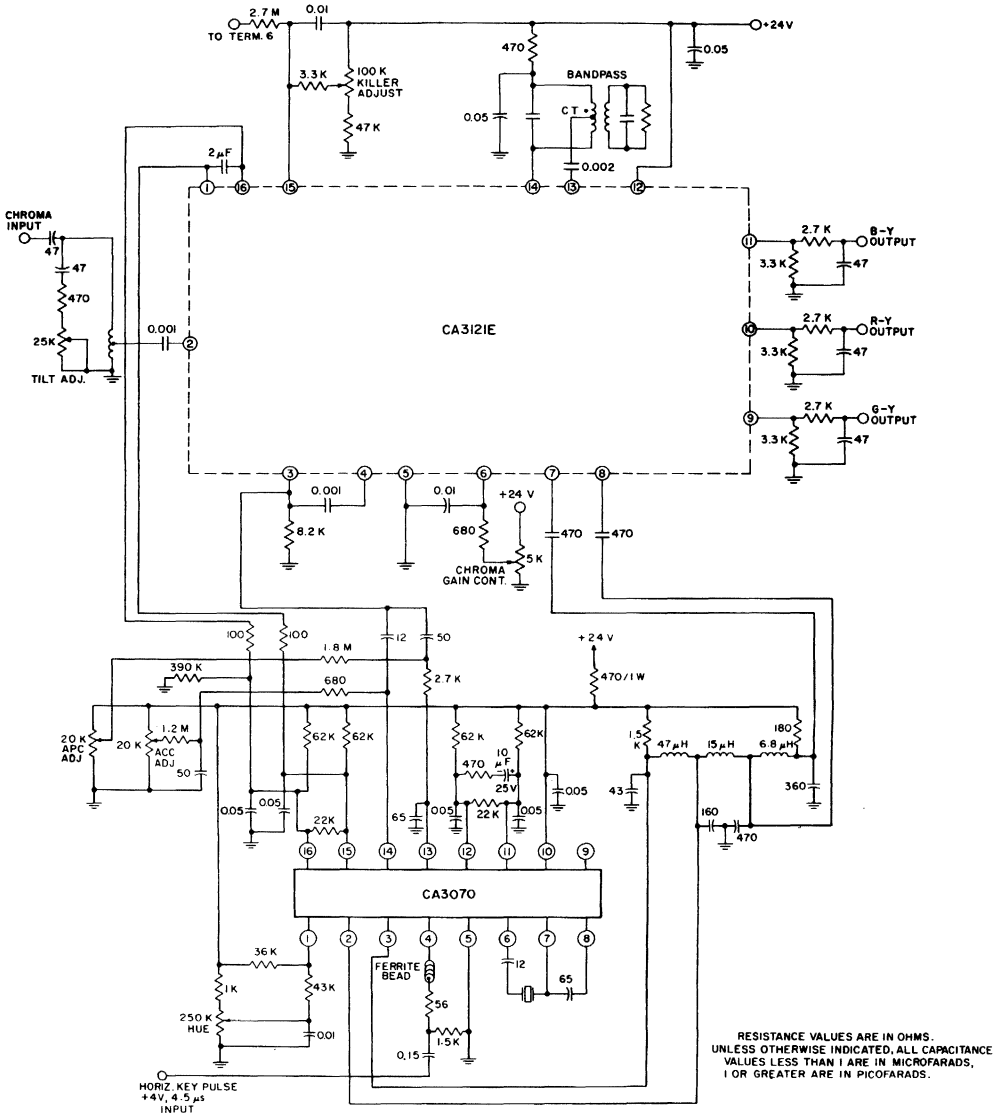
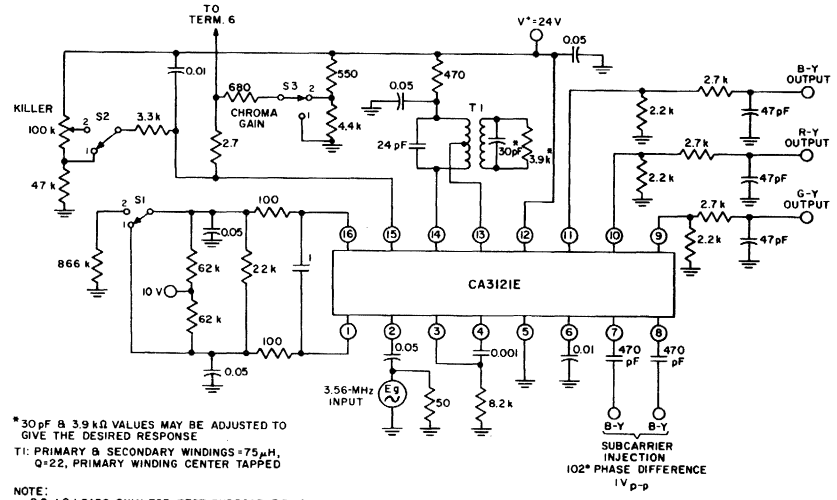


Fig. 4 — Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3070.

92CL-22724



92CM-22732

Fig. 5 — Typical characteristics test circuit for the CA3121E.

CA3123E

AM Radio Receiver Subsystem

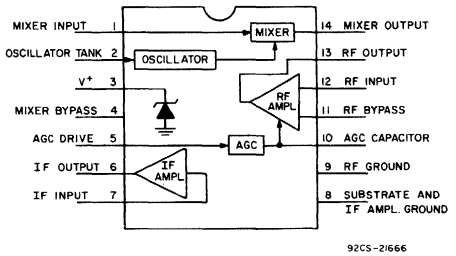
Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

Features:

- Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components
- Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils
- Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing
- Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor
- Integral regulation with built-in surge protection
- Separately accessible amplifiers



Terminal assignment diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- At Terminal No. 3 (V^+) ..... 9 V
- At Terminal No. 6 (IF Output) ..... 40 V
- At Terminal No. 13 (RF Output) ..... 20 V
- At Terminal No. 14 (Mixer Output) ... 20 V

DC CURRENT:
- Into Terminal No. 3 (V^+) ..... 35 mA

DEVICE DISSIPATION:
- Up to T_A = 55°C ..... 750 mW
- Above T_A = 55°C ..... derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... −55 to +125°C
- Storage ..... −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1,V_4			4.7		V
At Terminals 2, 3, 14	V_2,V_3,V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8,V_9			0		V
At Terminals 10, 11	V_{10},V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	I_1,I_4,I_5,I_7, I_8,I_9,I_{10},I_{11},I_{12}			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be ≤ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance Input pF	Parallel Capacitance Output pF	Parallel Resistance Input Ω	Parallel Resistance Output Ω	Transconductance μmhos
RF Amplifier	80	6	750	2 x 10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2 x 10^6 min.	2500 (Mixer) 3000 (Amplifier)

TYPICAL CHARACTERISTICS

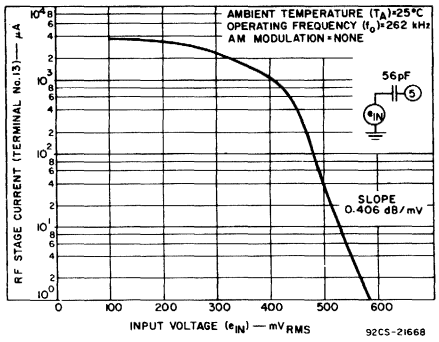


Fig. 1 — Control of RF stage by signal into Terminal No.5.

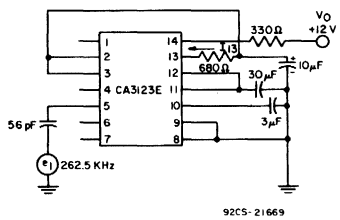
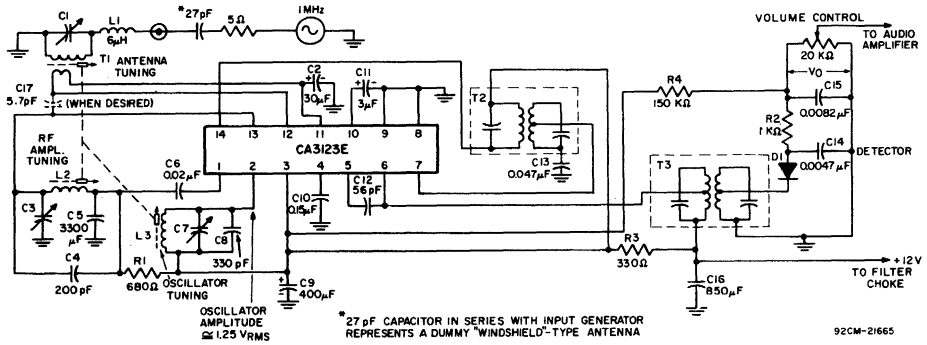


Fig. 2– Test circuit for Fig. 1.

CA3123E



Transformer	Symbol	Frequency	Inductance μh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF: Primary	T_2	262 kHz	2840	130	60	none	critical ≈0.017 ≈1/Q
Secondary			2840	130	60	or 30:1 31:1	
Second IF: Primary	T_3	262 kHz	2840	130	60	8.5:1	–
Secondary			2840	130	60	8.5:1	critical ≈0.017 ≈1/Q
Antenna: Primary	T_1	1 MHz	195	(C_1)–130	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be wound around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

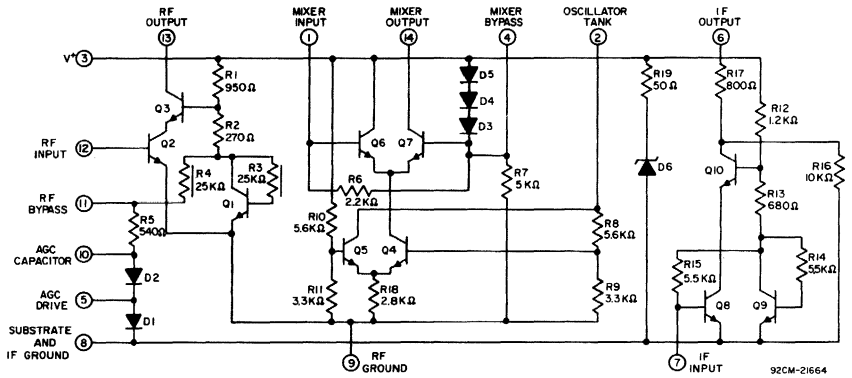


Fig. 4 – Schematic diagram of CA3123E.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3

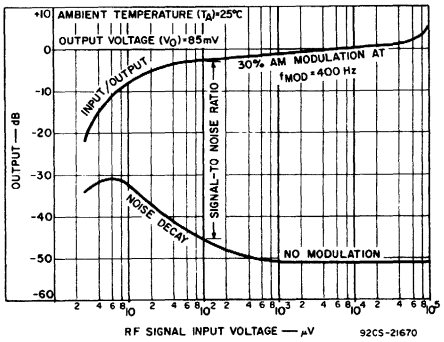


Fig.5 – Signal-to-noise performance.

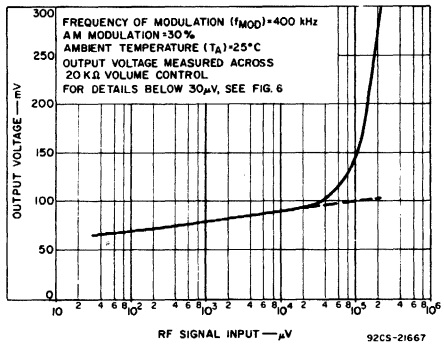


Fig.6 – AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig.3).

Change in slope in the vicinity of 40000 μV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig.3. The dotted curve indicates expected performance if C_{17} = 0.

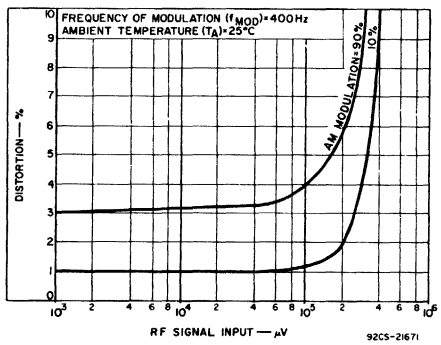


Fig.7 – Overload response.

CA3125E

Television Chroma Demodulator

RCA-CA3125E is a monolithic silicon integrated-circuit chroma demodulator having three separate demodulators with independent phase control. It is designed to function compatibly with the CA1398E IC Chroma Processor as well as other commercially available Chroma Processors in R-G-B Systems of color-TV receivers. The CA3125E is supplied in a 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

SUPPLY VOLTAGE	25 V
SUPPLY CURRENT	20 mA
AMBIENT-TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

Features:

- **Luminance input**
- **Blanking control input**
- **Three separate demodulators with independent phase control**
- **Low output offset voltage** ..... **0.4 V**

TYPICAL STATIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ VOLTS

SUPPLY CURRENT	9.6 mA
BRIGHTNESS CONTROL VOLTAGE:	
Measured with 8 volts at Terminals 11, 12, and 13	1.4 V
MAX. OUTPUT DIFFERENCE VOLTAGE:	
Measured between any two of Terminals 11, 12, and 13	±0.4 V
MAXIMUM DC DETECTOR UNBALANCE VOLTAGE:	
DC voltage shift on Terminals 11, 12, and 13 when Terminals 1, 2, and 3 are alternately biased 0.5 volt positive, then negative with reference to Terminal 14	+150 mV

TYPICAL DYNAMIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ volts

BLUE CHROMA GAIN:	
Peak-to-peak voltage at Terminal 11 with 1.0 volt peak-to-peak applied differentially between Terminals 6 and 7, and with a subcarrier injection voltage of 1 volt peak-to-peak	7.36 Vp-p
RED GAIN RATIO:	
$\frac{\text{Peak-to-peak voltage at Terminal 13}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	100%
GREEN GAIN RATIO:	
$\frac{\text{Peak-to-peak voltage at Terminal 12}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	30%
LUMINANCE GAIN:	
Peak-to-peak voltage measured at Terminals 11, 12, and 13, with a peak-to-peak voltage of 0.1 volt applied to Terminals 6 and 7 (common mode), and with no subcarrier injection	0.7 Vp-p

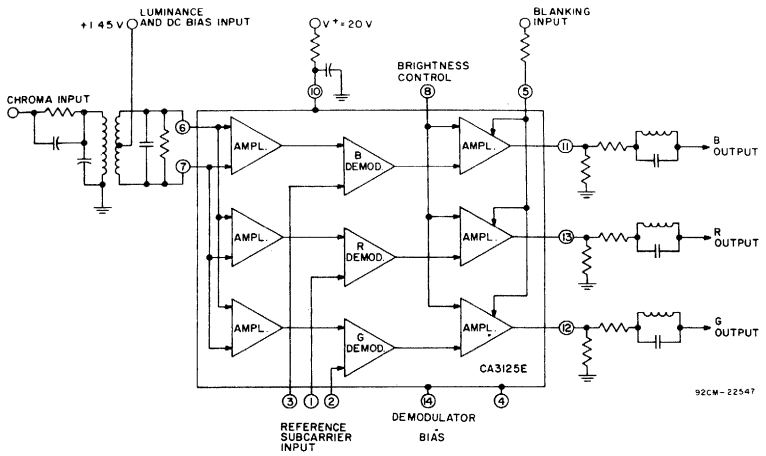


Fig. 1 – Functional block diagram of the CA3125E.

CA3126Q

TV Chroma Processor

RCA-CA3126Q is a monolithic silicon integrated circuit designed for chroma processing applications in color TV receivers. It is compatible with the CA3067 chroma demodulator as well as other chroma demodulators.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DEVICE DISSIPATION:
- Up to $T_A = 55^oC$ ..... 750 mW
- Above $T_A = 55^oC$ ..... derate linearly 7.9 mW/°C

DC SUPPLY VOLTAGE (Across Terms. 5 and 12)▲ ..... 13.2 V

DC CURRENT:
- Into Term. 12 ..... 38 mA
- Into Term. 14 ..... 20 mA

DC VOLTAGE (Terminal 9):
- Negative Rating ..... −5 V
- Positive Rating ..... 3 V

AMBIENT TEMPERATURE RANGE:
- Operating ..... −40 to +85°C
- Storage ..... −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At a distance not less than 1/32 in. (0.79 mm) from case for 10 seconds max. ..... +265°C

▲This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25^oC$, chroma control at maximum position for all characteristics tests except for chroma output test. For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Fig.2.

CHARACTERISTIC	TERMINAL, MEASUREMENT, AND SYMBOL	SWITCH POS.		CHROMA INPUT	LIMITS			UNITS
		S1	S2	TP1	Min.	Typ.	Max.	
Static Characteristics								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
Dynamic Characteristics (See Note 1)								
Pull-in Range*	V_8	*	2	0.5 V_{p-p}	±250	–	–	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	–	V_{p-p}
100% Chroma Output	V_{15}	1	2	0.5 V_{p-p}	1.4	2.7	–	V_{p-p}
Overload Detector	V_{15}	1	1	0.5 V_{p-p}	0.4	–	0.7	V_{p-p}
Minimum Chroma Output	V_{15}	1	2	0.5 V_{p-p}	–	–	20	mV_{p-p}
200% Chroma Output	V_{15}	1	2	1 V_{p-p}	70	100	140	% of 100% reading
20% Chroma Output	V_{15}	1	2	0.1 V_{p-p}	40	–	105	
Kill Level	V_{TP1}	1	2	vary	5	–	60	mV_{p-p}

Note 1: Except for pull-in range testing, tune oscillator trimmer capacitor for free-running frequency of 3.579545 MHz ± 10 Hz.
*Set Switch 1 to Position 2, detune oscillator ± 250 Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

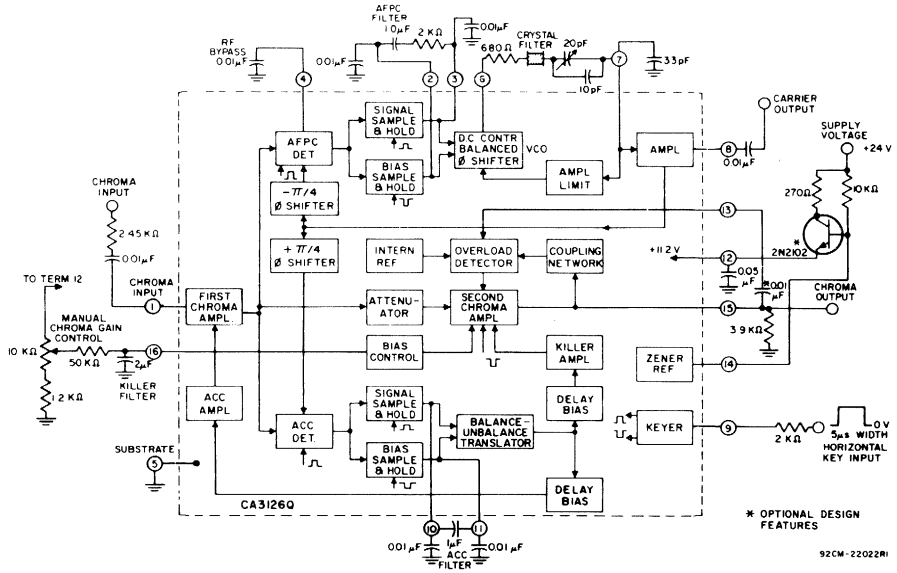


Fig. 1—Block diagram of CA3126Q TV Chroma Processor.

Features:

- **Phase-locked subcarrier regeneration utilizes sample-and-hold techniques**
- **Automatic chrominance control (ACC)/killer detector employs sample-and-hold techniques**
- **Supplementary ACC with an overload detector to prevent oversaturation of the picture tube**
- **Sinusoidal subcarrier output**
- **Keyed chroma output**
- **Emitter-follower buffered outputs for low output impedance**
- **Linear dc saturation control**
- **Internal zener-regulated reference potentials**
- **Only the initial crystal filter tuning is required. . . no killer or ACC adjustments required at any time**
- **Few external components required**
- **Compensation for temperature and supply variations**
- **All terminals protected against short circuits**

CIRCUIT DESCRIPTION

The following paragraphs briefly describe the circuit operation of the CA3126Q (shown in Fig. 1). A detailed description of the operation of various portions of the CA3126Q is given in ICAN-6247, "Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450-ohm resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase-shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45- and −45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

APPLICATIONS INFORMATION

General Considerations

The block diagram shown in Fig. 1 is typical of the type of circuit used in the practical application of the CA3126Q. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450 ohms (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.

CA3126Q

2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126Q is shown in Fig. 3.

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 4. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

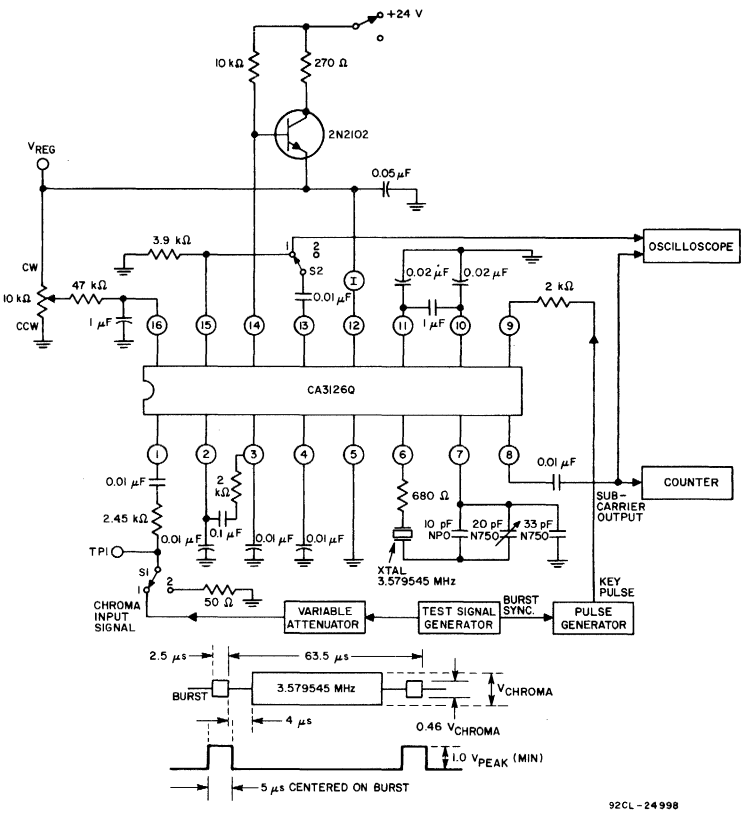


Fig. 2–Test circuit for CA3126Q.

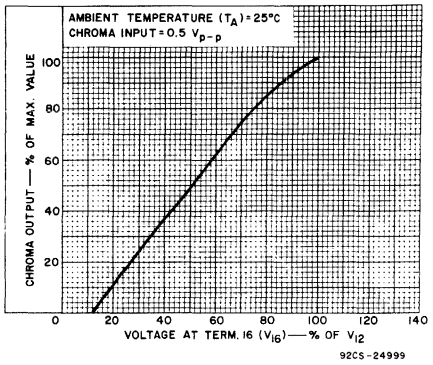


Fig. 3 –Chroma gain control.

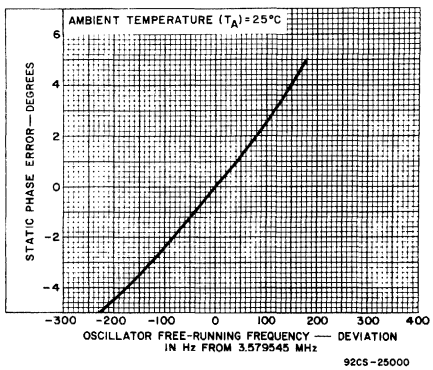


Fig. 4–Static phase error.

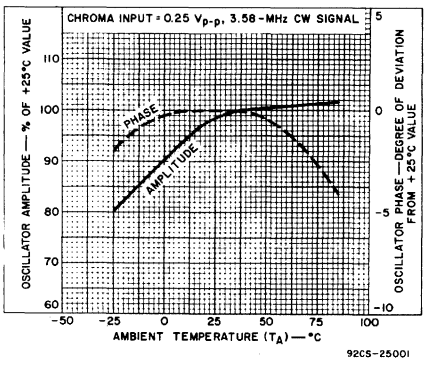


Fig. 5–Amplitude and phase variations of oscillator output vs. temperature.

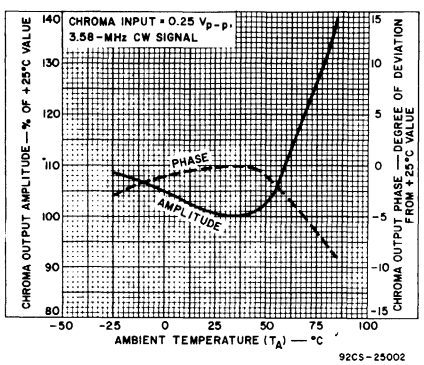


Fig. 6–Amplitude and phase variations of chroma output vs. temperature.

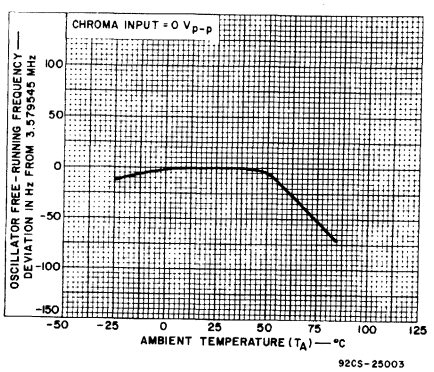


Fig. 7–Variation of oscillator free-running frequency vs. temperature.

Thermal Considerations

The circuit of the CA3126Q is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 5 and 6 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively.

Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 7. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 2.

CA3127E

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Gain-Bandwidth Product (f_T) > 1 GHz
- Power Gain = 30 dB (typ.) at 100 MHz
- Noise Figure = 3.5 dB (typ.) at 100 MHz
- Five independent transistors on a common substrate

Applications:

- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/mixer/oscillator
- IF Converter
- IF amplifiers
- Sense amplifiers
- Synthesizers
- Synchronous detectors
- Cascade amplifiers

RCA-CA3127E consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125°C.

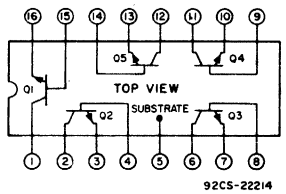


Fig. 1 – Schematic diagram of CA3127E.

MAXIMUM RATINGS, *Absolute-Maximum Values, at T_A = 25°C*

POWER DISSIPATION, P_D:
- Any one transistor ..... 85 mW
- Total Package:
- For T_A up to 75°C ..... 425 mW
- For T_A > 75°C Derate Linearly at ..... 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... −55 to +125°C
- Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the device.

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V

Collector-to-Base Voltage, V_{CBO} ..... 20 V

Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V

Collector Current, I_C ..... 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

CHARACTERISTICS CURVES
COMMON-EMITTER CONFIGURATION

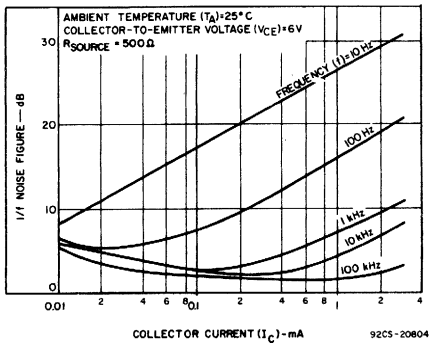


Fig. 2 – 1/f noise figure vs. collector current at R_{SOURCE} = 500 Ω.

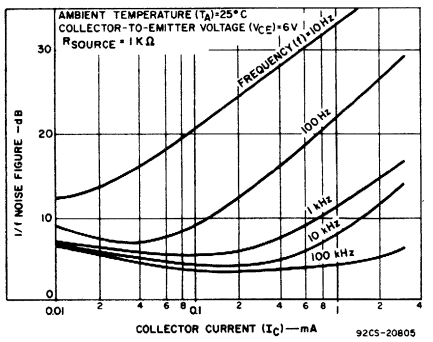


Fig. 3 – 1/f noise figure vs.collector current at R_{SOURCE} = 1 kΩ.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1} = 10 μA, I_B = 0, I_E = 0		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		4	5.7	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	0.5	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	40	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 6 V	I_C = 5 mA	35	88	–	
			I_C = 1 mA	40	90	–	
			I_C = 0.1 mA	35	85	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V	I_C = 5 mA	0.71	0.81	0.91	V
			I_C = 1 mA	0.66	0.76	0.86	
			I_C = 0.1 mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 mA, I_B = 1 mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	$\lvert\Delta V_{BE}\rvert$	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$\lvert\Delta I_B\rvert$	V_{CE} = 6V, I_C = 1 mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitive or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
I/F Noise Figure	NF	f = 100 kHz, R_S = 500 Ω, I_C = 4 mA	2	–	1.8	–	dB
Gain-Bandwidth Product	f_T	V_{CE} = 6 V, I_C = 5 mA	4	–	1.15	–	GHz
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 6 V, f = 1 MHz	5	–	See	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 6 V, f = 1 MHz	5	–	Fig.	–	pF
Emitter-to-Base Capacitance	C_{EB}	V_{BE} = 4 V, f = 1 MHz	5	–	5	–	pF
Voltage Gain	A	V_{CE} = 6 V, f = 10 MHz, R_L = 1 KΩ, I_C = 1 mA	6, 18	–	28	–	dB
Power Gain	G_p	Cascode Configuration f = 100 MHz, V^+ = 12 V	19, 20	27	30	–	dB
Noise Figure	NF	I_C = 1 mA	19, 20	–	3.5	–	dB
Input Resistance	$1/g_{11}$	Common-Emitter	10	–	400	–	Ω
Output Resistance	$1/g_{22}$	Configuration	12	–	4.6	–	kΩ
Input Capacitance	C_{11}	V_{CE} = 6 V	10	–	3.7	–	pF
Output Capacitance	C_{22}	I_C = 1 mA	12	–	2	–	pF
Magnitude of Forward Transadmittance	$\lvert Y_{21}\rvert$	f = 200 MHz	14, 15	–	24	–	mmho

CA3127E

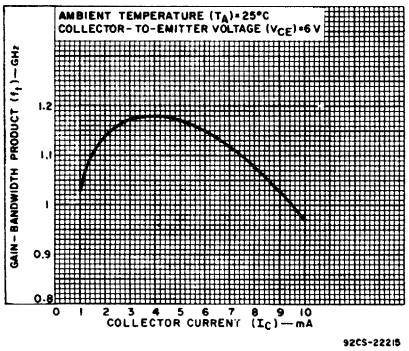


Fig. 4 – Gain-bandwidth product vs. collector current.

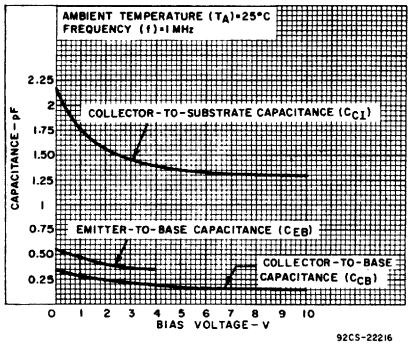


Fig. 5(a) – Capacitance vs. bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 5(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

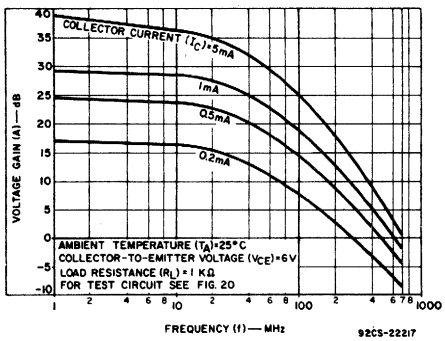


Fig. 6 – Voltage gain vs. frequency at R_L = 1 kΩ.

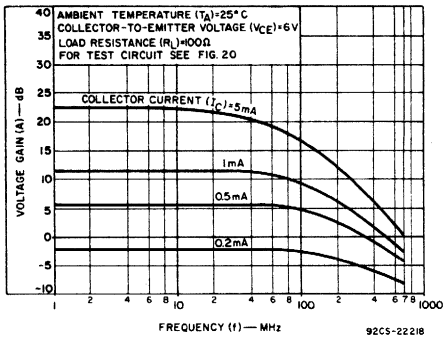


Fig. 7 – Voltage gain vs. frequency at R_L = 100 Ω.

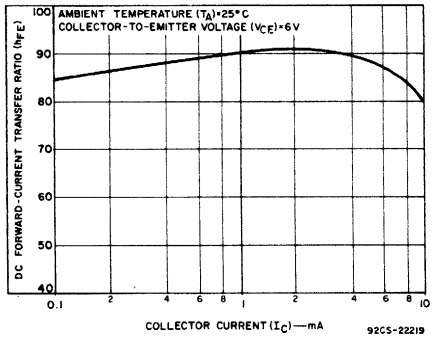


Fig. 8 – DC forward-current transfer ratio vs. collector current.

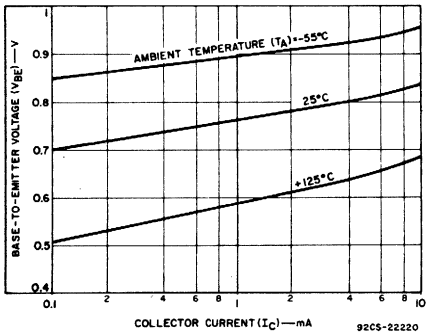


Fig. 9 – Base-to-emitter voltage vs. collector current.

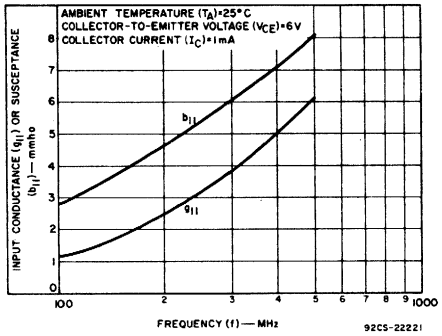


Fig. 10 – Input admittance (Y_{11}) vs. frequency.

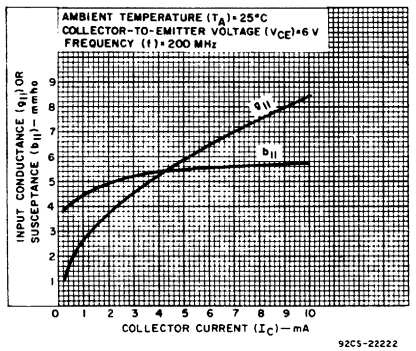


Fig. 11 – Input admittance (Y_{11}) vs. collector current.

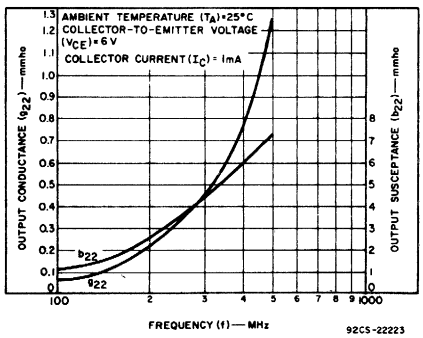


Fig. 12 – Output admittance (Y_{22}) vs. frequency.

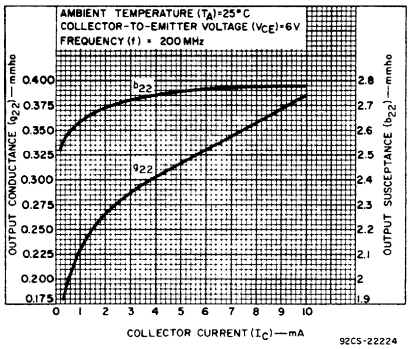


Fig. 13 – Output admittance (Y_{22}) vs. collector current.

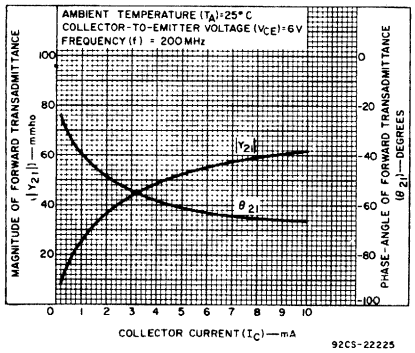


Fig. 14 – Forward transadmittance (Y_{21}) vs. collector current.

CA3127E

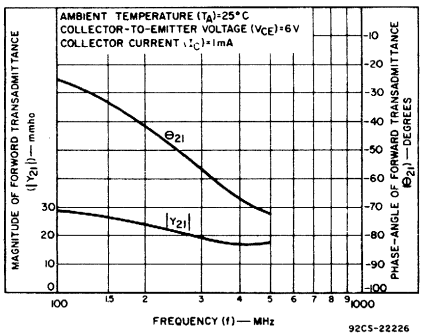


Fig. 15 – Forward transadmittance (Y_{21}) vs. frequency.

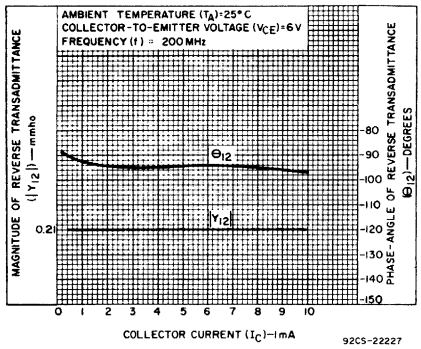


Fig. 16 – Reverse transadmittance (Y_{12}) vs. collector current.

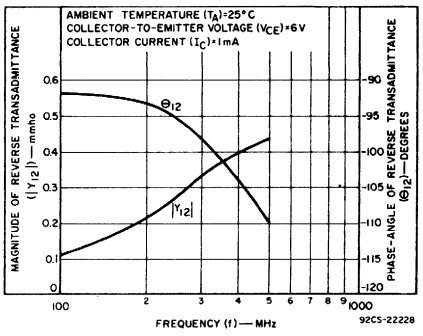


Fig. 17 – Reverse transadmittance (Y_{12}) vs. frequency.

TEST CIRCUITS

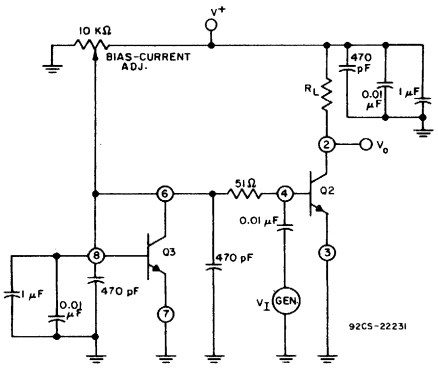
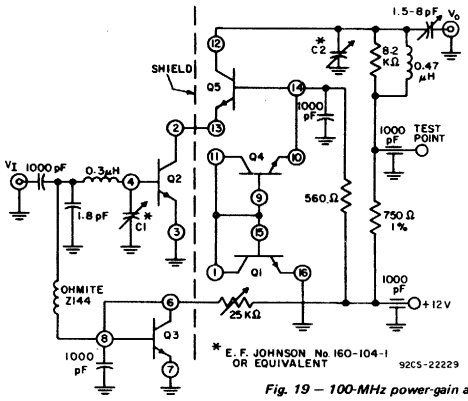


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveneietly represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

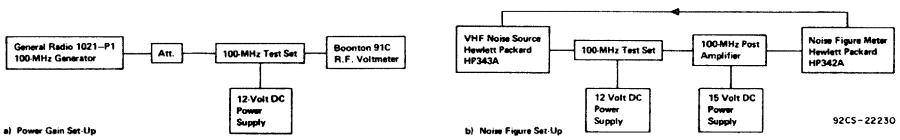


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

CA3128Q Preliminary Data

TV Chroma Processor for PAL Systems

The RCA-CA3128Q is a monolithic silicon integrated circuit designed primarily for PAL chroma processing applications in color TV receivers. For a circuit description of the CA3128Q and an explanation of this device in PAL systems, refer to "A New Chroma Processing IC Using Sample -and-Hold Techniques" by L. A. Harwood (ST6144).

Features:

- **Phase-locked subcarrier regeneration utilizes sample-and-hold techniques in the automatic frequency phase control (AFPC) servo loop**
- **Automatic chrominance control (ACC)/ killer detector employs sample-and-hold techniques**
- **Supplementary ACC with an overload detector to prevent oversaturation of the picture tube**
- **Sinusoidal subcarrier output**
- **Keyed chroma output**
- **Emitter-follower buffered outputs for low output impedance**
- **Linear dc saturation control**
- **PAL identification output**
- **Only the initial crystal filter tuning is required . . . no killer and ACC adjustments required at any time**
- **Few external components required**
- **Compensation for temperature and supply variations**
- **All terminals protected against short circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

DC SUPPLY VOLTAGE (Between Terms. 12 and 5)	13.2	V
DC VOLTAGE (Term. 9):		
Positive Value	+3	V
Negative Value	−5	V
DEVICE DISSIPATION:		
Up to $T_A = 55°C$	750	mW
Above $T_A = 55°C$	derate linearly at 7.9 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

TYPICAL STATIC CHARACTERISTICS at $T_A = 25°C$:

DC Supply Current (I_{12}) with $V_{12} = 11.2$ V dc	25	mA

TYPICAL DYNAMIC CHARACTERISTICS at $T_A = 25°C$ with a Burst-to-Chroma Ratio of 46.5%:

100% Chroma Output Voltage at $V_{I\,(p-p)} = 0.5$ V	3.5	Vp-p
Oscillator-Level Output Voltage	1	Vp-p
Killer Threshold Input Voltage	0.018	Vp-p
Pull-in Frequency	500	Hz
PAL Identification Output Voltage	1	Vp-p

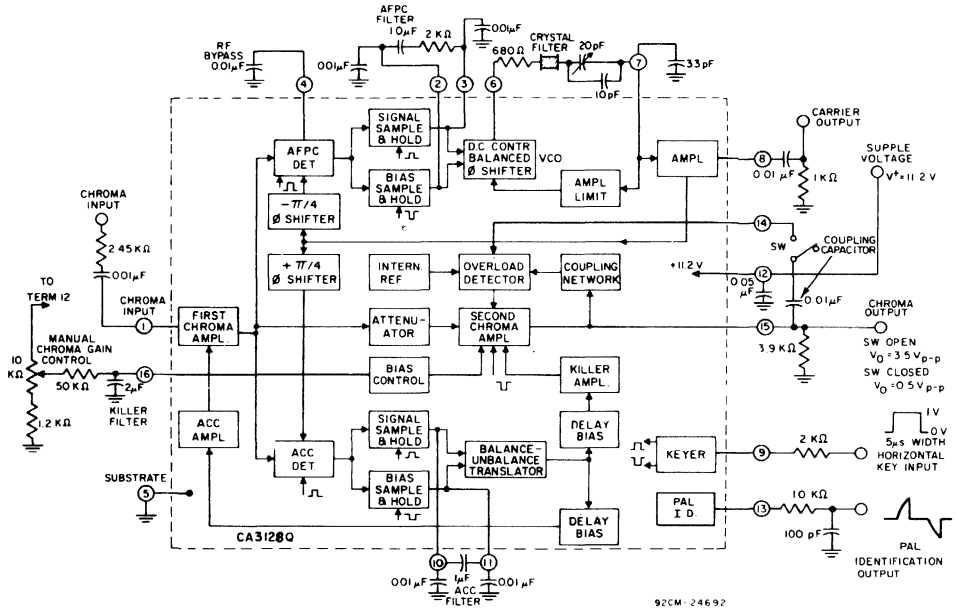


Fig. 1 – Block diagram of CA3128Q TV Chroma Processor.

CA3130, CA3130A, CA3130B Types
COS/MOS Operational Amplifiers

With MOS/FET Input

RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA-3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of −55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of −55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12} Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  2 pA typ. at 5 V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails

Ideal for single-supply applications

- Low V_{IO}: 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
  (ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers
  (e.g., follower for single-supply D/A converter)
- Voltage regulators
  (permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers

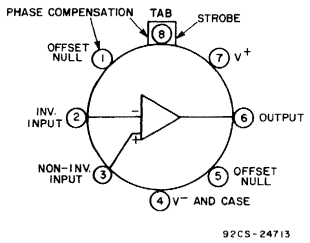


Fig. 1—Functional diagram of the CA3130 Series.

MAXIMUM RATINGS, *Absolute-Maximum Values*

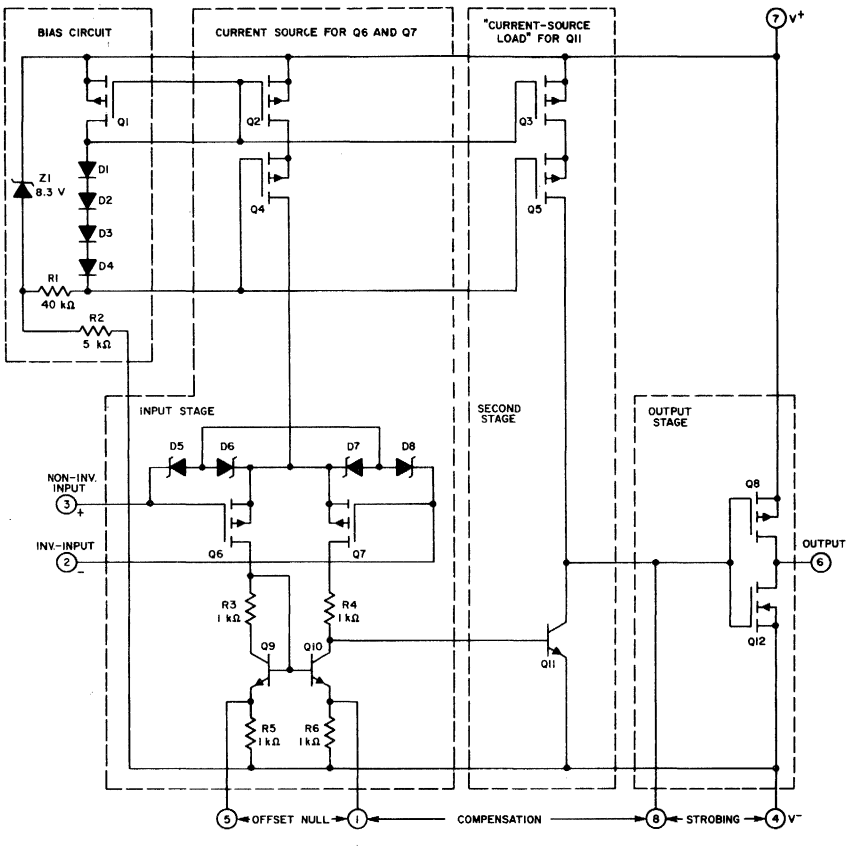
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	16 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	V^+ to (V^--0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
WITHOUT HEAT SINK–	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
WITH HEAT SINK–	
AT 125°C	418 mW
BELOW 125°C	Increase linearly at 16.7 mW/°C
TEMPERATURE RANGE:	
OPERATING	−55 to +125°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

*Short circuit may be applied to ground or to either supply.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

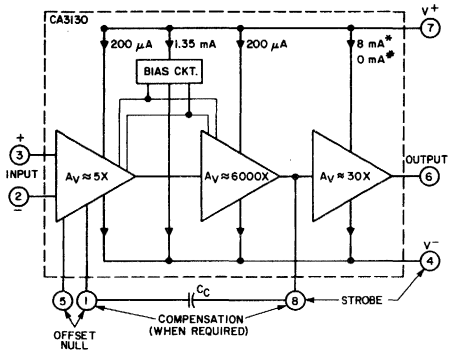
Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

92CL-24714

Fig. 2—Schematic diagram of the CA3130 Series.



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
*WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

92CS-24715

Fig. 3—Block diagram of the CA3130 Series.

CA3130, CA3130A, CA3130B Types

transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g. including static electricity during handling for Q6 and Q7.

Second Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

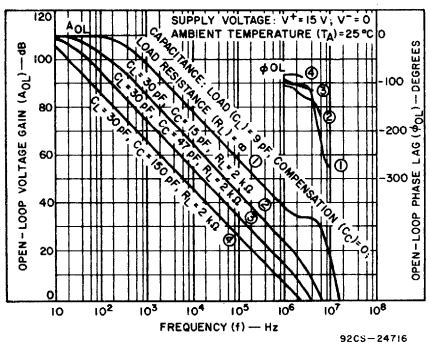


Fig. 4—Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q2 and Q3 are twice the size of Q1, the approximate 100-microampere current in Q1 establishes 200-microampere "mirrored" currents in Q2 and Q3 as constant-current sources for the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

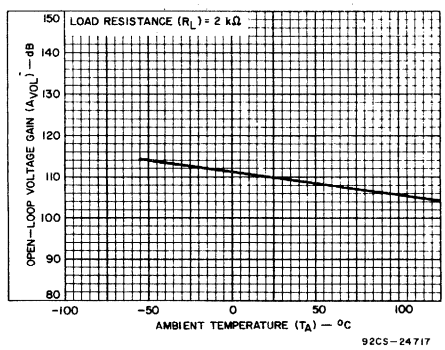


Fig. 5—Open-loop gain vs. temperature.

†For general information on the characteristics of COS/MOS transistor pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array."

ELECTRICAL CHARACTERISTICS — For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V^+=15 V, V^-=0 V, T_A=25°C (Unless Specified Otherwise)	CA3130B			CA3130A			CA3130			UNITS	FIG. NO.
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Offset Voltage	$\|V_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV	–
Input Offset Current	$\|I_{IO}\|$	$V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA	–
Input Current	I_I	$V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA	–
Large-Signal Voltage Gain	A_{OL}	V_O=10 V_{p-p}, R_L=2 kΩ	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V	4,5
			100	110	–	94	110	–	94	110	–	dB	
Common-Mode Rejection Ratio	CMRR		86	100	–	80	90	–	70	90	–	dB	–
Common-Mode Input-Voltage Range	V_{ICR}		0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V	–
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V	–
	$\Delta V_{IO}/\Delta V^-$		–	32	100	–	32	150	–	32	320		
Maximum Output Voltage	V_{OM}^+	R_L=2 kΩ	12	13.3	–	12	13.3	–	12	13.3	–	V	9
	V_{OM}^-		–	0.002	0.01	–	0.002	0.01	–	0.002	0.01		10
	$\|V_{OM}^+\|$	R_L=∞	14.99	15	–	14.99	15	–	14.99	15	–		9
	$\|V_{OM}^-\|$		–	0	0.01	–	0	0.01	–	0	0.01		10
Maximum Output Current: Source	I_{OM}^+	V_O=0 V	12	22	45	12	22	45	12	22	45	mA	9
Sink	I_{OM}^-	V_O=15 V	12	20	45	12	20	45	12	20	45		10
Supply Current	I^+	V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA	7,8
		V_O=0 V, R_L=∞	–	2	3	–	2	3	–	2	3		
Input Current	I_I	T_A=−55 to 125°C, $V^{\pm}$=±7.5 V▲, V_O=10 V_{p-p}*, R_L=2 kΩ*	–	Fig. 11	15	–	Fig. 11	–	–	Fig. 11	–	nA	–
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		–	5	15	–	10	–	–	10	–	μV/°C	–
Large-Signal Voltage Gain	A_{OL}		50 k	320 k	–	–	320 k	–	–	320 k	–	V/V	5
			94	110	–	–	110	–	–	110	–	dB	

* Applies only to A_{OL}.

▲ Applies only to I_I and $\Delta V_{IO}/\Delta T$.

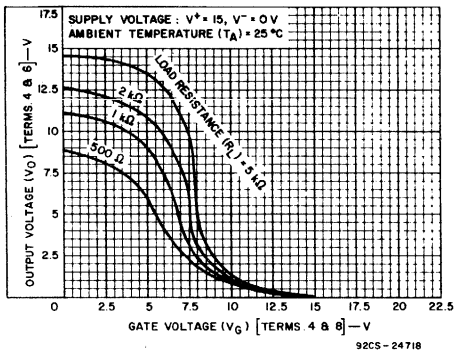


Fig. 6—Voltage transfer characteristics of COS/MOS output stage.

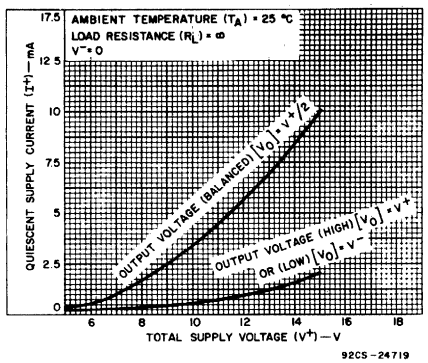


Fig. 7—Quiescent supply current vs. supply voltage.

CA3130, CA3130A, CA3130B Types

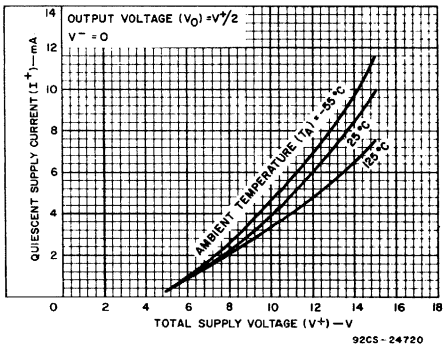


Fig. 8—Quiescent supply current vs. supply voltage at several temperatures.

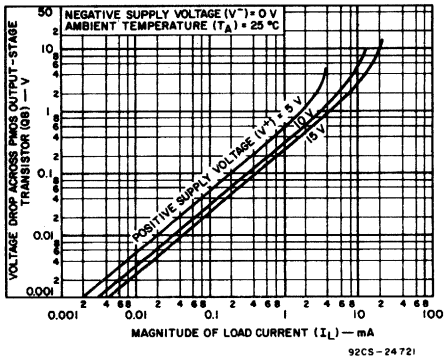


Fig. 9—Voltage across PMOS output transistor (Q8) vs. load current.

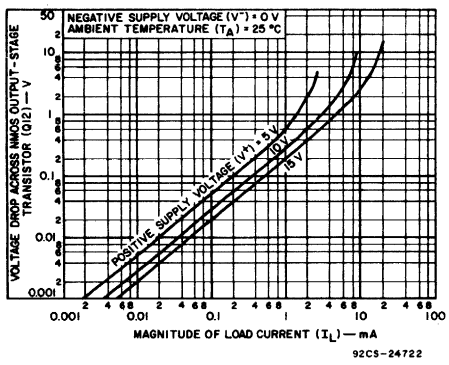


Fig. 10—Voltage across NMOS output transistor (Q12) vs. load current.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (V^+=+7.5 V, V^-=−7.5 V, T_A=25°C (Unless Specified Otherwise))	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	±22	mV	–
Input Resistance	R_I		1.5	1.5	1.5	TΩ	–
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	4.3	pF	–
Equivalent Input Noise	e_n	BW=0.2 MHz R_S=1 MΩ*	23	23	23	μV	14
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	15	MHz	4,15
		C_C = 47 pF	4	4	4		
Slew Rate: Open Loop	SR	C_C = 0	30	30	30	V/μs	–
Closed Loop		C_C = 56 pF	10	10	10		15
Transient Response: Rise Time	t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	0.09	μs	15
Overshoot			10	10	10	%	15
Settling Time (4 Vp-p Input to <0.1%)			1.2	1.2	1.2	μs	15

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for sources of R_S up to 10 MΩ.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS (V^+ = 5 V, V^- = 0 V, T_A = 25°C (Unless Specified Otherwise))	CA3130B	CA3130A	CA3130	UNITS	FIG. NO.
Input Offset Voltage	V_{IO}		1	2	8	mV	–
Input Offset Current	I_{IO}		0.1	0.1	0.1	pA	–
Input Current	I_I		2	2	2	pA	–
Common-Mode Rejection Ratio	CMRR		100	90	80	dB	–
Large-Signal Voltage Gain	A_{OL}	V_O = 4 Vp-p	100 k	100 k	100 k	V/V	–
		R_L = 5 kΩ	100	100	100	dB	–
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	0 to 2.8	V	–
Supply Current	I^+	V_O = 5 V, R_L = ∞	300	300	300	μA	7,8
		V_O=2.5 V, R_L = ∞	500	500	500		
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$		200	200	200	μV/V	–

HANDLING AND OPERATING CONSIDERATIONS

Handling Considerations

The CA3130 uses MOS field-effect transistors in the input circuit. Because MOS/FET's have extremely high input resistances, they are susceptible to damage when exposed to extremely high static electrical charges. To minimize the possibilities of damaging the input stage transistors, Q6 and Q7, the CA3130 utilizes a protective diode network in the input stage. Nevertheless, it is good practice that the following precautions be observed during handling, testing, and actual operation of the CA3130 devices to minimize exposure to damage-inducing hazards:

1. Soldering-iron tips, metal parts of fixtures, tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power ON because transient voltages may cause damage.
3. Signals should not be applied to the input (Terms. 2 and 3) when the device power supply is OFF. Input-terminal currents should not exceed 1 mA.
4. After CA3130 devices have been mounted on circuit boards, proper handling precautions should still be observed if the input terminals are unterminated. It is good practice during board-processing operations to return Terms. 2 and 3 to Term. 4 by jumping the appropriate conductors.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

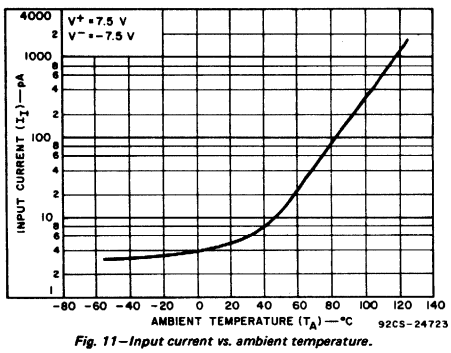


Fig. 11—Input current vs. ambient temperature.

CA3130, CA3130A, CA3130B Types

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig. 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices during life testing. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

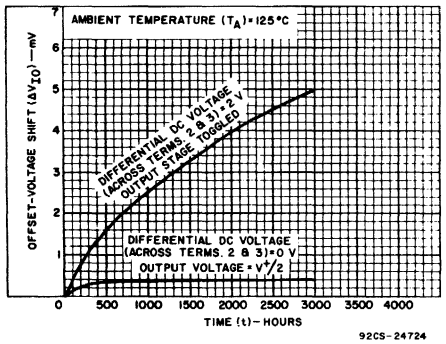


Fig. 12—Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single and dual-supply service. Figs. 13a and 13b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 13a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 13b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

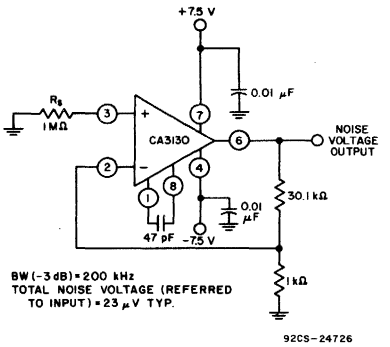
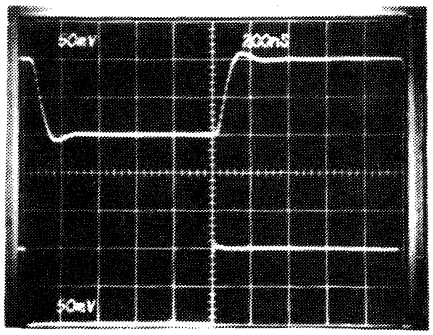
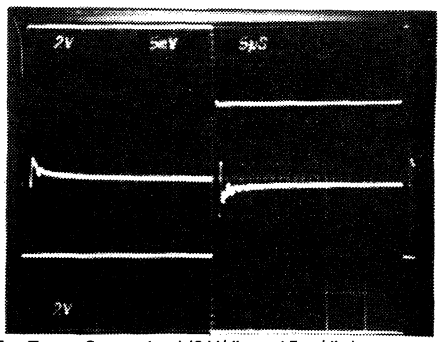


Fig. 14—Test-circuit amplifier (30-dB gain) used for wideband noise measurements.



Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

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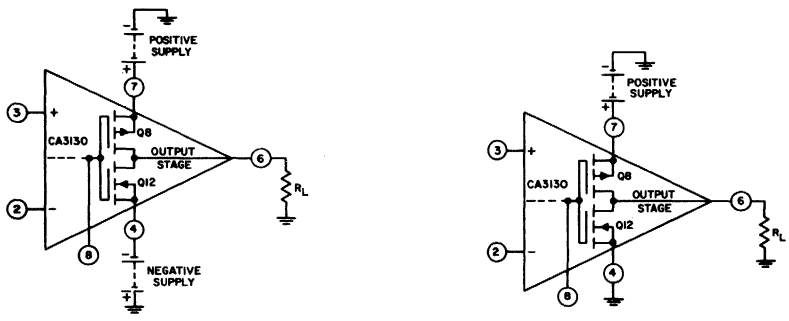


Fig. 13—CA3130 output stage in dual and single power-supply operation.

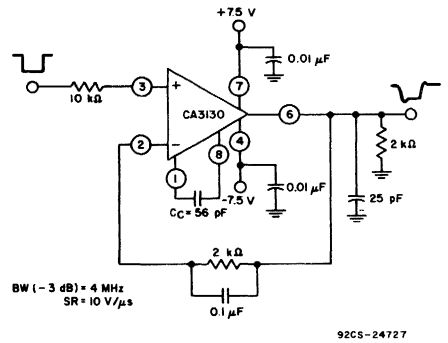


Fig. 15—Split-supply voltage follower with associated waveforms.

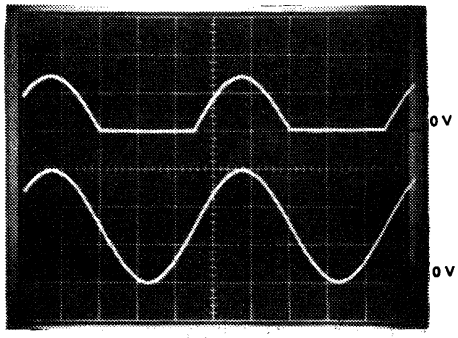
CA3130, CA3130A, CA3130B Types

TYPICAL APPLICATIONS

Voltage Followers

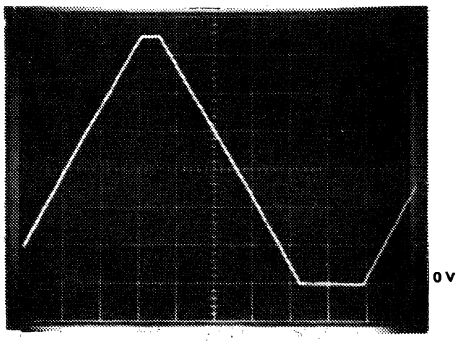
Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 16a with input-signal ramping. The waveforms in Fig. 16b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 16b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.



Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



(b) Output-waveform with ground-reference sine-wave input

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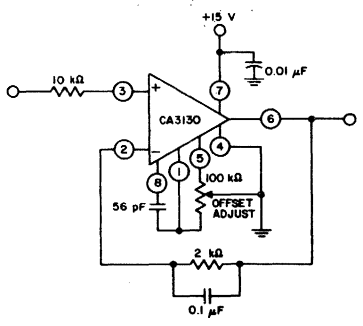

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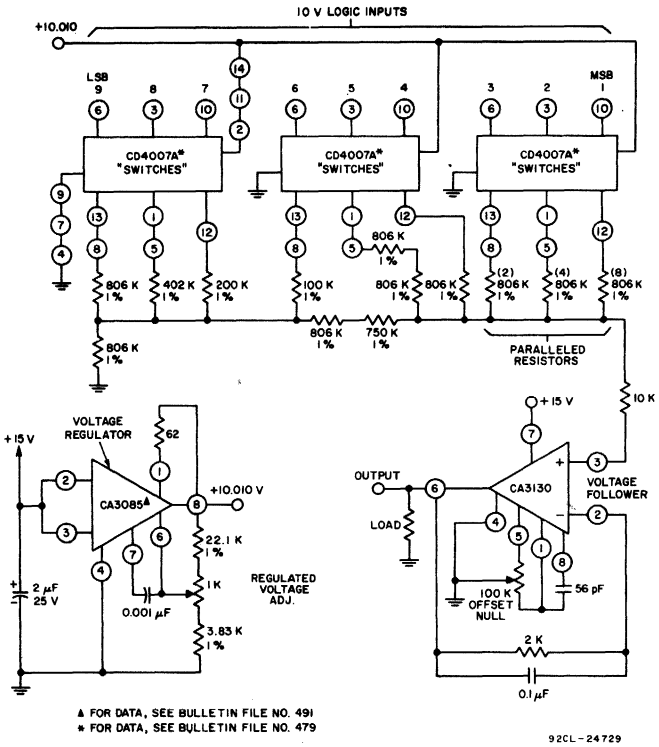
Fig. 16—Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

▲ FOR DATA, SEE BULLETIN FILE NO. 491
* FOR DATA, SEE BULLETIN FILE NO. 479

92CL-24729

Fig. 17—9-bit DAC using COS/MOS digital switches and CA3130.

9-BIT COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 17. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 17.

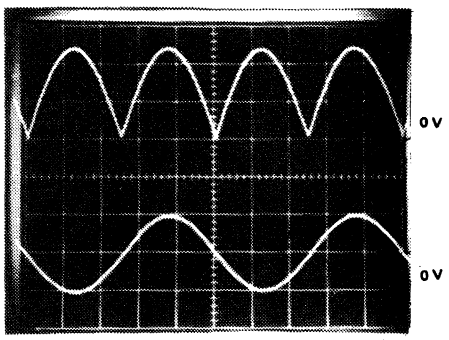
The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

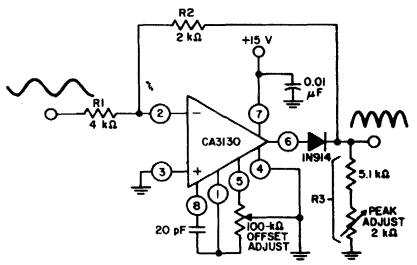
The absolute-value circuit using the CA3130 is shown in Fig. 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC," Application Note ICAN-6080.



Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

92CS-24738



$$\text{GAIN} = \frac{R2}{R1} \cdot X = \frac{R3}{R1+R2+R3}$$

$$R3 = R1\left(\frac{X+X^2}{1-X}\right)$$

FOR $X = 0.5$: $\frac{2\text{ k}\Omega}{4\text{ k}\Omega} = \frac{R2}{R1}$

$$R3 = 4\text{ k}\Omega\left(\frac{0.75}{0.5}\right) = 6\text{ k}\Omega$$

20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV

92CS-24730

Fig. 18—Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

CA3130, CA3130A, CA3130B Types

excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 18 is satisfied, the full-wave output is symmetrical.

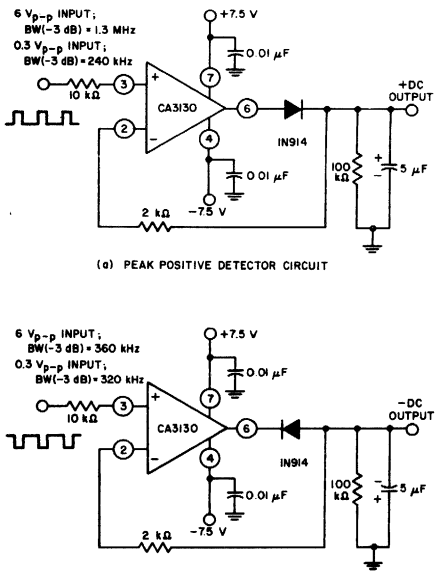


Fig. 19—Peak-detector circuits.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 20 shows the schematic diagram of a 40-mA power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

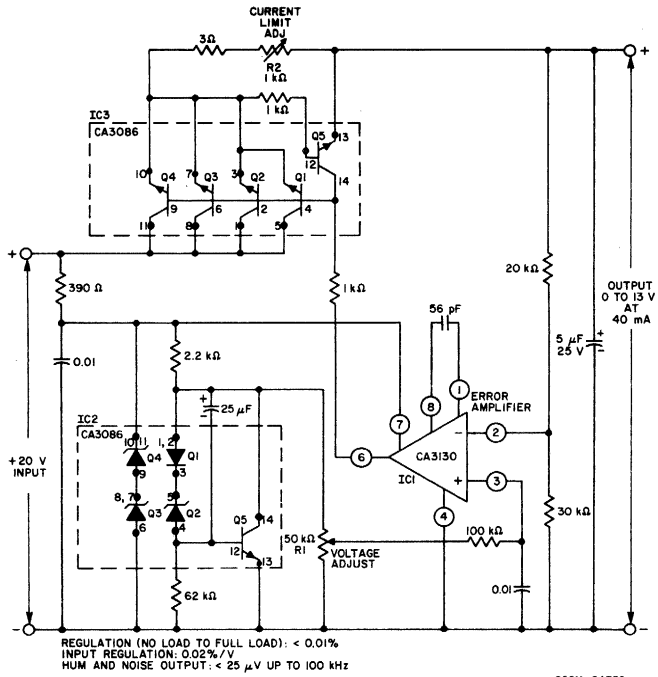


Fig. 20—Voltage regulator circuit (0 to 13 V at 40 mA).

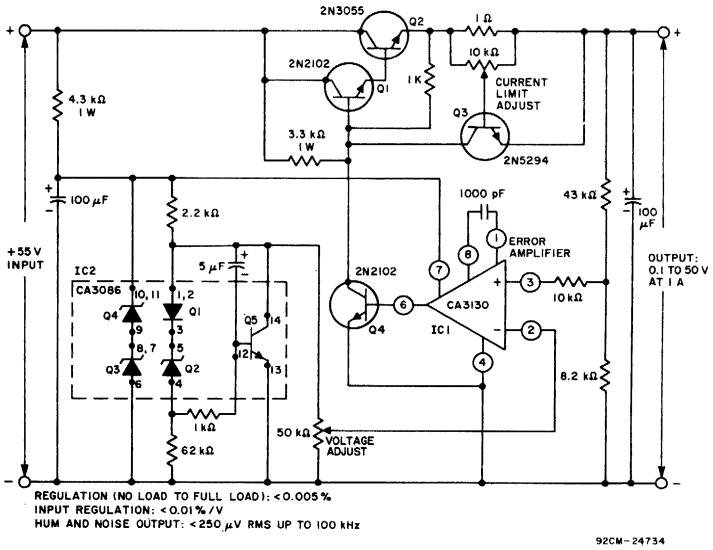


Fig. 21—Voltage regulator circuit (0.1 to 50 V at 1 A).

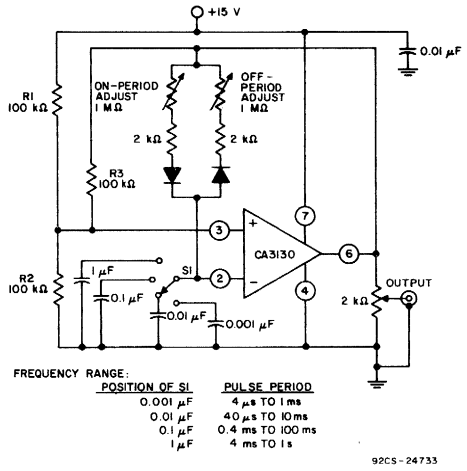


Fig. 22—Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

CA3130, CA3130A, CA3130B Types

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor.

Function Generator

Fig. 23 contains the schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 24, three COS/MOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15 V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5x.

The amplifier circuit in Fig. 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

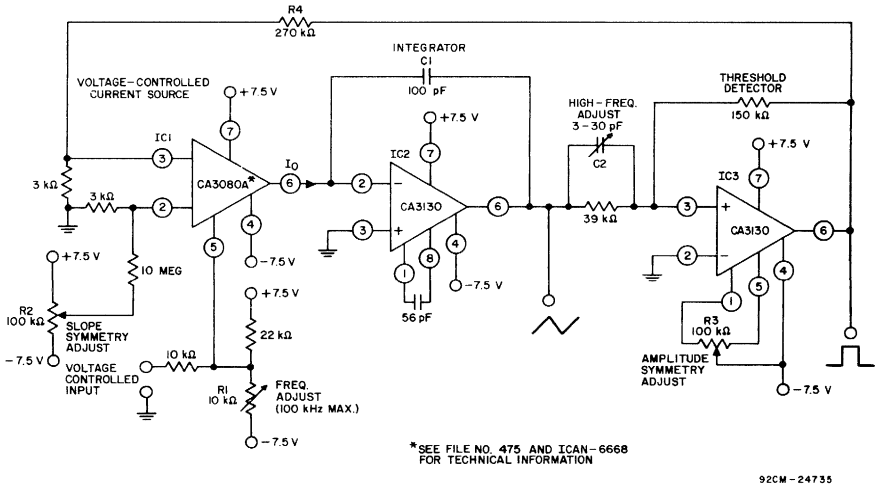


Fig. 23—Function generator (frequency can be varied 1,000,000/1 with a single control).

*See File No. 475 and ICAN-6668.

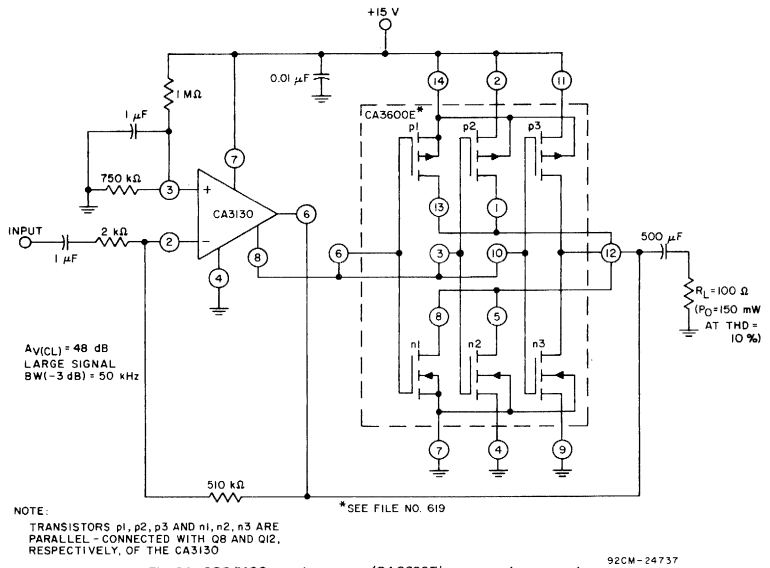


Fig. 24—COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

CA3131EM, CA3132EM Preliminary Data

5-Watt Audio Amplifiers

With Integral Heat Sink

RCA-CA3131EM and CA3132EM are audio amplifiers with integral preamplifier stages on single integrated-circuit monolithic chips.

Utilizing a uniquely designed package with an integral heat sink, these devices can provide a power-output signal in excess of five watts at an ambient temperature of 25°C.

The CA3131EM employs an internal feedback network that sets the over-all gain of the amplifier to typically 48 dB.

The CA3132EM omits the internal feedback network. This arrangement offers the circuit designer a wide latitude in the choice of an external feedback network more suitable to a specific application.

Both types are encapsulated in a 16-lead dual-in-line plastic package with 4 center leads removed.

The CA3131EM and CA3132EM are electrically equivalent to and pin compatible with types SN76013 and SN76023, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE, V^+	28 V
CONTINUOUS OUTPUT POWER, P_O (with R_L = 8 Ω and V^+ = 24 V)	8 W RMS
MINIMUM RECOMMENDED LOAD IMPEDANCE, R_L	8 Ω
AMBIENT OPERATING TEMPERATURE, T_A (at 6 W RMS Output Power)	70 °C
STORAGE TEMPERATURE RANGE	−55 to +150 °C

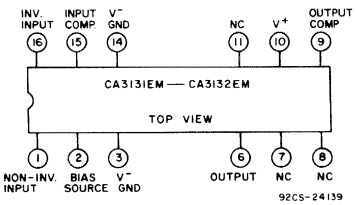


Fig. 1—Terminal assignment of the CA3131EM and CA3132EM.

Features:

- **Power Output: 4 W min., 5 W typ.**
- **Complete amplifier including: preamplifier stages, power-output amplifier, and integral heat sink**
- **High power-supply rejection ratio**
- **Operating voltage: V^+ = 24 V typ.**
- **Available with internal feedback (CA3131EM) or without feedback (CA3132EM)**

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V

Characteristic	Symbol	Conditions	Values Min.	Values Typ.	Unit
Input Impedance	Z_I		200k	–	Ω
Power Output	P_O	At clipping onset			
		R_L = 8 Ω	4	–	W
		R_L = 16 Ω	3	–	W
Closed-Loop Gain – CA3131EM	A	f = 1 kHz	46	48	dB
Supply Current	I^+	Zero signal	–	10	mA
Total Harmonic Distortion	THD	P_O = 50 mW–4 W, R_L = 8 Ω	–	1	%
		P_O = 50 mW–3 W, R_L = 15 Ω	–	1	%
Noise Voltage	V_n	f=20 Hz–20 kHz	–	1.5	mV RMS

Determining External Component Values (Refer to Figs. 2 & 3)

The dc quiescent output voltage is set by the voltage at Terminal 1. This voltage, in turn, is set by the internal voltage at Terminal 2 less I_I (input current, fixed by $R_A + R_B$, for Q4). The voltage at Terminal 2 is set slightly above half the supply voltage to allow for the voltage drop across $R_A + R_B$. Filter R_BC3 attenuates any ac ripple injected from the supply line and prevents positive feedback to Terminal 1. The rejection of supply voltage is a direct function of the filter attenuation.

The input impedance of the audio amplifiers is a function of the closed-loop gain and the magnitude of the Q8 current. In practice the input impedance is well above 1 megohm. The input signal, applied through C2, sees an impedance equivalent to the resistance of R_A connected in parallel with the amplifier input impedance. Hence, the value of R_A in most cases is dominant in establishing the input signal impedance.

The value of C1 depends on the regulation of the power supply. It is possible for the amplifier to work with a value of C1 as low as 0.1 μF to attenuate high-frequency signals in the supply line. Ideally, C1 should be placed as near Terminal 10 as possible. An electrolytic capacitor should be used for C1 if the power supply is poorly regulated to avoid ripple at the output.

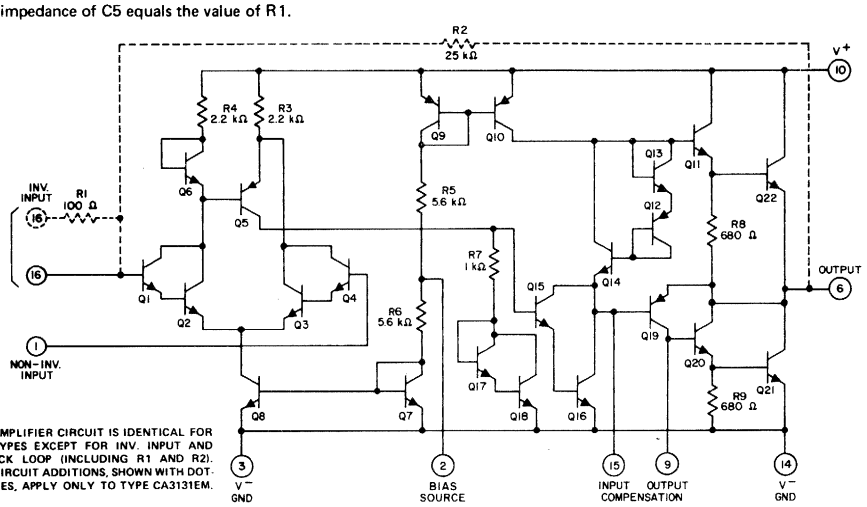
Capacitor C6 at Terminal 15 provides over-all compensation. If a 1000-pF capacitor is used for C6, then the first breakpoint for a 46-dB closed-loop gain occurs at 200 kHz. Higher capacitance values will cause the constant current from Q10 to charge C6 on the positive voltage swing and thus limit the slew rate at high-signal levels. Because p-n-p transistor Q19 has a lower gain-bandwidth product (f_T) than the n-p-n transistors, C7 is connected to Terminal 9 to compensate for gain losses occurring in the negative voltage swings.

The use of the filter networks C8 and R_D at the output Terminal 6 is a standard requirement for class B audio outputs driving reactive speaker loads. Capacitor C8 compensates for the speaker inductance and R_D limits the current surges through C8.

The value of the coupling capacitor C9 to the load determines the low-frequency response of the amplifier.

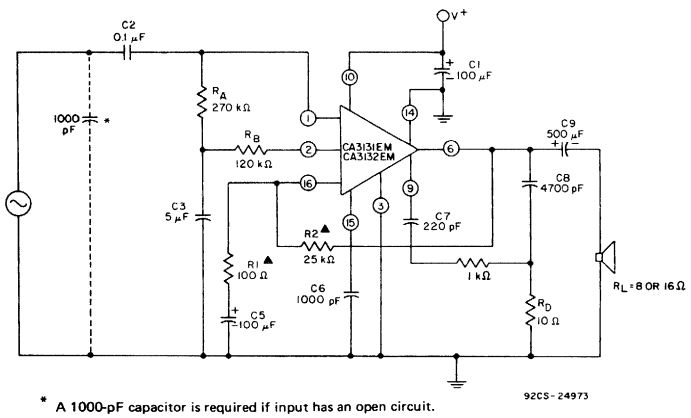
Closed-Loop Gain

The closed-loop gain for either type is set by the ratio (R1 + R2)/R1. These resistors are included in the CA3131EM circuit and are external when used with the CA3132EM. In either type, the low-frequency value (−3 dB point) is reached when the impedance of C5 equals the value of R1.



NOTE: AMPLIFIER CIRCUIT IS IDENTICAL FOR BOTH TYPES EXCEPT FOR INV. INPUT AND FEEDBACK LOOP (INCLUDING R1 AND R2). THESE CIRCUIT ADDITIONS, SHOWN WITH DOTTED LINES, APPLY ONLY TO TYPE CA3131EM.

Fig. 2—Schematic diagram of types CA3131EM and CA3132EM.



* A 1000-pF capacitor is required if input has an open circuit.

▲ External resistors R1 and R2 are used only with the CA3132EM. When testing the CA3131EM, omit R1 and R2 and connect the (+) termination of C5 to Terminal 16.

Fig. 3—Test circuit for types CA3131EM and CA3132EM.

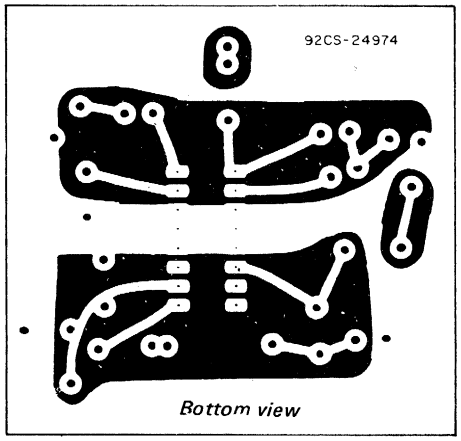


Fig. 4—Printed-circuit board (actual size) containing the test circuit, shown in Fig. 3, for the CA3131EM.

CA3134E, CA3134EM, CA3134QM Preliminary Data

TV Sound IF and Audio Output Subsystems

The RCA-CA3134E, CA3134EM, and CA3134QM combine the Sound IF and Audio Output Subsystems on a single monolithic integrated circuit to provide a Television Sound System. Each device includes a multistage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive an 8-, 16-, or 32-ohm speaker.

The CA3134E is encapsulated in a 16-lead plastic "power-stud" dual-in-line package.

This package arrangement lends itself to a wide variety of techniques for mounting heat sinks. The CA3134EM and CA3134QM are similar to the CA3134E except that they incorporate a tin-plated copper-strap heat sink. The CA3134QM also has quad formed leads and a shorter (side-length) heat sink. The heat sink provides a convenient means for directly mounting the CA3134EM or CA3134QM on a PC board and soldering the copper strap to the PC-board ground.

Features

- **Nominal power output: 3W**
- **Power amplifier with current limiting and thermal shutdown**
- **Wide power-supply range: 12 V to 33 V**
- **Low quiescent current: 30 mA typ.**
- **5-kHz deviation sensitivity: 1 W output typ.**
- **3-dB limiting sensitivity: 200 μV typ.**
- **Excellent AM rejection: 50 dB typ.**
- **Differential peak detector—requires one tuned coil**
- **Electronic volume control with improved taper**
- **Optional unattenuated audio output**
- **Optional power-supply ripple by-pass**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3134E	CA3134EM, CA3134QM	
DC SUPPLY VOLTAGE (Between Term. 1, V^+ and Terms. 4, audio-output ground and 13, substrate)	33	33	V
INPUT SIGNAL VOLTAGE (Between Terms. 14 and 15)	±3	±3	V
DEVICE DISSIPATION:			
With Infinite Heat Sink—			
Up to T_A = 70°C	6.5	–	W
Above T_A = 70°C ..... derate linearly	83.3	–	mW/°C
With no Heat Sink—			
Up to T_A = 25°C	1.4	–	W
Above T_A = 25°C.....derate linearly	11.1	–	mW/°C
With Copper-Strap Heat Sink—			
Soldered to PC Board			
Up to T_A = 25°C	–	3.9	W
Above T_A = 25°C ....derate linearly	–	31.2	mW/°C
Unsoldered			
Up to T_A = 25°C	–	2.5	W
Above T_A = 25°C ....derate linearly		20	mW/°C
THERMAL RESISTANCE			
Junction to Stud	12	12	°C/W
AMBIENT TEMPERATURE RANGE:			
Operating	–40 to +85		°C
Storage	–65 to +150		°C
LEAD TEMPERATURE (During Soldering):			
At a distance 1/16 in. ±1/32 in. (1.59 ±0.79 mm) from case for 10 seconds max.	+265		°C

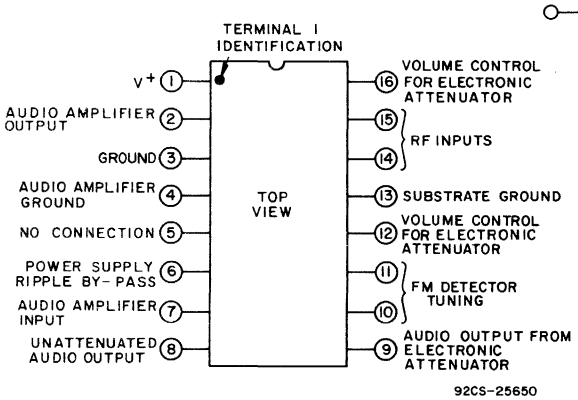


Fig. 1 – Terminal diagram of the CA3134E, CA3134EM, and CA3134QM.

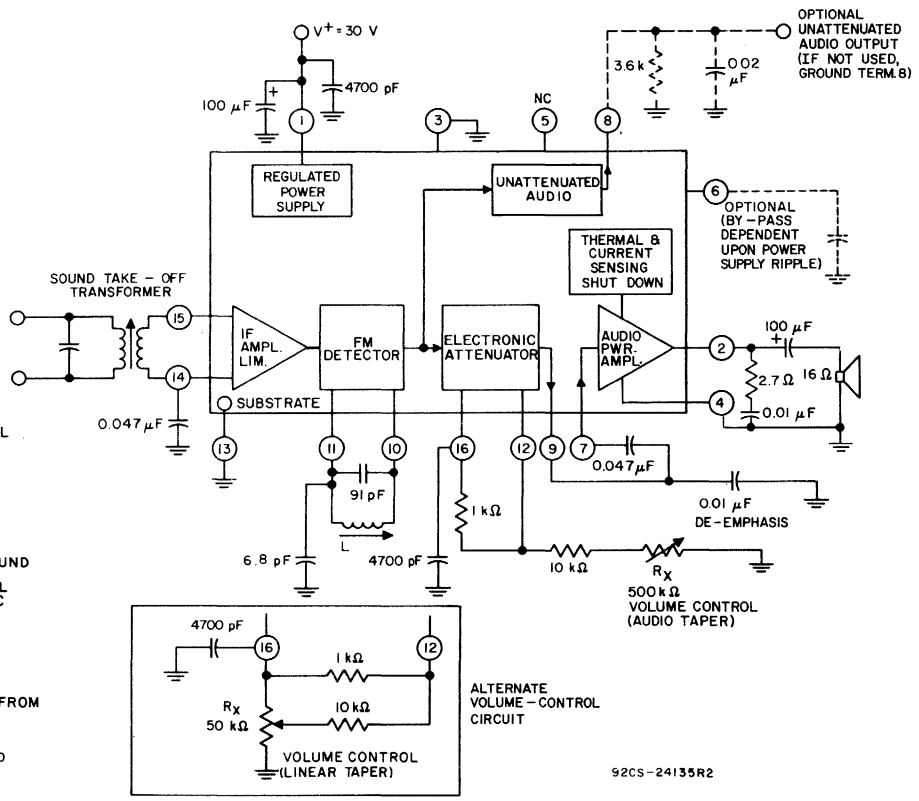


Fig. 2 – Block diagram of the CA3134 in a typical circuit application.

CA3134E, CA3134EM, CA3134QM

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V^+ = +30 V (applied to Term. 1), DC Volume Control, R_X = 500 kΩ, R_L = 16 Ω, unless otherwise indicated. Refer to Fig. 2.

CHARACTERISTIC	SPECIAL TEST CONDITIONS	NOMINAL VALUE	UNITS
Static Characteristics			
Current into Term. 1, I_1	P_O = 0	30	mA
Dynamic Characteristics			
IF AMPLIFIER: Input Limiting Voltage, V_{15}(lim) (at −3 dB point)	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ±25 kHz	200	μV
AM Rejection, AMR	f_O = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{15} = 20 mV	50	dB
DETECTOR: Recovered af Voltage (Term. 9), V_O(af)	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ±25 kHz, V_{15} = 100 mV	700	mV
Total Harmonic Distortion, (THD)		0.8	%
ATTENUATOR: Maximum Attenuation	R_X = 0	75■	dB
UNATTENUATED AUDIO: Recovered af Voltage (Term. 8), V_O(af)	Terminal 8 Load = 3.6 kΩ, f_O = 4.5 MHz, f_m = 400 Hz, Δf = ±25 kHz, V_{15} = 100 mV	600	mV
Total Harmonic Distortion (THD)		0.8	%
AUDIO POWER AMPLIFIER: Voltage Gain, A(af)	f = 1 kHz	35	dB
System Total Harmonic Distortion THD (System)	P_O = 1 W (I_T = 140 mA typ.) P_O = 2 W (I_T = 180 mA typ.)	1.5 1.6	% %
Power Output, P_O	THD (System) = 10% (I_T = 210 mA typ.)	3*	W
Input Resistance, (R_I(af)	f = 1 kHz	100	kΩ

* With suitable heat sink for the CA3134E.

■ The attenuation range can be increased by substituting lower-valued resistors for the 10-kΩ resistor in the volume-control circuit.

CA3137E

TV Chroma Demodulator

Preliminary Data

The RCA-CA3137E is a monolithic silicon integrated circuit that performs the demodulation, dynamic "flesh correction", tint control, and chroma gain-control functions. It is designed to function compatibly with the CA3126Q Chroma Processor, and is supplied in the 16-lead dual-in-line plastic package.

Features:

- Balanced chroma demodulators
- Color difference matrix (6500°K)
- DC tint control
- Three low-output-impedance drivers for direct coupling
- Reference subcarrier limiter
- Internal RF filtering
- DC chroma gain control
- Dynamic "flesh correction" — corrects purple and green flesh colors without affecting primary red, green, and blue colors
- Requires few external components
- No tuning adjustments are necessary

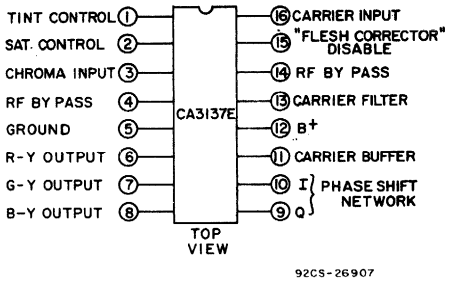


Fig.1 – CA3137E terminal assignment.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25°C$

DC SUPPLY VOLTAGE (between Terms. 5 and 12)	13.2 V
DEVICE DISSIPATION:	
Up to $T_A = 55°C$	750 mW
Above $T_A = 55°C$	derate linearly 7.9 mW/°C
AMBIENT-TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

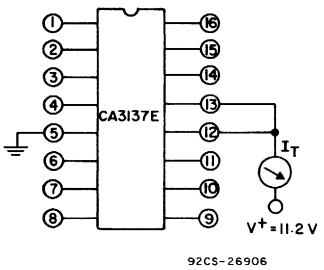


Fig.2 – DC test circuit.

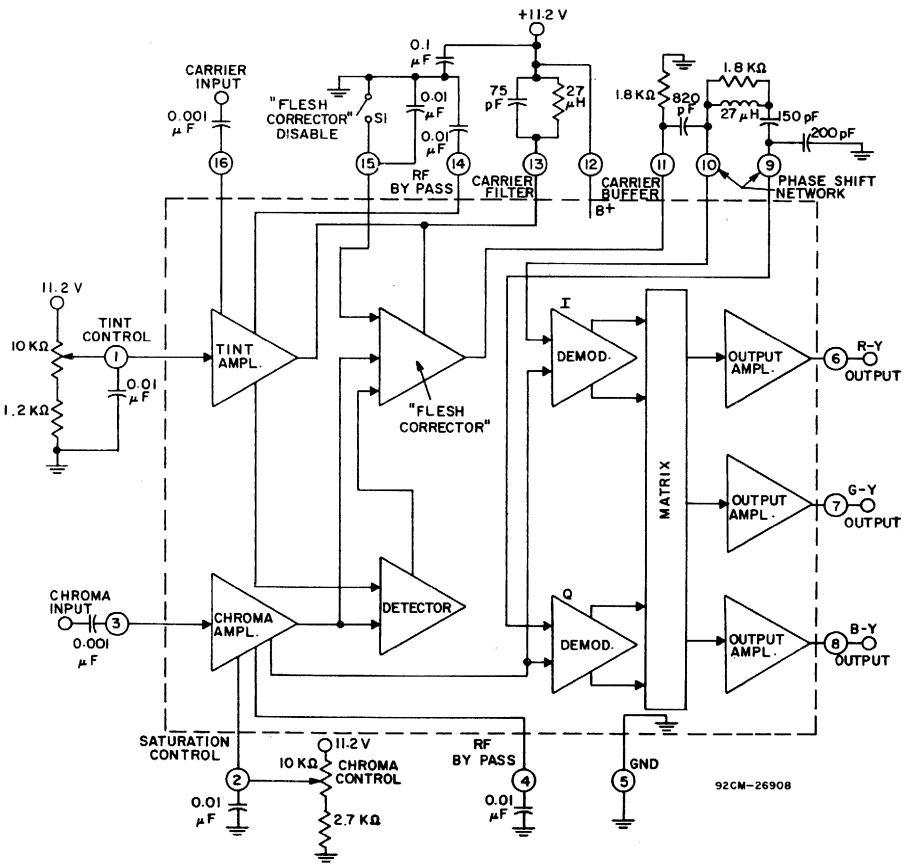


Fig.3 – Functional diagram and typical dynamic test circuit.

CA3137E

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 11.2$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYP. VALUE	UNITS
STATIC (See Fig.2)				
Supply Current	I_T		35	mA
Reference Subcarrier Input	V_{16}		6.7	VDC
Oscillator Reference Inputs	V_9, V_{10}		3.8	VDC
R-Y, G-Y, B-Y Outputs	V_6, V_7, V_8		5	VDC
Difference Outputs	$\triangle V_6, \triangle V_7, \triangle V_8$		±0.3	△VDC
Chroma Input	V_3		1.2	VDC
DYNAMIC (See Fig.3)				
Tint and Sensitivity Limiting	V_{11}	V_{16} = 200 mV p-p @ 3.58 MHz	300	mVp-p
Tint Limiting	V_{11}	V_{16} = 800 mV p-p @ 3.58 MHz	425	mVp-p
Tint Amplifier Phase Reference	ϕV_{11}	V_{16} = 400 mV p-p, Term.1 = 11.2 VDC	25	Degrees
Tint Amplifier Phase Shift	$\triangle\phi_{11}$	V_{16} = 800 mV p-p, Term.1 = 1.2 VDC	110	Degrees
Ratio G-Y to R-Y	V_7/V_6	V_{16} = 400 mV p-p,	33	%
Ratio B-Y to R-Y	V_8/V_6	V_3 = 40 mV p-p	120	%
Demodulated Chroma Output R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 40 mV p-p	550	mV p-p
Color Difference Output (Bandwidth at 3 dB)		V_3 = 40 mV p-p	900	kHz
Color Difference Output: R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 300 mVp-p	2.2	Vp-p
G-Y	V_7		0.7	
B-Y	V_8		2.65	
"Flesh Detector" Reference:		Set-Up: Term. 2 = 1.6 V Term. 1 = 11.2 V Term. 16 = 400 mV p-p @ 0° Reference Angle Term. 3 = 40 mV p-p @ 10° Reference Angle S_1 Closed (Term.15 at GND)	Ref. ↓	
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except S_1 open	0	Degrees
Amplitude	V_{11}		275	%
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except Term. 3 at 190°C	0	Degrees
Amplitude	V_{11}		100	%
Small-Signal Output Resistance (Terms.6,7,8)	r_o		50	Ω
Small-Signal Input Resistance: Term.3	r_i		3	kΩ
Terms. 9&10			2.5	

CA3139E, CA3139Q

TV Automatic Fine Tuning Circuit

With Intercarrier Mixer/Amplifier
For Color and Monochrome Receivers

Features:

- **Cascode-type high-gain amplifier (15-mV input for rated output)**
- **AFT differential peak detector**
- **Differential amplifier**
- **Bipolar outputs**
- **Five-stage intercarrier mixer/amplifier**
- **Internal voltage regulator**
- **For use in either color or monochrome receivers**

The RCA-CA3139 is a monolithic TV Automatic Fine Tuning (AFT) circuit that provides an AFT voltage and an amplified 4.5-MHz intercarrier sound signal. When connected to an output of an IF amplifier the CA3139 provides the signal processing (amplification and detection) necessary to generate the AFT correction signals required by the TV tuner. It also mixes the video and sound IF carriers and amplifies the resultant 4.5-MHz intercarrier sound signal. This sound output may then be connected to an FM detector such as the RCA-CA3134 "TV Sound IF and Audio Output Subsystem", or the RCA-CA3065 "FM Detector and Audio Driver".

The AFT portion of the CA3139 is similar to the RCA-CA3064 AFT circuit with the following exceptions: (a) the AFT filter capacitors are external and user selectable, allowing the detector to operate as a peak detector and resulting in a higher effective gain for the TV signal; (b) the detector bias resistor is external and user selectable, allowing the gain of the AFT and intercarrier signals to be adjusted; (c) the dynamic resistance of the shunt regulator has been decreased.

The CA3139 is supplied in a 14-lead dual-in-line plastic package (CA3139E) or a 14-lead plastic package with quad-formed leads (CA3139Q).

MAXIMUM RATINGS,

Absolute-Maximum Values:

DEVICE DISSIPATION:
Up to T_A = 25°C ..... 630 mW
Above T_A = 25°C. . . . .derate linearly 6.7 mW/°C
AMBIENT TEMPERATURE:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32"
(1.59 mm ± 0.79 mm)
from case for 10 s max. ..... 265°C

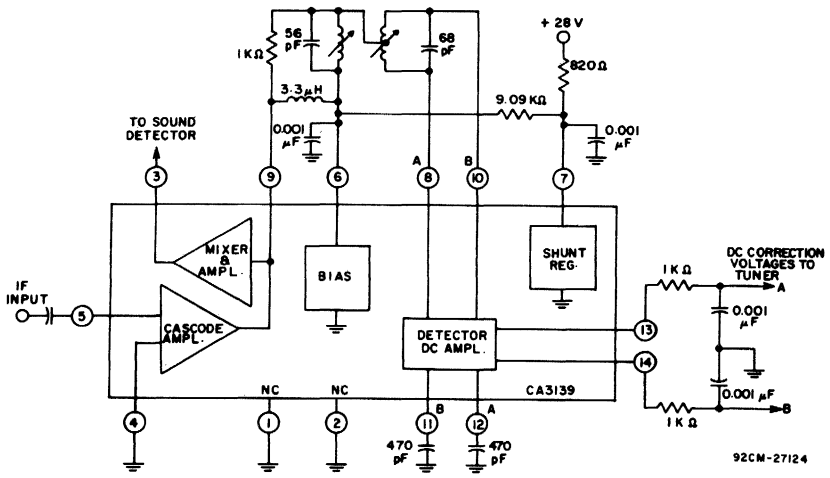


Fig. 1 – Block diagram and typical application of CA3139.

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 3 and horizontal terminal 12 is +8 to −1.5 volts.

Terminal No.	1,2♦	3	4■	5	6	7▲	8	9	10	11	12	13	14	MAXIMUM CURRENT RATINGS I_{IN}, I_{OUT} mA
1, 2♦	◄ NO INTERNAL CONNECTION ►													
3			+10 −0	+9 −1.5	+8 −1.5	+0 −10	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	+8 −1.5	10
4■				+0 −2	+0 −3	+0 −11	+0 −3	+0 −3	+0 −3	+0 −3	+0 −3	+0 −11	+0 −11	50
5					+0 −5	+0 −14	+2 −5	+1 −5	+2 −5	+2 −5	+2 −5	+1 −8	+1 −8	1
6						+0 −14	+2 −2	+0 −2	+2 −2	+1 −3	+1 −3	+0 −10	+0 −10	2
7▲							+15 −0	+13 −0	+15 −0	+13 −0	+13 −0	+10 −0	+10 −0	50
8								+1 −5	+5 −5	+5 −5	+1 −5	+0 −14	+0 −14	2
9									+10 −2	+8 −2	+8 −2	+0 −10	+0 −10	10
10										+1 −5	+5 −5	+1 −10	+1 −10	2
11											*	*	*	2
12												*	*	2
13													+14 −14	2
14														2

▲ Terminal number 7 may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor – provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♦ It is recommended that unused terminals 1 and 2 be grounded to act as shields.

CA3139E, CA3139Q

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V^+ = 28$ V (Unless Otherwise Specified)

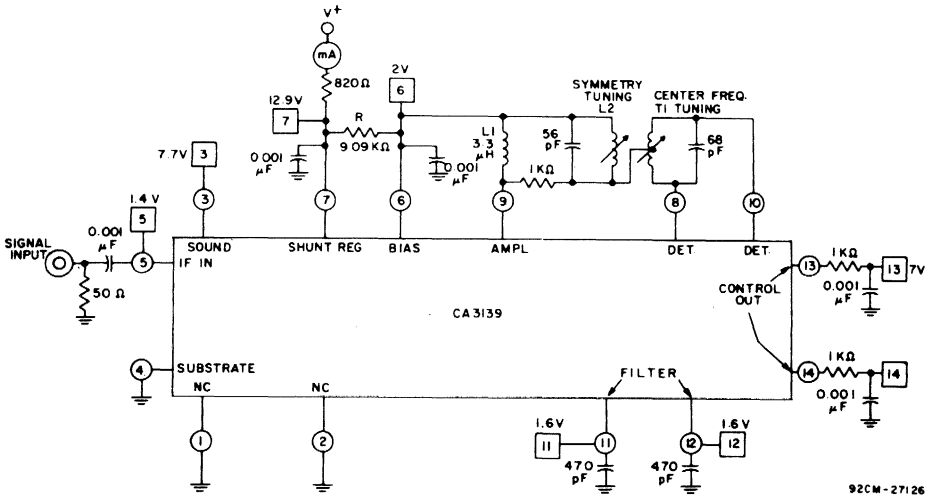
See Test Circuit, Fig. 2

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
NO SIGNAL INPUT				
Supply Current, I^+		15	20	mA
Low Voltage at Term. 7[1]	$V^+ = 20.8$ V	11	14.5	V
Shunt Reg. Voltage		12	14.5	V
Quiescent Voltage at Term. 3		4.5	10	V
Quiescent Voltage[2] at Terms. 13 and 14	Term. 13 connected to Term. 14	6	8.5	V
Quiescent Difference Voltage, Terms. 13 to 14		−0.8	+0.8	V
Quiescent Voltage at Term. 6		1.4	2.6	V
SIGNAL INPUT = 15 mV_{RMS} (Unless Otherwise Specified), Note 3				
Correction Voltage at Term. 13	f = 44.65 MHz	2.2	4.7	V
	f = 45.69 MHz	1.2	4.4	
	f = 45.81 MHz	9.6	13.8	
	f = 46.85 MHz	9.1	12.1	
Correction Voltage at Term. 14	f = 44.65 MHz	9.1	12.1	V
	f = 45.69 MHz	9.6	13.8	
	f = 45.81 MHz	1.2	4.4	
	f = 46.85 MHz	2.2	4.7	
4.5 MHz Output	Two-Tone Input f1 = 45.75 MHz at 15 mV f2 = 41.25 MHz at 5 mV	50	200	mV_{RMS}

NOTES: 1. $I_7 = 12$ mA maximum at $V_7 = 11$ V.

2. $V_{13} = 0.55\ V_Z \pm 0.7$ V

3. Resistor from term. 6 to term. 7 = 9.09 KΩ. Crossover steepens and "bow tie" width increases when resistor is decreased in value. Total peak swing decreases slightly.



NOTES:
1. Use 10 KΩ Isolation Resistor at DC Voltmeter Probe Tip When Making DC Measurements.
2. Typical No-Signal DC Potentials Are Shown.
3. Boxes Represent Test Points.

L1: RCA P.N. 122205
L2: RCA P.N. 14133
4½ Turns #22 Wire, O.D. = 0.25" (Typ.)
Q (Unloaded) = 100 (Min.)
f = 41.25 MHz
Inductance = 0.18 μh (Typ.)

T1: RCA P.N. 140507
3½ Turns (Center Tapped) #20 Wire, O.D. = 0.35" (Typ.)
Q (Unloaded) = 140 (Min.)
f = 45.75 MHz
Inductance = 0.18 μh (Typ.)

Fig. 2 — Test circuit.

CIRCUIT DESCRIPTION

The CA3139 consists of five functional circuits as shown in the block diagram, Fig. 1 (see Fig. 5 for schematic diagram).

1) **Cascode Amplifier** — Consists of emitter-follower Q1, common-emitter amplifier Q2, and common-base amplifier Q3.

2) **Bias Circuit** — Consists of Q4 and resistors R1, R4, R5, and an external resistor (user selectable) connected to the voltage regulator, terminal 7. The nominal value of the external resistor is 9.1 kΩ. Reduced values will raise the gain of the cascode amplifier chain, and higher values will reduce the gain. If the gain is increased, the AFT "Bow Tie" width will increase and the crossover slope will increase (become steeper). The input transistor Q1 is internally biased, so AC coupling is normally used to the input terminal 5.

3) **Intercarrier Mixer/Amplifier** — The output of the cascode amplifier at terminal 9 is also internally connected to the intercarrier mixer/amplifier chain consisting of transistors Q13 through Q17 and associated components. The video IF carrier at 45.75-MHz and the FM sound IF carrier at 41.25-MHz are down-converted to a 4.5-MHz FM signal by Q14. A low-pass filter removes the carriers and upper conversion signal components. The 4.5-MHz FM signal is further amplified and filtered by Q16 and C3. The FM sound output signal is at terminal 3. The gain with respect to a 5-mV sound carrier (tested with a 15-mV video carrier) input signal at terminal 5 is 10 to 40 when the resistor is connected between terminals 6 and 7 is 9.09 kΩ.

4) **AFT Detector and DC Amplifier** — Consists of Q6 through Q12 and related components. The detector inputs at terminals 8 and 10 are connected to the external discriminator transformer and biased through the transformer at terminal-6 potential. The total current through transistors Q7 and Q8 is held constant by the current-mirror transistors Q10, Q11, and Q12. External filter capacitors connected to terminals 11 and 12 assure that peak detection is accomplished. The AFT output voltages are shown in the Electrical Characteristics chart, and a graphical representation is shown in Fig. 4.

5) **Voltage Regulator** — An active shunt regulator, consisting of D1, D2, Z1, Z2, and Q5, is included to reduce the dynamic resistance.

CA3139E, CA3139Q

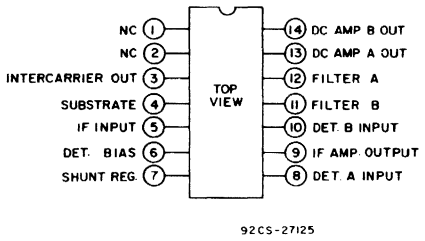


Fig. 3 – Terminal assignment.

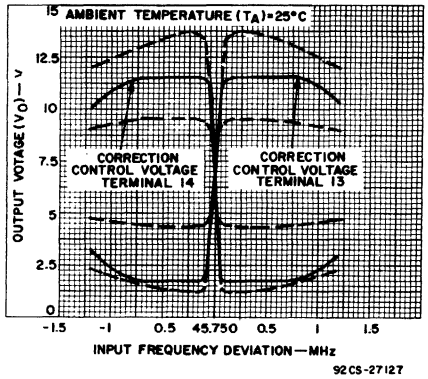


Fig. 4 – Dynamic control-voltage characteristics.

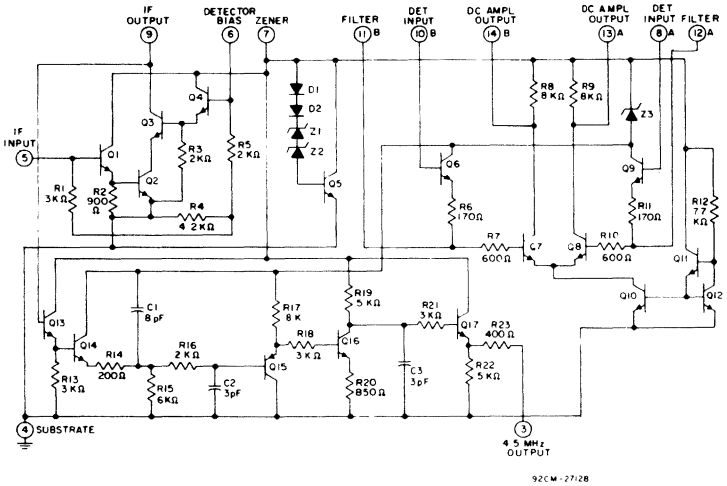


Fig. 5 – Schematic diagram of CA3139.

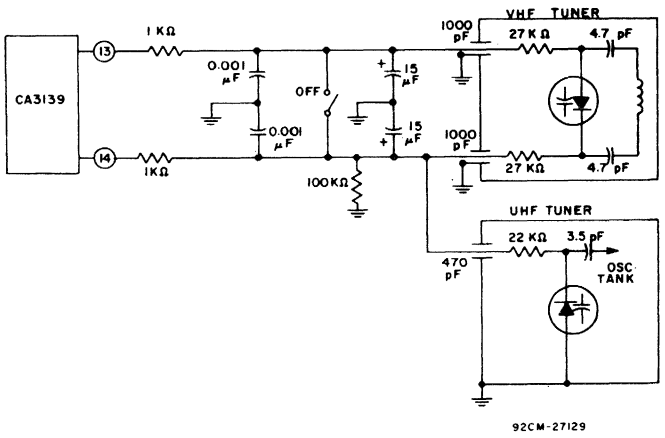


Fig. 6 – Typical tuner connection.

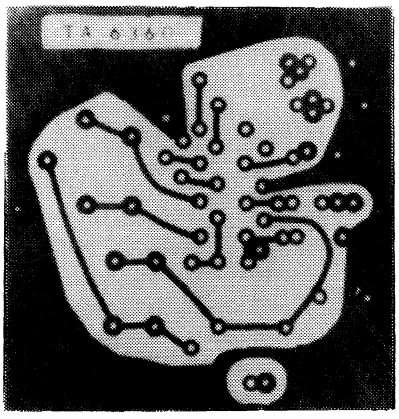


Fig. 7 – Template of CA3139Q circuit board (actual size, bottom view).

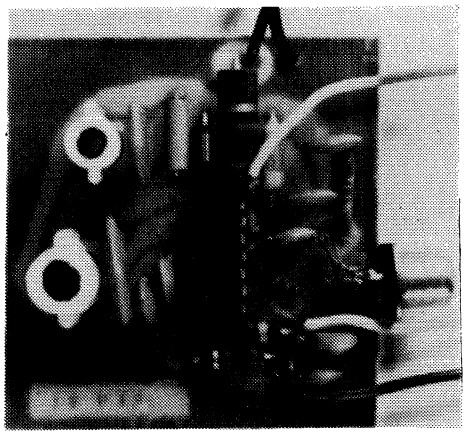


Fig. 8 – CA3139Q circuit board with components.

CA3140, CA3140A, CA3140B Types Preliminary Data

MOS Operational Amplifiers With MOS/FET Input

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS Operational Amplifier and the simplicity of the 741 series of industry-standard operational amplifiers.

The CA3140B, CA3140A, and CA3140 PMOS/bipolar operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The CA3140B operates at supply voltages, ranging from 4 to 44 volts; the CA3140 and CA3140A, from 4 to 36 volts. These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling.

The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail.

The CA3140 Series have the 8-lead terminal configuration used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, and for applications requiring premium-grade specifications and with electrical limits established for operation over the range from −55°C to +125°C. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (± 18 volts).

The CA3140 and CA3140A can also be operated safely over the temperature range from −55°C to +125°C without malfunctioning, although specification limits for their electrical parameters do not apply when they are operated beyond their specified temperature ranges.

Features:

- MOS/FET Input Stage provides:
  - a) Very high input impedance (Z_{IN}) — 1.5 TΩ typ.
  - b) Very low input current (I_I) — 10 pA typ. at ± 15 V
  - c) Low input offset voltage (V_{IO}) — to 2 mV max.
  - d) Wide common-mode input voltage range (V_{ICR}) — can be swung 0.5 volt below negative rail
  - e) output swing complements input common mode
- Directly replaces industry type 741 in most applications
- Operation from 4-to-44 volts single or dual supplies
- Internally compensated
- Characterized for + 5 volts TTL supply systems with operation down to 4 volts
- Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at + 5 V
- High slew rate — 9 Volts/μs
- Fast settling time — 1.4 μs typ. to 10 mV with a 10 V p-p signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

Applications:

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample and hold amplifiers
- Long-duration timers/multivibrators (microseconds — minutes — hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5 V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Tone controls
- Function generators
- Power supplies
- Portable instruments
- Intrusion alarm systems

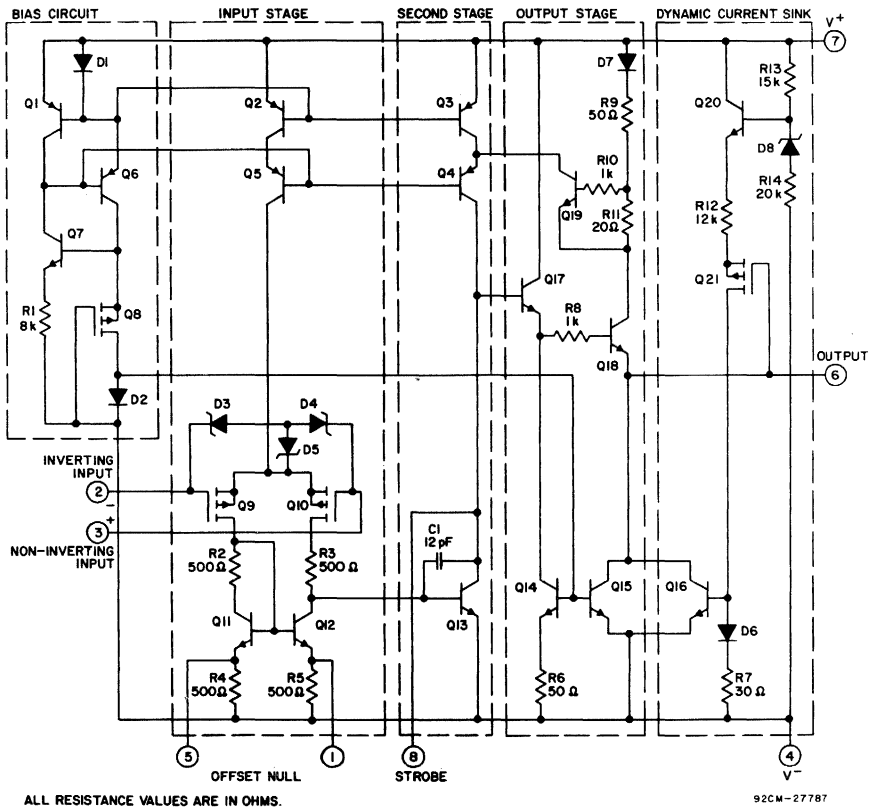


Fig. 1—Schematic diagram of CA3140 series.

CA3140, CA3140A, CA3140B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK —		
Up to 55°C	630 mW	
Above 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK —		
At 125°C	418 mW	
Below 125°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING	−55 to + 125°C	
STORAGE	−65 to + 150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

* Short circuit may be applied to ground or to either supply.

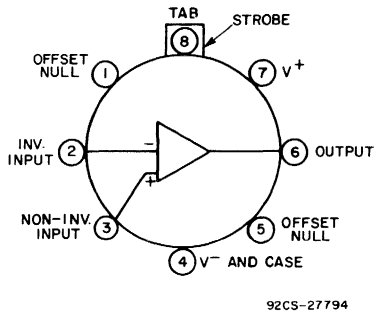


Fig. 2—Functional diagram of the CA3140 series.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

Characteristic	Test Conditions (V^+ = 15 V, V^- = 15 V, T_A = 25°C (Unless Specified Otherwise)	CA3140B			CA3140A			CA3140			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}		–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, I_{IO}		–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I		–	10	30	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}	V_O=26 V_{p-p}, +12V, −14V, R_L=2 kΩ	50k	100k	–	20k	100k	–	20k	100k	–	V/V
		94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR		–	20	50	–	32	320	–	32	320	μV/V
		86	94	–	70	90	–	70	90	–	dB
Common-Mode Input Voltage Range, V_{ICR}		−15	−15.5 to 12.5	1.2	−15	−15.5 to 12.5	12	−15	−15.5 to 12.5	11	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		–	32	100	–	100	150	–	100	320	μV/V
		80	90	–	76	80	–	76	80	–	dB
Maximum Output Voltage V_{OM}^+	R_L = 2 kΩ	+12	+12.5	–	+12	+12.5	–	+12	+12.5	–	V
Maximum Output Voltage V_{OM}^-	R_L = 2 kΩ	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	V
Supply Current, I^+		–	4	5.5	–	4	5.5	–	4	5.5	mA
Device Dissipation, P_D		–	120	165	–	120	165	–	120	165	mW
Input Current, I_I	T_A = −55 to +125°C, $V^\pm$ = ±15 V, V_O = 26 V_{p-p}, R_L = 2 kΩ	–	10	30	–	10	–	–	10	–	nA
Input Offset Voltage, V_{IO}		–	1.3	3	–	3	–	–	10	–	mV
Large-Signal Voltage Gain, A_{OL}		20k	100k	–	–	100k	–	–	100k	–	V/V
		86	100	–	–	100	–	–	100	–	dB
Maximum Output Voltage V_{OM}^+	$V^\pm$=±22V	+19	19.5	–	–	–	–	–	–	–	V
Maximum Output Voltage V_{OM}^-		−21	−21.4	–	–	–	–	–	–	–	V
Large Signal Voltage Gain, A_{OL}	R_L=2kΩ, V_O=+19V, −21V	20k	50k	–	–	–	–	–	–	–	V/V
		86	94	–	–	–	–	–	–	–	dB

CA3140, CA3140A, CA3140B Types

CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensated capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The functional circuit diagram of the CA3140 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q9,Q10) working into a mirror-pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second-Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the PMOS input stage. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q15, Q16) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V– bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink circuit is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V– supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17 Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V– bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load: any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow in D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

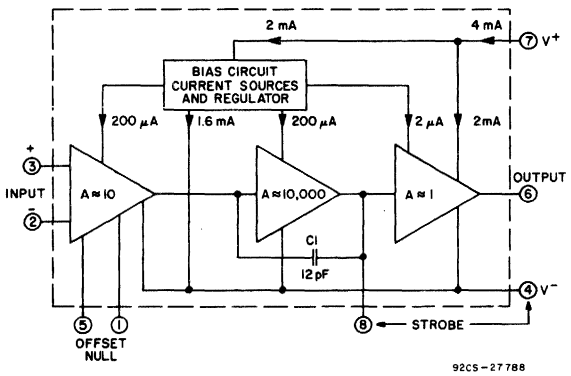


Fig. 3—Block diagram of CA3140 series.

CA3141E

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

- **Matched monolithic construction — V_F for each diode pair matched to within 0.55 mV (typ.) at I_F = 1 mA**
- **Low diode capacitance — 0.3 pF (typ.) at V_R = 2 V**
- **High diode-to-substrate breakdown voltage — 30 V (min.)**
- **Low reverse (leakage) current — 100 nA (max.)**

Applications:

- **Balanced modulators or demodulators**
- **Analog switches**
- **High-voltage diode gates**
- **Current ratio detectors**

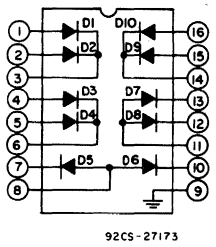


Fig. 1 — Terminal assignment.

The RCA-CA3141E High-Voltage Diode Array consists of ten general-purpose high-reverse-breakdown diodes. Six diodes are internally connected to form three common-cathode diode pairs, and the remaining four diodes are internally connected to form two common-anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141E extremely useful for a wide variety of applications in communications and switching systems.

The CA3141E is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

PEAK INVERSE VOLTAGE (PIV)	30 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE	30 V
PEAK FORWARD SURGE CURRENT [I_F (SURGE)]	100 mA
DC FORWARD CURRENT (I_F)	25 mA
DISSIPATION:	
Any one diode unit	50 mW
Total Package:	
Up to 55°C	650 mW
For $T_A > 55$°C	Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max.	+265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNIT
DC Forward Voltage Drop, V_F	I_F (Anode)	100 μA	—	0.7	0.9	V
		1 mA	—	0.78	1	
		10 mA	—	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	I_F = −10 μA		30	50	—	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	I_{DI} = 10 μA		30	50	—	V
DC Reverse (Leakage) Current, I_R	V_F = −20 V		—	—	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	V_{DI} = 20 V		—	—	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	V_{DI} = 20 V, I_{FA} = 1 mA		—	0.55	—	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	I_F = 1 mA		—	−1.5	—	mV/°C
Reverse Recovery Time, t_{rr}	I_F = 2 mA, I_R = 2 mA		—	50	—	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Anode-to-Cathode Current Ratio, $\lvert I_{FA}/I_{FC}\rvert$	I_{FA} = 1 mA, V_{DS} = 10 V		0.9	0.96	—	

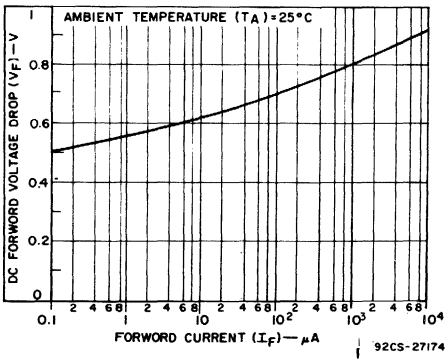


Fig. 2 — DC forward voltage drop vs. forward current.

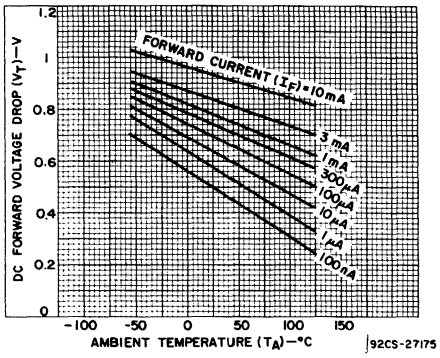


Fig. 3 — DC forward voltage drop vs. ambient temperature.

CA3141E

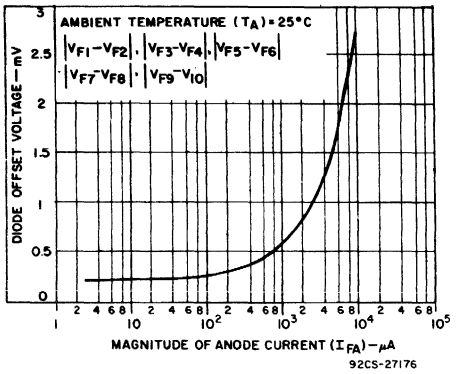


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

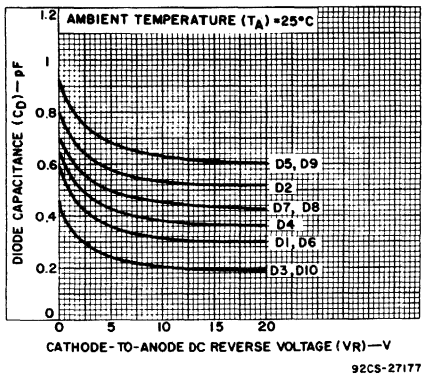


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

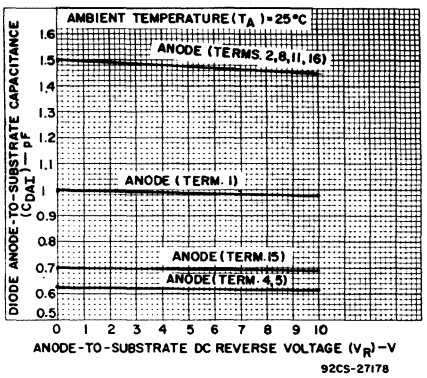


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

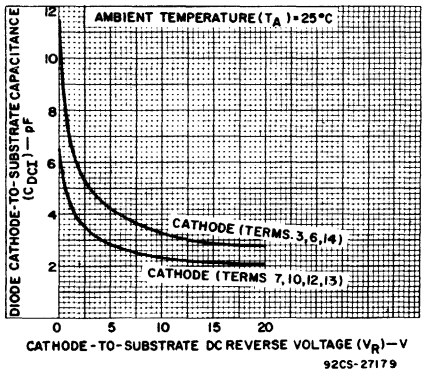


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

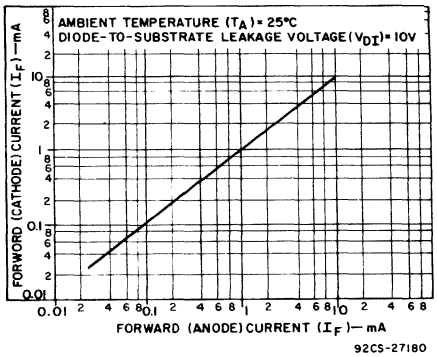


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

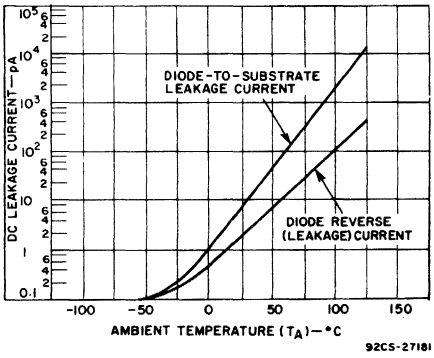


Fig. 9 — DC leakage current vs. ambient temperature.

CA3143E Preliminary Data

TV Luminance Processor

The CA3143E is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

This device, when used in conjunction with the CA3126Q chroma processor and the CA3137E chroma demodulator, will provide a luminance/chrominance system having excellent tracking of controls. The CA3143E is supplied in a 14-lead dual-in-line plastic package.

Features:

- **Black-level clamping**
- **Linear dc controls for brightness, contrast, and peaking**
- **Horizontal and vertical blanking**

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC SUPPLY CURRENT (Into Terminal 13)*	59.5 mA
DEVICE DISSIPATION:*	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly 7.9 mW/^oC
AMBIENT–TEMPERATURE RANGE:	
Operating	–40 to +85^oC
Storage	–65 to +150^oC
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265^oC

* Although the CA3143E is rated for maximum dissipation of 750 mW, it is recommended that the current into terminal 13 be limited by external circuit resistance to 39 mA for a typical voltage at terminal 13 of 11.8 volts.

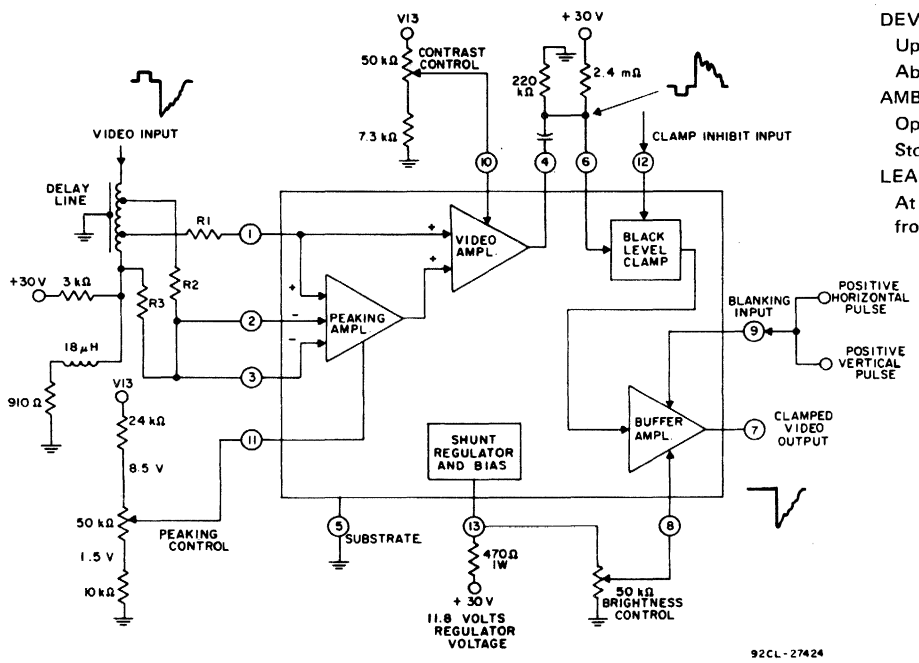


Fig. 1 – Functional block diagram.

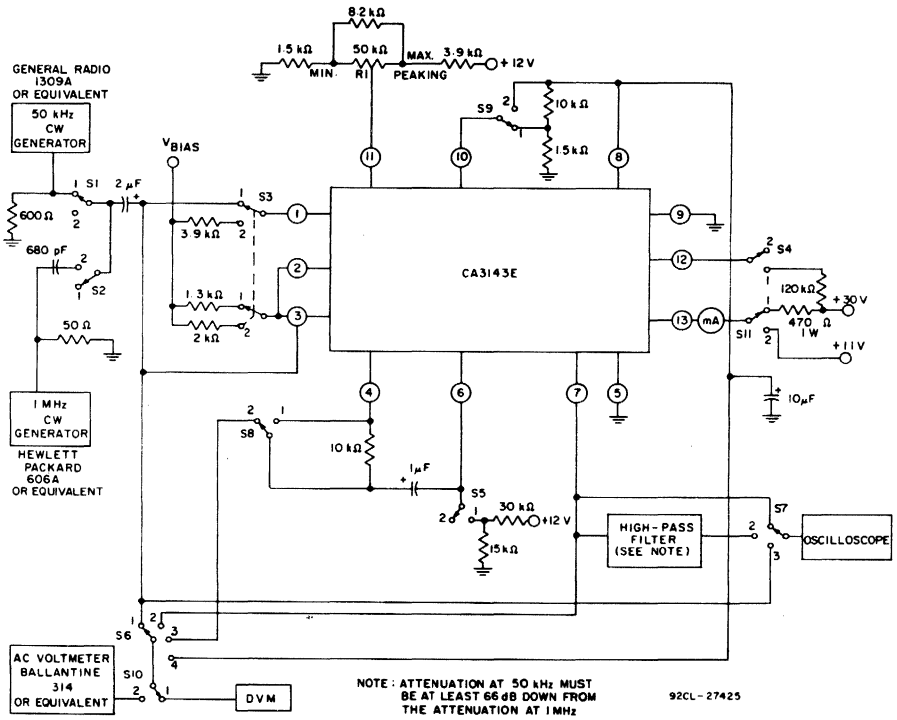


Fig. 2 – Test circuit.

CIRCUIT DESCRIPTION

Fig. 1 is a block diagram of the CA3143E indicating the internal functions as well as external circuitry and signals. The video input signal with positive-going sync is applied to the input of the tapped delay line. Signals from fixed taps of the delay line are applied to terminals 1, 2 and 3 of the CA3143E. In referring to Fig. 3, the signal from the delay line tap A is applied to the video input at terminal 1. The signals from

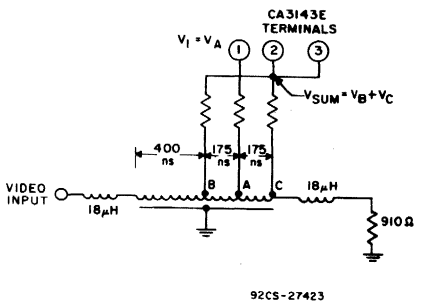


Fig. 3 – Tapped delay line.

taps B and C are summed where $V_A + V_B = V_{sum}$. The signal (V_{sum}) is then applied to the parallel connection of the peaking input terminals, 2 and 3. The video input signal is applied to a non-inverting input of the peaking amplifier while the peaking input signal (V_{sum}) is applied to an inverting input of the peaking amplifier.

CA3143E Preliminary Data

Low-frequency video components are unattenuated, while high-frequency components are attenuated as a function of the delay-line tap points. The peaking amplifier is a differential amplifier, so that the output is proportional to V_1 minus V_{sum}. At low frequencies, the signal at terminals 2 and 3 is unattenuated, and the peaking amplifier produces no output at these frequencies. However, at high frequencies the signal at terminals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D2. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D2. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D2 is forced to ground due to saturation of Q17. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 9. The pulses turn ON p-n-p transistor Q6 which shorts the base of transistor Q15 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 8. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 8 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Bias Volts (V)	Test Conditions: Switch Numbers S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11 — Switch Positions For Characteristics Measurements	Typ. Value	Units
STATIC														
Voltage: At Term. 13 (V13●)	6.1	2	1	1	2	2	4	1	2	2	1	1	11.8	V
Quiescent Voltage At Term. 4 (V4●)	6.1	2	1	1	2	2	3	1	2	2	1	1	4	V
Quiescent Voltage At Term. 7 (V7●)	6.1	2	1	1	2	2	2	1	2	2	1	1	7.7	V
Current into Term. 13 (Term. 13 Connected to +11 V) (I13●)	6.1	2	1	1	2	2	3	1	2	2	1	2	2.1	mA
DYNAMIC														
Wide-Band Gain (Note 1)	5.8	1	1	1	2	1	2	1	1	1	2	1	8.3	dB
Contrast Gain Reduction (Note 2)	5.8	1	1	1	2	1	2	1	1	2	2	1	−30	dB
Peaking Gain (Note 1)	5.8	1	1	2	2	1	2	1	1	1	2	1	18.4	dB
Peaking Gain Reduction (Note 3)	5.8	1	1	2	2	1	2	1	1	1	2	1	−18	dB
Max. Intermodulation Distortion: (Note 4) 2 V	5.8	1	–	1	1	1	2	–	2	1	2	1	20	%
3 V (Note 5)	5.8	1	–	1	1	1	2	–	2	1	2	1	40	%

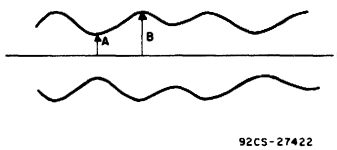
● Terminal measured and Symbol

Note 1: Set 50-kHz generator for 100 mVp-p. Adjust R1 Peaking Control (See Fig.2) for minimum setting. Measure wide-band gain at terminal 7.

Note 2: Set 50-kHz generator for 100 mVp-p. Adjust R1 for minimum setting. Measure contrast gain reduction at terminal 7.

Note 3: Set 50-kHz generator for 100 mV-p-p. Adjust R1 for maximum setting. Measure peaking gain reduction at terminal 7.

Note 4: Adjust R1 for minimum setting. With S2 at switch position1 and S7 at switch position 3, set 50-kHz generator for 2 Vp-p. Then with S2 at switch position 2, set 1 MHz generator for 100 mVp-p. Then with S7 at switch position 2, measure downward modulation of the 1-MHz signal due to the 50-kHz signal.



92CS-27422

A = Amplitude of 50 kHz signal at deepest trou

B = Peak amplitude of 50 kHz signal

Downward Modulation = $\frac{B-A}{B}$

Note 5: Repeat step 4 except that the 50-kHz generator must be set at 3 Vp-p.

CA3147E Preliminary Data

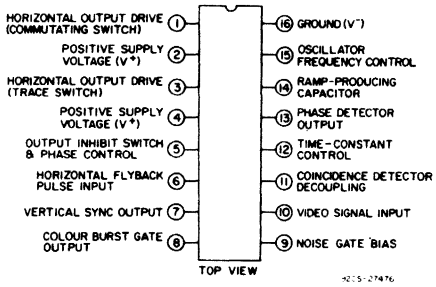
TV Horizontal Processor

For Colour and Monochrome Receivers

The RCA-CA3147E is a monolithic silicon integrated circuit Horizontal Processor designed to drive either SCR or transistorized deflection systems. In addition to providing performance similar to the CA920AE, the CA3147E incorporates a colour burst gating pulse and is capable of supplying suitable pulses for driving both the commutating and the trace switches of SCR deflection systems such as that shown in Fig. 2.

The duration of the commutating pulse is typically 6 μs, suitable for either single-standard or dual-standard 625/819 line receivers. The basic component arrangement for driving a transistorized output stage is shown in Fig. 1.

The CA3147E is supplied in a 16-lead dual-in-line plastic package that incorporates a copper lead-frame to enhance thermal dissipation capability.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS,
Absolute-Maximum Values at T_A=25°C

DC SUPPLY VOLTAGE ..... 16 V

DEVICE DISSIPATION:
Up to T_A = 60°C ..... 1 W
Above T_A = 60°C
..... Derate linearly at 11.1 mW/°C

AMBIENT TEMPERATURE RANGE:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C

OUTPUT CURRENT:
Commutating switch (peak) ..... 500 mA
Trace switch (peak) ..... 300 mA
Trace switch (avg.) ..... 40 mA

LEAD TEMPERATURE (During Soldering):
At a distance not less than 1/32 in. (0.79 mm) from case for 10 seconds max. ..... +265°C

Features:

- **Output pulses for driving both trace switch and commutating switch in SCR deflection systems**
- **Dual-time-constant phase-locked loop**
- **Vertical-sync pulse output**
- **Burst-gate pulse output**
- **Internal noise gate**
- **Low-voltage protection circuit**
- **Reduced peripheral components**

ELECTRICAL CHARACTERISTICS at T_A = 25°C, and Supply Voltage (V^+) = 12 V at Term. 4 unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Supply Current, Term. (2 + 4)	I^+	Terms. 1 & 3 open		37		mA
Phase Detector Characteristics (Term. 13): Output Current	I_{13}	Capture Mode		±3		mA
Output Current	I_{13}	Hold Mode		±1		
Vertical Sync Output Characteristics (Term. 7): Pulse Duration	t_7	Composite Video Input		160		μs
Pulse Amplitude	V_7			10		V
Colour Burst Characteristics (Term. 8): Pulse Duration	t_8			5		μs
Pulse Amplitude	V_8			10		V
Output Switch Characteristics (Term. 4):* Output Stage Enable	V_4	Switch closed		4.5		V
Output Stage Inhibit	V_4	Switch open		4		
Trace Output Drive Characteristics (Term. 3): Pulse Duration	t_3	80 mA pk. output		22 + t_d		μs
Pulse Amplitude	V_3	80 mA pk. output		10		V
Commutating Output Drive Characteristics (Term. 1): Pulse Duration	t_1	400 mA pk. output		6		μs
Pulse Amplitude	V_1	400 mA pk. output		10		V
Oscillator Pull-In Range (Term. 15):	Δf_o	f_o varied		±750		Hz

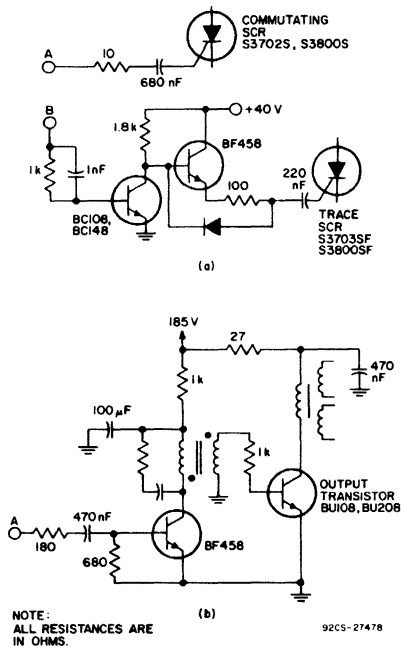


Fig. 1—Typical horizontal drive networks using (a) SCR switching and (b) transistor switching.

CA3147E Preliminary Data

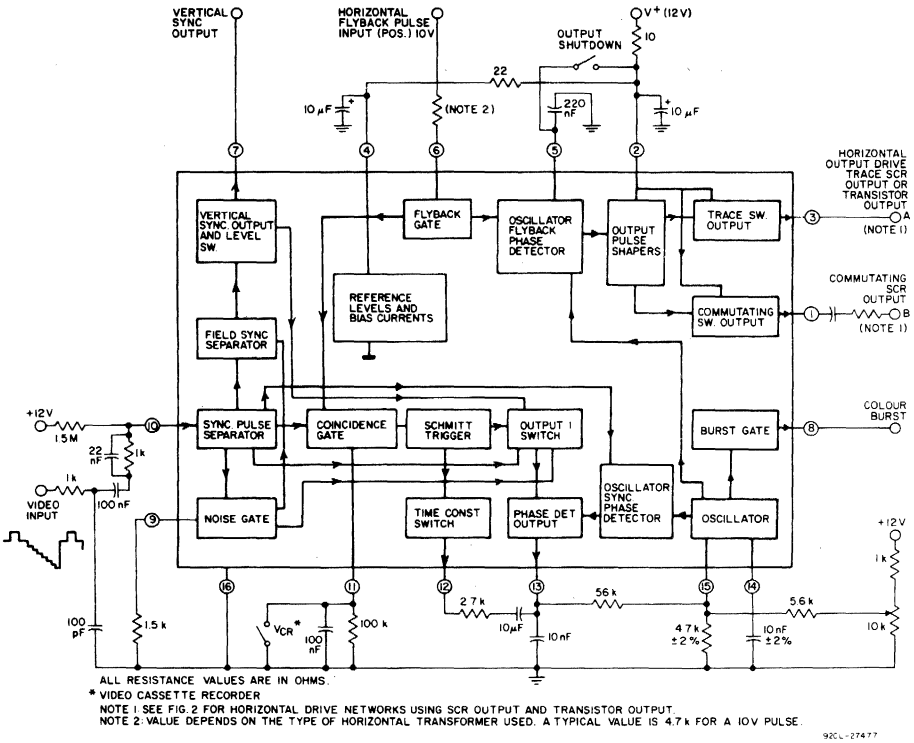


Fig. 2—Functional block diagram for CA3147E.

CA3170E Preliminary Data

TV Chroma System

The RCA-CA3170E is a monolithic silicon integrated circuit that performs the functions of subcarrier regeneration, ACC and APC detection, and tint control in color television receivers. It is designed to function compatibly with the CA3121E TV Chroma Amplifier/ Demodulator in a 2-package chroma system.

The CA3170E is a TV Chroma System of advanced design that incorporates all the features of the CA3070E but with the added advantage of a modified Hue Control Characteristic. With the CA3170E, the designer can provide a front panel hue control that functions linearly over its entire range, a particularly desirable consumer feature.

The CA3170E is supplied in a 16-lead dual-in-line plastic package (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DEVICE DISSIPATION:
- Up to T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C . . . . . derate linearly 7.9 mW/°C

AMBIENT–TEMPERATURE RANGE:
- Operating . . . . . –40 to +85°C
- Storage . . . . . –65 to +150°C

LEAD TEMPERATURE (During soldering):
- At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

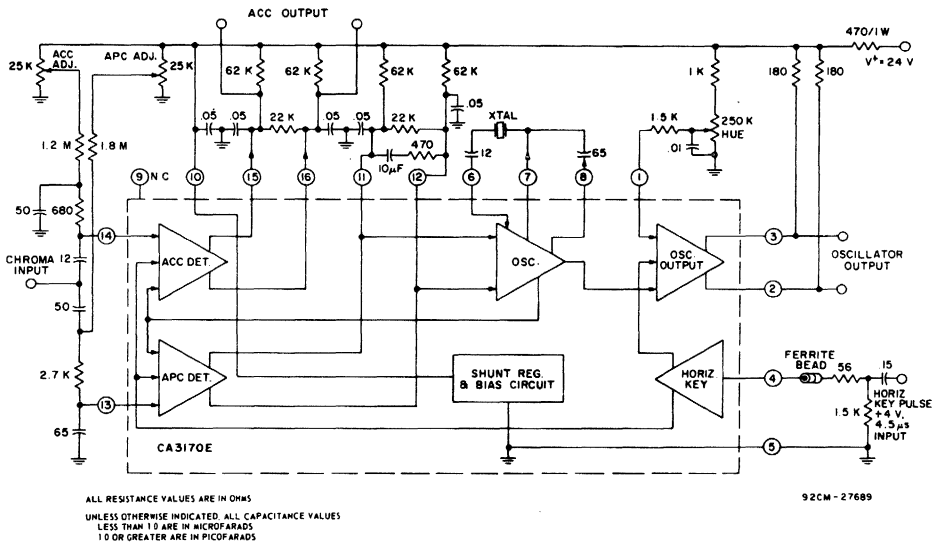


Fig. 1 – Functional block diagram of CA3170E.

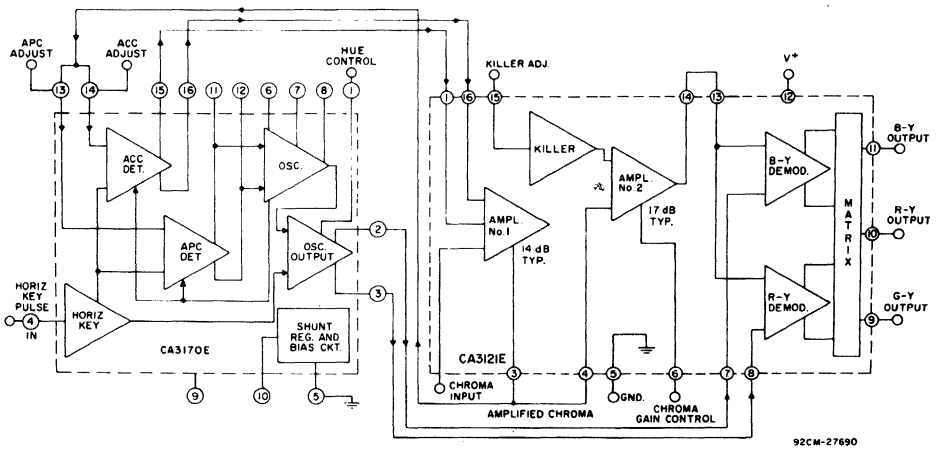


Fig. 2 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3170E and CA3121E.

CIRCUIT DESCRIPTION

The CA3170E is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3121E is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval. The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 16 of the CA3121E. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator. To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3170E includes a shunt regulator to establish a 12-volt dc supply.

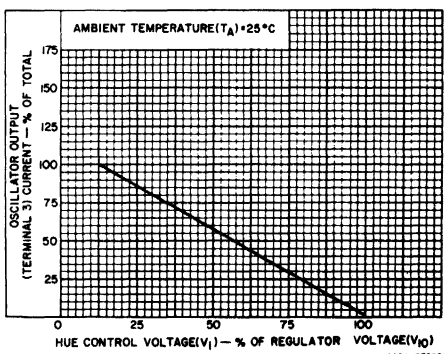


Fig. 3 – Typical hue control characteristic.

CA3170E Preliminary Data

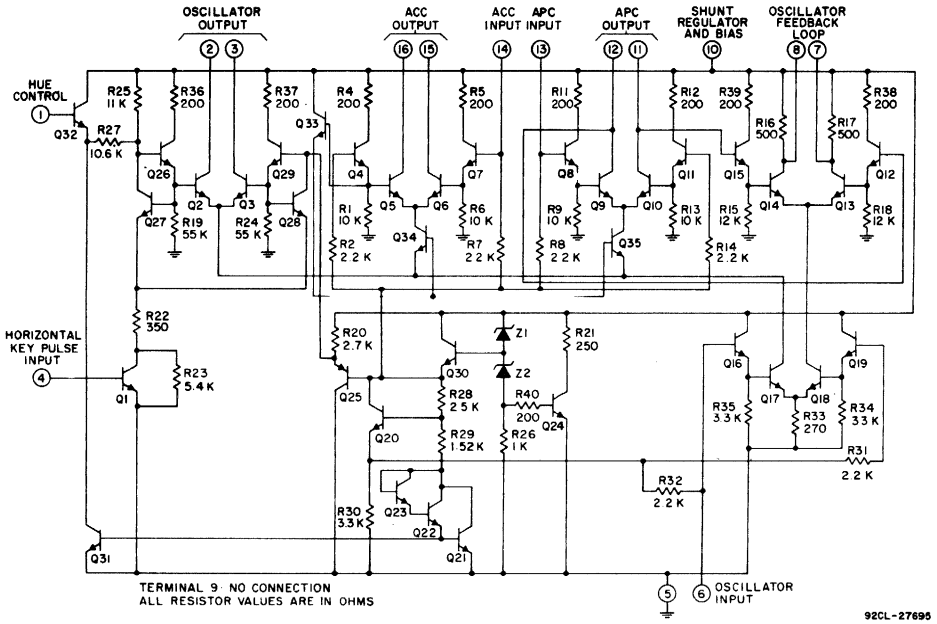


Fig. 5 – Schematic diagram of the CA3170E.

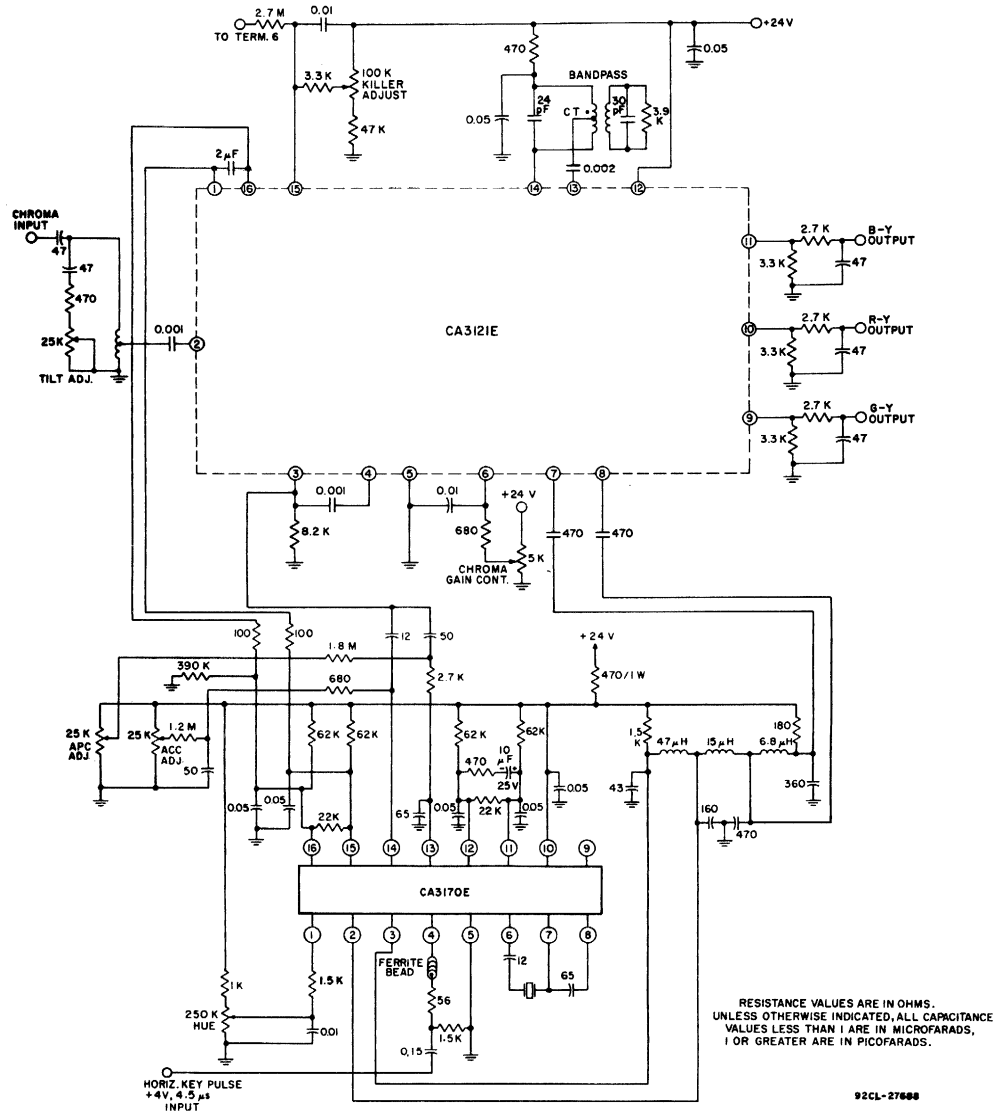


Fig. 6 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3170E.

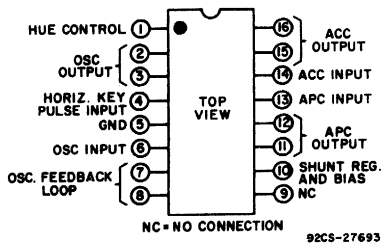


Fig. 4 – Terminal diagram of the CA3170E.

Features:

- **Voltage-controlled oscillator**
- **Keyed APC and ACC detectors**
- **DC hue control**
- **Shunt regulator**

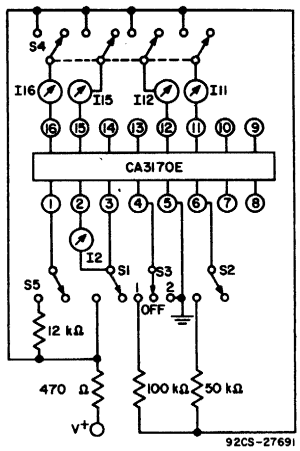


Fig. 7 – Static characteristics test circuit

CA3170E Preliminary Data

ELECTRICAL CHARACTERISTCS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS CA3170E MIN.	TYP.	MAX.	UNITS
Static Characteristics					
Voltage: Hue Control, V_1	See Fig. 8				V
Oscillator Input, V_6	S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN See Fig. 6	–	2.6	–	
APC Input, V_{13}		–	5.4	–	
Regulator, V_{10}	V^+ = 21 V	11	12.3	13.5	
Regulator Change, V_{10}	V^+ = 27 V	-0.2	–	+0.2	
Horizontal Key Input, V_4	I_4 = -10 μA	5	–	–	
Currents: Oscillator Output, I_2	S_1, S_2, S_4, S_5 CLOSED, S_3 in position 2, See Fig. 6	–	5.8	–	mA
APC Output, I_{11}, I_{12}	S_1, S_5 OPEN, S_2, S_4 CLOSED, S_3 in position 1, See Fig. 6	–	1.45	–	
ACC Output, I_{15}, I_{16}		–	1.45	–	
Dynamic Characteristics (See Figure 5)					
Oscillator Outputs: Terminal No. 2, V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}
Terminal No. 3, V_3	S_1 in position 2	0.75	1.0	–	
ACC Detected Output $V_{16} - V_{15}$	S_1 in position 1	115	150	–	mV
Oscillator Pull-In Range	S_1 in position 1	–	±400	–	Hz

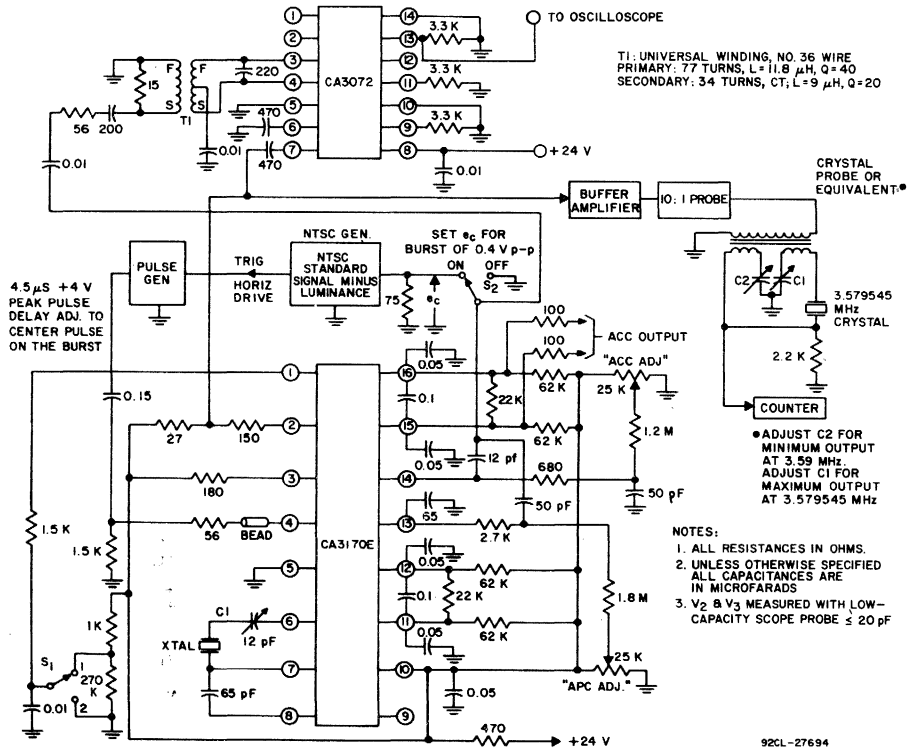


Fig. 8 — Dynamic characteristics test circuit.

DYNAMIC TEST PROCEDURE

1. With S2 in "OFF" position, short terminals 11 and 12. Then with S1 in 1 position, adjust CX for a frequency of 3.579545 MHz ± 5 Hz. Measure the frequency using the frequency counter or by zero beat indication on the oscilloscope.
2. Remove short from terminals 11 and 12, and adjust "APC" control for zero beat on the oscilloscope. With S2 in "ON" position, pattern on oscilloscope must lock.
3. With S2 in "OFF" position adjust "ACC" control to give output reading of 0 ± 2 mV between terminals 15 and 16. Then with S2 in "ON" position, read "ACC" output.
4. Example of pull-in testing to ± 200 Hz: With S2 in "OFF" position, adjust CX for frequency of 3.579545 + 200 Hz. Then with S1 in position 1 and S2 in "ON" position, pattern on oscilloscope must lock.
5. Repeat Step 4 with CX adjusted to - 200 Hz.

CA3401E, CA3401G

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

"G" Suffix Types — Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types — Standard Dual-In-Line Plastic Package

The RCA-CA3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is ideally suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), a hermetic gold-chip in 14-lead dual-in-line plastic package (G suffix), in chip form (H suffix), and as a hermetic gold-chip (HG suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semiconductor LM3900N. The CA3401 can be operated over the temperature range of −55 to +125°C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75°C.

Features:

- **Single-supply operation — +5 V to +18 Vdc**
- **Internally compensated**
- **Wide unity-gain bandwidth — 5 MHz typ.**
- **Low input bias current — 50 nA typ.**
- **High open-loop gain — 2000 V/V typ.**

Applications:

- **Automotive**
- **Constant-Current Sources**
- **Multivibrators**
- **Sample and Hold**
- **Square-Wave Generator**
- **Oscillators**
- **Tachometers**
- **Active Filters**
- **Multi-Channel Amplifiers**
- **Summing Amplifiers**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE	+18 V
INPUT SIGNAL CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25°C	625 mW
Above T_A = 25°C	Derate linearly 5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300 °C

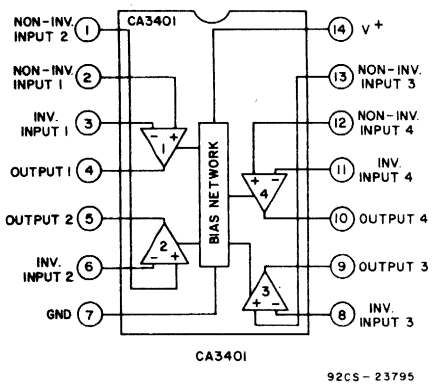


Fig.1 — Block diagram of CA3401.

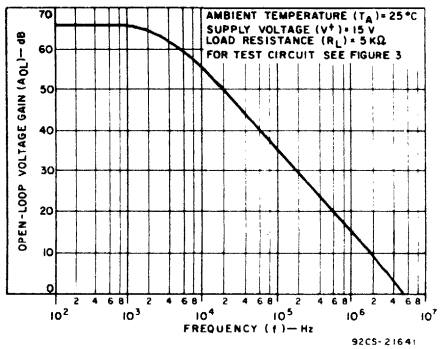


Fig.2 — Open-loop voltage gain vs. frequency.

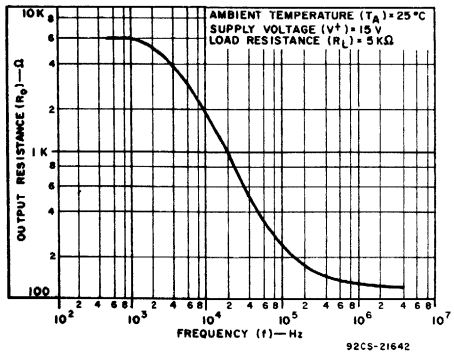


Fig.3 — Output resistance vs. frequency.

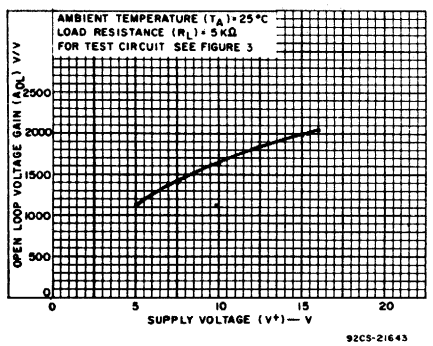


Fig.5 — Open-loop voltage gain vs. supply voltage.

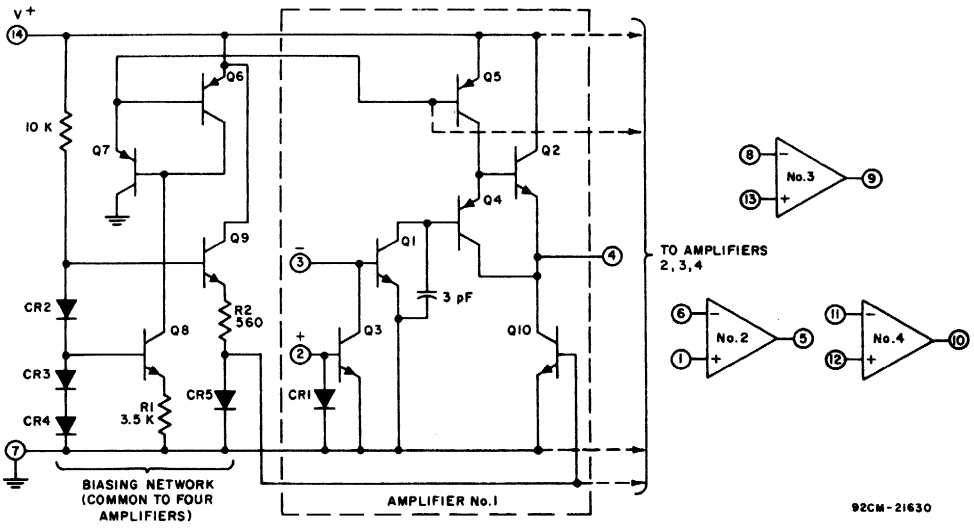


Fig.4 — Schematic diagram of CA3401.

CA3401E, CA3401G

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	0°C<T_A<75°C	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	R_L = ∞ T_A = 25°C	–	50	300	nA
	R_L = ∞ 0°C ≤T_A≤75°C	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	T_A = 25°C	1000	2000	–	V/V
	0°C≤T_A≤75°C	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	C_L = 100 pF, R_L = 5 kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

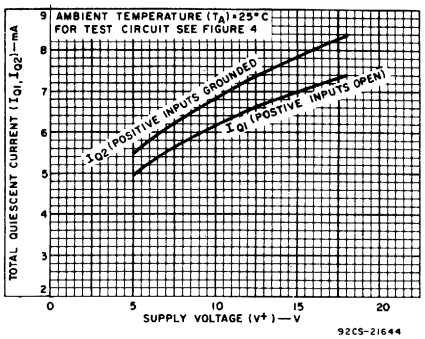


Fig.10 – Supply current vs. supply voltage.

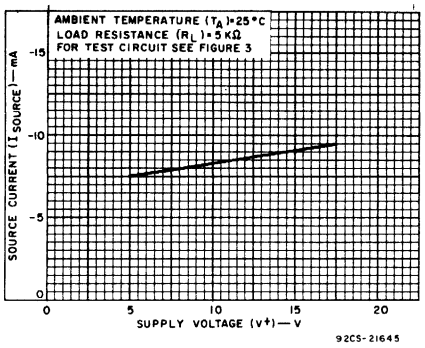


Fig.11 – Source current vs. supply voltage.

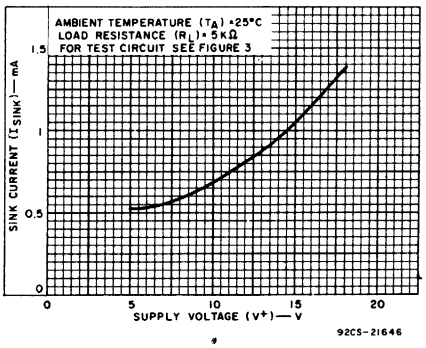


Fig.12 – Sink current vs. supply voltage.

TEST CIRCUITS

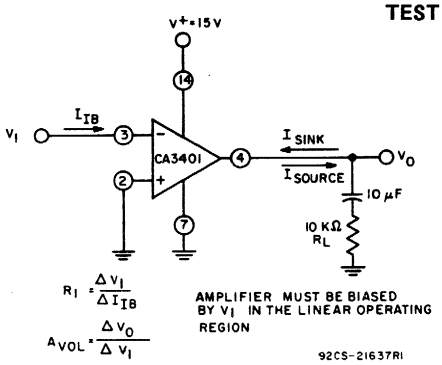


Fig.6 – Open-loop gain and input resistance, input bias current and output current test circuit.

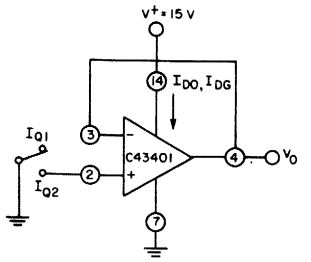


Fig.7 – Quiescent power supply current test circuit.

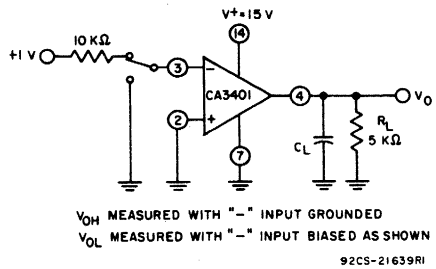


Fig.8 – Output voltage swing test circuit.

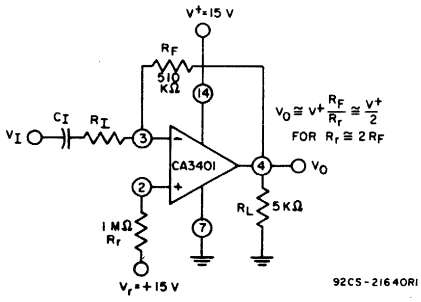


Fig.9 – Peak-to-peak output voltage test circuit.

CA3600E

COS/MOS Transistor Array

For Linear Circuit Applications

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA COS/MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-271.

Features:

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . 10 pA (typ.)
- Matched p-channel pair:
  Gate-voltage differential (I_D = -100 μA) ±20 mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per COS/MOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

Applications:

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DISSIPATION:

Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating	−55 to +125°C
Storage	−65 to +150°C

LEAD TEMPERATURE (During Soldering)

At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:	
n-channel	+15 V
p-channel	−15 V
DRAIN-TO-GATE VOLTAGE, V_{DG}:	
n-channel	+15 V
p-channel	−15 V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:	
n-channel	+15 V
p-channel	−15 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:	
p-channel transistors (p_1, p_2, p_3)	0 V(min.),−V_D(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),+V_D(max.)
COS/MOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),+V_{DD}(max.)
DRAIN CURRENT, $\|I_D\|$	10 mA
GATE CURRENT, $\|I_G\|$	100 μA

The Following Rating Applies for Each COS/MOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices"

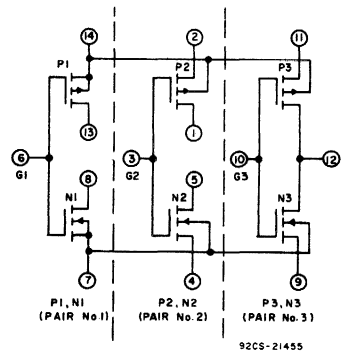


Fig. 1 – Schematic diagram for CA3600E COS/MOS transistor array.

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors · · · V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors · · · V_{DD} termina

Terminal Identification for Fig. 1.

TYPICAL CHARACTERISTICS CURVES

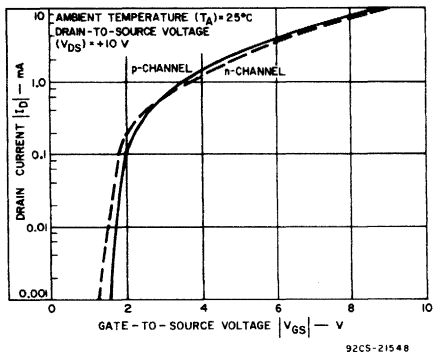


Fig. 2—Drain current vs. gate-to-source voltage.

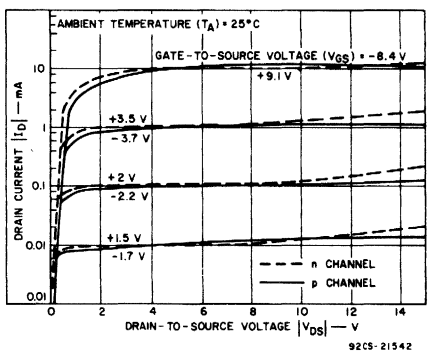


Fig. 3— Drain current vs. drain-to-source voltage.

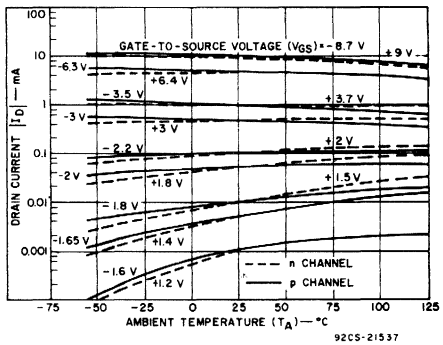


Fig. 4— Drain current vs. ambient temperature.

CA3600E

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500	–	μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	1.1		pF

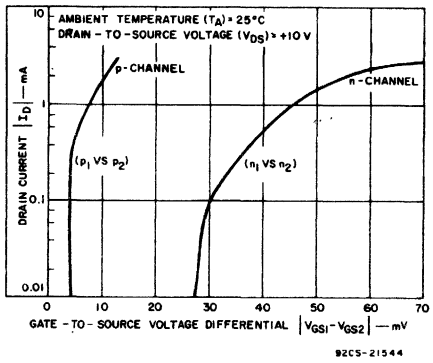


Fig. 5– Gate-to-source voltage differential vs. drain current.

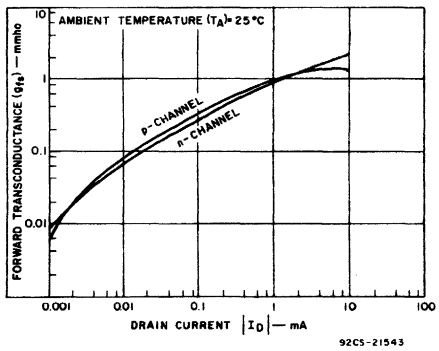


Fig. 6– Forward transconductance vs. drain current.

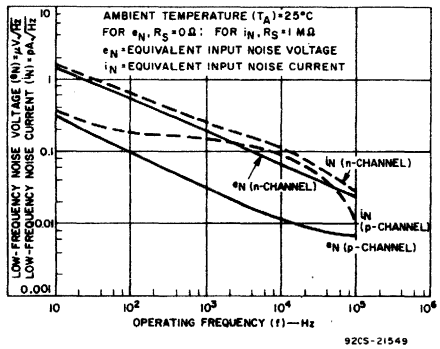


Fig. 7– Noise voltage and noise current vs. operating frequency.

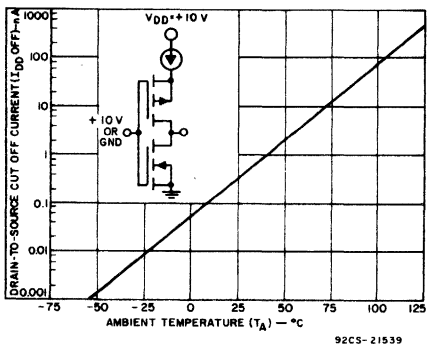


Fig. 8– Drain-to-source cutoff current vs. ambient temperature.

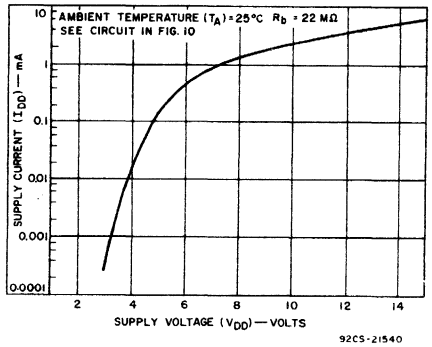


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

CA3600E

APPLICATIONS

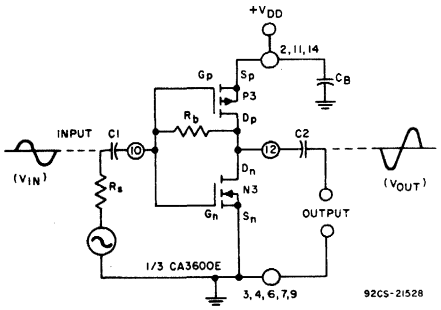


Fig. 10– COS/MOS transistor-pair biased for linear-mode operation.

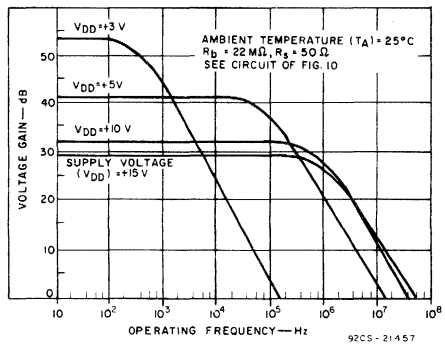


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

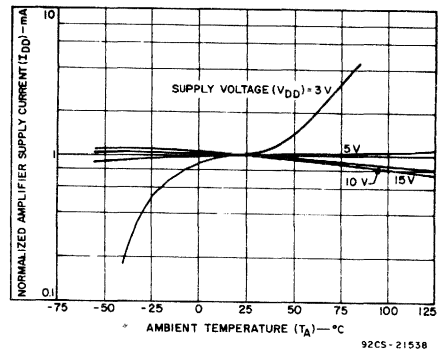


Fig. 12– Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

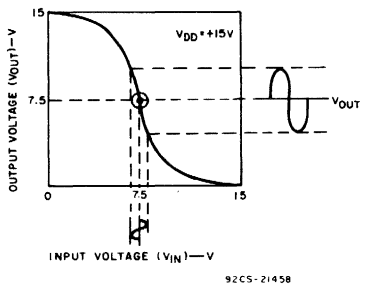


Fig.13 – Representation of voltage-transfer characteristics for COS/MOS transistor pair.

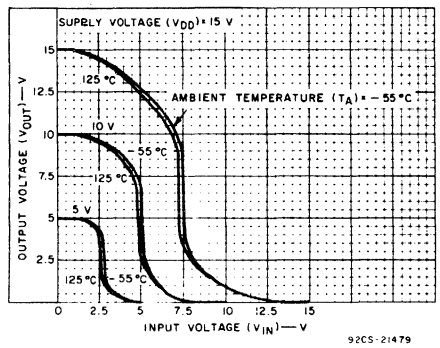


Fig. 14– Voltage transfer characteristics for COS/MOS transistor-pair amplifier in Fig. 10.

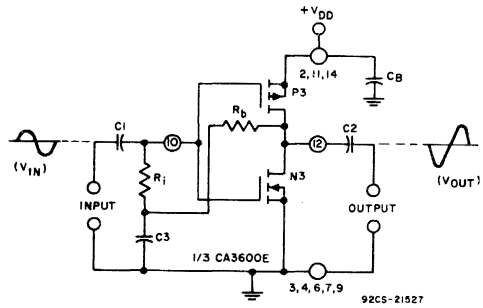


Fig. 15– Alternate method of biasing COS/MOS transistor-pair for linear-mode operation.

The Basic COS/MOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits . Since mutually compatible p-channel and n-channel MOS/FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, COS/MOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E COS/MOS transistor array shown in Fig. 1.

A "True-Complementary" Linear Amplifier Using COS/MOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a COS/MOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the COS/MOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When the signal input-voltage level (V_{in}) becomes very large, the output signal (V_{out}) waveforms become distorted because the transistors are driven into the non-linear portions of their voltage-transfer characteristics. If the positive-going input-signal is sufficiently large, for example, the p-channel transistor can be driven to cutoff and the amplifier supply current (I_{DD}) is reduced to essentially zero.

Fig. 14 shows typical voltage-transfer characteristics of each COS/MOS pair in the CA3600E at several values of V_{DD}. The shape of these transfer characteristics is comparatively constant despite temperature changes from −55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provides an easy method of establishing feedback for ac signals in accordance with the R_b/R_s ratio. When the feedback of ac signals is not desirable, the circuit of Fig. 15 may be used. The ac bypass capacitor (C_3) minimizes ac signal feedback.

Cascading Amplifier Stages of COS/MOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of COS/MOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

Post-Amplifiers For Op-Amps

COS/MOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the COS/MOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each COS/MOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the COS/MOS pair. A detailed description of the subject has been published previously.

The schematic diagram in Fig. 18 shows a COS/MOS transistor pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier. The approximate 30-dB gain in a single COS/MOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 18 is approximately 65 V/μs. When compensated for the unity gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/μs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage COS/MOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/μs. A slew rate of about 1 V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

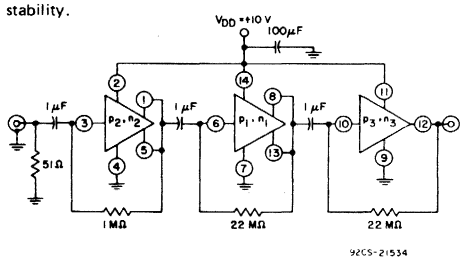


Fig. 16– High-gain amplifier uses cascaded COS/MOS transistor-pair in CA3600E.

CA3600E

APPLICATIONS – Post-Amplifiers for Op-Amps (Cont'd)

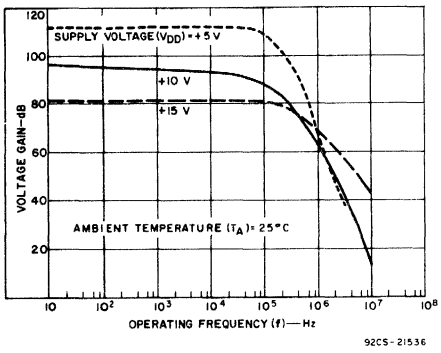


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

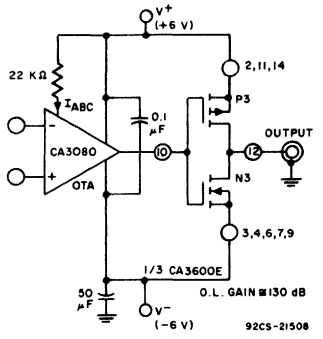


Fig. 18– COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

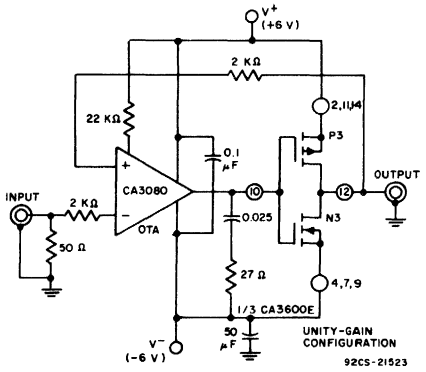


Fig. 19– COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published. The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier. Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

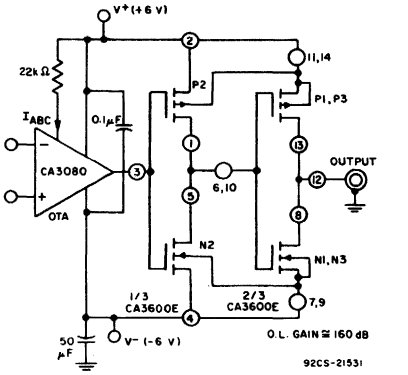


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

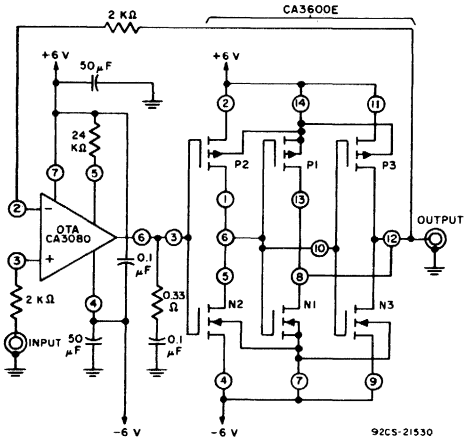


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.

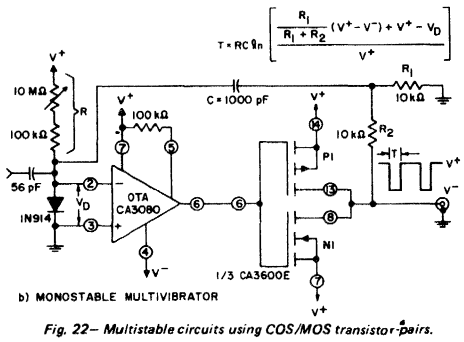


Fig. 22– Multistable circuits using COS/MOS transistor pairs.

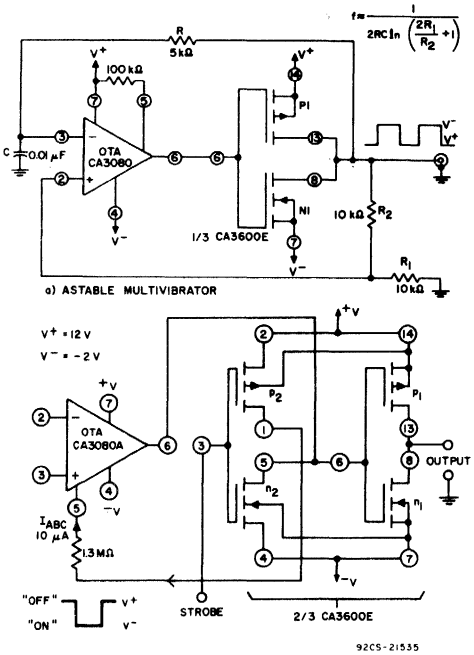


Fig. 23– Programmable micropower comparator.

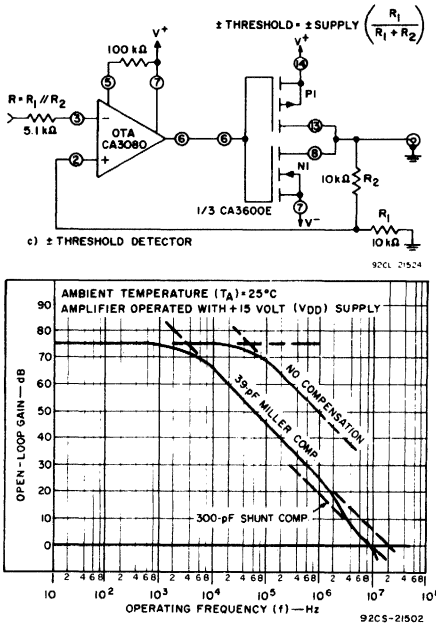


Fig. 24– Open-loop gain characteristic for op-amp.

CA3600E

Oscillator Circuits

Oscillator circuits using COS/MOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.

The design of COS/MOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single stage amplifier using a COS/MOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 25. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

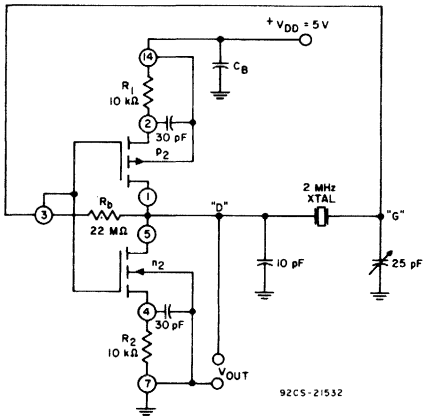


Fig. 25– Typical crystal-oscillator circuit using COS/MOS transistor-pair (1/3 CA3600E).

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature. As shown in Fig. 26, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit. MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 27, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E COS/MOS transistor array.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

Complementary Current Mirrors Using COS/MOS Transistor-Pairs

COS/MOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 30. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source $I_{D2\text{-}P}$ equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink $I_{D2\text{-}N}$ equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 28. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

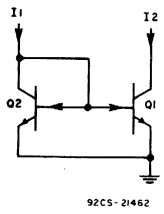


Fig. 26– Current mirror using n-p-n bipolar transistors.

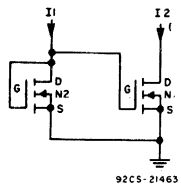


Fig. 27–Current mirror using n-channel MOS transistors.

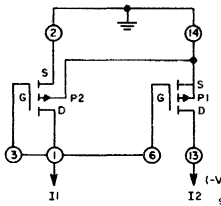


Fig. 28–Current mirror using p-channel MOS transistors in CA3600E.

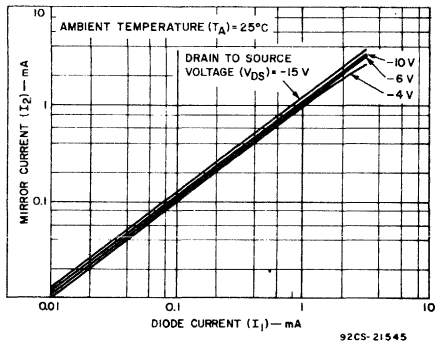


Fig. 29– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

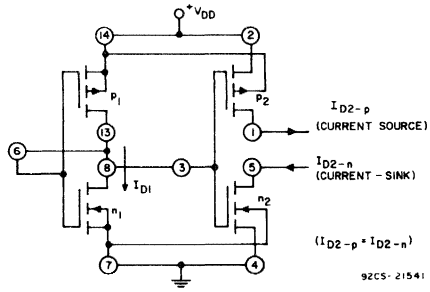


Fig. 30– Complementary current mirrors using COS/MOS transistor-pairs in CA3600E.

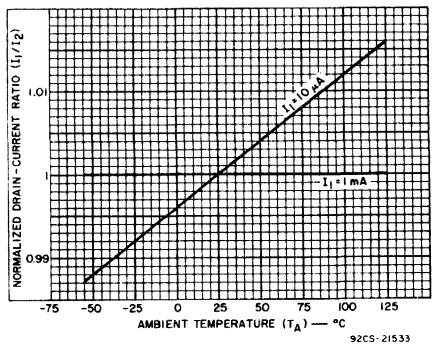


Fig. 31–Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 28).

CA3724G, CA3725G

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction High-Current N-P-N Transistors

The RCA-CA3724G and -CA3725G are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

These devices are alike except for breakdown voltage ratings.

The CA3724G and CA3725G are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C. The transistor chips used in these packages are of the sealed-junction type to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Applications:

- Core-Memory Driver
- High-Speed Switching
- High-Current LED Driver
- High-Voltage Switching
- Relay and Solenoid Driver
- Lamp Driver

Features:

- High Current – 1 A
- High Breakdown Voltage:
  CA3725G = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA3724G = 70 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
- Fast Switching Speeds:
  t_{on} = 30 ns typ. @ I_C = 500 mA
  t_{off} = 36 ns typ. @ I_C = 500 mA
- "Hermetic Chip" Construction
- Silicon Nitride Passivated
- Platinum Silicide Ohmic Contacts
- Gold Chip-Metallization
- Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages

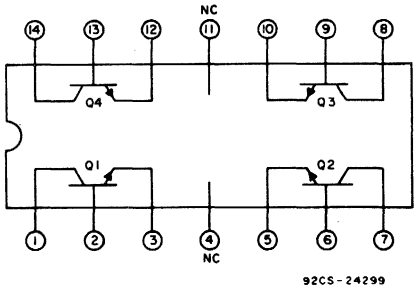


Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

		CA3724G	CA3725G	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6	6	V
COLLECTOR CURRENT	I_C	1.0	1.0	A
POWER DISSIPATION:	P_D			
At T_A up to 25°C:				
For Each Transistor		1.0	1.0	W
Total Package		2.0	2.0	W
At T_A above 25°C derate linearly		20		mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125	−55 to +125	°C
Storage		−65 to +150	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):				
At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300	300	°C

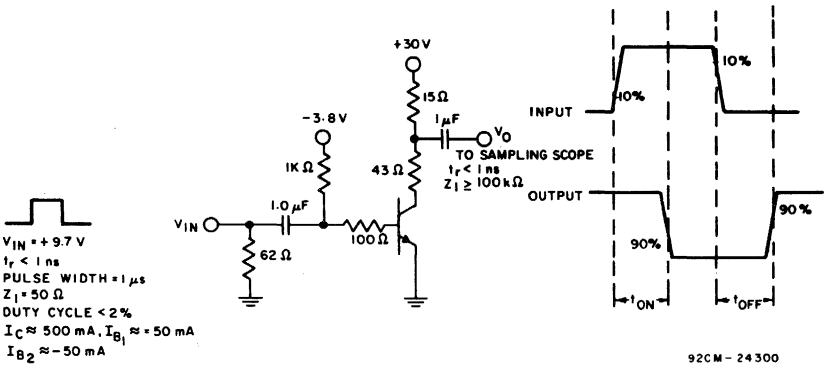


Fig. 2—Switching time test circuit.

CA3724G, CA3725G

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

Characteristic	Test Conditions	Limits						Units
		CA3724G			CA3725G			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*	I_C=10 mA, I_B=0	40	–	–	50	–	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C=10 μA, I_B=0	70	–	–	80	–	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C=10 μA, I_E=0	70	–	–	80	–	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E=10 μA, I_C=0	6	–	–	6	–	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*	I_C=500 mA, I_B=50 mA	0.75	–	1.0	0.75	–	1.0	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*	I_C=500 mA, I_B=50 mA	–	–	0.5	–	–	0.5	V
Collector-Cutoff Current, I_{CBO}	V_{CB}=40 V, I_E=0	–	–	1.7	–	–	1.7	μA
Static Forward-Current Transfer Ratio (Beta), h_{FE}	I_C=100 mA, V_{CE}=1.0 V	35	–	–	35	–	–	
	I_C=500 mA, V_{CE}=1.0 V	30	–	–	30	–	–	
	I_C=1 A, V_{CE}=1.0 V	20	–	–	20	–	–	
Small-Signal Forward-Current Transfer Ratio, h_{fe}	I_C=50 mA, V_{CE}=10 V, f=100 MHz	2.0	–	–	2.0	–	–	
Turn-On Time (See Test Ckt. Fig. 2), t_{on}	I_C=500 mA, I_{B1}=50 mA	–	–	40	–	–	40	ns
Turn-Off Time (See Test Ckt. Fig. 2), t_{off}	I_C=500 mA, I_{B1}= I_{B2}=50 mA	–	–	60	–	–	60	ns
Emitter-to-Base Capacitance, C_{eb}	I_C=0, V_{EB}=0.5 V	–	95	–	–	95	–	pF
Collector-to-Base Capacitance, C_{cb}	I_E=0, V_{CB}=10 V	–	12	–	–	12	–	pF

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

CA6078, CA6741 Types

Operational Amplifiers

CA6078AT – Micropower Type
CA6741T – General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

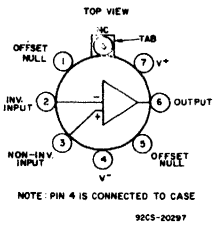
RCA-CA6078AT and CA6741T are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini–Dip) package.



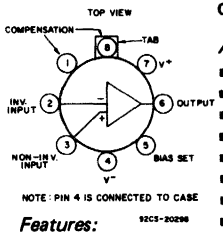
CA6741T

Applications:

- Low-noise AC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- DC amplifier
- Summing amplifier

Features:

- Internal phase compensation
- Input bias current: 500 nA max.
- Input offset current: 200 nA max.
- Open-loop voltage gain: 50,000 (94 dB) min.
- Input offset voltage: 5 mV max.



CA6078AT

Applications:

- Portable electronics
- Medical electronics
- DC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- Instrumentation
- Telemetry
- Summing amplifier

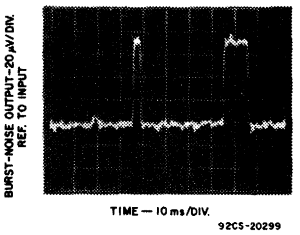
Features:

- Open-loop voltage gain: 40,000 (92 dB) min.
- Input offset voltage: 3.5 mV max.
- Operates with low total supply voltage: 1.5 V min. (± 0.75 V)
- Low quiescent operating current: adjustable for application optimization
- Input bias current: adjustable to below 1 nA

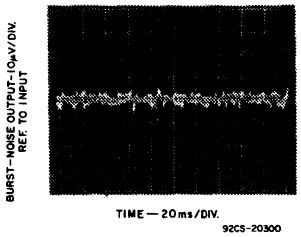
MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

	CA6741T	CA6078AT
DC Supply Voltage (between V+ and V− terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V+ to V−
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	–
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.
●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

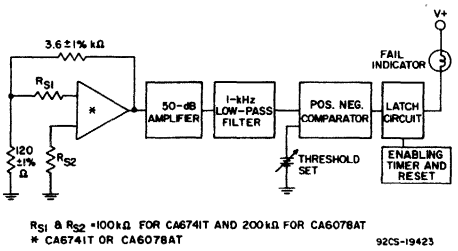


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

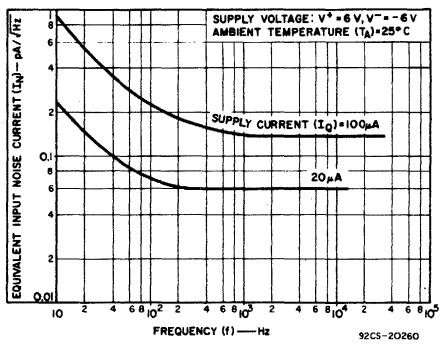


Fig.3—I_N vs. Frequency for CA6078AT.

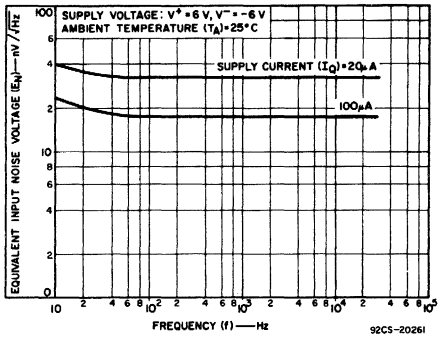


Fig.4—E_N vs. Frequency for CA6078AT.

CA6078, CA6741 Types

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz; $R_{S1} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + 1/f), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz; $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + 1/f), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\Omega$	±12	±14	–	V
		$R_L \geq 2\ k\Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

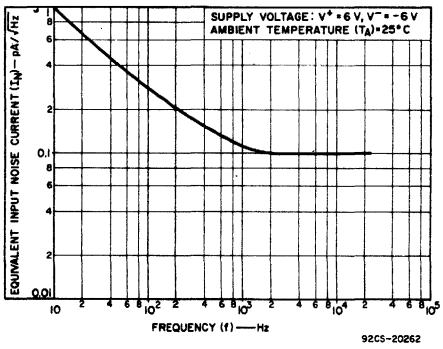


Fig.5–I_N vs. Frequency for CA6741T.

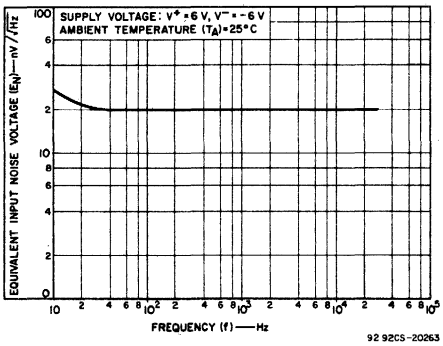


Fig.6–E_N vs. Frequency for CA6741T.

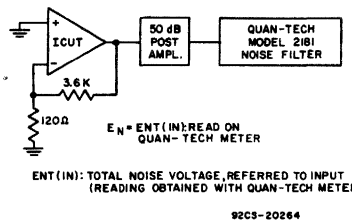


Fig.7–Test block diagram for E_N.

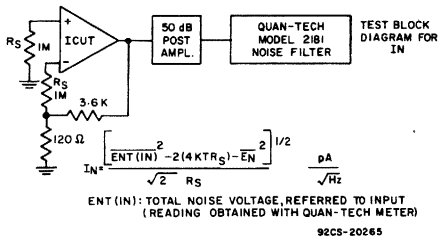


Fig.8–Test block diagram for I_N.

CD2500 Series

BCD to 7-Segment Decoder-Drivers 30mA and 80mA/Segment DECODER-DRIVERS For Use With Low-Voltage Digital Display Devices, Lamps, and Relays

RCA CD2500E series 7-Segment Decoder-Drivers are monolithic MSI integrated circuits which decode BCD (8-4-2-1 code) inputs to 7-line outputs representing a decimal number from 0 to 9 on 7-segment incandescent display devices.

RCA CD2500E and CD2501E are 30 mA per-output-line devices designed for use with incandescent display devices such as the RCA DR2000 and DR2010. The CD2500E, in addition to the outputs for the 7-segment display device, has a decimal point output; the CD2501E also has a special-feature, a terminal to provide for ripple blanking output and intensity control input. The ripple blanking output blanks out all non-significant zeroes in the numerical display. The ripple blanking output terminal is also available for use as an intensity control input from an external variable pulse-width control source, as shown in Fig. 7.

RCA CD2502E and CD2503E are 80 mA-per-line versions of the CD2500E and CD2501E, respectively, and are designed for use with high-current lamps and relays.

RCA CD2500E series devices are supplied in 16-lead dual in-line plastic packages which can be used over the operating temperature range of 0°C to +75°C.

FEATURES:

- High current sinking capability for direct display driving
- Intensity control provision
- BCD inputs are compatible with commercially available DTL & TTL devices
- Lamp test provision
- 5 V power supply
- Clamp diodes on all inputs
- Lamp supply up to +8 volts
- Ripple blanking capability
- Decimal point output
- Over-range detection (automatic blanking of display device when BCD input > 9)

DP_O - Decimal Point Output
DP_I - Decimal Point Input

DP_I must be supplied from an external source

CD2500E and CD2502E perform the inverter-driver function necessary to energize the decimal point filament in the display device.

Fig. 1 - CD2500E and CD2502E (with decimal point)

ABSOLUTE MAXIMUM RATINGS at 25°C unless otherwise specified:

Power Supply Voltage:

Continuous (0°C to +75°C)	−0.5 to +5.5 V
Pulsed (duration 1 second)	−0.5 to +8 V
Input Voltage	−0.5 to +5.5 V
Output Voltage (open collector transistor)	−0.5 to +8 V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

RB_O = Ripple-Blanking Output & Intensity Control Input
RB_I = Ripple-Blanking Input

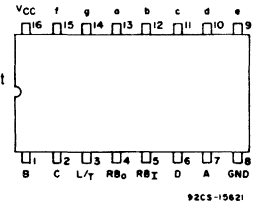
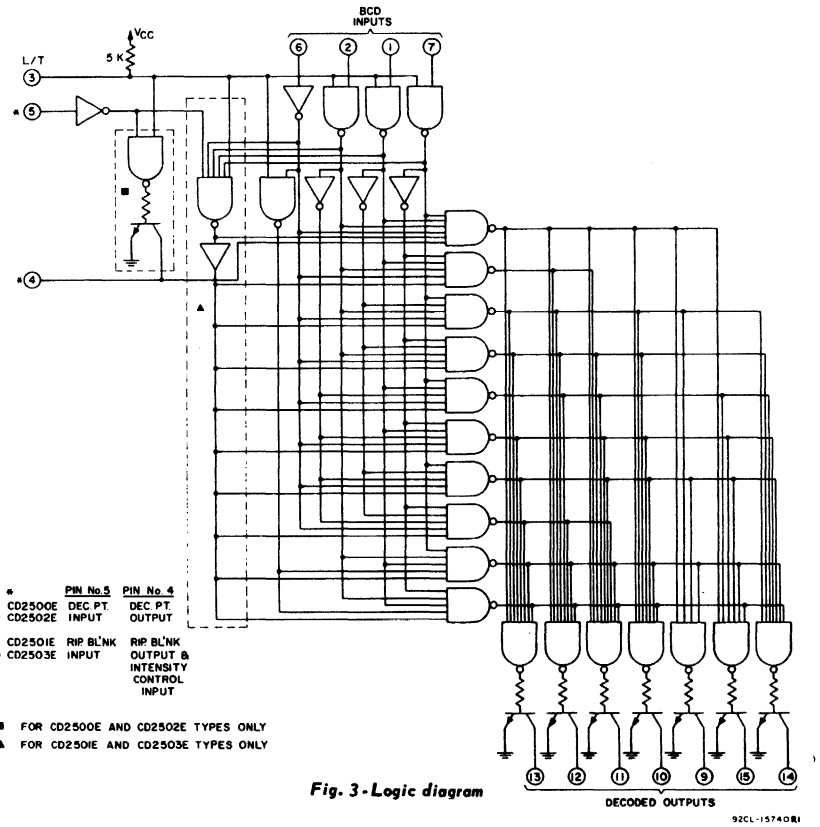


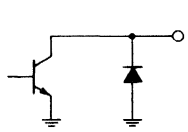
Fig. 2 - CD2501E and CD2503E (with ripple blanking and intensity control provision)



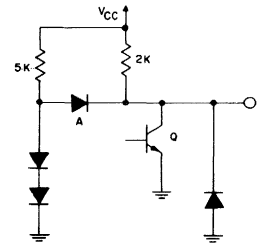
*	PIN No.5	PIN No. 4
CD2500E AND CD2502E	DEC. PT. INPUT	DEC. PT. OUTPUT
CD2501E AND CD2503E	RIP. BL'NK INPUT	RIP. BL'NK OUTPUT & INTENSITY CONTROL INPUT

■ FOR CD2500E AND CD2502E TYPES ONLY
▲ FOR CD2501E AND CD2503E TYPES ONLY

Fig. 3 - Logic diagram



For Terminals 9 through 15 and Terminal 4 of CD2500E and CD2502E only



For Terminal 4 of CD2501E and CD2503E.

Transistor Q is "turned on" when BCD code equals 0 and Terminal 5 is at "0 Level" (Grounded). When BCD code is between 0 and 9, transistor Q is "open". Diode A and transistor are "open" when BCD code is > 9.

Fig. 4 - Equivalent output circuits

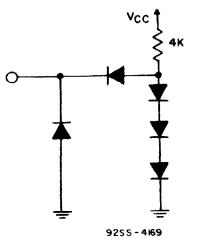


Fig. 5 - Equivalent input circuit for terminals 1, 2, 5, 6 & 7

CD2500 Series

ELECTRICAL CHARACTERISTICS at Ambient Temperature (T_A) Indicated

CHARACTERISTICS	SYMBOLS	MEASUREMENT TERMINALS	TEST CONDITIONS		0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS
Input High Voltage (Logic 1)	V_{IH}	1, 2, 5, 6, & 7	Input high threshold voltage		2.0	–	2.0	–	–	2.0	–	V
		3	V_{CC} = 4.75 V, I_{IH} = 0 Ground all other inputs		2.4	–	2.4	–	–	2.4	–	V
Input Low Voltage (Logic 0)	V_{IL}	1, 2, 5, 6, & 7	Input low threshold voltage		–	0.85	–	–	0.85	–	0.85	V
		3			–	0.45	–	–	0.45	–	0.45	
Input Forward Current	I_{IL}	1, 2, 5, 6, & 7	V_F = 0.45 V		–	– 1.6	–	– 1.0	– 1.6	–	– 1.6	mA
		3 { CD2501E, CD2503E		V_{CC} = 5.25 V	–	– 10.0	–	–	– 10.0	–	– 10.0	
		3 { CD2500E, CD2502E			–	– 10.4	–	–	– 10.4	–	– 10.4	
		1, 2, 5, 6, & 7	V_F = 0 Terminal 3 only		–	– 1.41	–	–	– 1.41	–	– 1.41	mA
		3 { CD2501E, CD2503E		V_{CC} = 4.75 V	–	– 9.0	–	–	– 9.0	–	– 9.0	
		3 { CD2500E, CD2502E			–	– 9.4	–	–	– 9.4	–	– 9.4	
Input Reverse Current	I_{IH}	1, 2, 5, 6, & 7	V_{CC} = 5.25 V Terminal 3 grounded	V_R = 4.5 V	–	40	–	–	40	–	60	μA
				V_R = 2.4 V	–	40	–	–	40	–	40	
Output Low Voltage	V_{OL}	9 thru 15 and 4 of { CD2500E, CD2501E, CD2500E	V_{CC} = 4.75 V, I_{OL} = 30 mA		–	0.40	–	0.30	0.40	–	0.40	V
		4 { CD2501E, CD2503E	V_{CC} = 5.25, I_{OL} = 3.2 mA		–	0.45	–	0.30	0.45	–	0.45	
			V_{CC} = 4.75, I_{OL} = 2.82 mA		–	0.45	–	0.30	0.45	–	0.45	
		9 thru 15 and 4 of { CD2502E, CD2503E, CD2502E	V_{CC} = 4.75 V, I_{OL} = 80 mA		–	1.0	–	0.60	1.0	–	1.0	
Output High Voltage	V_{OH}	9 thru 15 – All types and 4 of { CD2500E, CD2502E	V_{CC} = 5 V, I_{OH} = 200 μA		8.0	–	8.0	–	–	8.0	–	V
		4–CD2501E, CD2503E	V_{CC} = 4.75 V, I_{OH} = – 240 μA		2.4	–	2.4	–	–	2.4	–	
Input Capacitance	C_{IN}	1, 2, 5, 6, & 7	V_{CC} = 5.0 V		–	–	–	3	5	–	–	pF
Power Supply Current Drain (Terminal 16)	I_{CC_L}	CD2501E, CD2503E	V_{CC} = 5.0 V (Segment Output Currents = 0) Terminal 3 Grounded		–	–	–	48	–	–	–	mA
		CD2500E, CD2502E			–	–	–	50	–	–	–	

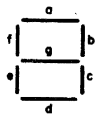
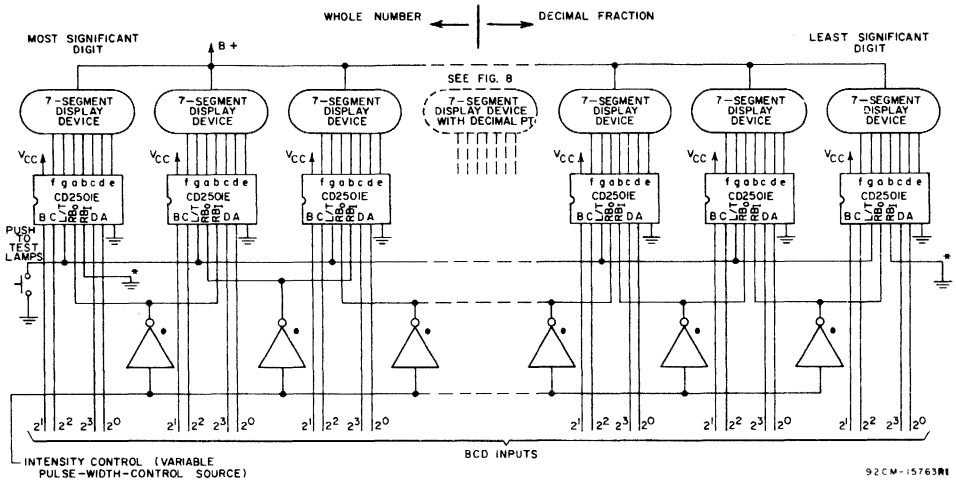


Fig. 6 - Digital display device segment designation



• Resistor pull-up output T^2L, DTL, or RTL inverter.

* Suppression of the non-significant zeroes (at both extremes of the display) is accomplished by grounding the RB_1 terminal of the devices associated with the most significant digit of the whole part of the number displayed and the least significant digit of the fractional portion of that number.

Fig. 7 - Typical ripple blanking and intensity control application diagram using RCA CD2501E and display devices DR2000 or equivalents (See Table A)

CD2500 Series

TRUTH TABLE

INPUT 0 = Low Level 1 = High Level							OUTPUT 0 = Filament Lit 1 = Filament OUT									TUBE DISPLAY
D	C	B	A	L/T	DP_I	RB_I	a	b	c	d	e	f	g	DP_O	RB_O	
X	X	X	X	0	–	X	0	0	0	0	0	0	0	–	1	8
0	0	0	0	1	–	0	1	1	1	1	1	1	1	–	0	
0	0	0	0	1	–	1	0	0	0	0	0	0	1	–	1	0
0	0	0	1	1	–	X	1	0	0	1	1	1	1	–	1	1
0	0	1	0	1	–	X	0	0	1	0	0	1	0	–	1	2
0	0	1	1	1	–	X	0	0	0	0	1	1	0	–	1	3
0	1	0	0	1	–	X	1	0	0	1	1	0	0	–	1	4
0	1	0	1	1	–	X	0	1	0	0	1	0	0	–	1	5
0	1	1	0	1	–	X	0	1	0	0	0	0	0	–	1	6
0	1	1	1	1	–	X	0	0	0	1	1	1	1	–	1	7
1	0	0	0	1	–	X	0	0	0	0	0	0	0	–	1	8
1	0	0	1	1	–	X	0	0	0	0	1	0	0	–	1	9
1	0	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	0	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	0	1	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	0	1	–	X	1	1	1	1	1	1	1	–	1	
1	1	1	1	1	–	X	1	1	1	1	1	1	1	–	1	
–	–	–	–	1	1	–	–	–	–	–	–	–	–	0	–	.
–	–	–	–	1	0	–	–	–	–	–	–	–	–	1	–	
–	–	–	–	0	X	–	–	–	–	–	–	–	–	0	–	.

X = Don't care (0 or 1 entry has no effect)
L/T = Lamp test
RB_I = Ripple Blanking Input
RB_O = Ripple Blanking Output
DP_I = Decimal Point Input
DP_O = Decimal Point Output

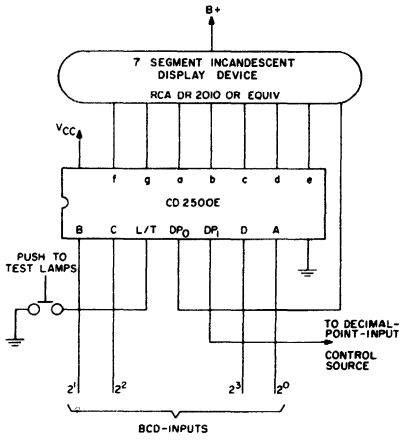


Fig. 8 - Typical decimal point feature application diagram using RCA CD2500E and RCA display device DR2010 (or equivalent)

TABLE A

DISPLAY DEVICE TYPE	TYPE OF DISPLAY	CHARACTERISTICS
DR2000		Required Driving Current = 24 ± 2 mA per segment
DR2010	X	0.6" Letter height

MOS Field-Effect (MOS/FET) Devices

		Industrial Types													Consumer Types																
		Single-Gate								Dual-Gate			Dual-Gate Protected			Single-Gate			Dual-Gate						Dual-Gate Protected						
		3N128	3N138	3N139	3N142	3N143	3N152	3N153	3N154	3N140	3N141	3N159	3N187	3N200	40819	40467A	40468A	40559A	40600	40601	40602	40603	40604	40673	3N211	3N212	3N213	40820	40821	40822	40823	40841
Page No.		322	324	325	329	322	330	331	332	326	326	333	334	338	350	345	346	346	347	347	347	348	348	349	341	341	341	351	351	353	353	354
Applications	RF Amplifier, Mixer	■			■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Chopper		■					■																								■
	General-Purpose Amplifier			■	■																■											■
	Oscillator	■		■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Features	Low-Noise						■					■	■	■											■	■						
	Low-Leakage		■					■		■	■	■							■	■	■	■	■									
	High-Gain						■			■		■	■	■											■	■	■					
	Gain-Controlled									■	■	■	■	■	■				■	■	■	■	■	■	■	■	■	■	■	■	■	■
	Premium-Performance						■					■	■	■																		

All MOS/FET devices are supplied in the JEDEC TO-72 package

3N128, 3N143

Silicon MOS Transistors N-Channel Depletion Types

For Amplifier, Mixer, & Oscillator Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

RCA-3N128 and 3N143 are N-channel depletion-type silicon insulated-gate field-effect transistors utilizing the MOS* construction. The 3N128 is intended primarily for VHF amplifier service in military and industrial applications. It also is extremely well suited for use in dc and low-frequency amplifier applications requiring a transistor having high power gain, very high input impedance, and low gate leakage.

The 3N143 is designed for use as a VHF mixer and oscillator. Because of their improved transfer characteristic and increased dynamic range the 3N128 and 3N143 provide substantially better cross-modulation performance in linear amplifier applications than conventional (bipolar) transistors and are free from diode-current loading common to junction type FET's. These transistors are hermetically sealed in JEDEC TO-72 metal packages.

Maximum Ratings, *Absolute-Maximum Values at* T_A = 25° C:

*DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . +20 V
*DRAIN-TO-GATE VOLTAGE, V_{DG} . . . . . +20 V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:
Continuous dc . . . . . +1, -8 V
Peak ac . . . . . ±15 V
*DRAIN CURRENT, I_D . . . . . 50 mA
*TRANSISTOR DISSIPATION, P_T:
At Ambient up to 25°C . . . . . 330 mW
Temperatures above 25° . . . . . Derate 2.2 mW/°C
*AMBIENT TEMPERATURE RANGE:
Storage and Operating . . . . . -65 to +175°C
*LEAD TEMPERATURE (During soldering):
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum . . . . . 265 °C

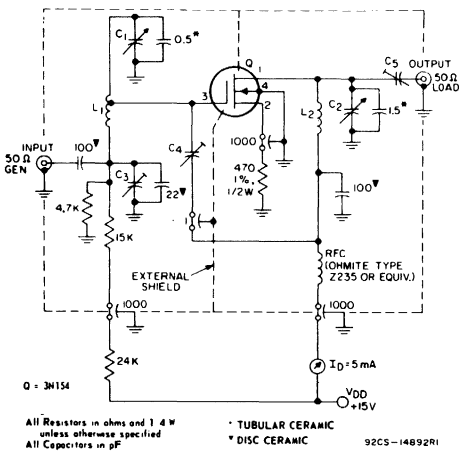
*In accordance with Jedec Registration Data Format JS9-RDF11B.

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS 3N128 MIN.	3N128 TYP.	3N128 MAX.	3N143 MIN.	3N143 TYP.	3N143 MAX.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V T_A = 25°C	–	0.1	50	–	0.1	1000	pA
			V_{DS} = 0, V_{GS} = -8 V T_A = 125°C	–	–	5	–	–	200	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	5	15	30	mA
*	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	–	–	50	–	–	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5,000	7,500	12,000	5,000	7,500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	–	200	–	–	200	–	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	0.12	0.25	0.38	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	5.5	7	–	5.5	7	pF
			Common-Source Configuration							
*	Input Admittance	Y_{is}	f = 200 MHz	–	0.4 + J7.3	–	–	–	–	mmho
*	Forward Transfer Admittance	Y_{ss}	V_{os} = 15 Volts	–	7 - J2	–	–	–	–	mmho
*	Output Admittance	Y_{os}	I_D = 5 mA	–	0.28 + J1.8	–	–	–	–	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz		21	–	–	–	–	dB
*	Insertion Power Gain (Fixed Neutralization) See Fig. 1	G_{PS}		13.5	16	–	–	–	–	dB
	Power Gain (Conversion (See Fig. 3)	$G_{PS(c)}$	V_{DS} = 15 V, I_D = 1 mA, f_{in} = 200 MHz, f_{out} = 30 MHz	–	–	–	10	13.5	–	dB
	Noise Figure (See Fig. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	3.5	5	–	–	–	–

*Inaccordance with **JEDEC** Registration Data Format JS9-RDF-11B.
▲Three-Terminal Measurement: Source Returned to Guard Terminal.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure for 3N128

Performance Features

- Large dynamic range
- Greatly reduces spurious responses in rceiver front ends
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior crossmodulation capability

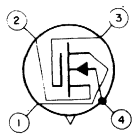
Device Features

- Low noise figure (3N128) – 3.5 dB typ. at 200 MHz
- High VHF amplifier gain (3N128) – 16 dB typ. at 200 MHz
- Low input capacitance – 5.5 pF typ.
- High transconductance – 7500 μmho typ.
- High input resistance – 10^{14} Ω typ.
- High conversion gain (3N143, mixer) – 13.5 dB typ. at 200 MHz

Applications

- VHF amplifiers, mixers, converters and if-amplifiers in communication receivers.
- High-impedance timing circuits
- Detectors, oscillators, frequency multipliers, phase splitters, pulse stretchers and current limiters
- Electrometer amplifiers
- Voltage-controlled attenuators
- High impedance differential amplifiers

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

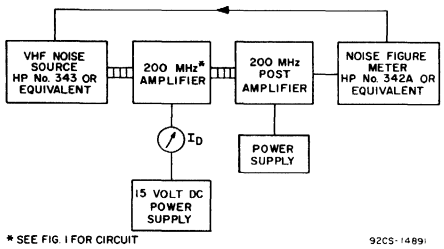
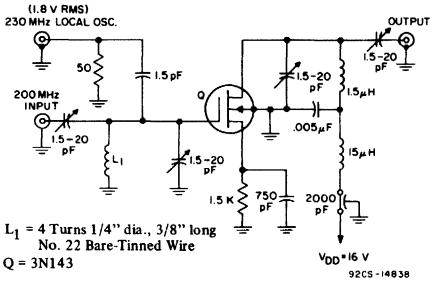


Fig. 2 - Noise figure measurement setup for 3N128



L_1 = 4 Turns 1/4" dia., 3/8" long No. 22 Bare-Tinned Wire
Q = 3N143

Fig. 3 - Conversion power gain test circuit for 3N143

3N128, 3N143

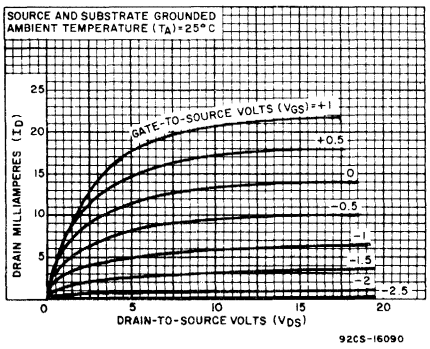


Fig. 4 - Drain current vs. drain-to-source voltage

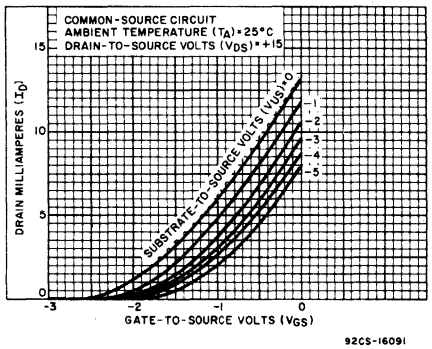


Fig. 5 - Drain current vs. gate-to-source voltage (V_{GS})

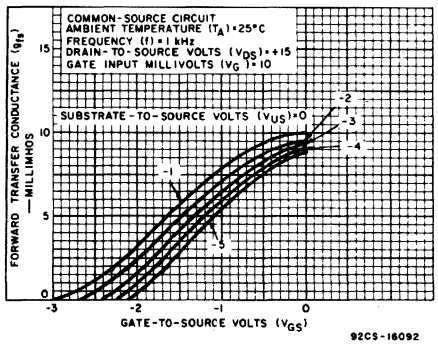


Fig. 6 - Forward transconductance vs. gate bias voltage

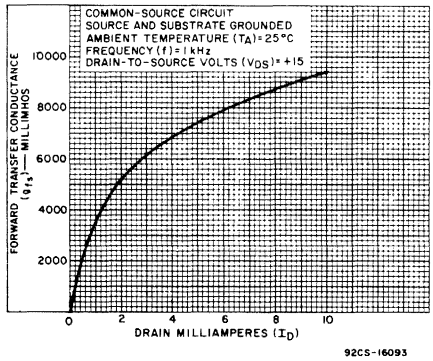


Fig. 7 - Forward transconductance vs. drain current

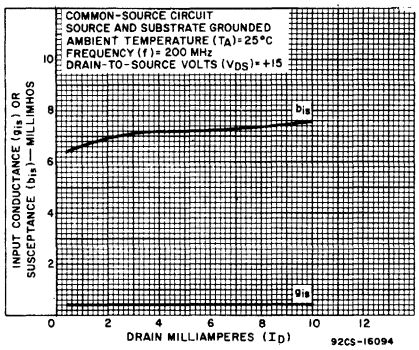


Fig. 8 - Input admittance vs. drain current

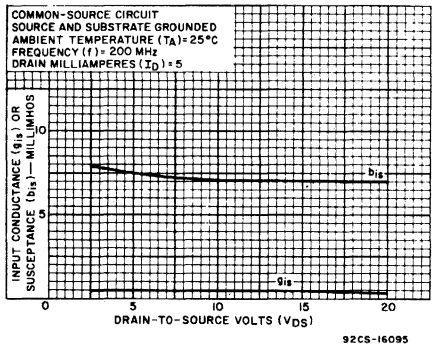


Fig. 9 - Input admittance vs. drain-to-source voltage

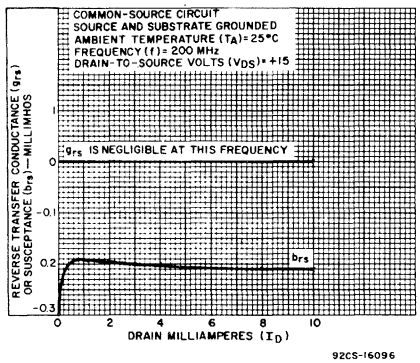


Fig. 10 - Reverse transadmittance vs. drain current

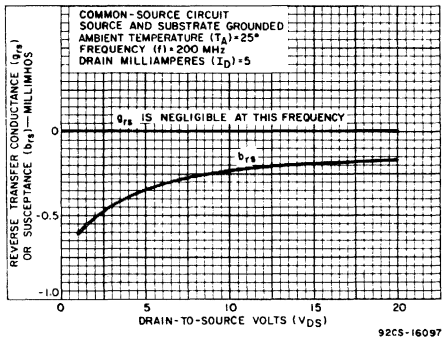


Fig. 11 - Reverse transadmittance vs. drain-to-source voltage

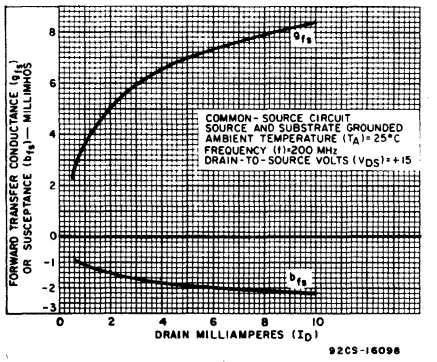


Fig. 12 - Forward transadmittance vs. drain current

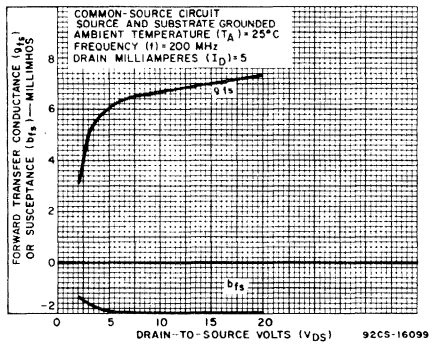


Fig. 13 - Forward transadmittance vs. drain-to-source voltage

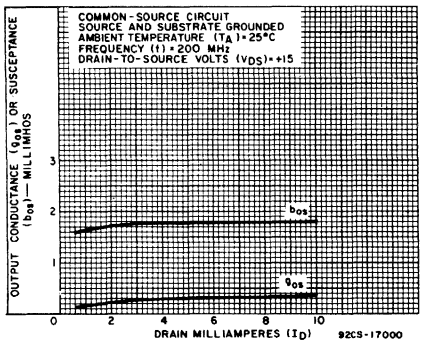


Fig. 14 - Output admittance vs. drain current

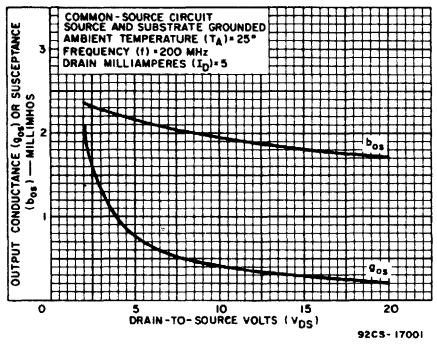


Fig. 15 - Output admittance vs. drain-to-source voltage

3N138

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

For Critical Chopper Applications and Multiplex Service in Instrumentation and Control Circuits

RCA-3N138 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60MHz.

The insulated gate provides a very high value of input resistance (10^{14} ohms typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N138 also features extremely low feed-through capacitance (0.18pF typ.) and zero inherent offset voltage.

The 3N138 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

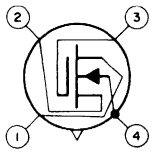
* Metal-Oxide-Semiconductor.

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, −0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, −0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS: V_{GS}, V_{GD}, V_{GB}, non-repetitive	±45 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T: At ambient temperatures up to 25°C	330 max.	mW
above 25°C	Derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE: Storage	−65 to +150	°C
Operating	−65 to +125	°C
LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32" to seating surface for 10 seconds max.	265 max.	°C

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

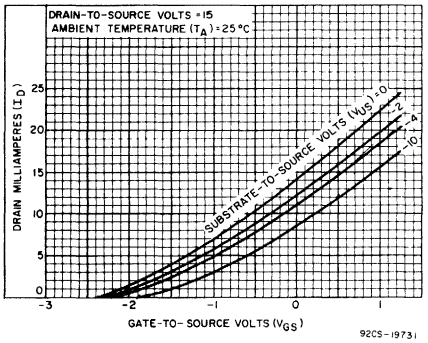


Fig. 1 – Drain Current vs Gate-to-Source Voltage

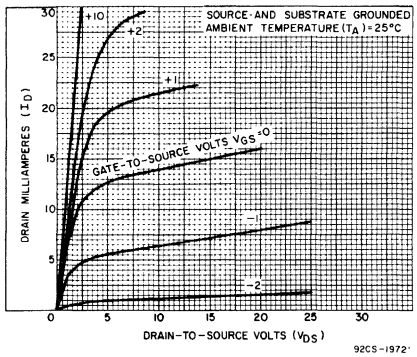


Fig. 2 – Drain Current vs Drain Voltage

Features

- excellent thermal stability
- zero inherent offset voltage
- low leakage current: 10 pA max.
- low "on" resistance — $r_{DS}(on)$ = 240Ω typ. (V_{GS} = 0V)
- high "off" resistance — $R_{DS}(off)$ = 10^{10}Ω typ.
- low feedback capacitance — C_{rss} = 0.18pF typ.
- low input capacitance — C_{iss} = 3pF typ.

Applications

- Servo Amplifiers
- Telemetry Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

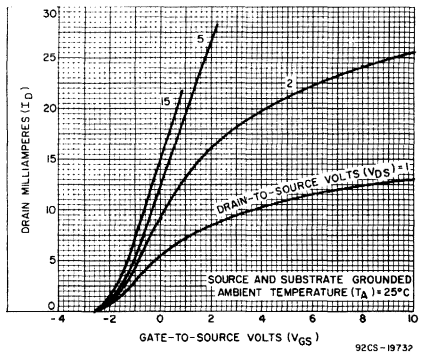


Fig. 3 – Drain Current vs Gate-to-Source Voltage

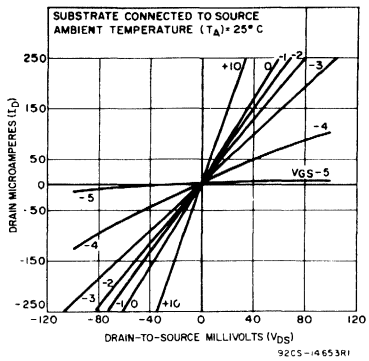


Fig. 4 – Low-Level Drain Current vs Drain-to-Source Voltage

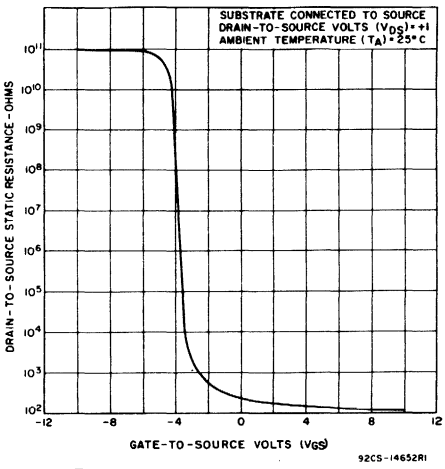


Fig. 5 – Drain-to-Source Static Resistance vs Gate-to-Source Voltage

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N138 Min.	Typ.	Max.	UNITS
Gate-Leakage Current	I_{GSS}	V_{GS} = ±10, V_{DS} = 0, T_A = 25°C	—	0.1	10	pA
		V_{GS} = ±10, V_{DS} = 0, T_A = 125°C	—	20	200	pA
Drain-to-Source "ON" Resistance	$r_{DS}(on)$	V_{GS} = 0, V_{DS} = 0, f = 1 KHz, T_A = 25°C	—	240	350	Ω
		V_{GS} = +10, V_{DS} = 0, f = 1 KHz, T_A = 25°C	—	135	—	Ω
		V_{GS} = 0, V_{DS} = 0, f = 1 KHz, T_A = 125°C	—	350	—	Ω
Drain-to-Source "OFF" Resistance	$R_{DS}(off)$	V_{GS} = −10, V_{DS} = +1	2×10^8	10^{10}	—	Ω
Drain-to-Source Cutoff Current	$I_D(off)$	V_{GS} = −10, V_{DS} = +1, T_A = 25°C	—	0.01	5	nA
		V_{GS} = −10, V_{DS} = +1, T_A = 125°C	—	0.01	0.5	μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = −10, V_{DS} = 0, f = 1 MHz	—	0.25	0.4	pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = −10, V_{DS} = 0, f = 1 MHz	—	3	5	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{DS} = 12, I_D = 5 mA	—	6000	—	μmho
Offset Voltage	V_O	V_{GS} = ±10, V_{DS} = 0	—	0*	—	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. There errors may be minimized by the use of solder having a low thermal e.m.f. such as Leeds & Northrup No.107-1.0.1, or equivalent.

3N139

SILICON MOS TRANSISTOR

N-Channel Depletion Type

For Audio, Video, and RF Amplifier Applications in Communications, Instrumentation and Control Circuits

RCA 3N139 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is a general purpose transistor especially suited for audio, video, and rf applications, and for wide-band amplifier designs. The insulated gate provides a very high input resistance (10^{14} Ω typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N139 also has a high transconductance, a low value of input capacitance (3 pF typ.), and a very low feedback capacitance (0.19 pF typ.).

The 3N139 is hermetically sealed in the standard 4-lead JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values:*

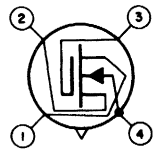
DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, -0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, -0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS; V_{GS}, V_{GD}, V_{GB}, non-repetitive	±42 max.	V
DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	Derate linearly at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distance not closer than 1/32 inch to seating surface for 10 seconds max.	265 max.	°C

* Metal-Oxide-Semiconductor

FEATURES

- high input resistance $R_{GS} = 10^{14}$ Ω typ.
- low input capacitance $C_{iss} = 3$ pF typ.
- low feed back capacitance $C_{rss} = 0.2$ pF typ.
- low gate leakage current $I_{GSS} = 0.1$ nA typ.
- high drain-to-source voltage: +35 max. V

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D				
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_{D(OFF)}$		15	−8		—	—	50	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	15	25	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	±10		—	—	1	nA
		T_A = 100°C	0	±10		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS(OFF)}$		15		0.05	−2	−4	−6	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	0.05	0.2	0.4	pF
Input Resistance	r_{is}	100	15		5		12	—	kΩ
Input Capacitance	C_{iss}	100	15		5	—	3	10	pF
Output Resistance	r_{os}	100	15		5		6	—	kΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	1 kHz	15		5		5	—	mmho

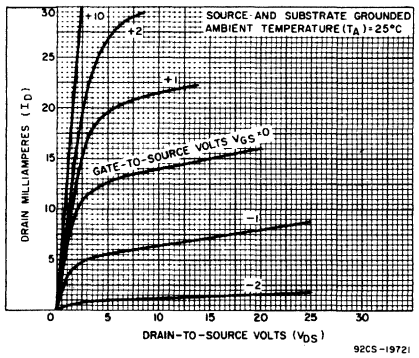


Fig. 1 — Drain Current vs Drain Voltage

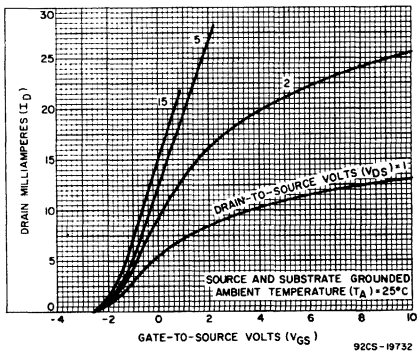


Fig. 2 — Drain Current vs Gate-to-Source Voltage

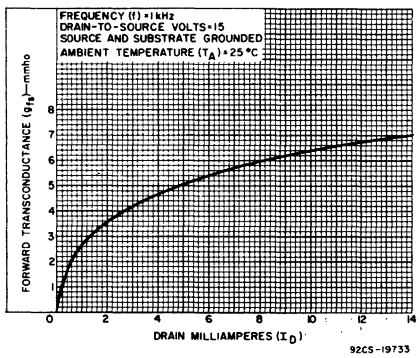


Fig. 3 — 1 KHz forward transconductance vs drain current

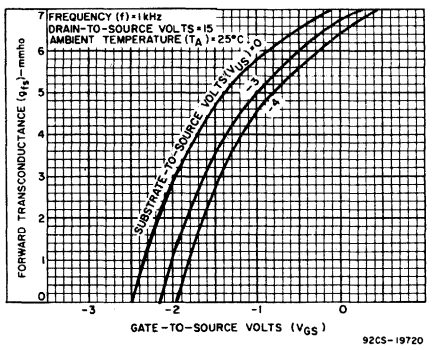


Fig. 4 — 1 KHz forward transconductance vs gate-to-source voltage

3N140, 3N141

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types

For Amplifier and Mixer Applications Up to 300 MHz

RCA-3N140 and 3N141* are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS** construction. They have exceptional characteristics for rf-amplifier and mixer applications at frequencies up to 300 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate.

The 3N140, used in a common-source configuration in which gate No.2 is ac grounded, reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation. The 3N141 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element.

The mixing function performed by the 3N141 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the nonlinear region of the device transfer characteristic.

The use of the 3N141 as described provides high useful conversion gains at all vhf frequencies, and the reduction in spurious responses is substantial and easily obtainable in simple circuits.

Maximum Ratings, *Absolute-Maximum Values, at* $T_A = 25^oC$

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed): Pulse duration ≤ 20 ms, duty factor ≤ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

The 3N140 and 3N141 are hermetically sealed in metal JEDEC TO-72 packages.

* Formerly Dev. Nos. TA2644 and TA7274, respectively.

** Metal-Oxide-Semiconductor.

APPLICATIONS

- RF amplifier and mixer in military and industrial communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's

DEVICE FEATURES

- low gate leakage currents - - I_{G1SS} & I_{G2SS} = 1 nA max. at T_A = 25°C
- high forward transconductance - - g_{fs} = 6000 μmho min.
- high unneutralized RF power gain - - G_{ps} = 16 dB min. at 200 MHz
- low VHF noise figure - - 4.5 dB max. at 200 MHz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C Unless Otherwise Specified. Common-Source Circuit.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS
			TYPE 3N140 RF AMPLIFIER			TYPE 3N141 MIXER			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S}(off)$	V_{DS} = +16V, I_D = 200 μA, V_{G2S} = +4V	-	-2	-4	-	-2	-4	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S}(off)$	V_{DS} = +16V, I_D = 200 μA, V_{G1S} = 0	-	-2	-4	-	-2	-4	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	-	-	0.2	μA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G2S} = +1V, V_{DS} = 0, V_{G1S} = 0, T_A = 25°C	-	-	1	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0, V_{G2S} = +4	5	18	30	5	18	30	mA
Forward Transconductance (Gate No.1 to Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA, V_{G2S} = +4V, f = 1 kHz	6000	10000	18000	6000	10000	18000	μmho
Cutoff Forward Transconductance (Gate No.1 to Drain)	$g_{fs}(off)$	V_{DD} = +14V, V_{G1S} = -0.5V, V_{G2S} = -2V, f = 1 kHz	-	-	100	-	-	-	μmho
Small-Signal, Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	3	5.5	7	3	5.5	7	pF
Small-Signal, Short-Circuit Reverse Transfer Capacitance (Drain to Gate No.1)▲	C_{rss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	0.01	0.02	0.03	pF
Small-Signal Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	-	2.2	-	-	2.2	-	pF
Power Gain (See Fig.1 for Measurement Circuit)	G_{ps}	V_{DD} = +15V, R_S = 270Ω, f = 200 MHz, R_G = 50Ω	16	18	-	-	-	-	dB
Conversion Power Gain (See Fig.2 for Measurement Circuit)	G_{psc}	V_{DD} = +15V, R_S = 120Ω, f_{IN} = 200 MHz, f_{OUT} = 30 MHz, Oscillator injection voltage● = 2.5 V (rms)	-	-	-	13	17	-	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω, f = 200 MHz, R_G = 50Ω	-	3.5	4.5	-	-	-	dB

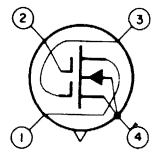
* Pusle test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.

▲ Capacitance between Gate No.1 and all other terminals.

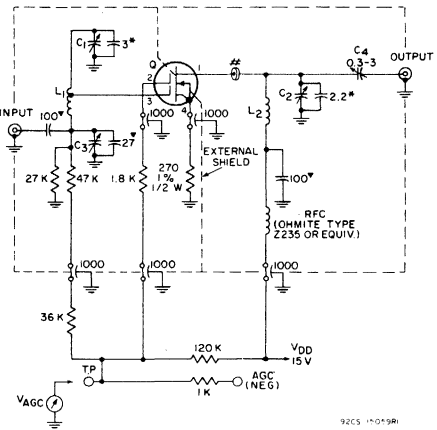
▲ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

● Measured from gate No.2 to source.

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE



Q = 3N140.

▼ Disc ceramic. All resistors in ohms

* Tubular ceramic. All capacitors in pF

Ferrite bead (1/2 used); Indiana General No.H1742C-(A-147), F-1157-1-H

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

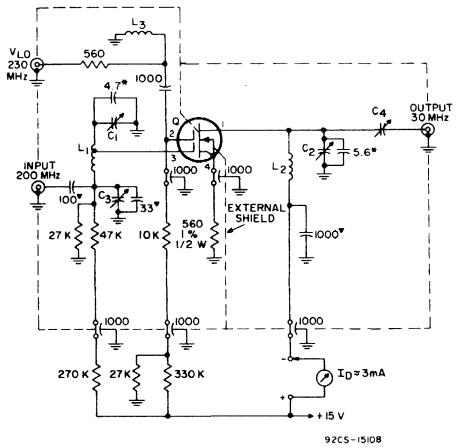
C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"±0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz power gain and noise figure test circuit for type 3N140.

3N140, 3N141



Q = 3N141.

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-144 RF choke or equivalent.

L_3: J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.2 - Conversion power gain test circuit for type 3N141.

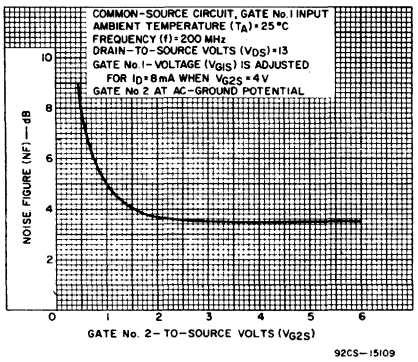


Fig.3 - NF vs V_{G2S}.

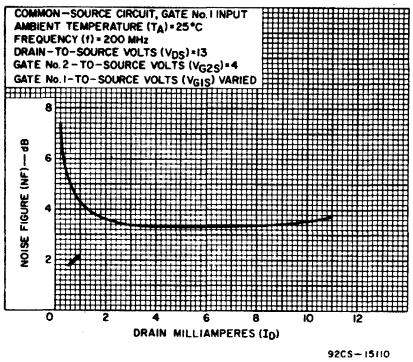


Fig.4 - NF vs I_D.

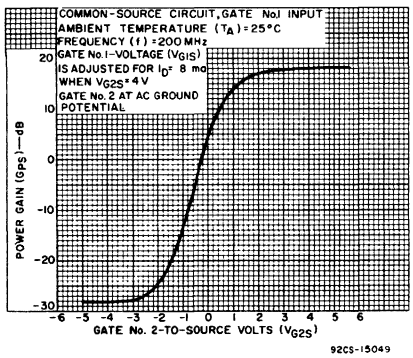


Fig.5 - G_{PS} vs V_{G2S} (For 3N140).

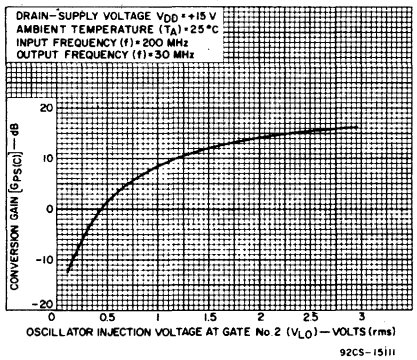


Fig.6 - $G_{PS(C)}$ vs V_{LO} (For 3N141).

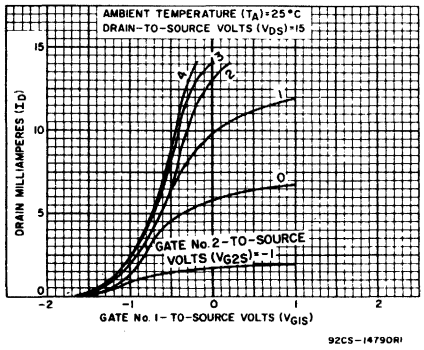


Fig.7 - I_D vs V_{G1S}.

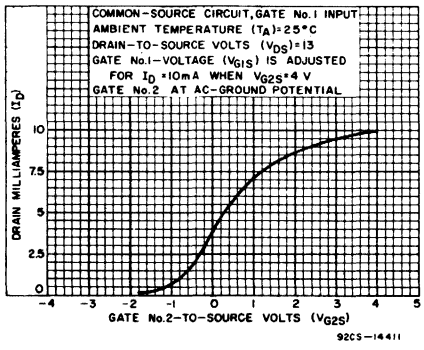


Fig.8 - I_D vs V_{G2S}.

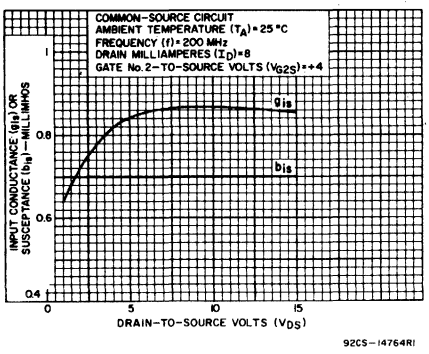


Fig.9 - y_{is} vs V_{DS}.

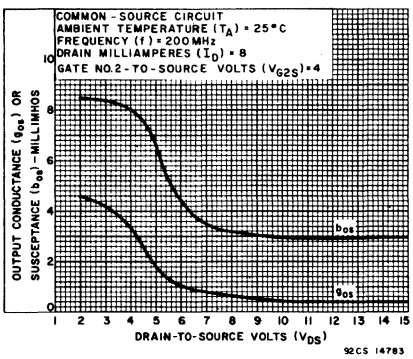


Fig.10 - y_{os} vs V_{DS}.

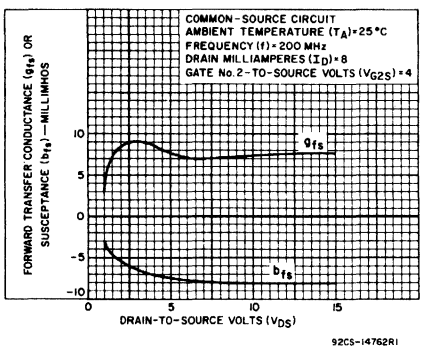


Fig.11 - y_{fs} vs V_{DS}.

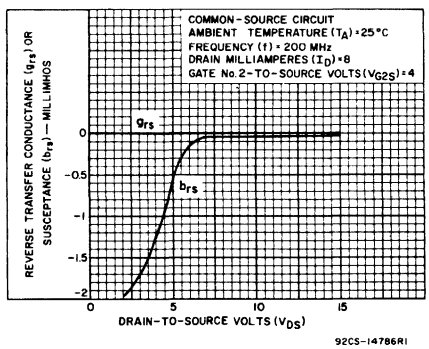


Fig.12 - y_{rs} vs V_{DS}.

3N140, 3N141

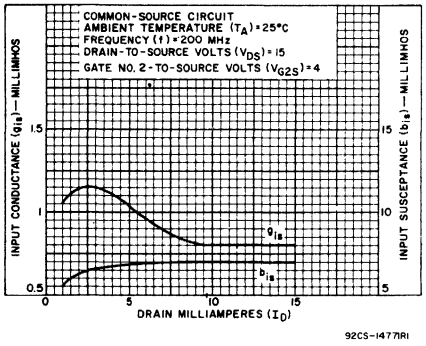


Fig.13 - y_{is} vs I_D.

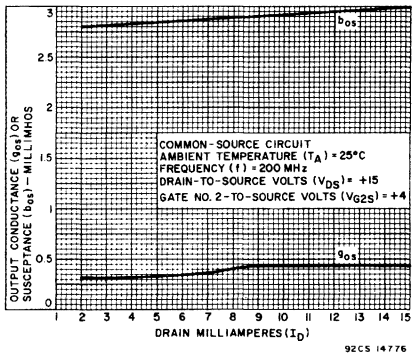


Fig.14 - y_{os} vs I_D.

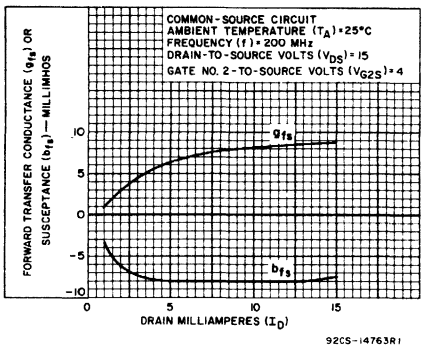


Fig.15 - y_{fs} vs I_D.

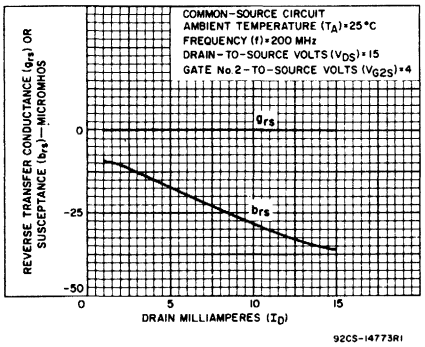


Fig.16 - y_{rs} vs I_D.

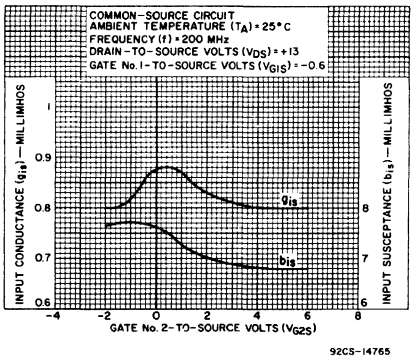


Fig.17 - y_{is} vs V_{G2S}.

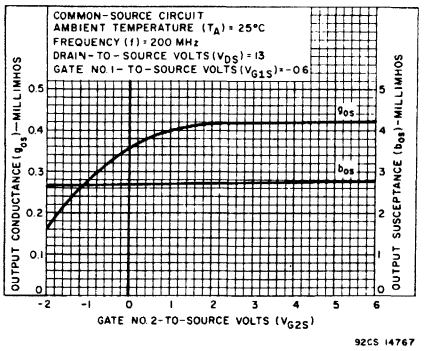


Fig.18 - y_{os} vs V_{G2S}.

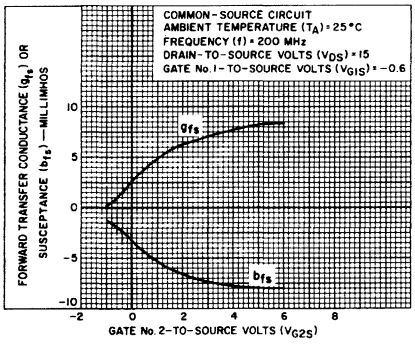


Fig.19 - y_{fs} vs V_{G2S}.

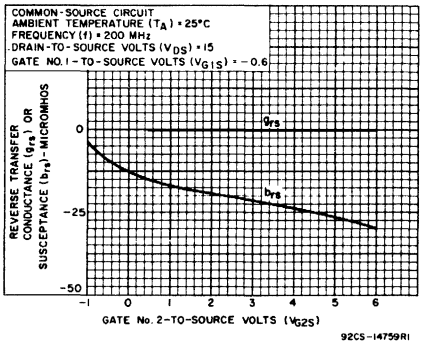


Fig.20 - y_{rs} vs V_{G2S}.

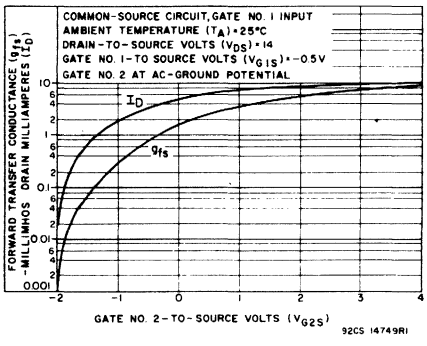


Fig.21 - g_{fs} and I_D vs V_{G2S}.

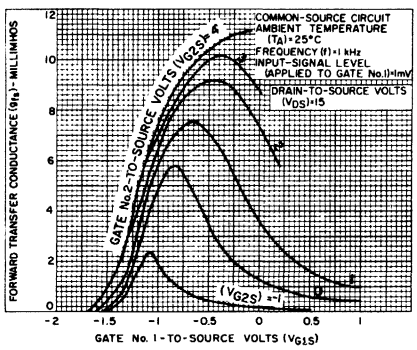


Fig.22 - g_{fs} vs V_{G1S}.

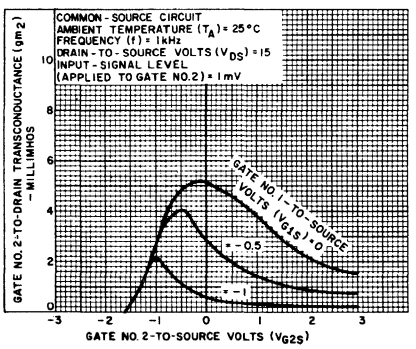


Fig.23 - g_{fs2} vs V_{G2S}.

3N142

Silicon MOS Transistor N-Channel Depletion Type

For Industrial and Military Applications to 175 MHz

The 3N142 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS■ construction.

The 3N142 is intended primarily for use as the rf amplifier in FM receivers and general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

■ Metal-Oxide-Semiconductor

Applications

- **RF amplifier, Mixer, and Oscillator in:**
  - **CB and Mobile Communication Receivers**
  - **Aircraft and Marine Receivers**
  - **CATV and MATV Equipment**
- **Industrial Control Circuits**
- **Variable Attenuators**
- **Current Limiters**
- **Instrumentation Equipment**
- **High-Impedance Timing Circuits**

Maximum Ratings, Absolute-Maximum Values at $T_A = 25^\circ C$

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	+1 to −8	V
Peak ac	±15	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	Derate at 2.2 mW/°C	
*AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +175	°C
Operating	−65 to +175	°C
*LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

* In accordance with JEDEC Registration Data Format JS-9 RDF11-B

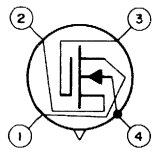
Performance Features

- **Large dynamic range**
- **Enhanced signal-handling capability for low cross-modulation**
- **Dual-polarity gate permits positive and negative swing without degradation of input impedance**
- **Reduced spurious responses in FM receivers**
- **Permits use of vacuum-tube biasing techniques**
- **Excellent thermal stability for critical oscillator designs**

Device Features

- **High input resistance - 1000 megohms**
- **Low feedback capacitance - 0.35 pF max.**
- **Low noise figure - 2.5 dB typ.**
- **High useful power gain - neutralized - 16 dB min. at 100 MHz**
- **Hermetically sealed TO - 72 metal package**

TERMINAL DIAGRAM



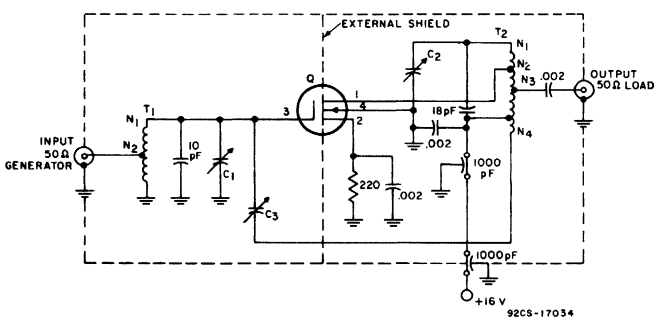
LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

ELECTRICAL CHARACTERISTICS: (At $T_A = 25^\circ C$)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C	-	-	200	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	200	nA
*	Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	mA
*	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance‡	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.10	0.22	0.35	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
*	Input Admittance	Y_{is}	Common Source Configuration f = 100 MHz V_{DS} = 15V I_D = 5 mA	-	0.155+J3.45	-	mmho
*	Forward Transfer Admittance	Y_{fs}		-	7.5-J0.9	-	mmho
*	Output Admittance	Y_{os}		-	0.21+J0.9	-	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	26	-	dB
	Maximum Usable Power Gain (Fixed Neutralization)	MUG		-	17	-	
*	Insertion Power Gain** (Fixed Neutralization)	G_{ps}		16	-	-	dB
*	Noise Figure**	NF	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	2.5	4	dB

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B ‡ Three-Terminal Measurement: Source Returned to Guard Terminal
**See Fig. 1



T_1 N_1 = 6 Turns #20 Tinned Copper Wire; ¼" I.D. ½" Long
Q_o = 205, N_1/N_2 = 4.85

T_2 $N_1 + N_4$ = 6¾ Turns #20 Tinned Copper Wire ¼" I.D. $^{9}/_{16}$" Long
Q_o = 190 N_1/N_2 = 1.9 N_1/N_3 = 12.3 N_1/N_4 = 8

C_1 = 10 pF Variable Air Capacitor (Hammarlund Mac-10 or Equivalent)
C_2 = 5 pF Variable Air Capacitor (Hammarlund Mac-5 or Equivalent)
C_3 = 0.7-3 pF Piston-Type Variable Air Capacitor (Erie 535C or Equivalent)
Q = 3N142

Fig. 1 - Test Set Up for 100 MHz Insertion Power Gain and Noise Figure

For characteristics curves, refer to types 3N128 and 3N143.

3N152

Silicon MOS Transistor N-Channel Depletion Type

For Low-Noise RF Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

RCA-3N152 is an N-channel depletion-type silicon insulated gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for VHF amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N152 with the substrate in the reversed bias mode can provide substantially better cross-modulation performance in linear amplifier applications than conventional bipolar transistors. The insulated gate with its extremely low reverse (leakage) current eliminates the problem of diode-current loading of the input circuit under strong input conditions, which is common to junction-type FET's. These features in addition to low feedback capacitance permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N152 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

* DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
* DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
* GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8 max.	V
* PEAK ac	±15 max.	V
* DRAIN CURRENT, I_D	50 max.	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures: up to 25°C	330 max.	mW
above 25°C	derate at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265 max.	°C

* In accordance with Jedec Registration Data Format JS-9 RDF 11-B.

Features

- Low gate leakage current — I_{GSS} = 0.1 pA typ.
- Low feedback capacitance — C_{rss} = 0.25 pF typ.
- High forward transconductance — g_{fs} = 7500 μmho typ.
- High vhf power gain — G_{PS} = 16 dB typ. at 200 MHz
- Low vhf noise figure — NF = 2.5 dB typ. at 200 MHz
- Exceptionally good cross-modulation characteristics

Performance

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

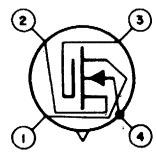
Measured with Substrate Connected to Source Unless Otherwise Specified

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N152 Min.	Typ.	Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8V, T_A = 25°C	·	0.0001	1	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125°C	·	·	200	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	30	mA
	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8V.	·	·	50	μA
*	Gate-to-Source-Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	·	200	·	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance▲	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	·	5.5	7	pF
	Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz	·	0.4 + J7.3	·	mmho
	Forward Transfer Admittance	Y_{fs}	V_{DS} = 15 V,	·	7-J2	·	mmho
	Output Admittance	Y_{os}	I_D = 5 mA	·	0.28 + J1.8	·	mmho
	Power Gain Maximum Available Gain	MAG		·	21	·	dB
	Insertion Power Gain (Fixed Neutralization) See Fig.1	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	14.5	16	·	dB
	Noise Figure (See Figs. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	·	2.5	3.5	dB

▲ Three-Terminal Measurement. Source Returned to Guard Terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B.

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

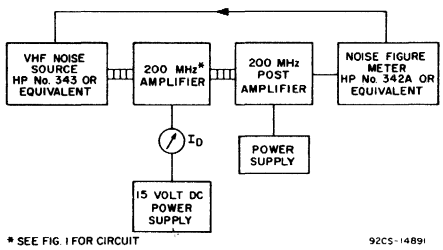
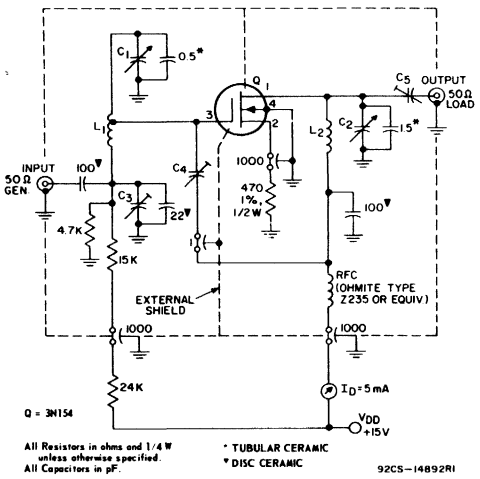


Fig. 2 - Noise figure measurement setup.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise Figure.

For characteristics curves, refer to types 3N128 and 3N143.

3N153

SILICON INSULATED GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

RCA 3N153 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60 MHz.

The insulated gate provides a very high value of input resistance (10^{10} ohms typ) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N153 also features extremely low feedback capacitance (0.34 pF typ) and virtually zero inherent offset voltage.

This transistor features a Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

* Metal-Oxide-Semiconductor

Maximum Ratings, *Absolute-Maximum Values:*

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, -0.3	max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, -0.3	max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	+6, -8	max.	V
PEAK GATE-TO-SOURCE VOLTAGE, v_{GS}	±14	max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50	max.	mA
TRANSISTOR DISSIPATION, P_T:			
At ambient temperatures from -65 to +25°C	400	max.	mW
above 25°C	derate linearly at 2.67		mW/°C
AMBIENT TEMPERATURE RANGE:			
Storage	-65 to +175		°C
Operating	-65 to +175		°C
LEAD TEMPERATURE (During soldering):			
At distance $\geq 1/32$" to seating surface for 10 seconds max.	265	max.	°C

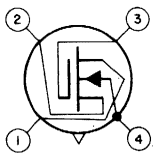
FEATURES

- excellent thermal stability
- virtually zero inherent offset voltage
- low leakage current: 50 pA max.
- low "on" resistance — $r_{DS(on)}$ = 200 Ω typ.
- high "off" resistance — $R_{DS(off)}$ = 10^{10} Ω typ.
- low feedback capacitance — C_{rss} = 0.34 pF typ.
- low input capacitance — C_{iss} = 6 pF typ.

APPLICATIONS

- Choppers
- Multiplexers
- Servo Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153 Min.	Typ.	Max.	UNITS
Gate-Leakage Current	I_{GSS}	V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 25°C V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS(on)}$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS(off)}$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{GS} = -8V, V_{DS} = +1V, T_A = 25°C V_{GS} = -8V, V_{DS} = +1V, T_A = 125°C	- -	0.1 0.1	1 1	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz V_{DS} = 15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.25	0.5 0.38	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	μmho
Offset Voltage	V_O	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0.1, or equivalent.

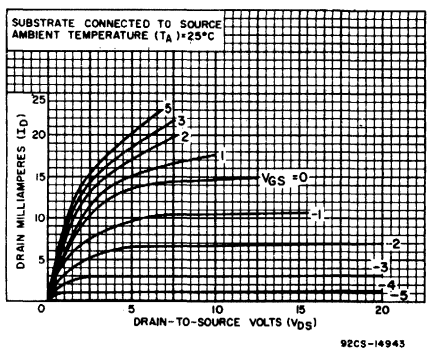


Fig.1 - Drain current vs. drain-to-source voltage.

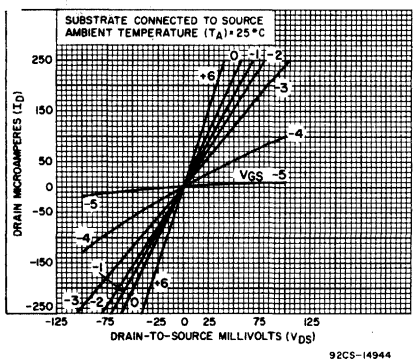


Fig.2 - Low-level drain current vs. drain-to-source voltage.

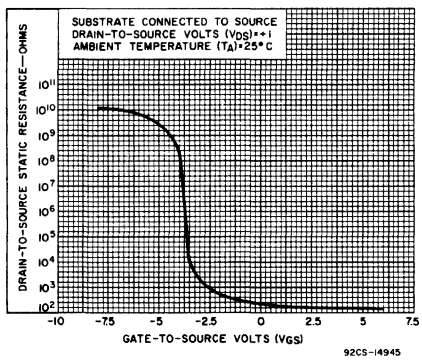


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

3N154

Silicon MOS Transistor N-Channel Depletion Type

For Critical Amplifier Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

RCA 3N154 is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N154 can provide substantially better crossmodulation performance in linear amplifier applications than conventional bipolar transistors. The extremely low gate leakage current eliminates diode-current loading of the input circuit under strong signal conditions, a problem which is common to junction-type FET's. These features, in addition to low feedback capacitance, permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N154 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

■ Metal-Oxide-Semiconductor

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^oC$:

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
* CONTINUOUS (dc)	+1, -8	V
* PEAK ac	±15	V
*DRAIN CURRENT, I_D▲	50	mA
*TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
*AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

In accordance with JEDEC Registration Data Format JS9-RDF-11B

▲ Pulsed:
Pulse duration ≤ 20 ms
Duty factor ≤ 0.15

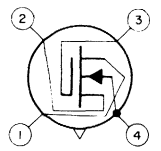
Device Feature:

- **Closely controlled IDSS – 10 to 25 mA**
- **Low gate leakage current – I_{GSS} = 0.1 pA typ.**
- **Low feedback capacitance – C_{rss} = 0.25 pF typ.**
- **High forward transconductance – g_{fs} = 7500 μmho typ.**
- **High vhf power gain – G_{PS} = 16 dB typ. at 200 MHz**
- **Low vhf noise figure – NF = 3.5 dB typ. at 200 MHz**
- **Exceptionally good cross-modulation characteristics**

Performance Features

- **Large dynamic range**
- **Greatly reduced spurious responses**
- **Permits use of vacuum-tube biasing techniques**
- **Excellent thermal stability**
- **Superior cross-modulation performance and greater dynamic range than bipolar transistors**

TERMINAL DIAGRAM

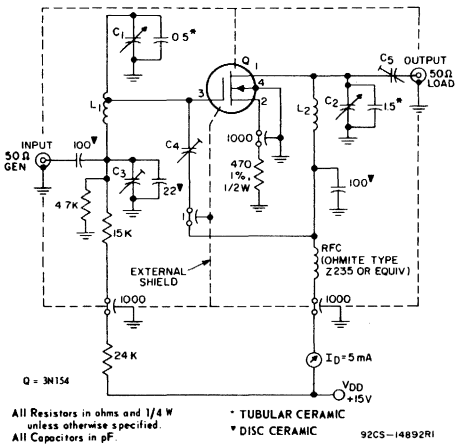


ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N154 Min.	Typ.	Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C	-	-	5	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	0.05	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	5	nA
*	Zero-Bias Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	10	15	25	mA
	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.15	0.25	0.35	pF
	Small-Signal Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
	Input Admittance	Y_{is}	Common Source Configuration f = 200 MHz, V_{DS} = 15 V, I_D = 5 mA	-	0.4 + J7.3	-	mmho
	Forward Transfer Admittance	Y_{fs}		-	7 – J2	-	mmho
	Output Admittance	Y_{os}		-	0.28 + J1.8	-	mmho
	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	21	-	dB
*	Insertion Power Gain (Fixed Neutralization) (see Fig. 1)	G_{PS}		13.5	16	-	dB
*	Noise Figure (see Figs.1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	3.5	5	dB

* In Accordance with JEDEC Registration Data Format JS-9 RDF-11B
▲ Three-Terminal Measurement: Source Returned to Guard Terminal



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

Q = 3N154

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 - Test circuit used to measure 200-MHz maximum usable power gain and noise figure

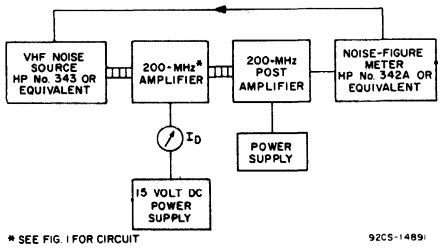


Fig. 2 - Noise figure measurement setup

For characteristics curves, refer to types 3N128 and 3N143.

3N159

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

For Military and Industrial Low-Noise RF-Amplifier Applications Up to 300 MHz

The 3N159 is an n-channel silicon, depletion type, dual insulated-gate, field-effect transistor utilizing the MOS** construction. It has exceptional characteristics for rf-amplifier applications at frequencies up to 300 MHz. This transistor features a series arrangement of two separate channels, each channel having an independent control gate.

Type 3N159 has an exceptionally low-noise figure, which makes this type particularly suitable for critical vhf applications. When used in a common-source configuration in which gate No.2 is ac grounded, this device reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation.

The 3N159 is hermetically sealed in the metal JEDEC TO-72 package.

** Metal-Oxide-Semiconductor.

APPLICATIONS

- **RF amplifier in military and industrial communications equipment**
- **aircraft, marine and vehicular receivers**
- **CATV and MATV equipment**
- **telemetry and multiplex equipment**

Maximum Ratings, *Absolute-Maximum Values:*
at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . 0 to +20 V
GATE-No.1-TO-SOURCE VOLTAGE, V_{G1S}:
Continuous (dc) . . . . . -8 to +1 V
Peak ac . . . . . -8 to +20 V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:
Continuous (dc) . . . . . -8 to 40% of V_{DS} V
Peak ac . . . . . -8 to +20 V
DRAIN-TO-GATE VOLTAGE:
V_{DG1} or V_{DG2} . . . . . +20 V
DRAIN CURRENT, I_D
Pulsed: Pulse duration ≤ 20 ms,
duty factor ≤ 0.15 . . . . . 50 mA
TRANSISTOR DISSIPATION, P_T:
At ambient temperatures up to 25°C . . . . . 400 mW
above 25°C . . . . . derate linearly at 2.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Storage and Operating . . . . . -65 to +175 °C
LEAD TEMPERATURE (During soldering):
At distances ≥ 1/32 inch from seating surface for 10 seconds max. . . . . 265 °C

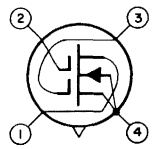
PERFORMANCE FEATURES

- **wide dynamic range permits large-signal handling before overload**
- **dual-gate permits simplified agc circuitry**
- **virtually no agc power required**
- **greatly reduces spurious responses in FM receivers**
- **permits use of vacuum-tube biasing techniques**
- **excellent thermal stability**
- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate field-effect transistors**

DEVICE FEATURES

- **low gate leakage currents — — I_{G1SS} & I_{G2SS} = 1 nA max.**
- **high forward transconductance — — g_{fs} = 7000 μmho min.**
- **high unneutralized RF power gain — — G_{ps} = 16 dB min. at 200 MHz**
- **low vhf noise figure — — NF = 3.5 dB max. at 200 MHz**

TERMINAL DIAGRAM



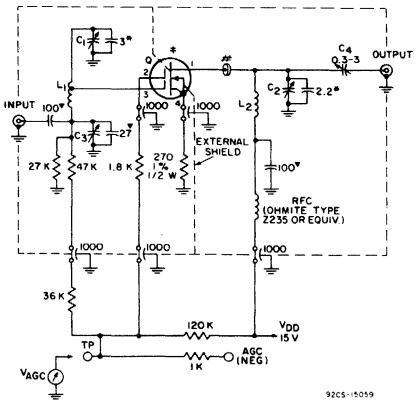
LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 3N159 Min.	Typ.	Max.	UNITS
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +16V, I_D = 200 μA, V_{G2S} = +4V	-	-2	-4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +16V, I_D = 200 μA, V_{G1S} = 0	-	-2	-4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = +1, V_{DS} = 0, V_{G1S} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0, V_{G2S} = +4V	5	18	30	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA, V_{G2S} = +4V, f = 1 kHz	7000	10,000	18,000	μmho
Cutoff Forward Transconductance (Gate-No.1-to-Drain)	$g_{fs(off)}$	V_{DD} = +14V, V_{G1S} = -0.5V, V_{G2S} = -2V, f = 1 kHz	-	-	100	μmho
Small-Signal, Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	3	5.5	7	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	-	2.2	-	pF
Maximum Usable Power Gain (See Fig.1 for Measurement Circuit)	MUG	V_{DD} = +15V, R_S = 270Ω, R_G = 50Ω, f = 200 MHz	16	18	22	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω, f = 200 MHz, R_G = 50Ω	-	2.5	3.5	dB

* Pulse Test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.
▲ Capacitance between Gate No.1 and all other terminals.
♦ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

For characteristics curves refer to types 3N140, 3N141.



* Tubular ceramic
▼ Disc ceramic
Ferrite bead (1/2 used); Indiana General No. H 1742C-(A-147) or F1157-1-H or equivalent.
‡ VHF plug in socket Jettron CD72-148 and CD72149 (part No.7977-1) or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent.
C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.
L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.
L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200-MHz power gain and noise-figure test circuit for type 3N159.

3N187

Silicon Dual Insulated-Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 300 MHz

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 12,000 μmho (typ.)
- High unneutralized RF power gain — G_{PS} = 18 dB(typ.) at 200 MHz
- Low VHF noise figure — 3.5 dB(typ.) at 200 MHz

RCA-3N187 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N187 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N187 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N187 is hermetically sealed in the metal JEDEC TO-72 package.

▲ Metal-Oxide-Semiconductor

Applications

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

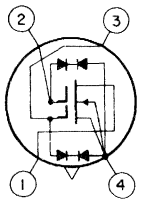
Maximum Ratings,

Absolute-Maximum Values, at T_A = 25°C

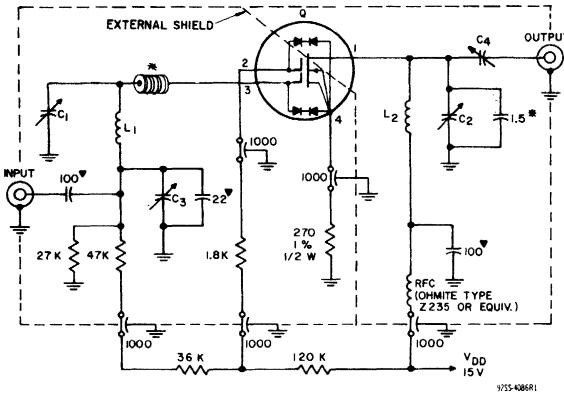
DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

TERMINAL DIAGRAM



LEAD 1-DRAIN
LEAD 2-GATE No. 2
LEAD 3-GATE No. 1
LEAD 4-SOURCE, SUBSTRATE AND CASE



Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.
All resistors in ohms
All capacitors in pF
C_1: 1.8–8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.
C_2: 1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.
C_3: 1–10 pF piston-type variable air capacitor: JFD Type VAM-010: Johanson Type 4335, or equivalent.
C_4: 0.8–4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.
L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.08 in.
L_2: 4½ turns silver-plated 0.02-in thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈.90 in. long.
Q = 3N187
▼ Disc ceramic.
* Tubular ceramic.

Fig. 1 - 200-MHz Power gain and noise-figure test circuit

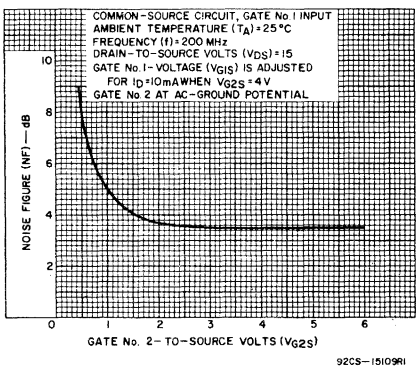


Fig. 2 - NF vs. V_{G2S}

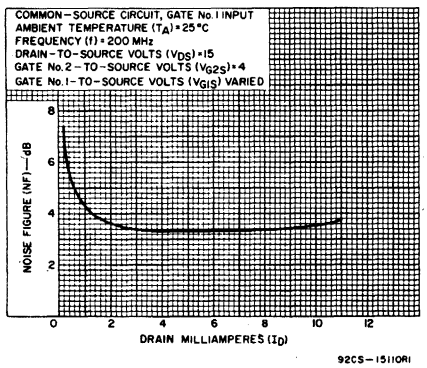


Fig. 3 - NF vs. I_D

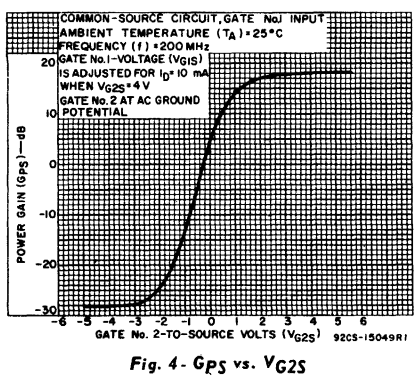


Fig. 4 - G_{PS} vs. V_{G2S}

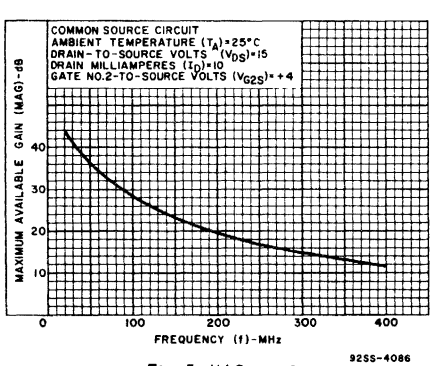


Fig. 5 - MAG. vs. f

3N187

ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.5	-2	-4	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.5	-2	-4	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V V_{G2S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V V_{G1S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
*	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
*	Small-Signal, Short-Circuit Output Capacitanc	C_{oss}			–	2.0	–	pF
	Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
	Maximum Available Power Gain	MAG			–	20	–	dB
	Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
	Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
*	Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
*	Phase Angle of Forward Transadmittance	θ			–	-35	–	Degrees
	Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
	Angle of Reverse Transadmittance	θ_{rs}			–	-25	–	Degrees
*	Input Resistance	r_{iss}			–	1.0	–	kΩ
*	Output Resistance	r_{oss}			–	2.8	–	kΩ
*	Gate-to-Source Forward Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSF}$ $V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA		6.5	10	–	V
*	Gate-to-Source Reverse Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSR}$ $V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = -100 μA		-6.5	-10	–	V

▲Limited only by practical design considerations.

† Capacitance between Gate No. 1 and all other terminals

♦Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

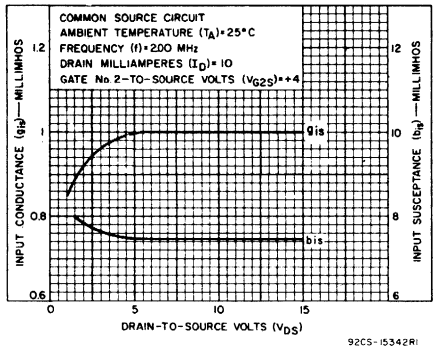


Fig. 8- y_{is} vs. V_{DS}

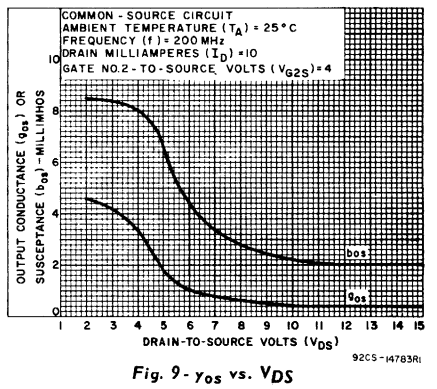


Fig. 9- y_{os} vs. V_{DS}

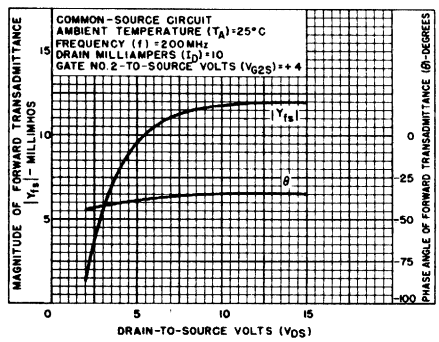


Fig. 10- y_{fs} vs. V_{DS}

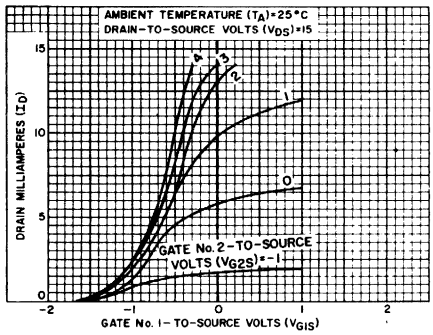


Fig. 6- I_D vs. V_{G1S}

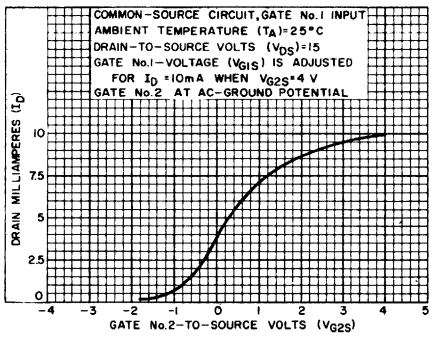


Fig. 7- I_D vs. V_{G2S}

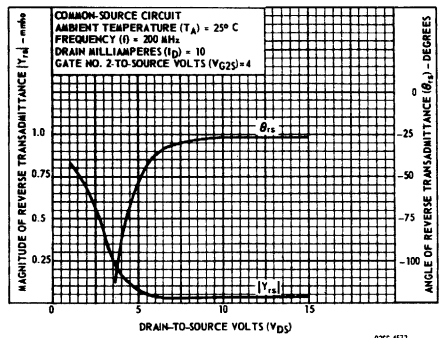


Fig. 11- y_{rs} vs. V_{DS}

3N187

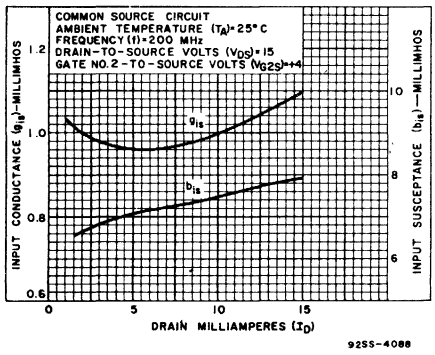


Fig. 12 - y_{is} vs. I_D

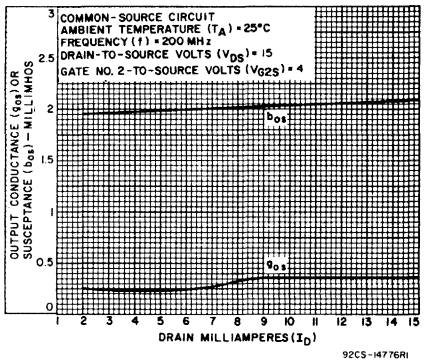


Fig. 13 - y_{os} vs. I_D

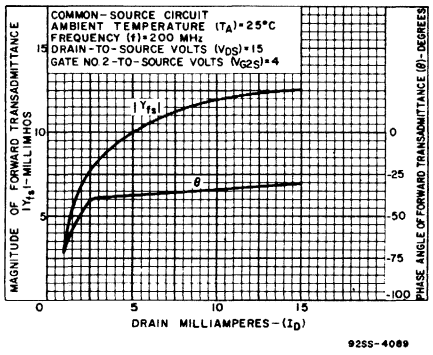


Fig. 14 - y_{fs} vs. I_D

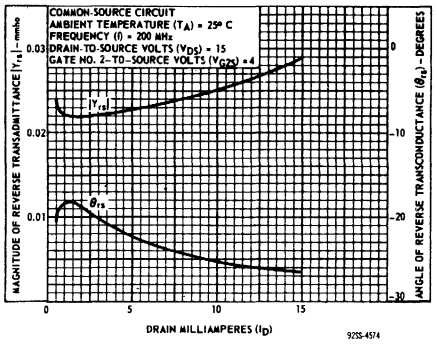


Fig. 15 - y_{rs} vs. I_D

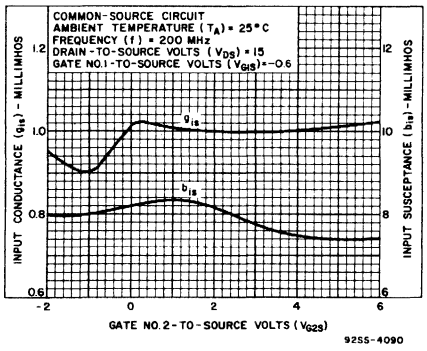


Fig. 16 - y_{is} vs. V_{G2S}

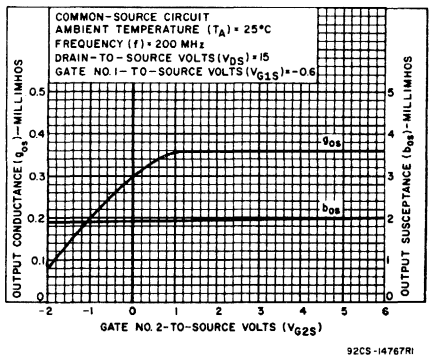


Fig. 17 - y_{os} vs. V_{G2S}

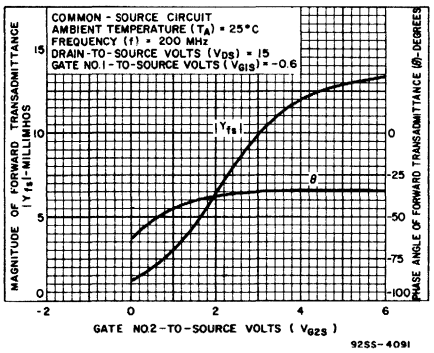


Fig. 18 - y_{fs} vs. V_{G2S}

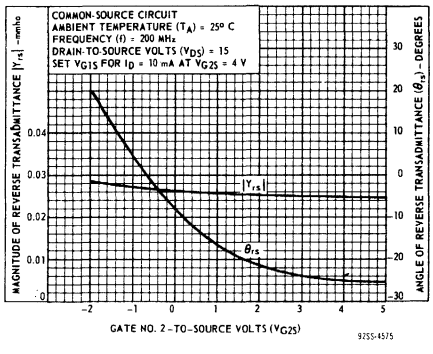


Fig. 19 - y_{rs} vs. V_{G2S}

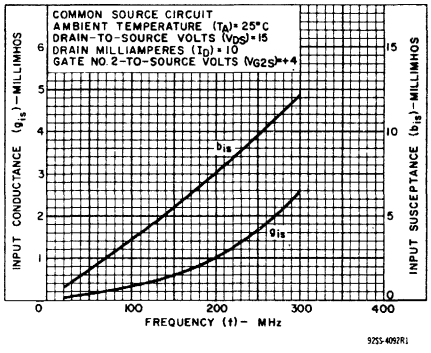


Fig. 20 - y_{is} vs. frequency

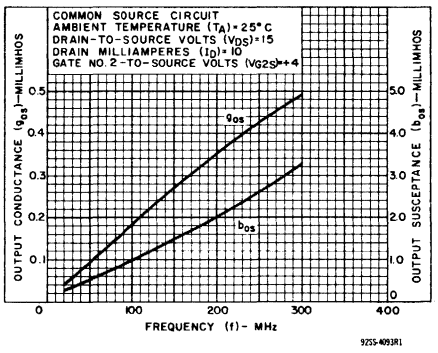


Fig. 21 - y_{os} vs. frequency

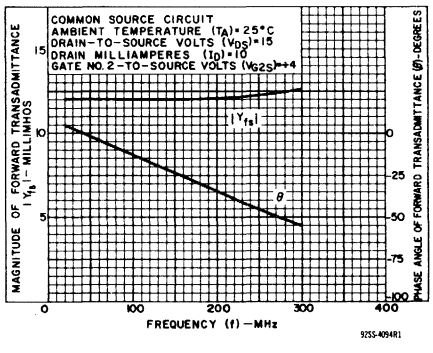


Fig. 22 - y_{fs} vs. frequency

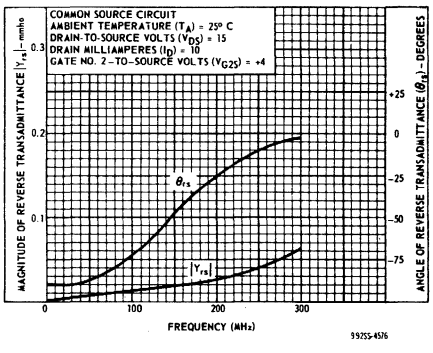


Fig. 23. - y_{rs} vs. frequency

3N187

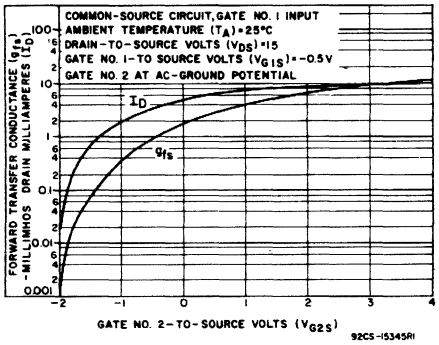


Fig. 24 - g_{fs} and I_D vs. V_{G2S}

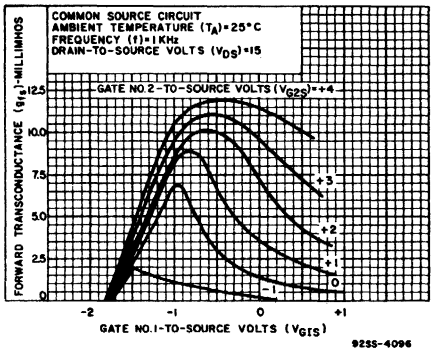


Fig. 25. - g_{fs} vs. V_{G1S}

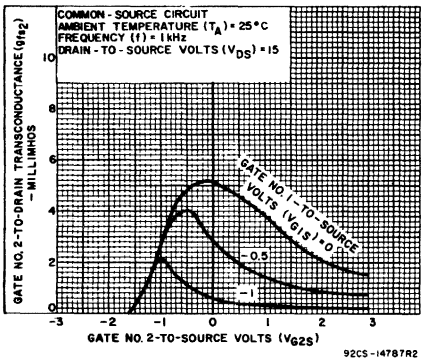


Fig. 26 - g_{fs_2} vs. V_{G2S}

3N200

Silicon Dual Insulated-Gate Field-Effect Transistor

N-Channel Depletion Types

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

RCA-3N200 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

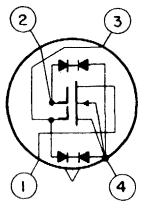
Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz
- Low VHF noise figure — 3.9 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz

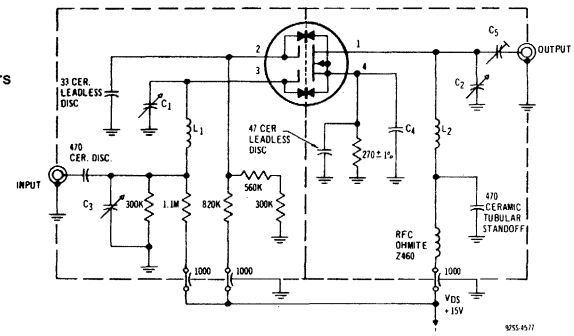
Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

TERMINAL DIAGRAM



LEAD 1-DRAIN
LEAD 2-GATE No. 2
LEAD 3-GATE No. 1
LEAD 4-SOURCE, SUBSTRATE AND CASE



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent

C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent

C_4: Approx. 300 pF-capacitance formed between socket cover & chassis

C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent

L_1,L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-15	-25	-35	-47	-60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	-60	-25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\lvert s_{is} \rvert$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	-20	-32	-55	-68	-82	degrees
Magnitude of Forward Transmission Coeff.	$\lvert s_{fs} \rvert$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\lvert s_{os} \rvert$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	-7.5	-16	-22	-28	-34	degrees
Magnitude of Reverse Transmission Coeff.	$\lvert s_{rs} \rvert$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

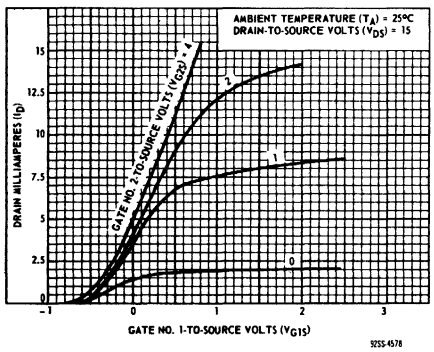


Fig. 2 - I_D vs. V_{G1S}

3N200

	ELECTRICAL CHARACTERISTICS *at T_A = 25°C unless otherwise specified*		SYMBOLS	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage		$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.1	-1	-3	V
*	Gate No. 2-to-Source Cutoff Voltage		$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.1	-1	-3	V
*	Gate No. 1-Terminal Forward Current		I_{G1SSF}	V_{G1S} = +1 V $V_{G2S} = V_{DS} \equiv 0$	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current		I_{G1SSR}	V_{G1S} = -6 V $V_{G2S} = V_{DS}$ = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current		I_{G2SSF}	V_{G2S} = +6 V $V_{G1S} = V_{DS}$ = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current		I_{G2SSR}	V_{G2S} = -6 V $V_{G1S} = V_{DS}$ = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current		I_{DS}	V_{DS} = +15 V, V_{G1S} = 0 V_{G2S} = +4 V		0.5	5.0	12	mA
*	Forward Transconductance (Gate No. 1-to-Drain)		g_{fs}	V_{DS} = +15 V I_D = 10 mA V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
	Small-Signal, Short-Circuit Input Capacitance†		C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦		C_{rss}			0.005	0.02	0.03	pF
	Small-Signal, Short-Circuit Output Capacitance		C_{oss}			–	2.0	–	pF
*	Power Gain (see Fig. 1)		G_{PS}		f = 400 MHz	10	12.5	–	dB
	Noise Figure (see Fig. 1)		NF			–	3.9	6.0	dB
*	Bandwidth		BW			28	–	38	MHz
*	Gate-to-Source Forward Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	$V_{G2S} = V_{DS}$ = 0 $V_{G1S} = V_{DS}$ = 0	6.5	–	13	V
		Gate No. 2	$V_{(BR)G2SSF}$						
*	Gate-to-Source Reverse Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	$V_{G2S} = V_{DS}$ = 0 $V_{G1S} = V_{DS}$ = 0	-6.5	–	-13	V
		Gate No. 2	$V_{(BR)G2SSR}$						

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

†Capacitance between Gate No. 1 and all other terminals.

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

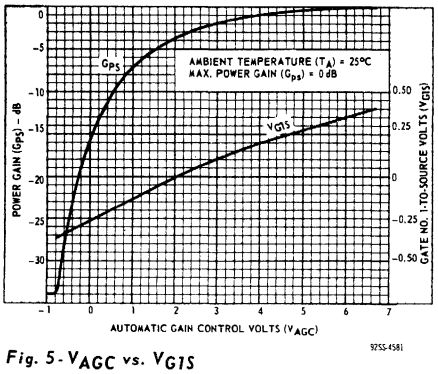


Fig. 5 - V_{AGC} vs. V_{G1S}

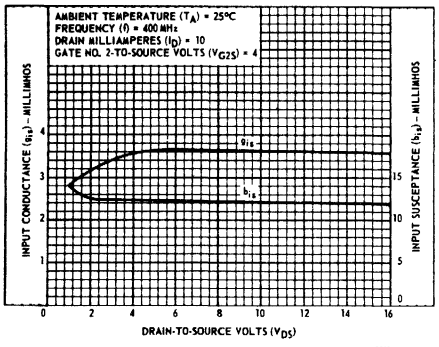


Fig. 6 - y_{is} vs. V_{DS}

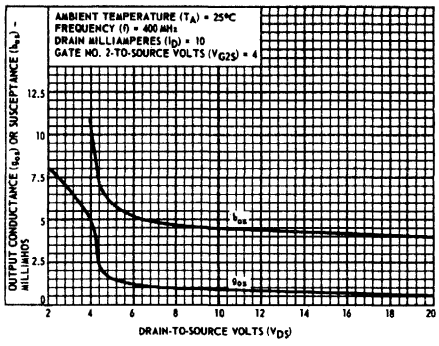


Fig. 7 - y_{os} vs. V_{DS}

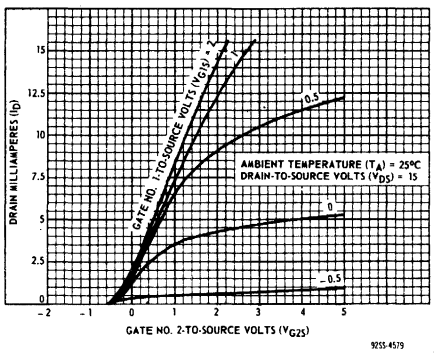


Fig. 3 - I_D vs. V_{G2S}

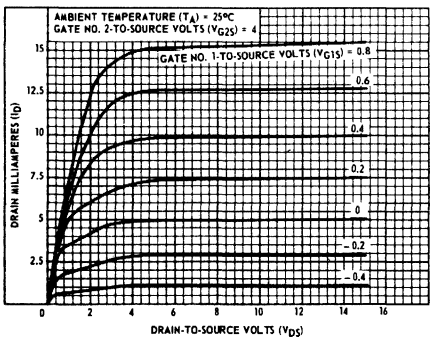


Fig. 4 - I_D vs. V_{DS}

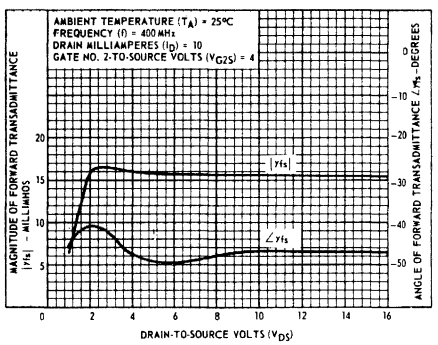


Fig. 8 - y_{fs} vs. V_{DS}

3N200

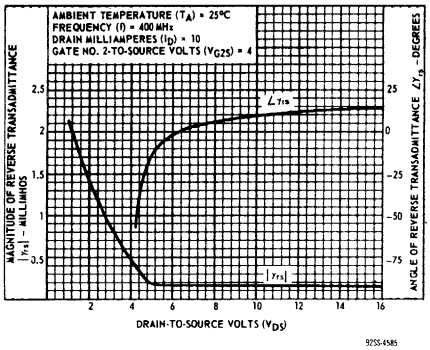


Fig. 9 - y_{rs} vs. V_{DS}

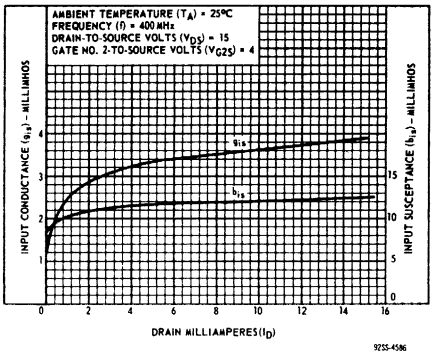


Fig. 10 - y_{is} vs. I_D

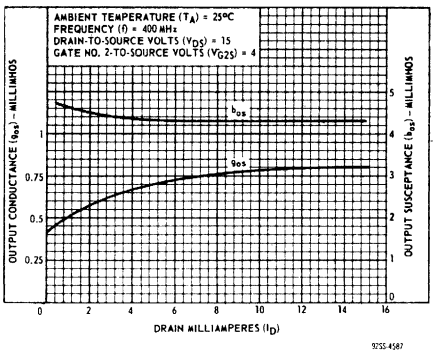


Fig. 11 - y_{os} vs. I_D

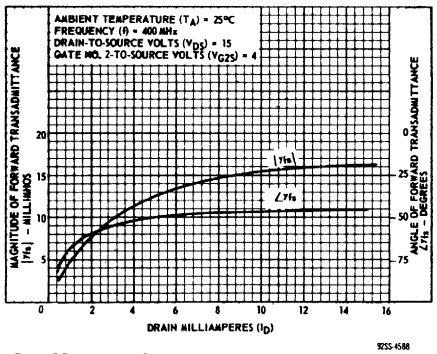


Fig. 12 - y_{fs} vs. I_D

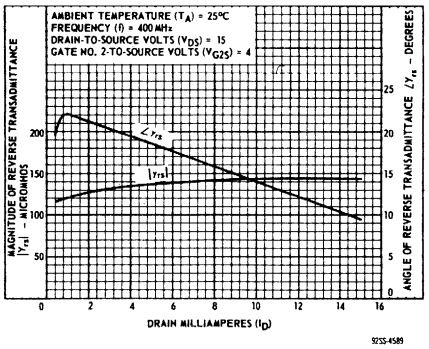


Fig. 13 - y_{rs} vs. I_D

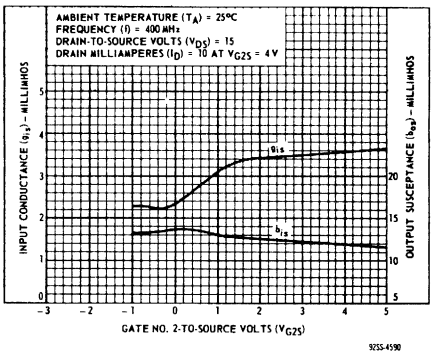


Fig. 14 - y_{is} vs. V_{G2S}

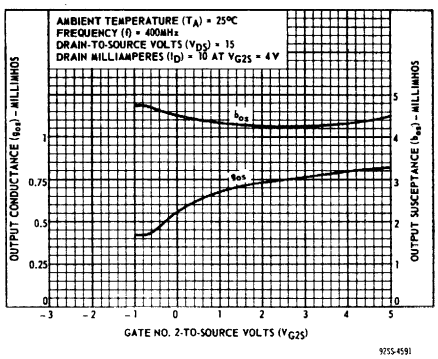


Fig. 15 - y_{os} vs. V_{G2S}

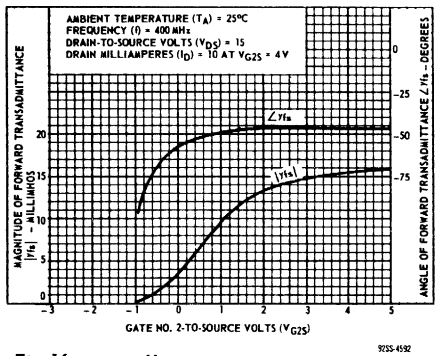


Fig. 16 - y_{fs} vs. V_{G2S}

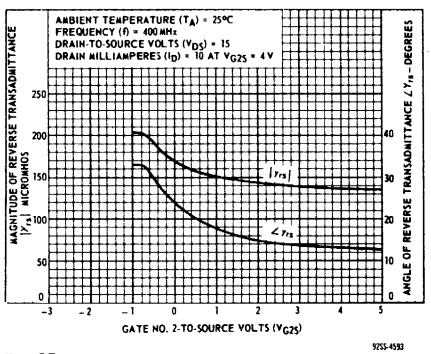


Fig. 17 - y_{rs} vs. V_{G2S}

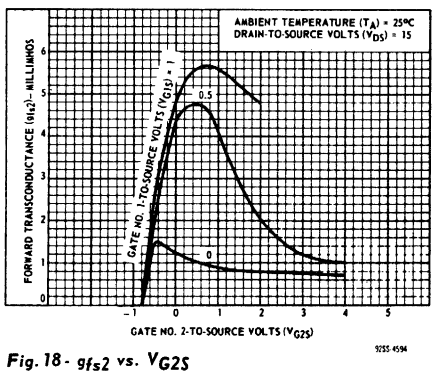


Fig. 18 - g_{fs2} vs. V_{G2S}

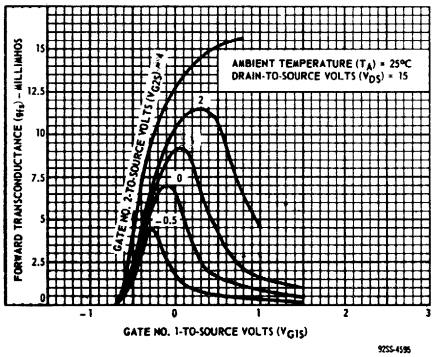


Fig. 19 - g_{fs} vs. V_{G1S}

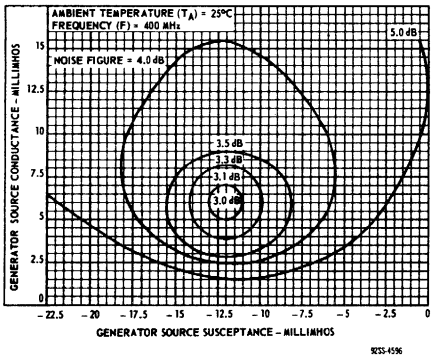


Fig. 20 - Noise figure vs. generator source admittance

3N211, 3N212, 3N213

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits
For VHF TV Applications

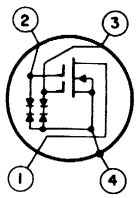
3N211 – RF Amplifiers
3N212 – Mixers
3N213 – TV IF Strips

Features:
- Low C_{rss} – 0.05 pF max.
- High $|Y_{fs}|$ – 30 mmho typ. for 3N211 and 3N212
- Integrated gate-protection diodes

The RCA-3N211, 3N212, and 3N213 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for VHF TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N211 is intended for use in VHF RF amplifiers and delivers linear, low-noise amplification. Its extremely low feedback capacitance allows high-gain stable operation without neutralization. The 3N212 is specified for low-noise VHF mixer applications. The 3N213 is intended for use in tuned high-frequency amplifiers such as TV IF strips.

TERMINAL DIAGRAM
Bottom View



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

MAXIMUM RATINGS,
Absolute Maximum Values at $T_A = 25°C$

	3N211, 3N212	3N213	
DRAIN-TO-GATE No.1 VOLTAGE	35	40	V
DRAIN-TO-GATE No.2 VOLTAGE	35	40	V
DRAIN-TO-SOURCE VOLTAGE	27	35	V
GATE No.1-TERMINAL FORWARD CURRENT*	10		mA
GATE No.2-TERMINAL FORWARD CURRENT*	10		mA
GATE No.1-TERMINAL REVERSE CURRENT	−10		mA
GATE No.2-TERMINAL REVERSE CURRENT	−10		mA
CONTINUOUS DRAIN CURRENT	50		mA
DEVICE DISSIPATION:			
Up to $T_A = 25°C$	360		mW
Above $T_A = 25°C$ derate linearly	2.4		mW/°C
Up to $T_C = 25°C$	1.2		mW
Above $T_C = 25°C$ derate linearly	8		mW/°C
AMBIENT TEMPERATURE RANGE:			
Operating	−65 to +175		°C
Storage	−65 to +200		°C
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300		°C

* Forward gate-terminal current is the current into a gate terminal with a forward gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.

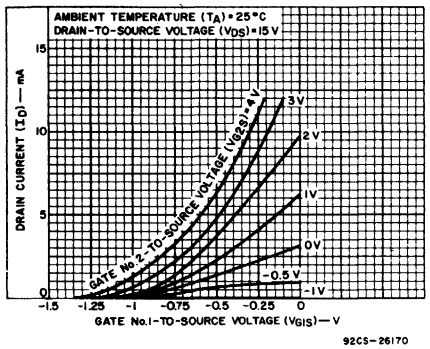


Fig.3—Drain current vs. gate No. 1-to-source voltage for all types.

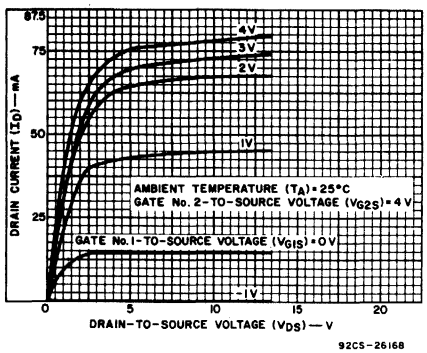


Fig.1—Drain current vs. drain-to-source voltage for all types.

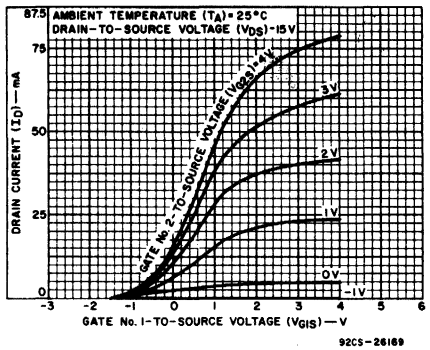


Fig.2—Drain current vs. gate No. 1-to-source voltage for all types.

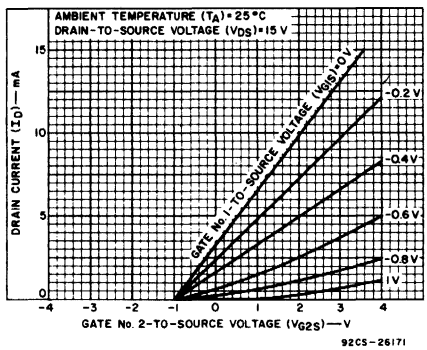


Fig.4—Drain current vs. gate No. 2-to-source voltage for all types.

(Figures 1 – 4 are pulse tested. Pulse duration = 300 μs, duty cycle ≤2%.)

3N211, 3N212, 3N213

ELECTRICAL CHARACTERISTICS, At T_A = 25°C (unless otherwise specified)

	CHARACTERISTIC	TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	I_D = 10μA, $V_{G1S}=V_{G2S}$= −4V	3N211	27	–	V
			3N212	27	–	
			3N213	35	–	
*	Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF}$[1]	I_{G1}=10mA, $V_{G2S}=V_{DS}$=0		6	–	V
*	Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR}$[1]	I_{G1}= −10mA, $V_{G2S}=V_{DS}$=0		−6	–	V
*	Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF}$[1]	I_{G2}=10mA, $V_{G1S}=V_{DS}$=0		6	–	V
*	Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR}$[1]	I_{G2}= −10mA, $V_{G1S}=V_{DS}$=0		−6	–	V
*	Gate No.1-Terminal Forward Current, I_{G1SSF}	V_{G1S}=5V, $V_{G2S}=V_{DS}$=0		–	10	nA
*	Gate No.1-Terminal Reverse Current, I_{G1SSR}	V_{G1S}= −5V, $V_{G2S}=V_{DS}$=0	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Gate No.2-Terminal Forward Current, I_{G2SSF}	V_{G2S}=5V, $V_{G1S}=V_{DS}$=0		–	10	nA
*	Gate No.2-Terminal Reverse Current, I_{G2SSR}	V_{G2S}= −5V, $V_{G1S}=V_{DS}$=0	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Zero-Gate No.1-Voltage Drain Current, I_{DS}[2]	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V		6	40	mA
*	Gate No.1-to-Source Cutoff Voltage, $V_{G1S(off)}$	V_{DS}=15V, V_{G2S}=4V, I_D=20μA	3N211	−0.5	−5.5	V
			3N212	−0.5	−4	
			3N213	−0.5	−5.5	
*	Gate No.2-to-Source Cutoff Voltage, $V_{G2S(off)}$	V_{DS}=15V, V_{G1S}=0, I_D=20μA	3N211	−0.2	−2.5	V
			3N212	−0.2	−4	
			3N213	−0.2	−4	
*	Small-Signal Common-Source Forward Transfer Admittance, $\lvert y_{fs}\rvert$[3]	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V, f=1 kHz	3N211	17	40	mmho
			3N212	17	40	
			3N213	15	35	
*	Small-Signal Common-Source Reverse Transfer Capacitance, C_{rss}	V_{DS}=15V, V_{G2S}=4V, I_D=1mA, f=1MHz		0.005	0.05	pF

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
2. This characteristic must be measured using pulse techniques (t_W = 300μs, duty cycle ⩽ 2%).
3. This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

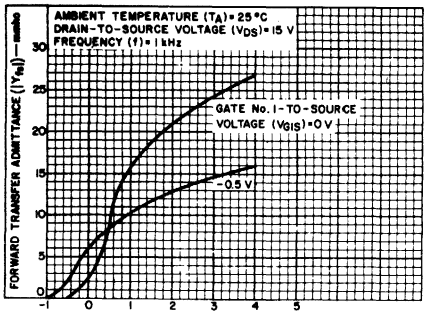


Fig. 5 – $|Y_{fs}|$ vs. V_{G2S} for 3N211 and 3N212.

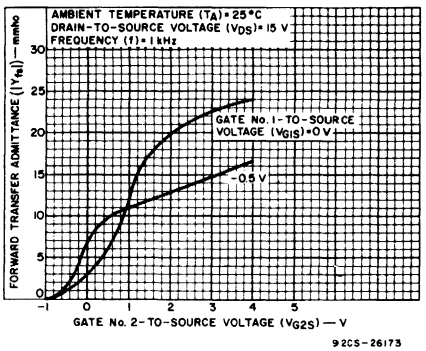


Fig. 6 – $|Y_{fs}|$ vs. V_{G2S} for 3N213.

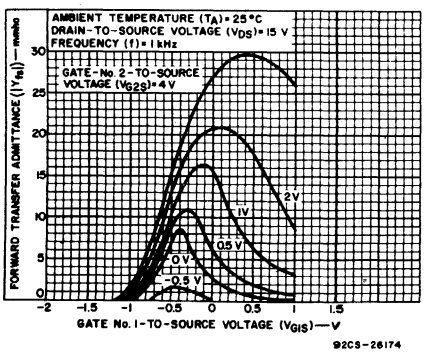


Fig. 7 – $|Y_{fs}|$ vs. V_{G1S} for 3N211, and 3N212.

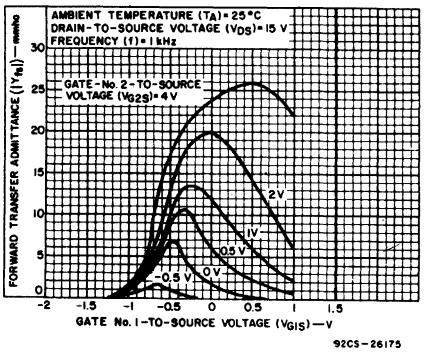


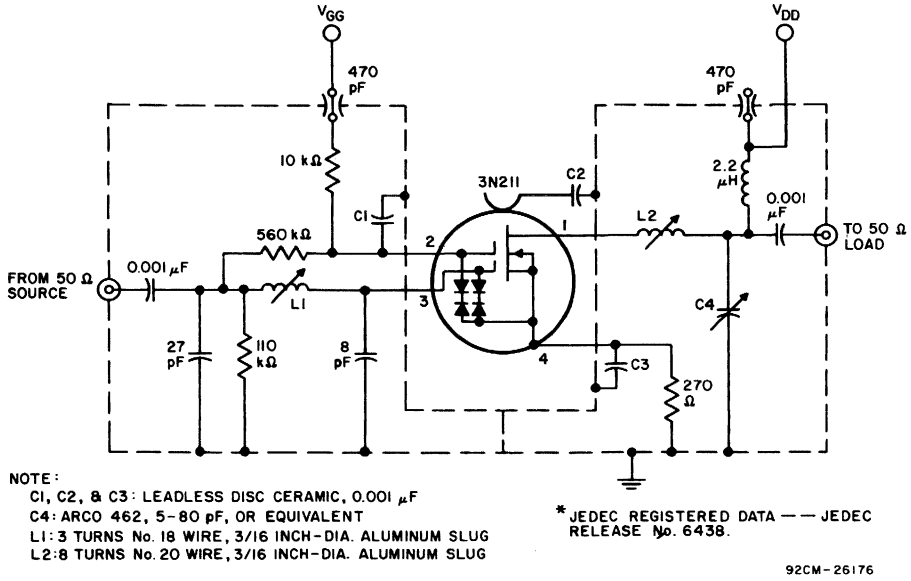
Fig. 8 – $|Y_{fs}|$ vs. V_{G1S} for 3N213.

3N211, 3N212, 3N213

OPERATING CHARACTERISTICS at $T_A = 25°C$

	CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
	3N211					
*	Common-Source Spot Noise Figure, F	V_{DD}=18V, V_{GG}=7V, f = 200MHz, See Fig.9	–	–	3.5	dB
*	Small-Signal Common-Source Insertion Power Gain, G_{ps}		24	–	35	dB
*	Bandwidth, B		5	–	12	MHz
*	Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=18V, ΔG_{ps}= –30dB,[1] f=200MHz, See Fig.9	0	–	–2	V
*	Common-Source Spot Noise Figure, F	V_{DD}=24V, V_{GG}=6V, f=45MHz, See Fig.10	–	–	4	dB
*	Small-Signal Common-Source Insertion Power Gain, G_{ps}		29	–	37	dB
*	Bandwidth, B		3.5	–	6	MHz
*	Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24V, ΔG_{ps}= –30dB,[2] f=45MHz, See Fig.10	–	–	±1	V
	3N212					
*	Small-Signal Conversion Power Gain, G_{ps} (conv)	V_{DD}=18V, f_{LO}=245MHz,[3] f_{RF}=200MHz, See Fig.11	21	–	28	dB
*	Bandwidth, B		4	–	7	MHz
	3N213					
*	Common-Source Spot Noise Figure, F	V_{DD}=24V, V_{GG}=6V, f=45MHz, See Fig.9	–	–	4	dB
*	Small-Signal Common-Source Insertion Power Gain, G_{ps}		27	–	35	dB
*	Bandwidth, B		3.5	–	6	MHz
*	Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24V, ΔG_{ps}= –30dB,[2] f=45MHz, See Fig.9	–	–	±1	V

*In accordance with JEDEC registration data format (JS-9 RDF-19B). 2. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6V.
1. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7V. 3. Amplitude at input from local oscillator is adjusted for maximum G_{ps}(c



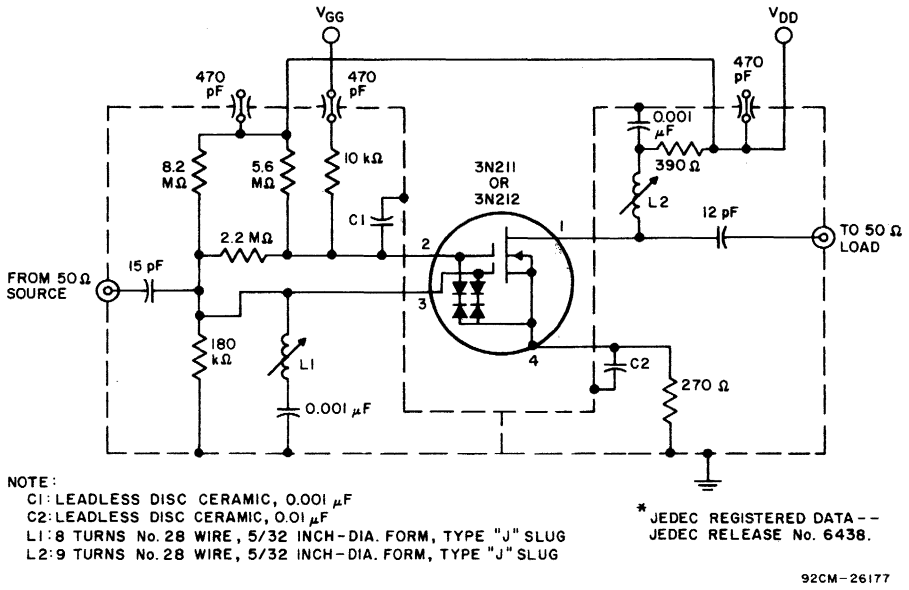
NOTE:
C1, C2, & C3: LEADLESS DISC CERAMIC, 0.001 μF
C4: ARCO 462, 5-80 pF, OR EQUIVALENT
L1: 3 TURNS No. 18 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG
L2: 8 TURNS No. 20 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG

*JEDEC REGISTERED DATA — — JEDEC RELEASE No. 6438.

92CM-26176

Fig.9—200 MHz power gain, gain control voltage, and noise figure test circuit for 3N211.*

3N211, 3N212, 3N213



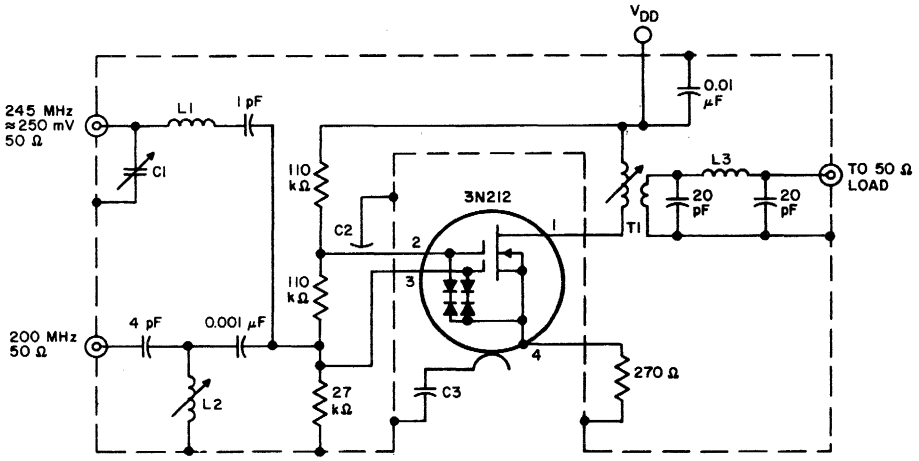
NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 μF
C2: LEADLESS DISC CERAMIC, 0.01 μF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

*JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

92CM-26177

Fig. 10—45 MHz power gain and noise figure test circuit for 3N211 and 3N213.*

TEST CIRCUITS (CONT'D)



NOTE:
L1: 7 TURNS No. 34 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L2: 5 1/2 TURNS No. 20 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L3: 7 TURNS No. 24 WIRE, 1/4 INCH DIA. AIR CORE
T1: PRI: 25 TURNS No. 30 WIRE CLOSE WOUND ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 4 TURNS No. 30 WIRE CENTERED OVER PRIMARY
C1: ARCO TYPE 462, 5-80 pF
C2: 0.001 μF LEADLESS DISC
C3: 0.01 μF LEADLESS DISC

*JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

92CM-26178

Fig. 11—200 MHz-to-45 MHz circuit for conversion power gain for 3N212.*

40467A

Silicon MOS Transistor N-Channel Depletion Type

For VHF Tuners and Other VHF Amplifier
Applications in Industrial & Commercial Electronic Equipment
Operating up to 220 MHz

Device Features:

- Low feedback capacitance - C_{rss} = 0.25 pF typ.
- High forward transconductance - g_{fs} = 7500 μmho typ.
- High vhf power gain - G_{PS} = 16 dB typ at 200 MHz
- Low vhf noise figure - NF = 3.5 dB typ at 200 MHz
- Exceptionally good cross-modulation characteristics

Performance Features:

- Large dynamic range
- Greatly reduced spurious responses
- Permits use of vacuum-tube biasing techniques
- Excellent thermal stability
- Superior cross-modulation performance and greater dynamic range than bipolar transistors

RCA-40467A is an n-channel depletion-type silicon insulated-gate field-effect transistor utilizing the MOS■ construction. It is intended primarily for vhf-amplifier applications in industrial and commercial electronic equipment.

The 40467A is useful in vhf applications requiring devices capable of providing high useful power gains at frequencies up to approximately 220 MHz.

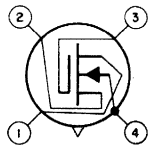
The 40467A features high forward transconductance, high dc gate-to-source resistance, and low feedback capacitance. Because of the improved transfer characteristic and increased dynamic range, the 40467A provides substantially better cross-modulation performance in linear-amplifier applications than conventional (bipolar) transistors and is free from diode-current loading, a problem that exists in junction type FET s. This device is hermetically sealed in the TO-72 metal case and utilizes full-gate construction.

■ Metal-Oxide Semiconductor

Maximum Ratings, *Absolute-Maximum Values at T_A=25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ..... +20 V
DRAIN-TO-GATE VOLTAGE, V_{DG} ..... +20 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:
  CONTINUOUS (dc) ..... +1, −8 V
  PEAK ac ..... +15 V
DRAIN CURRENT, I_D ..... 50 mA
TRANSISTOR DISSIPATION:
  At ambient temperatures up to 25°C ..... 330 mW
  At ambient temperatures above 25°C ..... derate at 2.2 mW/°C
AMBIENT TEMPERATURE RANGE:
  Storage ..... −65 to +175°C
  Operating ..... −65 to +175°C
LEAD TEMPERATURE (During Soldering):
  At distances not closer than 1/32 inch to seating surface for 10 seconds maximum ..... 265°C

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS AT T_C = 25°C WITH BULK (SUBSTRATE) CONNECTED TO SOURCE

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC DRAIN CURRENT I_D	RCA 40467A			
		MHz	V	mA	Min	Typ.	Max.	
Gate-to-Source Cutoff Voltage	V_{GS}(off)		12	0.1	-	-	-8	V
Gate Leakage Current	I_{GSS}		0	V_{GS} = +1V	-	-	1	nA
			0	V_{GS} = -8V	-	-	1	nA
Zero-Bias Drain Current	I_{DSS}		15	V_{GS} = 0	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 KHz	15	5	4000	7500	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	0.12	0.25	0.35	pF
Small Signal Short-Circuit Input Capacitance	C_{iss}	1	15	5	-	5.5	-	pF
Input Admittance	Y_{is}	Common Source Configuration f = 200 mHz V_{DS} = 15V I_D = 5 mA			-	0.4 + j7.3	-	
Forward Transfer Admittance	Y_{fs}				-	7 - j2	-	
Output Admittance	Y_{os}				-	0.28 +j1.8	-	
Maximum Available Power Gain	MAG	200	15	5	-	21	-	dB
Maximum Usable Power Gain (unneutralized)	MUG	200	15	5	-	12	-	dB
Maximum Usable Power Gain (neutralization)	MUG	200	15	5	12	16	-	dB
Noise Figure	NF	200	15	5	-	3.5	5	dB

For characteristics curves, refer to types 3N128 and 3N143.

40468A, 40559A

MOS Silicon Transistors

N-Channel Depletion Types

For RF Amplifier and Mixer Applications in FM and AM/FM Receivers

RCA-40468A and 40559A are silicon insulated-gate field-effect transistors of the n-channel depletion type utilizing the MOS* construction. They are intended primarily for use as the rf amplifier and mixer, respectively, in FM receivers covering the 88 to 108 MHz band, but can be used for general amplifier applications at frequencies up to 125 MHz. For circuit design and typical performance data refer to RCA Application Note AN3535 "An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer".

The wide dynamic range of these transistors reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

Operating as a neutralized amplifier at 100 MHz, the 40468A can provide a power gain of 17 dB (typ.). A power gain of 14 dB (typ.) can be realized without neutralization.

* Metal-Oxide-Semiconductor.

Performance Features:

- **reduced spurious responses in FM tuners**
- **reverse bias on substrate improves linearity**
- **reduced cross-modulation effects in AM receivers**

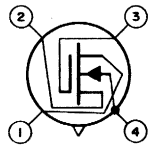
Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^oC$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS (dc)	+1, -8	V
PEAK ac	±15	V
DRAIN CURRENT, I_D	25	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
above 25°C	derate at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

Device Features:

- **high forward transconductance - - gfs = 7500 μmho typ. for 40468A**
- **low feedback capacitance - - c_{rss} = 0.35 pF max. for 40468A 0.38 pF max. for 40559A**
- **high useful power gains - - neutralized - 17 dB typ. unneutralized - 14 dB typ.**
- **hermetically sealed in TO-72 metal package**

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

ELECTRICAL CHARACTERISTICS, at T_A = 25°C
With Bulk (Substrate) Connected to Source Unless Otherwise Specified

Characteristics	Symbols	TEST CONDITIONS: Frequency f	DC Drain-to-Source V_{DS}	DC Drain Current I_D	LIMITS: RCA-40468A RF Amplifier Min.	Typ.	Max.	RCA-40559A Mixer Min.	Typ.	Max.	Units
		MHz	V	mA							
Drain-to-Source Cutoff Current	$I_{D(off)}$	-	12	V_{GS} = -8V	-	-	100	-	-	500	μA
Gate Leakage Current	I_{GSS}	-	0	V_{GS} = -8V	-	-	1	-	-	1	nA
		-	0	V_{GS} = +1V	-	-	1	-	-	1	nA
Zero-Bias Drain Current	I_{DSS}	-	15	V_{GS} = 0	5	15	30	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 kHz	15	5	-	7500	-	-	-	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	-	0.25	0.35	-	0.25	0.38	pF
Input Capacitance	C_{iss}	1	15	5	-	5.5	-	-	5.5	-	pF
Admittance	-	RF | Mixer		RF | Mixer	-			-			-
Input Admittance	Y_{is}	100 MHz	15	5 | 3	0.155 + j 3.45			0.14 + j 3.38			mmho
Forward Transfer Admittance	Y_{fs}	100 MHz	15	5 | 3	7.4 + j 0.9			-			mmho
Output Admittance	Y_{os}	100 MHz | 10.7 MHz	15	5 | 3	0.21 + j 0.9			0.076 + j 0.153			mmho
Forward Conversion Transconductance	$g_{fs(c)}$	1 kHz	15	3	-	-	-	-	2800*	-	μmho
Maximum Available Power Gain	MAG	100	15	5	-	26	-	-	-	-	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15	5	-	14	-	-	-	-	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15	5	14	17	-	-	-	-	dB
Maximum Available Conversion Gain	MAG_C	f_{in} = 100 f_{out} = 10.7	15	3	-	-	-	-	22	-	dB
Noise Figure	NF	100	15	5	-	3.5	5	-	-	-	dB

* Bulk (Substrate)-to-Source Volts (V_{BS}) = -3.

For characteristics curves, refer to types 3N128 and 3N143.

40600, 40601, 40602

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types
For VHF TV Receiver Applications

RCA 40600, 40601, and 40602 are n-channel depletion type, dual-insulated-gate, field-effect transistors utilizing the MOS construction. These devices have characteristics which make them highly desirable for rf-amplifier applications (40600), mixer applications (40601), and first-if-amplifier applications (40602) in vhf TV receivers and other types of commercial equipment operating at frequencies up to approximately 250 MHz.

These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. In amplifier applications the 40600 and 40602 with their wide dynamic range provide substantially better cross-modulation performance than is obtainable with bipolar or single-gate field-effect transistors. In mixer applications the 40601 provides excellent isolation between the oscillator and rf signals because each of the two signal frequencies being mixed has its own control element. The wide dynamic range of the 40601 minimizes cross-modulation which is generally encountered in mixer stages.

Provision of two insulated gates also results in extremely low feedback capacitances (0.02 pF typ.), a feature which enables the 40600 and 40602 to provide high maximum useable power gains in unneutralized circuits – for example, 20 dB at 200 MHz typ. for the 40600, and 35 dB typ. at 44 MHz for the 40602. The gain of the rf and if stages can be controlled by applying agc voltage to gate No.2 and agc delay is easily obtained. Virtually no agc power is required for full gain reduction.

Types 40600, 40601, and 40602 are hermetically sealed in metal JEDEC TO-72 packages.

APPLICATIONS

- **VHF TV Receiver**
  - **40600 for rf amplifier applications**
  - **40601 for mixer applications**
  - **40602 for first-if-amplifier applications**

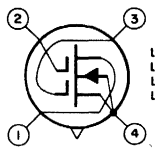
PERFORMANCE FEATURES

- **superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors**
- **permits use of vacuum-tube biasing techniques**
- **excellent thermal stability**

DEVICE FEATURES

- **extremely low feedback capacitance**
  C_{rss} = 0.02 pF typ.
- **high power gain**
  MUG_u = 20 dB typ. for 40600
  MAG = 35 dB typ. for 40602
  MAG_c = 14 dB typ. for 40601

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	+1 to -8	V
Peak ac	+20 to -8	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration ≤ 20 ms, duty factor ≤ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

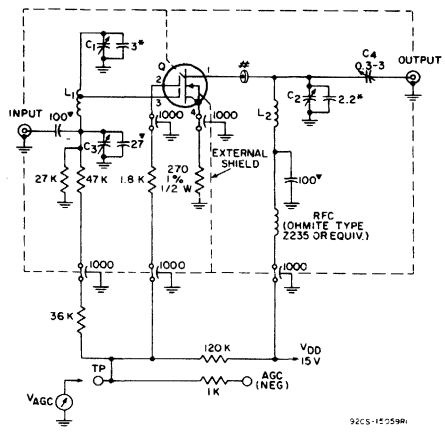
ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 40600, 40601, 40602			UNITS
			Min.	Typ.	Max.	
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200 μA, V_{G2S} = +4V	-	-2	-	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200 μA, V_{G1S} = 0	-	-2	-	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0	-	-	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0	-	-	1	nA
Drain Current	I_{DSS}	V_{DS} = +13V, V_{G1S} = 0, V_{G2S} = +4V	-	18	-	mA
Forward Transconductance	g_{fs}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 kHz	-	10000	-	μmho

TYPICAL PERFORMANCE CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	40600 RF AMPLIFIER f = 200 MHz	40602 IF AMPLIFIER f = 44 MHz	40601 MIXER f = 200 MHz	UNITS
		V_{G1S} is adjusted for I_D = 10 mA, Gate No.2 at AC ground potential, V_{DS} = 13V, V_{G2S} = +4V		Local-oscillator injection Voltage on Gate No.2 = 750 mV, V_{DS} = 15V, V_{G2S} = +0.6V, V_{G1S} = 0.75V	
Small-Signal, Short Circuit Reverse-Transfer Capacitance (Drain-to-Gate No.1) at f = 1 MHz	C_{rss}	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	0.02 typ. 0.03 max.	pF
Output Capacitance	C_{oss}	2.2	2.2	2.2 at f = 44 MHz	pF
Input Capacitance	C_{iss}	5.5	5.5	5.5	pF
Input Resistance	r_{iss}	1.2	10	1.2	KΩ
Output Resistance	r_{oss}	2.8	12	12 at f = 44 MHz	KΩ
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$	11000	11000	2700*	μmho
Phase Angle of Forward Transadmittance	$\angle\theta$	-46	-11	-	degrees
Maximum Available Power Gain	MAG	20	35	14**	dB
Maximum Usable Power Gain (Unneutralized)	MUG_u	20▲	1 Stage 28 2 Stages 26 3 Stages 24	-	dB dB dB
Power Gain See Fig.1 for measurement circuit	G_{PS}	17.5	-	-	dB
Noise Figure	NF	5 max.	-	-	dB

* Magnitude of forward conversion transadmittance ** Maximum available conversion gain ▲ Limited by practical design considerations



* Tubular ceramic.
▼ Disk ceramic.
\# Ferrite bead (½ used); Indiana General No. H1742C-(A-147) or F1157-1-H, or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13, or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"- 0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200 MHz Power Gain and Noise Figure Test Circuit for 40600 and 40602

For characteristics curves, refer to type 3N140.

40603, 40604

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types
For FM Tuner Applications

RCA 40603 and 40604 are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS construction.

These devices have exceptional characteristics for rf-amplifier (40603) and mixer applications (40604) in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. For amplifier applications the 40603 with its wide dynamic range provides substantially better cross-modulation performance and relative freedom from spurious responses than is obtainable with bipolar or single-gate field-effect transistors. The mixing function performed by the 40604 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

Because of the low feedback capacitance (0.02 typ. pF) the 40603 can provide a power gain of 25 dB (typ.) at 100 MHz in an unneutralized amplifier circuit.

The gain of the rf stage can be controlled by applying agc voltage to gate No.2. Virtually no agc power is required for full gain reduction.

The 40603 and 40604 are hermetically sealed in JEDEC TO-72 packages.

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25°C$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration $\leq$ 20 ms, duty factor $\leq$ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
At ambient temperatures above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances > 1/32" from seating surface for 10 seconds max.	265	°C

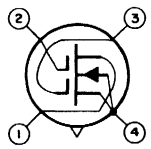
PERFORMANCE FEATURES

- large dynamic range permits large-signal handling before overload
- dual gates allow product mixing with extremely low harmonic generation
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors

DEVICE FEATURES

- extremely low feedback capacitance
  C_{rss} = 0.02 pF typ.
- high unneutralized RF power gain
  MUG = 25 dB (typ.) for 40603
- low noise figure
  NF = 2.5 dB typ. for 40603

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 40603 RF AMPLIFIER Typ.	40603 RF AMPLIFIER Max.	40604 MIXER Typ.	40604 MIXER Max.	UNITS
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G2S} = +4 V	-2	--	-2	--	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G1S} = 0	-2	--	-2	--	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20 V, V_{G2S} = 0, V_{DS} = 0	--	1	--	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20 V, V_{G1S} = 0, V_{DS} = 0	--	1	--	1	nA
Zero-Bias-Voltage Drain Current	I_{DSS}	V_{G2S} = +4 V, V_{G1S} = 0, V_{DS} = +13 V	18	--	18	--	mA
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate-No.1)	C_{rss}	V_{DS} = +13 V, I_D = 10 mA, f = 1 MHz, V_{G2S} = +4 V	0.02	0.03	0.02	0.03	pF
Input Capacitance	C_{iss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	5.5	--	5.5	--	pF
Output Capacitance	C_{oss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz	2.1	--	2.3	--	pF
Input Resistance	r_{is}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz	3.5	--	3.5	--	kΩ
Output Resistance	r_{os}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz	4	--	--	--	kΩ
		V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 10.7 MHz	--	--	20	--	kΩ
Forward Transconductance	g_{fs}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	10,000	--	2800*	--	μmho
Maximum Available Power Gain	MAG	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz, f_{out} for 40604 (mixer) = 10.7 MHz	26	--	21	--	dB
Maximum Usable Power Gain (Unneutralized)	MUG		25▲	-	--	--	dB
Noise Figure	NF		2.5	--	--	--	dB

* conversion transconductance

▲ or limited by practical design considerations

For characteristics curves, refer to type 3N140.

40673

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR
N-Channel Depletion Type With Integrated Gate-Protection Circuits
For RF Amplifier Applications up to 400 MHz

RCA-40673 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS* pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 40673 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-40673 make it useful for a wide variety of rf-amplifier applications at frequencies up to 400 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two gate arrangement of the 40673 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 40673 is hermetically sealed in the metal JEDEC TO-72 package.

*Metal-Oxide-Semiconductor.

Maximum Ratings, *Absolute-Maximum Values, at T_A = 25°C*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +1	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
DRAIN CURRENT, I_D	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥1/32 inch from seating surface for 10 seconds max.	265	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G2S} = +4V	–	-2	-4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G1S} = 0	–	-2	-4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = +1 or -6 V, V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ±6V, V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = +15V, V_{G2S} = +4V, V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15V, I_D = 10mA, V_{G2S} = +4V, f = 1kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}	V_{DS} = +15V, I_D = 10mA, V_{G2S} = +4V, f=1MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1) ♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15V, I_D = 10mA, V_{G2S} = +4V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\lvert Y_{fs} \rvert$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	-35	–	degrees
Input Resistance	r_{iss}		–	1.0	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	$I_{DIODE(REVERSE)}$ = ±100μA	–	±10	–	V

*Limited only by practical design considerations.

†Capacitance between Gate No. 1 and all other terminals

♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

For characteristics curves, refer to type 3N187.

APPLICATIONS

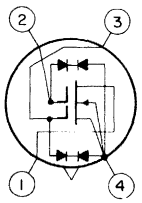
- RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment
- aircraft and marine vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

PERFORMANCE FEATURES

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in fm receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability

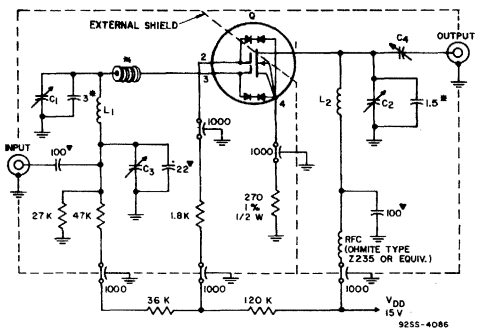
DEVICE FEATURES

- back-to-back diodes protect each gate against handling and in-circuit transients
- low gate leakage currents —— I_{G1SS} & I_{G2SS} = 20 nA(max.) at T_A = 25°C
- high forward transconductance —— g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain —— G_{ps} = 18 dB(typ.) at 200 MHz
- low VHF noise figure —— 3.5 dB(typ.) at 200 MHz



TERMINAL DIAGRAM

LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.
All resistors in ohms
All capacitors in pF

Q = 40673
▼ Disc ceramic.
*Tubular ceramic.

C_1: 1.8 – 8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈ .90 in. long.

Fig. 1. 200-MHz Power gain and noise-figure test circuit

40819

Silicon Dual-Insulated-Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

For RF Amplifier Applications up to 250 MHz

RCA-40819 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor (FET).

The excellent overall performance characteristics of the RCA-40819 make it useful for a wide variety of rf-amplifier applications at frequencies up to 250 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 40819 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac grounding Gate No.2. The reduced capacitance allows operation at maximum gain *without neutralization* and reduces local oscillator feedthrough to the antenna – features of special importance in rf and if amplifiers.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts and protect the gates against damage in all normal handling and usage.

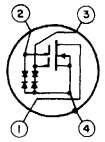
The back-to-back diode configuration permits the 40819 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The 25-volt drain-to-source rating permits the use of higher voltage power supplies.

The 40819 is hermtically sealed in the metal JEDEC TO-72 package.

TERMINAL DIAGRAM

LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE



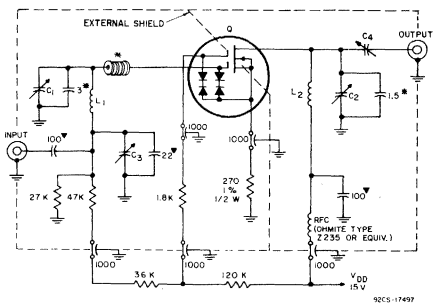
ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G2S} = +4 V	–	–2	–4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G1S} = 0	–	–2	–4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = ± 6 V, V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ± 6 V, V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = + 15 V, V_{G2S} = +4 V, V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	–35	–	degrees
Input Resistance	r_{iss}		–	1	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	I_{diode} (reverse) = ±100 μA	–	±10	–	V

* Limited only by practical design considerations.

† Capacitance between Gate No.1 and all other terminals.

♦ Three-terminal measurement with Gate No.2 and Source returned to guard terminal.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID; 0.063 in thickness.

Q = 40673

▼Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2*: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095-in wide, 5/16-in; ID Coil = .90 in long.

Fig. 1. 200 MHz power gain and noise figure test circuit

For characteristics curves, refer to type 3N187.

Device Features

- **back-to-back diodes protect each gate against handling and in-circuit transients**
- **high forward transconductance: g_{fs} = 12,000 μmho (typ.)**
- **high unneutralized RF power gain: G_{ps} = 18 dB (typ.) at 200 MHz**
- **low VHF noise figure: 3.5 dB (typ.) at 200 MHz**
- **low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25° C**
- **increased drain-to-source voltage rating: V_{DS} = –0.2 to +25 V**

Performance Features

- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s**
- **wide dynamic range permits large-signal handling before overload**
- **virtually no agc power required**
- **greatly reduces spurious responses in FM receivers**
- **dual gate permits simplified AGC circuitry**

Applications

- **RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment**
- **aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **telemetry and multiplex equipment**

Absolute Maximum Values, at T_A = 25°C:

Drain-to-Source Voltage, V_{DS}	–0.2 to +25	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+31	V
Drain Current, I_D	50	mA
Transistor Dissipation, P_T:		
At T_A up to 25°C	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C	
Ambient Temperature Range:		
Operating and Storage	–65 to +175	°C
Lead Temperature (During Soldering):		
At distances 1/32 in from seating surface for 10 s max.	265	°C

Maximum Ratings

Continuous Working Voltage#, at T_A = 25°C:

Gate No.1-to-Source Voltage, V_{G1S}	–6 to +3	V
Gate No.2-to-Source Voltage, V_{G2S}	–6 to +6 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+25	V

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the absolute Maximum Ratings are not exceeded.

40820, 40821

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits
For VHF-TV Tuner Applications

40820 – RF Amplifier **40821** – Mixer

Device Features

- back-to-back diodes protect each gate against handling and in-circuit transients
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 17 dB (typ.) at 200 MHz (40820)
- low VHF noise figure: 3.5 dB (typ.) at 200 MHz (40820)
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA

RCA-40820 and 40821 are n-channel silicon, depletion type, dual-insulated-gate, MOS▲ field-effect transistors for RF amplifier (40820) and mixer (40821) applications in VHF-TV receivers and other commercial equipment operating at frequencies up to 250 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

Virtually no AGC power is required because of the high gate input resistance of the MOS FET types. Automatic AGC delay can be achieved with a very slight change in the input impedance by the application of AGC voltage to Gate No. 2.

▲ Metal-Oxide-Semiconductor.

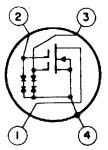
Performance Features

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- dual gate permits simplified AGC circuitry

The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a separate gate.

Integral back-to-back diodes protect the gates against damage in normal handling and usage by limiting transient voltages that exceed ±10 volts. The 40820 and 40821 are hermetically sealed in metal JEDEC TO-72 packages.

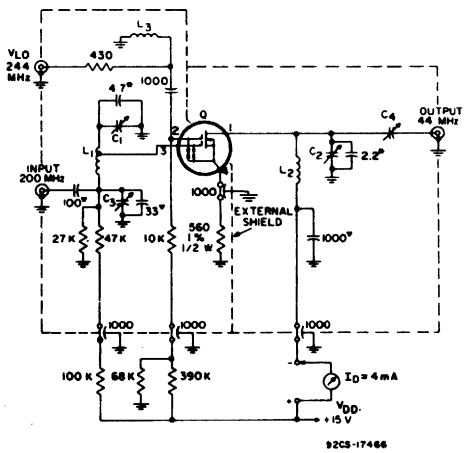
TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE, AND CASE

Maximum Ratings *Continuous Working Voltage#, at T_A = 25°C:*	**40820**	**40821**	
Gate No. 1-to-Source Voltage, V_{G1S}	−6 to +3	−4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or -4.5 to 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +20	−0.2 to +20	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+26	+24.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.



Q = 40821
▼Disc. ceramic.
* Tubular ceramic.
All resistors in ohms
All capacitors in pF

C_1, C_2: 1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.9–7 pF compression-type capacitor: ARCO 400 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"–0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-235 RF choke or equivalent

L_3: J. W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.1 – Conversion power gain test circuit for type 40821.

For characteristics curves, refer to type 3N187.

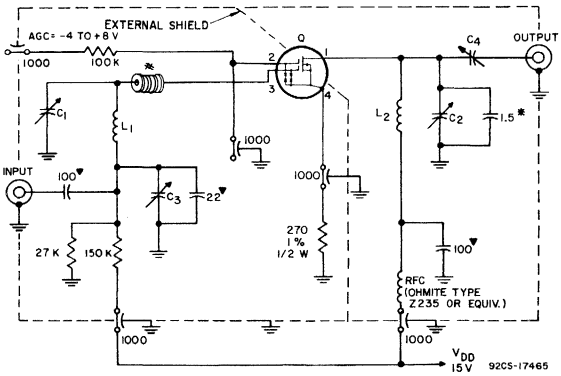
40820, 40821

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40820 Min.	40820 Typ.	40820 Max.	40821 Min.	40821 Typ.	40821 Max.	UNITS
Gate No. 1 to Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G2S}= +4V		–	–1	–3	–	–1	–3	V
Gate No. 2 to Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G1S}=0		–	–1	–3	–	–1	–3	V
Gate-to-Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} I_{G2SSF} 100 μA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} I_{G2SSR} 100 μA	V_{G2S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} V_{DS} 0	–	9	–	–	11	–	V
Gate No. 1 Terminal Forward Current	I_{G1SSF}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50	–	–	–	nA
			V_{G1S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 1 Terminal Reverse Current	I_{G1SSR}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	–	–	50	–	–	–	nA
			V_{G1S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 2 Terminal Forward Current	I_{G2SSF}	V_{DS} V_{G1S} 0	V_{G2S} 6 V	–	–	50	–	–	–	nA
			V_{G2S} 4.5 V	–	–	–	–	–	50	nA
Gate No. 2 Terminal Reverse Current	I_{G2SSR}	V_{DS} V_{G1S} 0	V_{G2S} –6 V	–	–	50	–	–	–	nA
			V_{G2S} 4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} +15 V, V_{G1S} 0, V_{G2S} +4 V		0.5	8	15	0.5	8	20	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} +15 V I_D 10 mA V_{G2S} +4 V	f 1 kHz	–	12000	–	–	12000	–	μmho
Small-Signal, Short-Circuit Input Capacitance♦	C_{iss}		f 1 MHz		6	8.5	–	6	9	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.02	0.03	0.005	0.02	0.04	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 6)	G_{PS}			14	17	–	–	–	–	dB
Noise Figure (see Fig. 6)	NF		f 200 MHz	–	4.5	6	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f 200/44 MHz	–	–	–	11	–	–	dB

♦ Capacitance between Gate No. 1 and all other terminals

♣ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID, 0.063 in thickness.

Q = 40820
▼ Disc ceramic.
* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095-in wide, 5/16-in; ID Coil ≈0.90 in. long.

Fig.2 – 200 MHz power gain and noise figure test circuit for type 40820.

Table 1 – y parameters vs. frequency

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 50	100	200	250	UNITS
Y Parameters						
Input Conductance	g_{is}	0.08	0.33	1.0	1.6	mmho
Input Susceptance	b_{is}	1.8	3.6	7.5	9.8	mmho
Magnitude Forward Transadmittance	$\|y_{fs}\|$	12	12	12	12.3	mmho
Angle of Forward Transadmittance	$<y_{fs}$	–2	–13	–35	–45	degrees
Output Conductance	g_{os}	0.10	0.18	0.36	0.42	mmho
Output Susceptance	b_{os}	0.5	1.0	2.0	2.6	mmho
Magnitude of Reverse Transadmittance	$\|y_{rs}\|$	8	12	25	40	μmho
Angle of Reverse Transadmittance	$<y_{rs}$	–88	-73	–25	–10	degrees

40822-40823

Silicon Dual-Insulated-Gate Field-Effect Transistors

N-Channel Depletion Types

With Integrated Gate-Protection Circuits

For FM Tuner Applications

40822 – RF Amplifier **40823** – Mixer

RCA-40822 and 40823 are n-channel silicon, depletion type, dual-insulated-gate, field-effect transistors for RF amplifier (40822) and mixer (40823) applications in FM receivers and other commercial equipment operating at frequencies up to 150 MHz.

These devices designed for VHF performance, provide excellent power gain, low-noise figures and have wide dynamic range. The dual-gate feature offers good cross-modulation performance over the AGC range and reduces feedback capacitance by shielding Gate No. 1 from the drain. The very low feedback capacitance also eliminates the need for circuit neutralization and reduces local oscillator feed-through to the antenna.

Virtually no power is required in AGC utilizing the 40822 and 40823. In addition, these devices minimize input impedance variations and automatically achieve AGC delay when AGC is applied to Gate No. 2. The dual-gate arrangement also makes it possible to isolate the local oscillator signal from the incoming signal by applying each signal to a specific gate.

Back-to-back diodes, diffused directly into the MOS pellet, protect the gates against damage in normal handling and usage by limiting transient voltages that exceed +10 volts. The 40822 and 40823 are hermetically sealed in metal JEDEC TO-72 packages.

Performance Features

- superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- wide dynamic range permits large-signal handling before overload
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- dual gate permits simplified AGC circuitry

Device Features

- back-to-back diodes protect each gate against handling and in-circuit transier
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high unneutralized RF power gain: G_{ps} = 24 dB (typ.) at 100 MHz (40822)
- low VHF noise figure: 2 dB (typ.) at 100 MHz (40822)
- low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25°C

Maximum Ratings

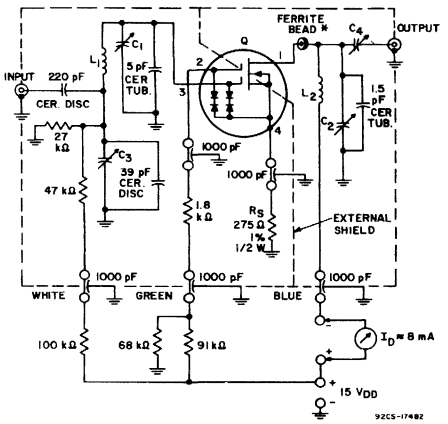
	40822	40823	
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	−6 to +3	−4.5 to +3	V
Gate No. 2-to-Source Voltage, V_{G2S}	-6 to +6 or 40% of V_{DS} (whichever value is less)	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	+20	V
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +18	−0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	+22.5	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C

Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40822 Min.	40822 Typ.	40822 Max.	40823 Min.	40823 Typ.	40823 Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G2S}= +4V		–	−2	−4	–	−2	−4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G1S}=0		–	−2	−4	–	−2	−4	V
Gate-to-Source Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0	–	9	–	–	11	–	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{DS} = V_{G2S} = 0	V_{G1S} = 6 V	–	–	50	–	–	–	nA
			V_{G1S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{DS} = V_{G2S} = 0	V_{G1S} = −6 V	–	–	50	–	–	–	nA
			V_{G1S} = −4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{DS} = V_{G1S} = 0	V_{G2S} = 6 V	–	–	50	–	–	–	nA
			V_{G2S} = 4.5 V	–	–	–	–	–	50	nA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{DS} = V_{G1S} = 0	V_{G2S} = -6 V	–	–	50	–	–	–	nA
			V_{G2S} = −4.5 V	–	–	–	–	–	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		5	15	30	5	15	35	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V I_D = 10 mA V_{G2S} = +4 V	f = 1 kHz	–	12000	–	–	12000	–	μmho
Small-Signal, Short-Circuit Input Capacitance †	C_{iss}		f = 1 MHz	–	6.5	9.5	–	6.5	10	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.020	0.030	0.005	0.025	0.045	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Power Gain (see Fig. 5)	G_{PS}			19	24	–	–	–	–	dB
Noise Figure (see Fig. 5)	NF		f = 100 MHz	–	2	3.5	–	–	–	dB
Conversion Gain	$G_{PS(C)}$		f = 100 to 10.7 MHz	–	–	–	14	18	–	dB

† Capacitance between Gate No. 1 and all other terminals.

♦ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.



1.3-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

2.7-19.6 pF variable air capacitor: E.F. Johnson Type 160-110 or equivalent.

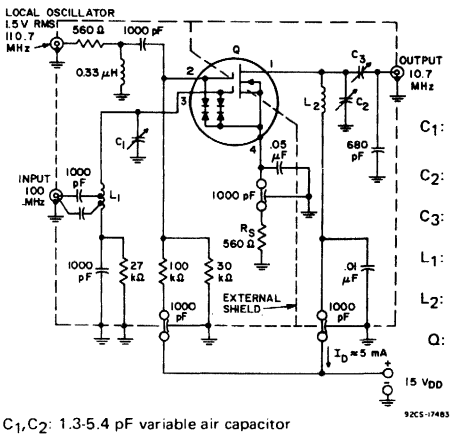
80 pF max. compression-type capacitor: Arco 405 or equivalent

8 turns No. 22 wire on 1/4" diameter air core. One turn spacing between windings. Tapped at one turn from low end.

37 turns No. 34 wire on 3/16" diameter air core. Unloaded Q = 63

40823.

Fig.1 - 100/10.7-MHz conversion power gain test circuit for type 40823.



C_1, C_2: 1.3-5.4 pF variable air capacitor

C_3: 1-10 pF variable air capacitor, piston type: Johanson Co., No. 4335

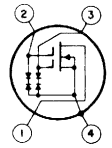
C_4: 1-15 pF variable air capacitor, precision piston type: Roanwell Corp. SG11129/AG

L_1, L_2: 0.22 μH RF choke (7T): Miller, No. 4584

*Ferramic toroid (1/2 used): Indiana General, No. CF101-(0-6)

Fig.2 - 100-MHz power gain and noise figure test circuit for type 40822.

TERMINAL DIAGRAM



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

For characteristics curves, refer to type 3N187.

40841

Silicon Dual-Insulated Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

General-Purpose Economy Type for Applications from DC to 500 MHz

RCA-40841 is an n-channel silicon, depletion type, dual-insulated gate, field-effect transistor intended for general-purpose applications from DC to frequencies up to 500 MHz.

This MOS/FET provides excellent power gain, linear-circuit operation and has a wide dynamic operating range. Its square-law characteristics result in low cross-modulation performance over the AGC range. Its dual-gate construction reduces feedback capacitance by shielding Gate No. 1 from the drain, and makes it possible to isolate the local oscillator signal from the incoming signal bv applying the two signals to separate gates. The very low feedback capacitance of this device eliminates the need for neutralization in circuits using the dual-gate configuration. Use of the device in the RF input stage of a receiver reduces local oscillator feed-through to the antenna. The 40841 requires negligible AGC power, provides automatic delay when AGC is applied to Gate No. 2, and exhibits slight input impedance variations during AGC functioning. The device has exceptionally high input impedance, an attribute for timing-circuit design.

Back-to-back diodes are fabricated on the same monolithic silicon pellet as the MOS/FET to protect the gates against damage due to electrostatic charges frequently encountered during normal handling. These back-to-back diodes also function as "transient trappers" by limiting in-circuit transient voltages that exceed ±10 volts.

Maximum ratings and electrical characteristics are included in the data for operation of the 40841 as the equivalent of a single-gate device. For single-gate operation, connect Gate No. 1 (Term. 2) to Gate No. 2 (Term. 3), as shown in the Terminal Diagrams on Page 2. The 40841 MOS/FET is hermetically sealed in the metal JEDEC TO-72 package.

Device Features:

- back-to-back diodes protect gate insulation against damage due to static changes frequently encountered during handling
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high power gain: G_{ps} = 32 dB (typ.) at 44 MHz
- gate leakage currents: I_{G1SS} and I_{G2SS} = 60 nA (max.) at T_A = 25°C
- high input impedance
- excellent thermal stability

Performance Features:

- superior cross-modulation performance and greater dynamic range than bipolar and junction-gate FETs
- wide dynamic range permits large-signal handling before overloading
- virtually no agc power required
- greatly reduced spurious responses in AM and FM receivers
- dual-gate configuration permits simplified AGC circuitry
- operates at frequencies to 500 MHz without neutralization in circuits utilizing the dual-gate configuration
- operates up to UHF with low-noise performance

The following dual-gate MOS/FET types are specified for applications requiring premimum-grade performance: 3N200, 3N187, 40673, 40819, 40820, 40821, 40822, and 40823.

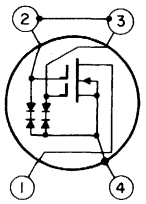
Detailed information, utilizing RCA dual-gate protected MOS/FETs in RF applications, is given in the following RCA Application Notes: AN-4431 "RF Applications of the Dual-Gate MOS/FET up to 500 MHz" and AN-4018 "Design of Gate-Protected MOS Field-Effect Transistors".

Applications:

- DC amplifiers
- RF amplifiers
- mixers
- IF amplifiers
- video amplifiers
- differential amplifiers
- frequency multipliers
- phase splitters
- choppers
- voltage-controlled attenuators
- constant-current source
- voltage regulators
- telemetry & multiplex
- servo amplifiers
- proximity switches
- industrial timers — long time delays
- thyristor trigger circuits

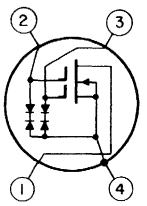
TERMINAL DIAGRAMS

SINGLE-GATE CONFIGURATION



LEAD 1—DRAIN
LEADS—2 AND 3—GATE
LEAD 4—SOURCE, SUBSTRATE AND CASE

DUAL-GATE CONFIGURATION



LEAD 1—DRAIN
LEAD 2—GATE No.2
LEAD 3—GATE No.1
LEAD 4—SOURCE SUBSTRATE AND CASE

Maximum Ratings

	Dual-Gate Configuration	Single-Gate Configuration	
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +18	−0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	—	μA
Gate Terminal Current, I_{GS}	—	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	—	V
Drain-to-Gate Voltage, V_{DG}	—	+24	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	−4.5 to +3	—	V
Gate No. 2-to-Source Voltage, V_{G2S}	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	—	V
Gate-to-Source Voltage, V_{GS}	—	−4.5 to +3	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	—	V
Drain-to-Gate Voltage, V_{DG}	—	+20	V

#Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

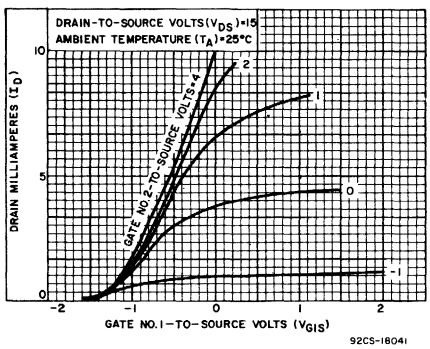


Fig.1—I_D vs. V_{G1S}.

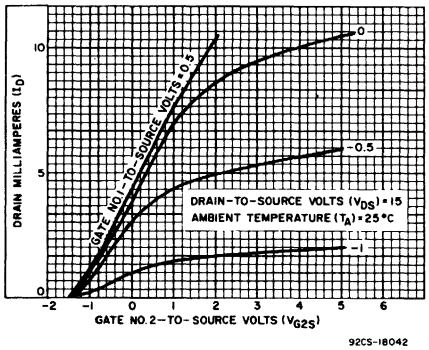


Fig.2—I_D vs. V_{G2S}.

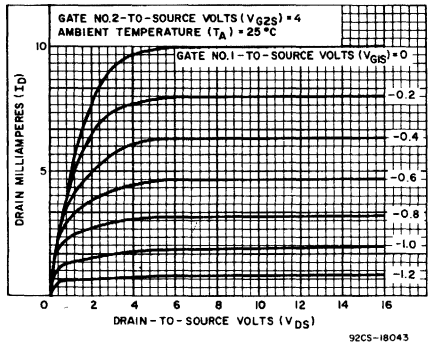


Fig.3—I_D vs. V_{DS}.

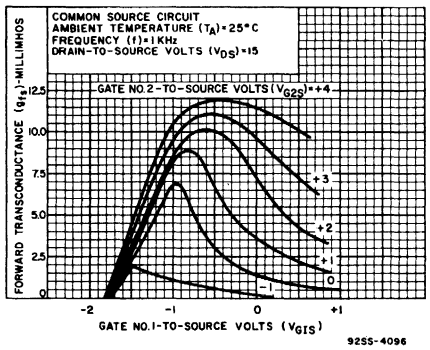


Fig.4—g_{fs} vs. V_{G1S}.

40841

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CONFIGURATION DUAL-GATE MIN.	DUAL-GATE TYP.	DUAL-GATE MAX.	SINGLE-GATE MIN.	SINGLE-GATE TYP.	SINGLE-GATE MAX.	UNITS
Gate-to-Source Cutoff Voltage:										
Dual-Gate (No. 1)	$V_{G1S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G2S} = +4V		–	-2	–	–	–	–	V
Dual-Gate (No. 2)	$V_{G2S(off)}$	V_{DS} = +15V, I_D = 200μA, V_{G1S} = 0		–	-2	–	–	–	–	V
Single Gate	$V_{GS(off)}$	V_{DS} = +15V, I_D = 200μA		–	–	–	–	-1.8	–	V
Gate-to-Source Forward Breakdown Voltage:		I_{G1SSF} =								
Dual-Gate (No. 1)	$V_{(BR)G1SSF}$	I_{G2SSF} =	V_{G2S} = V_{DS} = 0	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSF}$	100μA	V_{G1S} = V_{DS} = 0	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSF}$	I_{GSSF} = 100μA, V_{DS} = 0		–	–	–	–	9	–	V
Gate-to-Source Reverse Breakdown Voltage:		I_{G1SSR} =								
Dual-Gate (No. 1)	$V_{(BR)G1SSR}$	I_{G2SSR} =	V_{G2S} = V_{DS} = 0	–	9	–	–	–	–	V
Dual-Gate (No. 2)	$V_{(BR)G2SSR}$	100μA	V_{G1S} = V_{DS} = 0	–	9	–	–	–	–	V
Single-Gate	$V_{(BR)GSSR}$	I_{GSSR} = 100μA, V_{DS} = 0		–	–	–	–	9	–	V
Gate Terminal Forward Current:										
Dual-Gate (No. 1)	I_{G1SSF}	V_{DS} = V_{G2S} = 0, V_{G1S} = 6 V		–	–	60	–	–	–	nA
Dual Gate (No. 2)	I_{G2SSF}	V_{DS} = V_{G1S} = 0, V_{G2S} = 6 V		–	–	60	–	–	–	nA
Single-Gate	I_{GSSF}	V_{DS} = 0, V_{GS} = 6 V		–	–	–	–	–	120	nA
Gate Terminal Reverse Current:										
Dual-Gate (No. 1)	I_{G1SSR}	V_{DS} = V_{G2S} = 0, V_{G1S} = -6 V		–	–	60	–	–	–	nA
Dual-Gate (No. 2)	I_{G2SSR}	V_{DS} = V_{G1S} = 0, V_{G2S} = -6 V		–	–	60	–	–	–	nA
Single-Gate	I_{GSSR}	V_{DS} = 0, V_{GS} = -6 V		–	–	–	–	–	120	nA
Zero-Bias Drain Current:										
Dual-Gate	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		–	10	–	–	–	–	mA
Single-Gate	I_{DSS}	V_{DS} = +15 V, V_{GS} = 0		–	–	–	–	3.7	–	mA
Forward Transconductance (Gate-to-Drain)†										
Dual-Gate	g_{fs}		1 kHz	–	12000	–	–	–	–	μmho
Single-Gate	g_{fs}			–	–	–	–	7000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	–	6.5	–	–	11	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}	V_{DS} = +15 V, I_D = 10 mA, [Dual-Gate only V_{G2S} = +4 V]		–	0.02	–	–	0.54	–	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2	–	–	2	–	pF
Audio Spot Noise Figure*										
Dual-Gate	NF		f = 1 kHz	–	0.46	–	–	–	–	dB
Single-Gate	NF		f = 1 kHz	–	–	–	–	0.29	–	dB
Power Gain	G_{ps}		44 MHz	–	32	–	–	–	–	dB
Conversion Gain	$G_{ps(C)}$			–	24	–	–	–	–	dB

† Capacitance between Gate No. 1 and all other terminals (Dual-Gate), Gate and all other terminals (Single-Gate)

♦ Three-terminal measurement with Gate No. 2 and Source returned to guard terminal (Dual-Gate)

* Noise Figure = $10 \log_{10}\left[1 + \frac{e_n^2}{4\,KT\,BW\,R_g}\right]$ where K = 1.38×10^{-23}. T = Temperature in °Kelvin; BW = Bandwidth in Hz; R_g = Generator resistance

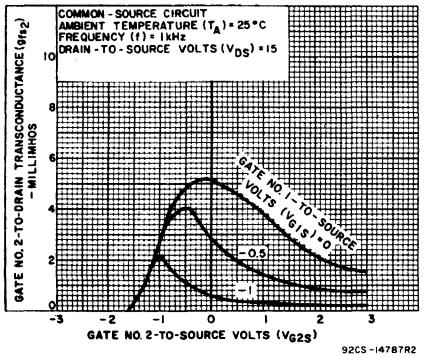


Fig.5—g_{fs2} vs. V_{G2S}.

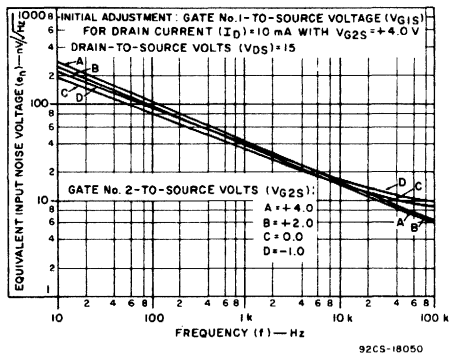


Fig.6—e_n vs. f.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE CONFIGURATION
(Terminals 2 and 3 tied together to comprise effective single-gate)

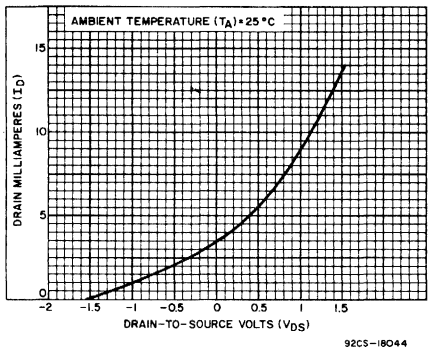


Fig.7—I_D vs. V_{DS}.

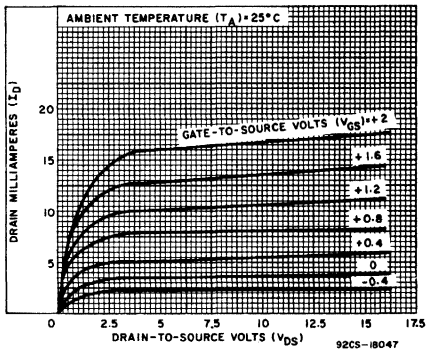


Fig.8—I_D vs. V_{DS}.

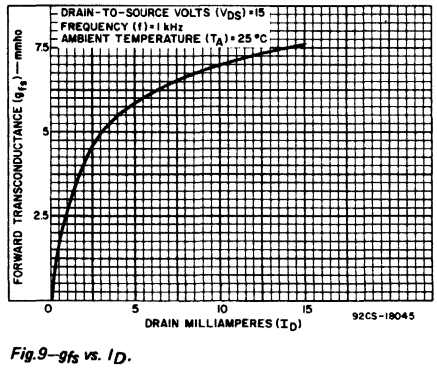


Fig.9—g_{fs} vs. I_D.

TYPICAL CHARACTERISTICS FOR 40841 IN SINGLE-GATE & DUAL-GATE CONFIGURATION

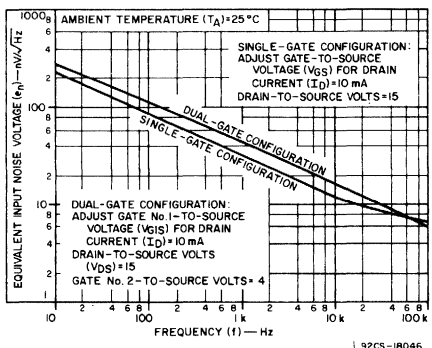


Fig.10—e_n vs. f.

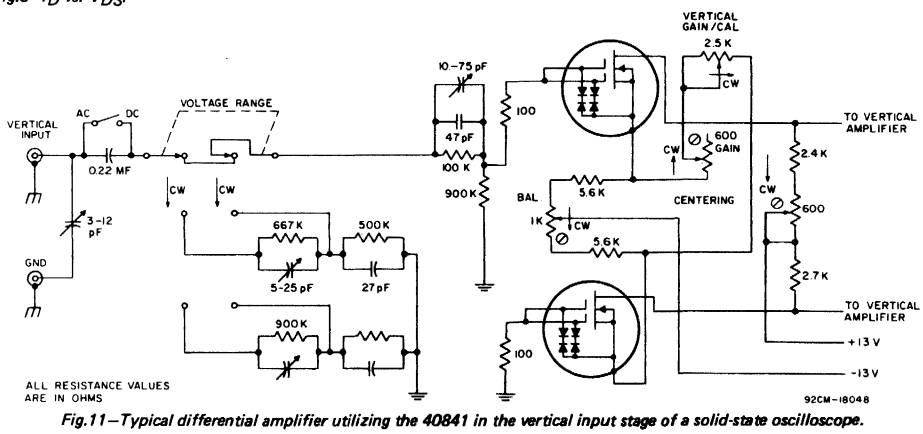
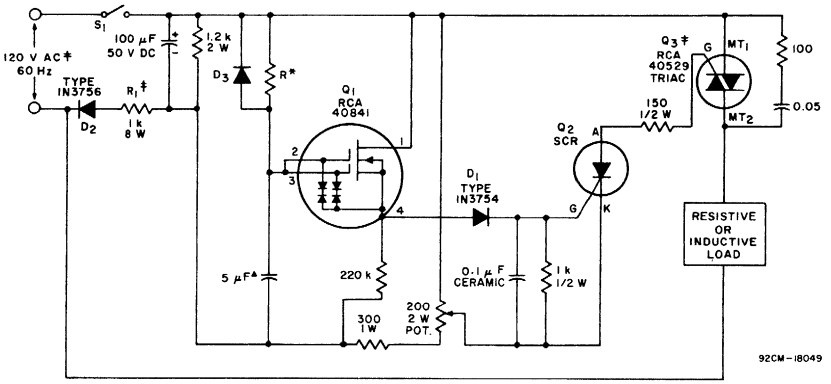


Fig.11—Typical differential amplifier utilizing the 40841 in the vertical input stage of a solid-state oscilloscope.

40841

SOLID-STATE TIMER FOR INDUSTRIAL APPLICATIONS



▲ Cornell-Dubilier Electronics—Type MMW or equivalent.

• R controls duration of time delay. At R = 60 MΩ up to 5-minute delay (IRC resistor, Type CGH or equivalent)

‡ This circuit can also be used at supply voltages of 240 V AC and 24V AC (60Hz) by changing the values of R1 and Q3.

TIMING CIRCUIT CHARACTERISTICS

T_A = −25°C to +60°C

Accuracy: ±10% (over temperature)

Repeatability: ±3% (at 25°C)

Reset Time: Less than 150 ms

Q2: V_{DRM} = 60V
I_{GT} = 200μA
I_T = 0.8A

D3: I_R = 1 nA
V_R = 60V

Fig.12—Typical timing circuit utilizing the 40841 in a single-gate configuration.

COS/MOS Digital Integrated Circuits

COS/MOS IC Standard (CD4000A) Series Function Classification Chart

GATES						MULTIVIBRATORS	
SINGLE-LEVEL			MULTI-LEVEL				
NOR/NAND	OR/AND	BUFFERS & INVERTERS	MULTIFUNCTION/ AOI	DECODERS/ ENCODERS	SCHMITT TRIGGER	FLIP-FLOPS/ LATCHES	ASTABLE/ MONOSTABLE
CD4000A CD4001A CD4002A CD4011A CD4012A CD4023A CD4025A		CD4007A CD4009A CD4010A CD4041A CD4049A CD4050A	CD4019A CD4030A■ CD4037A CD4048A ■See Comparators	CD4028A		CD4013A CD4027A CD4042A CD4043A CD4044A	CD4047A

REGISTERS			COUNTERS		DISPLAY DRIVERS		
SHIFT	STORAGE	FIFO BUFFER	BINARY RIPPLE	SYNCHRONOUS	WITH COUNTER	FOR LCD☆ DRIVE	FOR LED●● DRIVE
Static CD4006A CD4014A CD4015A CD4021A CD4031A CD4034A CD4035A Dynamic CD4062A			CD4020A CD4024A CD4040A CD4045A CD4060A	CD4017A CD4018A CD4022A CD4029A CD4059A	CD4026A CD4033A		

MULTIPLEXERS/ DEMULTIPLEXERS	PHASE-LOCKED LOOP	ARITHMETIC CIRCUITS				MEMORIES RAM'S		QUAD BILATERAL SWITCHES
ANALOG/ DIGITAL DATA SELECTORS		ADDERS/ COMPARATORS	ALU/RATE MULTIPLIERS	PARITY GENERATOR/ CHECKER	MULTIPORT REGISTER	WORD-ORGANIZED	BIT-ORGANIZED	
CD4016A▲ CD4019A‡ CD4066A▲ ‡See Multifunction A01 ▲See Quad Bilateral Switch	CD4046A	CD4008A CD4032A CD4038A CD4030A♦ ♦See Multifunction/ AOI	CD4057A			CD4036A CD4039A	CD4061A	CD4016A♦ CD4066A♦ ♦See Multiplexers

☆ Liquid Crystal Display ●● Light-Emitting Diode

COS/MOS IC High-Voltage (CD4000B) Series Function Classification Chart

GATES						MULTIVIBRATORS	
SINGLE-LEVEL			MULTI-LEVEL				
NOR/NAND	OR/AND	BUFFERS & INVERTERS	MULTIFUNCTION/ AOI	DECODERS/ ENCODERS	SCHMITT TRIGGER	FLIP-FLOPS/ LATCHES	ASTABLE/ MONOSTABLE
CD4000B CD4001B CD4002B CD4011B CD4012B CD4023B CD4025B CD4068B CD4078B CD40107B	CD4071B CD4072B CD4073B CD4075B CD4081B CD4082B	CD4009B CD4010B CD4041B CD4049B CD4050B CD4069B CD4502B CD40107B Level Shifter CD40109B	CD4070B■ CD4077B■ CD4085B CD4086B ■See Comparators	CD4514B CD4515B CD4532B CD4555B★ CD4556B★ ★See Demultiplexers	CD4093B	CD4013B CD4027B CD4042B CD4043B CD4044B CD4076B** CD4095B CD4096B CD4099B** CD4508B **See Storage Registers	CD4098B

REGISTERS			COUNTERS		DISPLAY DRIVERS		
SHIFT	STORAGE	FIFO BUFFER	BINARY RIPPLE	SYNCHRONOUS	WITH COUNTER	FOR LCD☆ DRIVE	FOR LED●● DRIVE
Static CD4094B CD40100B CD40104B CD40194B	CD4076B CD4099B CD40108B● ●See Multiport Register	CD40105B		CD4510B CD4516B CD4518B CD4520B CD40102B CD40103B CD40192B CD40193B		CD4054B CD4055B CD4056B	CD4511B

MULTIPLEXERS/ DEMULTIPLEXERS	PHASE-LOCKED LOOP	ARITHMETIC CIRCUITS				MEMORIES RAM'S		QUAD BILATERAL SWITCHES
ANALOG/ DIGITAL DATA SELECTORS		ADDERS/ COMPARATORS	ALU/RATE MULTIPLIERS	PARITY GENERATOR/ CHECKER	MULTIPORT REGISTER	WORD-ORGANIZED	BIT-ORGANIZED	
CD4016B▲ CD4051B CD4052B CD4053B CD4067B CD4097B CD4555B⊕ CD4556B⊕ CD40257B ▲See Quad Bilateral Switch ⊕See Decoders/ Encoders		CD4008B CD4063B CD4070B♦ CD4077B♦ ♦See Multifunction/ AOI	CD4089B CD4527B CD40181B CD40182B	CD40101B	CD40108B	CD40108B●		CD4016B♦ ♦See Multiplexers

☆ Liquid Crystal Display ●● Light-Emitting Diode

Replacement Guide

For information on the package types available for any given type, refer to the manufacturer's published data. RCA Similar Type may not be identical with other Mfg. Type in every detail. Refer to manufacturer's published date for further information.

Analog Devices Type	RCA Similar Type
AD7502	CD4052
AD7506	CD4067
AD7507	CD4097

Fairchild Semiconductor Type	RCA Similar Type
4528	CD4098
4581	CD40181
4582	CD40182
34001	CD4001
34002	CD4002
34006	CD4006
34007	CD4007
34008	CD4008
34011	CD4011
34012	CD4012
34013	CD4013
34014	CD4014
34015	CD4015
34016	CD4016
34017	CD4017
34018	CD4018
34019	CD4019
34020	CD4020
34021	CD4021
34022	CD4022
34023	CD4023
34024	CD4024
34025	CD4025
34027	CD4027
34028	CD4028
34029	CD4029
34030	CD4030
	CD4070
34035	CD4035
34040	CD4040
34041	CD4041
34042	CD4042
34043	CD4043
34044	CD4044
34046	CD4046
34049	CD4049
34050	CD4050
34051	CD4051
34052	CD4052
34053	CD4053
34066	CD4066
34067	CD4067
34068	CD4068
34069	CD4069
34070	CD4070
34071	CD4071
34072	CD4072
34073	CD4073
34075	CD4075
34076	CD4076
34077	CD4077
34078	CD4078
34081	CD4081
34082	CD4082
34085	CD4085
34086	CD4086
34097	CD4097
34099	CD4099
34104	CD40104
34510	CD4510
34511	CD4511
34514	CD4514
34515	CD4515
34516	CD4516
34518	CD4518
34520	CD4520
34527	CD4527
34528	CD4098
34532	CD4532

Fairchild Semiconductor Type	RCA Similar Type
34555	CD4555
34556	CD4556
34585	CD4063
34703	CD40105
34731	CD4031
340083	CD4008
340085	CD4063
340192	CD40192
340193	CD40193
340194	CD40194
34710	CD4036
34710	CD4039
34720	CD4061

General Instrument Type	RCA Similar Type
MEM4001	CD4001
MEM4007	CD4007
MEM4011	CD4011
MEM4013	CD4013
MEM4016	CD4016
MEM4016	CD4066
MEM4049	CD4049
MEM4050	CD4050
MEM4051	CD4051
MEM4053	CD4053

Harris Semiconductor Type	RCA Similar Type
HD74C00	CD4011
HD74C02	CD4001
HD74C04	CD4069
HD74C10	CD4023
HD74C20	CD4012
HD74C42	CD4028
HD74C74	CD4013
HD74C76	CD4027
HD74C173	CD4076
HD74C192	CD40192
HD74C193	CD40193
HD4000	CD4000
HD4001	CD4001
HD4002	CD4002
HD4006	CD4006
HD4007	CD4007
HD4008	CD4008
HD4009	CD4009
HD4010	CD4010
HD4011	CD4011
HD4012	CD4012
HD4013	CD4013
HD4014	CD4014
HD4015	CD4015
HD4016	CD4016
HD4017	CD4017
HD4018	CD4018
HD4019	CD4019
HD4020	CD4020
HD4021	CD4021
HD4022	CD4022
HD4023	CD4023
HD4024	CD4024
HD4025	CD4025
HD4027	CD4027
HD4028	CD4028
HD4029	CD4029
HD4030	CD4030
	CD4070
HD4035	CD4035
HD4040	CD4040
HD4049	CD4049
HD4050	CD4050

Harris Semiconductor Type	RCA Similar Type
HD4066	CD4066
HD4093	CD4093
HD4094	CD4094
HD4507	CD4097
HD4518	CD4518
HD4520	CD4520
HD4529	CD4052
HD4811	CD4077
HD4814	CD4069
HI506A	CD4067
HI507A	CD4097
HI508A	CD4051
HI509A	CD4052
HI1818A	CD4051
HI1828A	CD4052

Intersil Type	RCA Similar Type
TM6523	CD4061

Motorola Type	RCA Similar Type
MC14000	CD4000
MC14001	CD4001
MC14002	CD4002
MC14006	CD4006
MC14007	CD4007
MC14008	CD4008
MC14011	CD4011
MC14012	CD4012
MC14013	CD4013
MC14014	CD4014
MC14015	CD4015
MC14016	CD4016
MC14017	CD4017
MC14020	CD4020
MC14021	CD4021
MC14022	CD4022
MC14023	CD4023
MC14024	CD4024
MC14025	CD4025
MC14027	CD4027
MC14028	CD4028
MC14032	CD4032
MC14034	CD4034
MC14035	CD4035
MC14038	CD4038
MC14040	CD4040
MC14042	CD4042
MC14043	CD4043
MC14044	CD4044
MC14046	CD4046
MC14049	CD4049
MC14049	CD4009
MC14050	CD4050
MC14050	CD4010
MC14051	CD4051
MC14052	CD4052
MC14053	CD4053
MC14066	CD4066
MC14068	CD4068
MC14069	CD4069
MC14070	CD4070
MC14071	CD4071
MC14072	CD4072
MC14073	CD4073
MC14075	CD4075
MC14076	CD4076
MC14077	CD4077
MC14078	CD4078
MC14081	CD4081
MC14082	CD4082

Motorola Type	RCA Similar Type
MC14501	CD4068
MC14502	CD4502
MC14506	CD4085
MC14507	CD4030
MC14507	CD4070
MC14508	CD4508
MC14510	CD4510
MC14510	CD4029
MC14510	CD40192
MC14511	CD4511
MC14514	CD4514
MC14515	CD4515
MC14516	CD4516
MC14516	CD40193
MC14518	CD4518
MC14519	CD4019
MC14520	CD4520
MC14521	CD4045
MC14522	CD4018
MC14525	CD4089
MC14527	CD4527
MC14528	CD4098
MC14529	CD4067
MC14531	CD40101
MC14532	CD14532
MC14543	CD4056
MC14555	CD4555
MC14556	CD4556
MC14557	CD4031
MC14558	CD4055
MC14562	CD4062
MC14569	CD4059
MC14572	CD4069
MC14580	CD40108
MC14581	CD40181
MC14581	CD4057
MC14582	CD40182
MC14583	CD40100
MC14584	CD4016
MC14585	CD4063
MCM14537	CD4061

National Type	RCA Similar Type
MM14511	CD4511
MM74C00	CD4011
MM74C02	CD4001
MM74C04	CD4069
MM74C08	CD4081
MM74C10	CD4023
MM74C20	CD4012
MM74C30	CD4068
MM74C32	CD4071
MM74C42	CD4028
MM74C74	CD4013
MM74C76	CD4027
MM74C83	CD4008
MM74C85	CD4063
MM74C86	CD4030
	CD4070
MM74C173	CD4076
MM74C192	CD40192
MM74C193	CD40193
MM74C200	CD4061
MM74C221	CD4098
MM4000	CD4000
MM4001	CD4001
MM4002	CD4002
MM4006	CD4006
MM4007	CD4007
MM4008	CD4008
MM4009	CD4009
MM4010	CD4010
MM4011	CD4011

National Type	RCA Similar Type
MM4012	CD4012
MM4013	CD4013
MM4014	CD4014
MM4015	CD4015
MM4016A	CD4016
MM4017	CD4017
MM4018	CD4018
MM4019	CD4019
MM4020	CD4020
MM4021	CD4021
MM4022	CD4022
MM4023	CD4023
MM4024	CD4024
MM4025	CD4025
MM4027	CD4027
MM4028	CD4028
MM4029	CD4029
MM4030	CD4030
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MM4031	CD4031
MM4035	CD4035
MM4040	CD4040
MM4042	CD4042
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MM4051	CD4051
MM4052	CD4052
MM4053	CD4053
MM4066	CD4066
MM4069	CD4069
MM4070	CD4070
MM4076	CD4076
MM4086	CD4086
MM4510	CD4510
MM4511	CD4511
MM4516	CD4516
MM4518	CD4518
MM4520	CD4520
MM4601	CD4001
MM4602	CD4002
MM4606	CD4006
MM4607	CD4007
MM4609	CD4009
MM4610	CD4010
MM4611	CD4011
MM4612	CD4012
MM4613	CD4013
MM4614	CD4014
MM4616	CD4016
	CD4066
MM4617	CD4017
MM4619	CD4019
MM4620	CD4020
MM4621	CD4021
MM4622	CD4022
MM4623	CD4023
MM4624	CD4024
MM4625	CD4025
MM4627	CD4027
MM4630	CD4030
MM4635	CD4035
MM4649	CD4049
MM4650	CD4050
MM4676	CD4076
MM40106	CD40106
MM40192	CD40192
MM40193	CD40193

Ragen Type	RCA Similar Type
MS504	CD4051
MS612	CD4006

Replacement Guide (Cont'd)

SGS Type	RCA Similar Type
HBF4001	CD4001
HBF4002	CD4002
HBF4007	CD4007
HBF4008	CD4008
HBF4009	CD4009
HBF4010	CD4010
HBF4011	CD4011
HBF4012	CD4012
HBF4013	CD4013
HBF4014	CD4014
HBF4016	CD4016
	CD4066
HBF4017	CD4017
HBF4020	CD4020
HBF4021	CD4021
HBF4022	CD4022
HBF4023	CD4023
HBF4024	CD4024
HBF4025	CD4025
HFB4027	CD4027
HBF4028	CD4028
HBF4029	CD4029
HBF4035	CD4035

Signetics Type	RCA Similar Type
N4000	CD4000
N4001	CD4001
N4002	CD4002
N4006	CD4006
N4007	CD4007
N4009	CD4009
N4010	CD4010
N4011	CD4011
N4012	CD4012
N4013	CD4013
N4015	CD4015
N4016	CD4016
N4019	CD4019
N4021	CD4021
N4023	CD4023
N4025	CD4025
N4027	CD4027
N4030	CD4030
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N4049	CD4049
N4050	CD4050
N4066	CD4066
N4068	CD4068
N4069	CD4069
N4071	CD4071
N4072	CD4072
N4073	CD4073
N4075	CD4075
N4078	CD4078
N4081	CD4081
N4528	CD4098

Solid State Scientific Type	RCA Similar Type
SCL4000	CD4000
SCL4001	CD4001
SCL4002	CD4002
SCL4006	CD4006
SCL4007	CD4007
SCL4008	CD4008
SCL4009	CD4009
SCL4010	CD4010
SCL4011	CD4011
SCL4012	CD4012
SCL4013	CD4013
SCL4014	CD4014
SCL4015	CD4015
SCL4016	CD4016
	CD4066
SCL4017	CD4017
SCL4018	CD4018
SCL4019	CD4019
SCL4020	CD4020

Solid State Scientific Type	RCA Similar Type
SCL4021	CD4021
SCL4022	CD4022
SCL4023	CD4023
SCL4024	CD4024
SCL4025	CD4025
SCL4026	CD4026
SCL4027	CD4027
SCL4028	CD4028
SCL4029	CD4029
SCL4030	CD4030
SCL4030	CD4070
SCL4033	CD4033
SCL4034	CD4034
SCL4035	CD4035
SCL4040	CD4040
SCL4041	CD4041
SCL4042	CD4042
SCL4043	CD4043
SCL4044	CD4044
SCL4045	CD4045
SCL4046	CD4046
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SCL4050	CD4050
SCL4051	CD4051
SCL4052	CD4052
SCL4053	CD4053
SCL4060	CD4060
SCL4066	CD4066
SCL4069	CD4069
SCL4070	CD4070
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SCL4072	CD4072
SCL4073	CD4073
SCL4075	CD4075
SCL4076	CD4076
SCL4081	CD4081
SCL4082	CD4082
SCL4302	CD4085
SCL4302	CD4086
SCL4402	CD4048
SCL4412	CD4068
SCL4445	CD4045
SCL4449	CD4069
SCL4502	CD4502
SCL4510	CD4510
SCL4511	CD4511
SCL4514	CD4514
SCL4515	CD4515
SCL4516	CD4516
SCL4518	CD4518
SCL4520	CD4520
SCL4528	CD4098
SCL4585	CD4063
SCL5520	CD4061
SCL4527	CD4527
SCL4555	CD4555
SCL4556	CD4556

Stewart Warner Type	RCA Similar Type
SW4001	CD4001
SW4002	CD4002
SW4011	CD4011
SW4012	CD4012
SW4013	CD4013
SW4015	CD4015
SW4016	CD4016
	CD4066
SW4017	CD4017
SW4019	CD4019
SW4020	CD4020
SW4021	CD4021
SW4023	CD4023
SW4024	CD4024
SW4025	CD4025
SW4027	CD4027
SW4028	CD4028
SW4029	CD4029
SW4030	CD4030
	CD4070

Stewart Warner Type	RCA Similar Type
SW4049	CD4049
SW4050	CD4050

Solitron Type	RCA Similar Type
CM4000	CD4000
CM4001	CD4001
CM4002	CD4002
CM4006	CD4006
CM4007	CD4007
CM4008	CD4008
CM4009	CD4009
CM4010	CD4010
CM4011	CD4011
CM4012	CD4012
CM4013	CD4013
CM4014	CD4014
CM4015	CD4015
CM4016	CD4016
	CD4066
CM4017	CD4017
CM4018	CD4018
CM4019	CD4019
CM4020	CD4020
CM4021	CD4021
CM4022	CD4022
CM4023	CD4023
CM4024	CD4024
CM4025	CD4025
CM4026	CD4026
CM4027	CD4027
CM4028	CD4028
CM4029	CD4029
CM4030	CD4030
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CM4032	CD4032
CM4033	CD4033
CM4034	CD4034
CM4035	CD4035
CM4036	CD4036
CM4037	CD4037
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CM4039	CD4039
CM4040	CD4040
CM4041	CD4041
CM4042	CD4042
CM4043	CD4043
CM4044	CD4044
CM4045	CD4045
CM4047	CD4047
CM4048	CD4048
CM4049	CD4049
CM4050	CD4050
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CM4052	CD4052
CM4053	CD4053
CM4066	CD4066
CM4068	CD4068
CM4069	CD4069
CM4070	CD4070
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CM4073	CD4073
CM4075	CD4075
CM4076	CD4076
CM4077	CD4077
CM4078	CD4078
CM4081	CD4081
CM4508	CD4508
CM4510	CD4510
CM4511	CD4511
CM4514	CD4514
CM4515	CD4515
CM4518	CD4518
CM4520	CD4520

Teledyne Type	RCA Similar Type
MM74C00	CD4011
MM74C02	CD4001
MM74C04	CD4069

Teledyne Type	RCA Similar Type
MM74C10	CD4023
MM74C20	CD4012
MM74C42	CD4028
MM74C74	CD4013
MM74C76	CD4027
MM74C173	CD4076
MM74C192	CD40192
MM74C193	CD40193

Texas Instruments Type	RCA Similar Type
TP4000	CD400
TP4001	CD4001
TP4002	CD4002
TP4007	CD4007
TP4008	CD4008
TP4009	CD4009
TP4010	CD4010
TP4011	CD4011
TP4012	CD4012
TP4013	CD4013
TP4014	CD4014
TP4015	CD4015
TP4016	CD4016
	CD4066
TP4017	CD4017
TP4018	CD4018
TP4019	CD4019
TP4020	CD4020
TP4021	CD4021
TP4022	CD4022
TP4023	CD4023
TP4024	CD4024
TP4025	CD4025
TP4027	CD4027
TP4028	CD4028
TP4029	CD4029
TP4035	CD4035
TP4040	CD4040
TP4042	CD4042
TP4043	CD4043
TP4044	CD4044
TP4049	CD4049
TP4050	CD4050
TP4051	CD4051
TP4052	CD4052
TP4053	CD4053
TP4071	CD4071
TP4072	CD4072
TP4073	CD4073
TP4075	CD4075
TP4076	CD4076
TP4077	CD4077
TP4081	CD4081
TP4082	CD4082
TP4085	CD4085
TP4305	CD4093
TP4315	CD4069
TP4320	CD4067
TP4507	CD4030
	CD4070
TP4518	CD4518
TP4520	CD4520

T^2L Type No.	COS/MOS Functionally Equivalent Type No.
7400	CD4011
7401	CD40107
7402	CD4001
7404	CD4009, CD4049
7404	CD4069
7406	CD4009, CD4049
7407	CD4010, CD4050
7408	CD4081
7410	CD4023
7411	CD4073
7420	CD4012
7425	CD4002
7427	CD4025

T^2L Type No.	COS/MOS Functionally Equivalent Type No.
7428	CD4001
7430	CD4068
7432	CD4071
7437	CD4011
7440	CD4012
7442	CD4028
7445	CD4028
7446	CD4511, CD4055
7447	CD4511, CD4055
7448	CD4511, CD4055
7449	CD4511, CD4055
7450	CD4085
7453	CD4086
7454	CD4086
7470	CD4096
7472	CD4095
7473	CD4027
7474	CD4013
7475	CD4042
7476	CD4027
7477	CD4042
7478	CD4027
7483	CD4008
7485	CD4063
7486	CD4030, CD4070
7490	CD4518
7491	CD4015, CD4094
7493	CD4520
7494	CD4035
7495	CD40104, CD4019
7499	CD40104, CD4019
7690	CD4017
74100	CD4034
74104	CD4095
74105	CD4095
74107	CD4027
74110	CD4095
74111	CD4027
7414	CD40106
74121	CD4047, CD4098
74122	CD4047, CD4098
74123	CD4098
74125	CD4502
74126	CD4502
74132	CD4093
74136	CD4030, CD4070
74141	CD4028
74145	CD4028
74148	CD4532
74150	CD4067
74151	CD4051, CD4097
74152	CD4051, CD4097
74153	CD4052
74154	CD4514, CD4515
74155	CD4555, CD4556
74156	CD4555, CD4556
74157	CD4019
74164	CD4015
74165	CD4021
74166	CD4014
74167	CD4527
74173	CD4076
74178	CD4035
74179	CD4035
74180	CD40101
74181	CD40181
74182	CD40182
74190	CD4510
74191	CD4516
74192	CD40192
74193	CD40193
74194	CD40104, CD4019
74195	CD4035, CD40195
74198	CD4034
74200	CD4061
74221	CD4098
74251	CD4051, CD4097
74279	CD4044
74283	CD4008
74290	CD4518
74293	CD4520

General Considerations

General Considerations

Ratings and Characteristics

RCA COS/MOS digital integrated circuits are specified in one of two voltage-supply ranges: standard ("A"-series) types operate from 3 to 15 volts, and high-voltage ("B"-series) types from 3 to 20 volts. The maximum ratings for the devices depend on both the series and the package type, as shown at the right.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE- TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPES E, Y ..... -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal):
STANDARD"A"-SERIES TYPES ..... -0.5 to +15 V
HIGH-VOLTAGE "B"-SERIES TYPES ..... -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A=-40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW
FOR T_A=+60 to +85°C (PACKAGE TYPES E, Y) ....Derate Linearly at 12 mW/°C to 200 mW
FOR T_A=-55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
FOR T_A=+100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16±1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

COS/MOS circuits are available in a wide variety of packages: dual-in-line white ceramic (D suffix), dual-in-line frit-seal ceramic (F suffix), dual-in-line plastic (E suffix), and ceramic flat pack (K suffix). Both standard and high-voltage types in dual-in-line packages are also available with special screening and testing, as shown below:

- Stabilization bake
- Temperature cycling
- 168-hour, 125° C, 12-V bias burn-in
- 0.25% dc parameter AQL
- 0.15% functional AQL

These "extra-value" types are identified by an additional suffix "X" following the standard package suffix notation.

Standard A-Series Characteristics

CD4000A-series types have a maximum dc supply-voltage rating of -0.5 to 15 volts, and a recommended operating supply-voltage range of 3 to 12 volts. The major features of this series are as follows:

- Quiescent current specified to 15 volts
- 5-volt and 10-volt parametric ratings
- Maximum input leakage of 1 μA at 15 volts over the full package operating-temperature range
- 1-volt noise margin (full package temperature range)

Static Electrical Characteristics. Table I shows the standardized dc electrical characteristics for A-series types. The data sheet for each of these types contains the family characteristics shown in Table I plus additional dc characteristics that are type-dependent.

Dynamic Electrical Characteristics. A-series dynamic electrical characteristics are specified for individual types under the following conditions: V_{DD} = 5 V and 10 V; T_A = 25° C (temperature coefficient is typically 0.3%/°C); C_L = 15 pF; t_r and t_f of inputs = 20 ns.

TABLE I — A-Series Static Electrical Characteristics (Full Package Temperature Range)

SYMBOL	PARAMETER	CONDITIONS				LIMITS			
		V_{IN}	V_O (volts)		V_{DD}				
		VOLTS	MIN.	MAX.	VOLTS	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	5	–	–	5	–	0	0.05	V
		10	–	–	10	–	0	0.05	V
V_{OH}	Output High Voltage	0	–	–	5	4.95	5	–	V
		0	–	–	10	9.95	10	–	V
V_{NL} (SSI Types)	Noise Voltage (Input Low)	–	3.6	–	5	1.5	2.25	–	V
		–	7.2	–	10	3	4.5	–	V
V_{NH} (SSI Types)	Noise Voltage (Input High)	–	–	1.4	5	1.5	2.25	–	V
		–	–	2.8	10	3	4.5	–	V
V_{NL} (MSI Types)	Noise Voltage (Input Low)	–	4.2	–	5	1.5	2.25	–	V
		–	9.0	–	10	3	4.5	–	V
V_{NH} (MSI Types)	Noise Voltage (Input High)	–	–	0.8	5	1.5	2.25	–	V
		–	–	1.0	10	3	4.5	–	V
V_{NML}	Noise Margin (Input Low)	–	4.5	–	5	1	–	–	V
		–	9.0	–	10	1	–	–	V
V_{NMH}	Noise Margin (Input High)	–	–	0.5	5	1	–	–	V
		–	–	1.0	10	1	–	–	V
I_{IL}, I_{IH}	Input Leakage Low	–	–	–	15	–	$\pm 10^{-5}$	±1	μA
I_L	Quiescent Device Leakage	–	–	–	5,10,15	See Data Sheets			μA
I_{DN}, I_{DP}	Output Source and Sink current	–	–	–	5,10	See Data Sheets			ma

Note: Logic Level Inversion Assumed in Table I

General Considerations (cont'd)

High-Voltage B-Series Characteristics

CD4000B-series types have a maximum dc supply-voltage rating of -0.5 to 20 volts, and a recommended operating supply-voltage range of 3 to 18 volts. The major features of this series are as follows:

- Quiescent current specified to 20 volts
- 5-, 10-, and 15-volt parametric ratings
- Standardized symmetrical output characteristics
- Maximum input leakage of 1 μA to 20 volts over the full package operating-temperature range
- 1-volt noise margin (full package temperature range)

Static Electrical Characteristics. Tables II, III, and IV show the standardized dc electrical characteristics for B-series types. The data sheet for each of these types contains all the family characteristics shown in these tables, plus additional dc characteristics that are type-dependent.

CD4000B-series types are classified as SSI and MSI functions as shown at the right.

SSI Types

CD4000B	CD4071B	
CD4001B	CD4072B	
CD4002B	CD4073B	
CD4009B	CD4075B	
CD4010B	CD4077B	
CD4011B	CD4078B	
CD4012B	CD4081B	
CD4016B	CD4082B	
CD4023B	CD4085B	
CD4025B	CD4086B	
CD4041B	CD4093B	
CD4049B	CD4502B	
CD4050B	CD40107B	
CD4068B		
CD4069B		
CD4070B		

MSI Types

CD4008B	CD4094B	CD4555B
CD4013B	CD4095B	CD4556B
CD4027B	CD4096B	CD40100B
CD4042B	CD4097B	CD40101B
CD4043B	CD4098B	CD40102B
CD4044B	CD4099B	CD40103B
CD4051B	CD4508B	CD40104B
CD4052B	CD4510B	CD40105B
CD4053B	CD4511B	CD40108B
CD4054B	CD4514B	CD40109B
CD4055B	CD4515B	CD40181B
CD4056B	CD4516B	CD40182B
CD4063B	CD4518B	CD40192B
CD4067B	CD4520B	CD40193B
CD4076B	CD4527B	CD40194B
CD4089B	CD4532B	CD40257B

SSI noise-immunity specifications shown in Table II apply to inverters and buffered gates. Non-buffered gates have a noise immunity of ±0.2 V_{DD} (all inputs), as specified on the individual data sheets for these types.

Tables III and IV show that B-series quiescent device current and output sink and source current at 25° C are the same for all package styles. Figs. 1 through 4 show the standardized output n-channel and p-channel drain characteristics for B-series types, and Figs. 5 through 8 show the normalized variation of output source and sink currents with respect to temperature and voltage.

TABLE II – B-Series Static Electrical Characteristics (Full Package Temperature Range)

SYMBOL	PARAMETER	CONDITIONS				LIMITS			UNITS
		V_{IN}	V_O (volts)		V_{DD}				
		VOLTS	MIN.	MAX.	VOLTS	MIN.	TYP.	MAX.	
V_{OL}	Output Low Voltage	5	–	–	5	–	0	0.05	V
		10	–	–	10	–	0	0.05	V
		15	–	–	15	–	0	0.05	V
V_{OH}	Output High Voltage	0	–	–	5	4.95	5	–	V
		0	–	–	10	9.95	10	–	V
		0	–	–	15	14.95	15	–	V
V_{NL} (SSI Types)	Noise Voltage (Input Low)	–	3.6	–	5	1.5	2.25	–	V
		–	7.2	–	10	3	4.5	–	V
		–	10.8	–	15	4.5	6.75	–	V
V_{NH} (SSI Types)	Noise Voltage (Input High)	–	–	1.4	5	1.5	2.25	–	V
		–	–	2.8	10	3	4.5	–	V
		–	–	4.2	15	4.5	6.75	–	V
V_{NL} (MSI Types)	Noise Voltage (Input Low)	–	4.2	–	5	1.5	2.25	–	V
		–	9.0	–	10	3	4.5	–	V
		–	13.5	–	15	4.5	6.75	–	V
V_{NH} (MSI Types)	Noise Voltage (Input High)	–	–	0.8	5	1.5	2.25	–	V
		–	–	1.0	10	3	4.5	–	V
		–	–	1.5	15	4.5	6.75	–	V
V_{NML}	Noise Margin (Input Low)	–	4.5	–	5	1	–	–	V
		–	9.0	–	10	1	–	–	V
		–	13.5	–	15	1	–	–	V
V_{NMH}	Noise Margin (Input High)	–	–	0.5	5	1	–	–	V
		–	–	1.0	10	1	–	–	V
		–	–	1.5	15	1	–	–	V
I_{IL}, I_{IH}	Input Leakage Low	–	–	–	20	–	$\pm 10^{-5}$	±1	μA
I_{OL}, I_{OH}	3-State Output Lkg	–	Force 20 V/0 V		20	–	$\pm 10^{-4}$	±2	μA

General Considerations (cont'd)

TABLE III – B-Series Standard Quiescent Device Current

Symbol	V_{DD} Volts	LIMITS										
		SSI TYPES – ALL PACKAGES					MSI TYPES – ALL PACKAGES					
		* -40° C/ △ -55° C	+25° C		* +85° C	△ +125° C	* -40° C/ △ -55° C	+25° C		* +85° C	△ +125° C	
		MAX.	TYP.	MAX.	MAX.	MAX.	MAX.	TYP.	MAX.	MIN.	MAX.	UNITS
I_L	5	0.5	0.01	0.5	5	10	5	0.02	5	50	100	μA
	10	1	0.01	1	10	20	10	0.02	10	100	200	μA
	15	2	0.01	2	20	40	20	0.02	20	200	400	μA
	20	10	0.02	10	100	200	100	0.04	100	1000	2000	μA

△ Applies only to D, F, K, H, and T packages
* Applies to E and Y packages

TABLE IV – B-Series Standard Output Drive Current

PARAMETER	TEST CONDITIONS		LIMITS – ALL PACKAGES						UNITS
	V_O Volts	V_{DD} Volts	△ -55° C	* -40° C	+25° C		* +85° C	△ +125° C	
			MIN.	MIN.	MIN.	TYP.	MIN.	MIN.	
N-Channel (Sink, I_{DN})	0.4	5	0.5	0.45	0.4	0.8	0.36	0.30	mA
	0.5	10	1.1	1	0.9	1.8	0.75	0.65	mA
	1.5	15	3.3	3.2	3	6	2.5	2.2	mA
P-Channel (Source, I_{DP})	4.6	5	-0.5	-0.45	-0.4	-0.8	-0.36	-0.3	mA
	2.5	5	-2	-1.8	-1.6	-3.2	-1.3	-1.15	mA
	9.5	10	-1.1	-1	-0.9	-1.8	-0.75	-0.65	mA
	13.5	15	-3.3	-3.2	-3	-6	-2.5	-2.2	mA

△ Applies only to D, F, K, H, and T packages
* Applies to E and Y packages

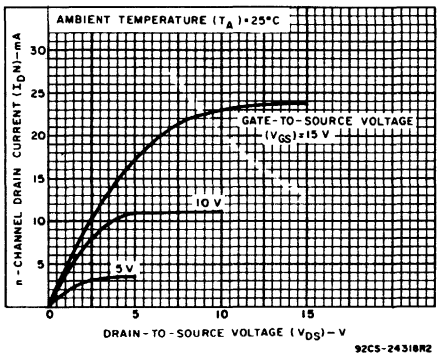


Fig. 1 – Typical output n-channel drain characteristics.

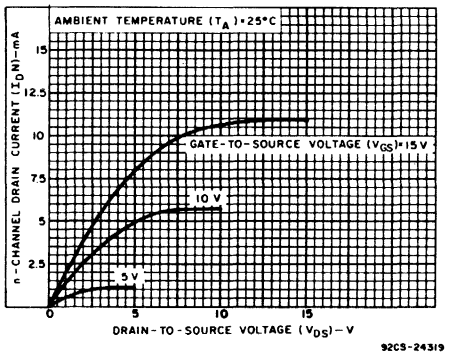


Fig. 2 – Minimum output n-channel drain characteristics.

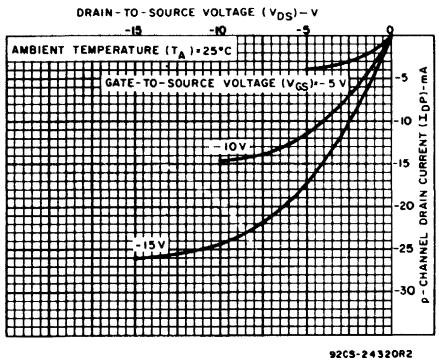


Fig. 3 – Typical output p-channel drain characteristics.

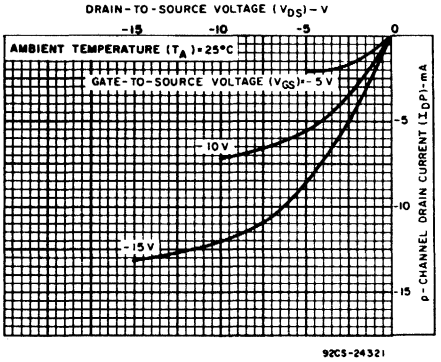


Fig. 4 – Minimum output p-channel drain characteristics.

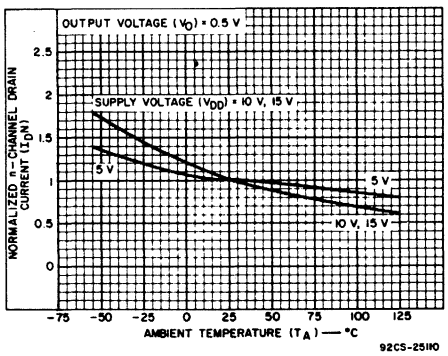


Fig. 5 – Variation of normalized sink current (I_{DN}) with temperature.

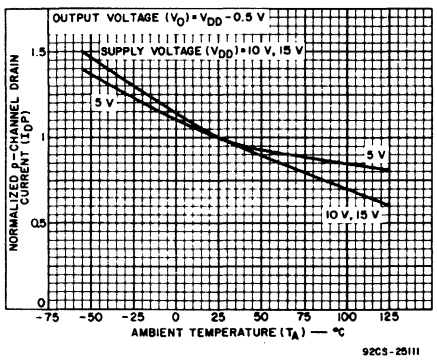


Fig. 6 – Variation of normalized source current (I_{DP}) with temperature.

General Considerations (cont'd)

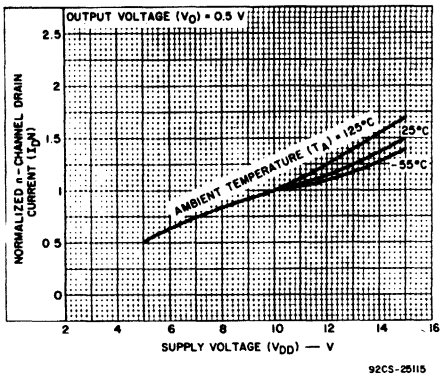


Fig. 7 — Variation of normalized sink current (I_{DN}) with supply voltage.

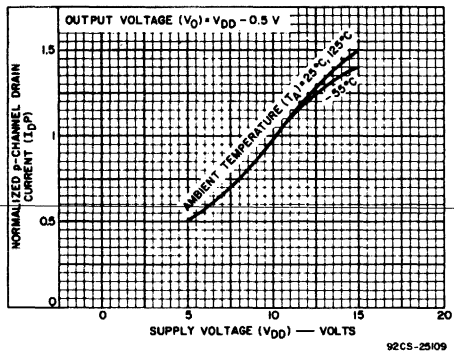


Fig. 8 — Variation of normalized source current (I_{DP}) with supply voltage.

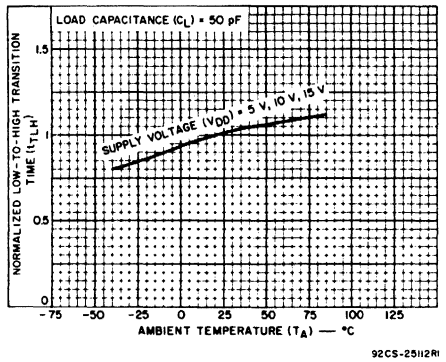


Fig. 10 — Variation of low-to-high transition time (t_{TLH}) with temperature.

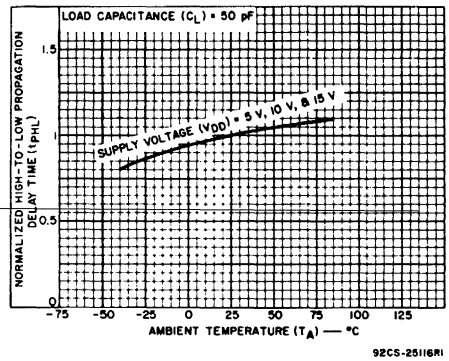


Fig. 11 — Variation of high-to-low propagation delay time (t_{PHL}) with temperature.

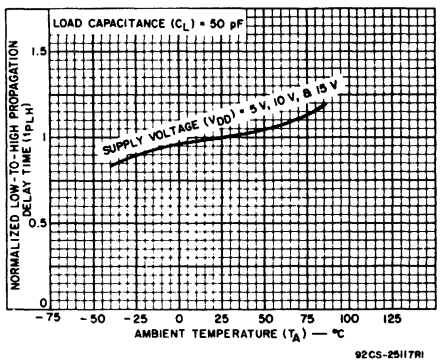


Fig. 12 — Variation of low-to-high propagation delay time (t_{PLH}) with temperature.

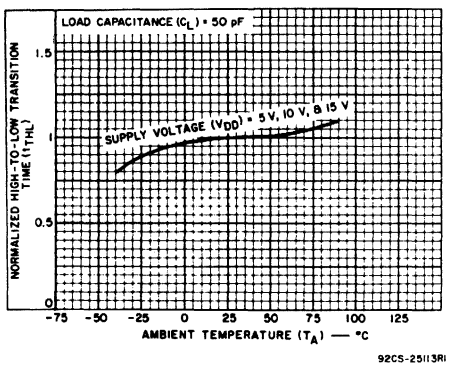


Fig. 9 — Variation of high-to-low transition time (t_{THL}) with temperature.

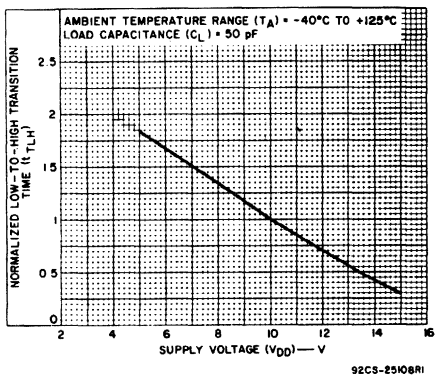


Fig. 13 — Variation of low-to-high transition time (t_{TLH}) with supply voltage.

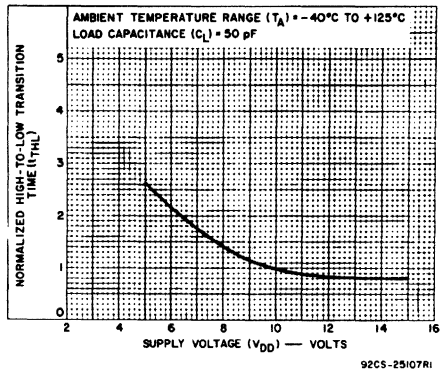


Fig. 14 — Variation of high-to-low transition time (t_{THL}) with supply voltage.

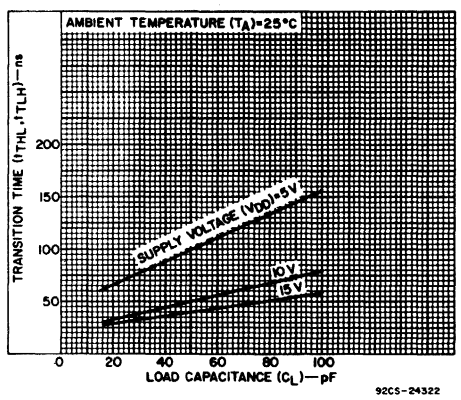


Fig. 15 — Variation of transition time (t_{THL}, t_{TLH}) with load capacitance at three levels of supply voltage.

Dynamic Electrical Characteristics. B-series dynamic electrical characteristics are specified for individual types under the following conditions: V_{DD} = 5 V, 10 V, and 15 V; T_A = 25° C; C_L = 50 pF; R_L = 200 kΩ; t_r and t_f = 20 ns. Figs. 9 through 12 show the variation of B-series dynamic parameters with temperature. Figs. 13 and 14 show the variation of output transition time with supply voltage. Fig. 15 shows the variation of the standardized output transition time with load capacitance.

Dynamic (AC) Switching Parameters

Table V defines the major COS/MOS ac characteristics, with reference to the waveforms shown in Figs. 16 through 19. Test conditions of V_{DD}, load capacitance (C_L), and input conditions are given for individual types in the published data.

Test Circuits

Figs. 20 through 24 show standard test circuits used to measure noise immunity, quiescent device current, input leakage current, 3-state device output leakage, and output current of COS/MOS devices.

Design and Operating Considerations

Operating Supply-Voltage Range. Because logic systems occasionally experience transient conditions on the power-supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply-voltage ranges are 3 to 12 volts for A-series devices and 3 to 18 volts for B-series devices. The recommended maximum power-supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power-supply transient and regulation limits. For circuits that operate in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum supply voltage of at least 4 volts is recommended.

General Considerations (cont'd)

TABLE V – Dynamic (AC) Switching Parameters

CHARACTERISTICS	SYMBOL	LIMITS		WAVEFORMS
		MAX.	MIN.	
Propagation Delay:				
Outputs going High to Low	T_{PHL}	X		Figs. 16, 17, 18
Outputs going Low to High	T_{PLH}	X		
Output Transition Time:				
Outputs going High to Low	T_{THL}	X		Figs. 16, 17, 18
Outputs going Low to High	T_{TLH}	X		
Min. Pulse Width – Set, Reset, Preset, Enable, Disable Strobe, Clock	t_w	X		Figs. 17, 18
Max. Clock Input Frequency	f_{CL}		X	Figs. 17, 18 ($1/2t_w$)
Clock Input Rise and Fall Time	t_{rCL}, t_{fCL}	X		Figs. 17, 18
Min. Set-Up Time or Min. Reset Removal Time	t_s	X		Figs. 17, 18
Min. Hold Time	t_H	X		Figs. 17, 18
Three-State Disable Delay Times:				
Output 1 to High Impedance	t_{PHZ}	X		
High Impedance to Output 1	t_{PZH}	X		
Output 0 to High Impedance	t_{PLZ}	X		
High Impedance to Output 0	t_{PZL}	X		Fig. 19
Average Input Capacitance (Typ) (1)	C_I			–
Output Capacitance (Typ) (2)	C_O			–

(1) 5 pF typical – incremented by 5-pF increments.
(2) Specified as typical value for all High-Impedance-Output 3-state devices; specified in increments of 5 pF.

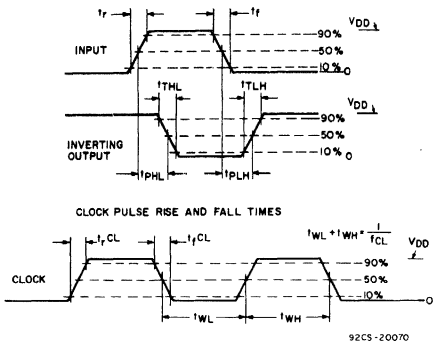


Fig. 16 – Transition times and propagation delay times for combinational logic circuits.

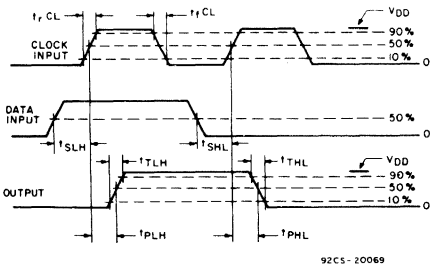


Fig. 17 – Setup times, hold times, and propagation delay times for positive-edge-triggered sequential logic circuits.

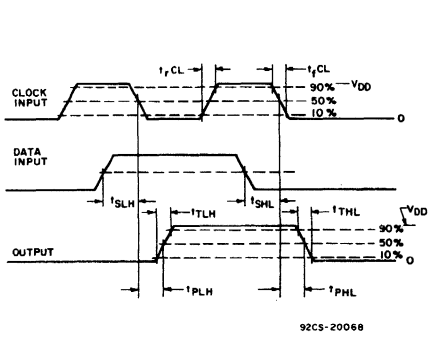


Fig. 18 – Setup times, hold times, and propagation delay times for negative-edge-triggered sequential logic circuits.

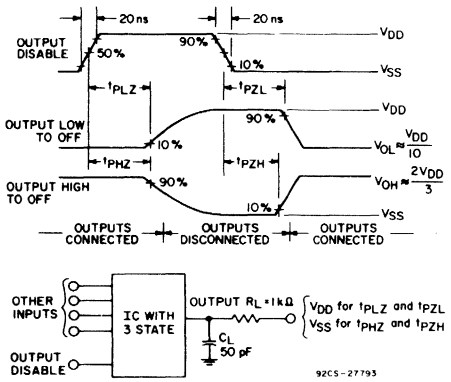


Fig. 19 – Three-state propagation delay waveshapes and circuit.

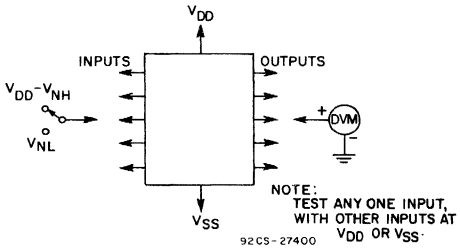


Fig. 20 – Noise immunity test circuit.

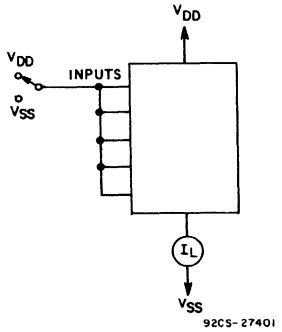


Fig. 21 – Quiescent device current test circuit.

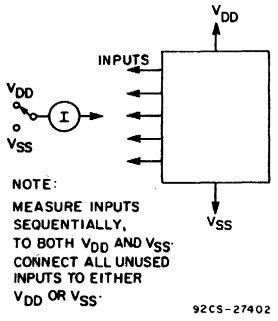


Fig. 22 – Input leakage current test circuit.

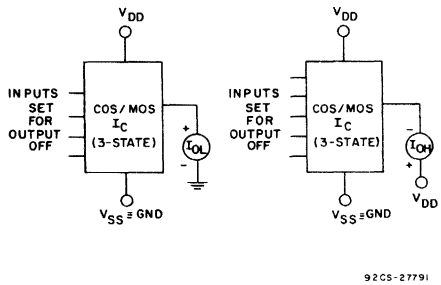


Fig. 23 – Three-state device output leakage test circuit.

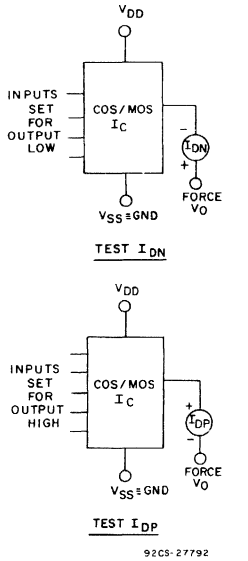


Fig. 24 – Output current test circuit.

General Considerations (cont'd)

Power Dissipation and Derating. All COS/MOS devices are rated at 200 mW per package at the maximum operating ambient temperature rating (T_A) for the package type (85° C for E, Y suffixes and 125° C for D, F, K suffixes). Power ratings for temperatures below the maximum operating temperature are shown in the standard COS/MOS thermal derating chart in Fig. 25. This chart assumes that (a) the device is mounted and soldered (or placed in a socket) on a PC board; (b) there is natural convection cooling, with the PC board mounted horizontally; and (c) the pressure is standard (14.7 PSIA). In addition to the over-all package dissipation rating, device dissipation per output transistor is limited 100 mW maximum over the full package operating-temperature range.

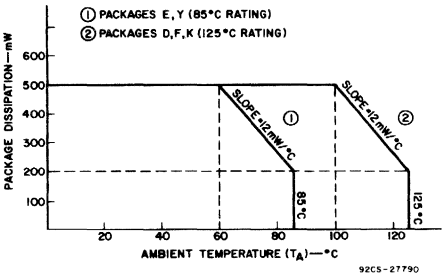


Fig. 25 — Standard COS/MOS thermal derating chart.

System Noise Considerations. In general, COS/MOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power-supply voltage, and more importantly as a function of synchronism between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus.

Power-Source Rules. Fig. 26 shows the basic COS/MOS inverter and its gate-oxide protection network plus inherent diodes. The safe operating procedures listed below can be understood by reference to this inverter:

1. When separate power supplies are used for the COS/MOS device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage to the D2 input-protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage should not result; ac inputs can be rectified by diode D2 to act as a power supply.
2. The power-supply operating voltage should by kept safely below the absolute maximum supply rating, as indicated previously.

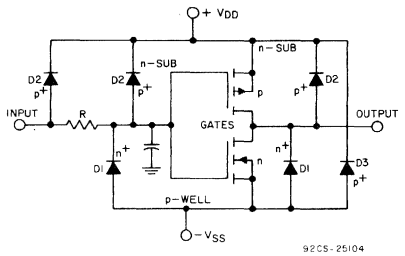


Fig. 26 — Basic COS/MOS inverter.

3. The power-supply polarity for COS/MOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5 volt negative with respect to the negative (V_{SS}) terminal ($V_{DD}-V_{SS} > -0.5$ V). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.
4. V_{DD} should be equal to or greater than V_{CC} for COS/MOS buffers which have two power supplies (in particular, for CD4009 and CD4010 COS/MOS-to-TTL "down"-conversion devices).
5. Power-source current capability should be limited to as low a value as reasonable to assure good logic operation.
6. Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

Gate-Oxide Protection Networks. A problem occasionally encountered in handling and testing low-power semiconductor devices, including MOS and small-geometry bipolar devices, has been damage to gate oxide and/or p-n junctions. Fig. 27 shows the gate-oxide protection circuits used to protect COS/MOS devices from static electricity damage. ICAN-6218 gives further information on protection circuits. Although these circuits are included in all COS/MOS devices, the handling precautions in ICAN-6218 and ICAN-6000 should be observed.

Input Signals and Ratings

1. Input signals should be maintained within the power-supply voltage range, $V_{SS} \leq V_I \leq V_{DD}$. In applications such as astable and monostable multivibrators, input current can flow and should be limited to the microampere level by use of a resistor in series with the input terminal affected.
2. All COS/MOS inputs should be terminated. When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor should be connected to V_{DD} or V_{SS} in case the inputs become unterminated with the power supply on.
3. When COS/MOS circuits are driven by TTL logic, a "pull-up" resistor should be connected from the COS/MOS input to 5 volts (further information is given in ICAN-6602).

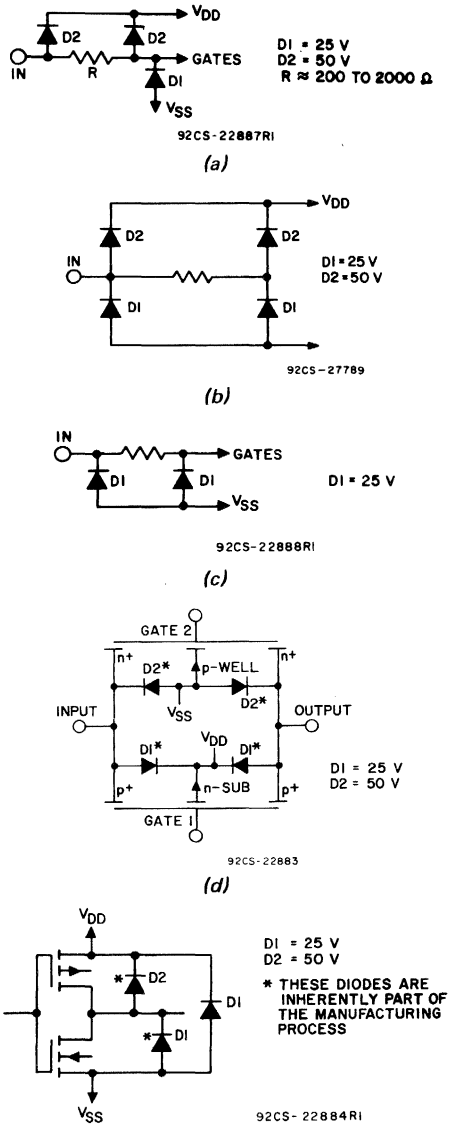


Fig. 27 — Protection circuits used in COS/MOS devices: (a) normal gate-input protection; (b) improved gate-input protection; (c) CD4049 and CD4050 gate-input protection; (d) transmission-gate input-output protection; (e) active (inverter) output protection.

4. Input signals should be maintained within the recommended input-signal-swing range.

Output Rules

1. The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, or (c) directly driving the base of a p-n-p or n-p-n bipolar transistor.
2. Output short circuits often result from testing errors or improper board assembly.

General Considerations (cont'd)

Shorts on buffer outputs or across power supplies greater than 5 volts can damage COS/MOS devices.

3. COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails.
4. Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.
5. Output loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).
6. Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.
7. Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

Noise Immunity. The complementary structure of the inverter, common to all COS/MOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high dc noise immunity.

Fig. 28 illustrates minimum and maximum transfer characteristics useful for defining noise immunity and an inverter and a non-inverter. The noise-immunity voltage (V_{NL}, V_{NH}) is that noise voltage at any one input which will not propagate through the system. Minimum noise immunity is 30% of the supply voltage (20% for some un-buffered gate and inverter types).

Noise immunity increases as the input noise pulse width becomes less than the propagation delay of the circuit. This condition is often described as ac noise immunity. (Further information on noise immunity is given in ICAN-6176).

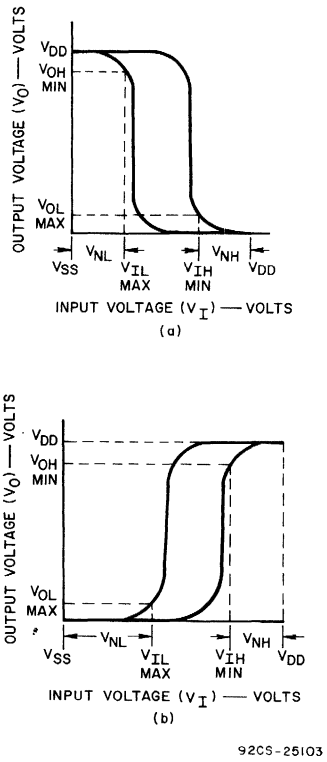


Fig. 28 — Minimum and maximum transfer characteristics for (a) inverting logic function, and (b) non-inverting logic function.

Clock Rise- and Fall-Time Requirements. Most COS/MOS clocked devices have maximum rise- and fall-time ratings (normally 5 to 15 microseconds). With longer rise or fall times, a device may not function properly because of data ripple-through, false triggering problems, etc. Long rise and fall times on COS/MOS buffer-type inputs cause increased power dissipation which may exceed device capability for power supplies above 5 volts.

Parallel Clocking. Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clocked sequential circuits, as shown in Fig. 29. This problem can be avoided if the clock rise time (t_rCL) is made less than the total of the fixed propagation delay plus the output transition time of the first stage, as determined from the device data for the specific loading condition in effect.

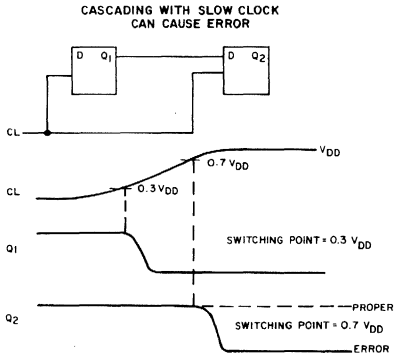


Fig. 29 — Error effect that results from a slow clock in cascaded circuits.

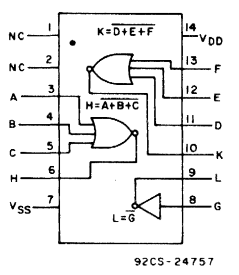
Schmitt trigger circuits such as the CD4093B are an ideal solution to applications requiring wave-shaping.

Three-State Logic. Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

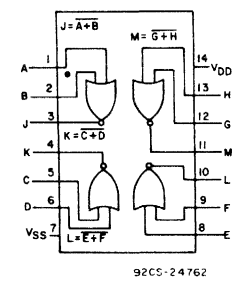
CD4000A, CD4001A, CD4002A, CD4025A Types

COS/MOS NOR Gates

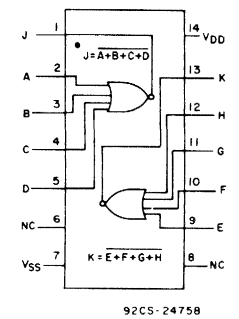
Dual 3 Input plus Inverter—CD4000A
Quad 2 Input—CD4001A
Dual 4 Input—CD4002A
Triple 3 Input—CD4025A



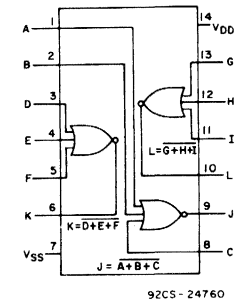
CD4000A



CD4001A



CD4002A



CD4025A

The RCA-CD4000A, CD4001A, CD4002A, and CD4025A NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000A, CD4001A, CD4002A, and CD4025A types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
  PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 20 ns*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (Volts)	LIMITS D, F, K, H PACKAGES TYP.	D, F, K, H PACKAGES MAX.	E, Y PACKAGES TYP.	E, Y PACKAGES MAX.	UNITS
Propagation Delay Time: High-to-Low Level, t_{PHL}	5	35	50	35	80	ns
	10	25	40	25	55	
Low-to-High Level, t_{PLH}	5	35	95	35	120	ns
	10	25	45	25	65	
Transition Time: High-to-Low Level, t_{THL}	5	65	125	65	200	ns
	10	35	70	35	115	
Low-to-High Level, t_{TLH}	5	65	175	65	300	ns
	10	35	75	35	125	
Input Capacitance, C_I	Any Input	5	—	5	—	pF

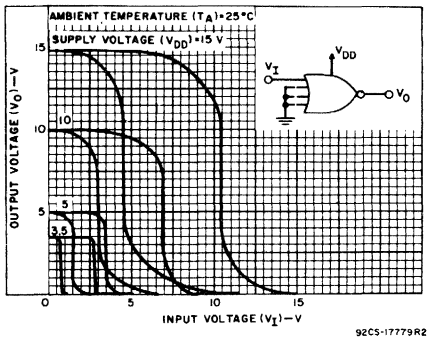


Fig. 1 – Minimum & maximum voltage transfer characteristics.

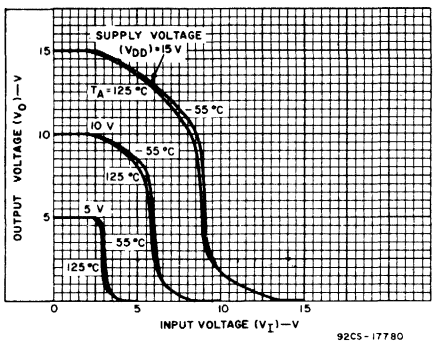


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

CD4000A, CD4001A, CD4002A, CD4025A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max								V
	–	0, 10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.4	–	5	0.5	1	0.4	0.28	0.35	1	0.3	0.24	mA
I_DN Min.	0.5	–	10	1.1	2.5	0.9	0.65	0.72	2.5	0.6	0.48	
P-Channel (Source):	2.5	–	5	-0.62	-2	-0.5	-0.35	-0.35	-2	-0.3	-0.24	
I_DP Min.	9.5	–	10	-0.62	-1	-0.5	-0.35	-0.3	-1	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

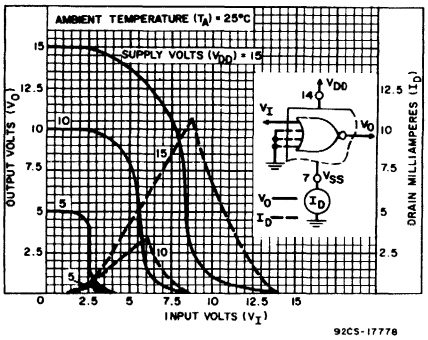


Fig. 3 – Typical current & voltage transfer characteristics.

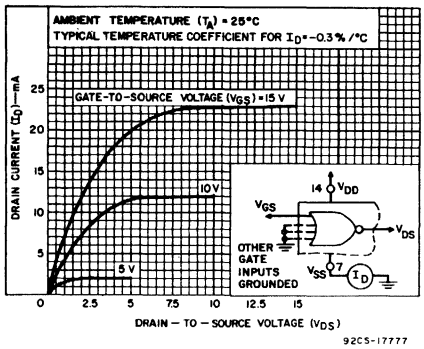


Fig. 4 – Typical n-channel drain characteristics.

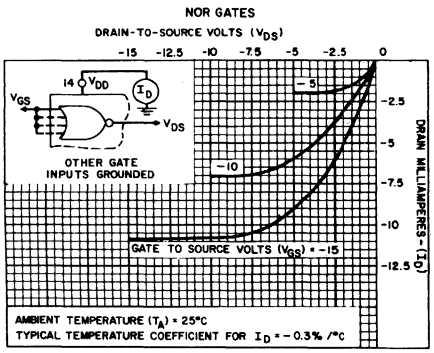


Fig. 5 – Typical p-channel drain characteristics.

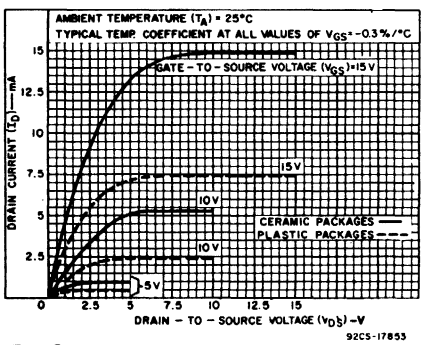


Fig. 6 – Minimum n-channel drain characteristics.

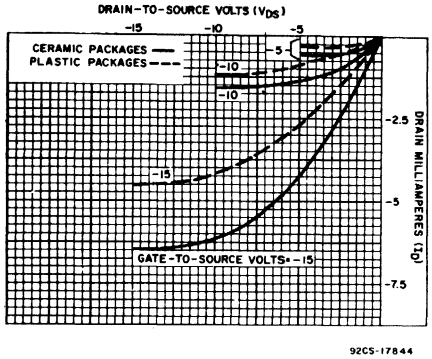


Fig. 7 – Minimum p-channel drain characteristics.

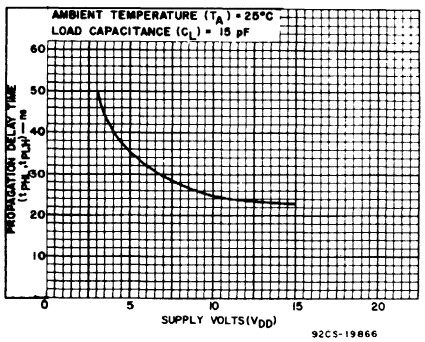


Fig. 8 – Typical propagation delay time vs. V_{DD}.

CD4000A, CD4001A, CD4002A, CD4025A Types

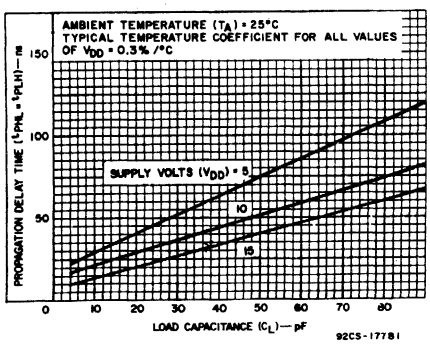


Fig. 9 – Typical propagation delay time vs. C_L.

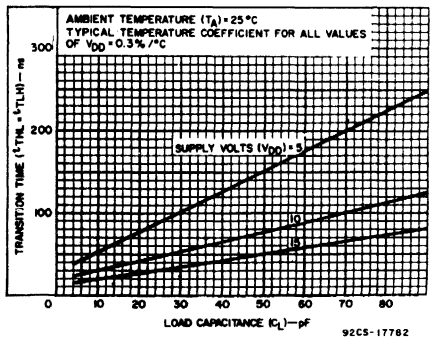


Fig. 10 – Typical transition time vs. C_L.

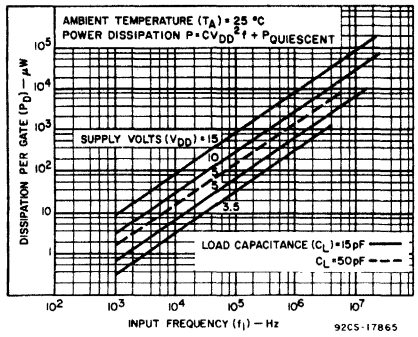


Fig. 11 – Typical dissipation characteristics.

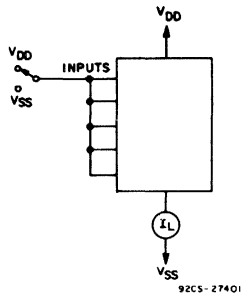
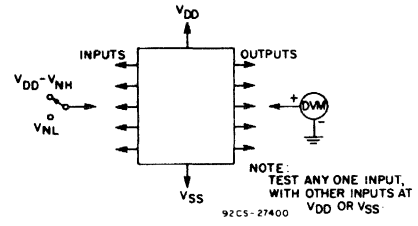


Fig. 12 – Quiescent device current test circuit.



NOTE:

CD4000, CD4002, CD4025 – TEST ANY ONE INPUT WITH OTHER INPUTS AT V_{DD} OR V_{SS}.

CD4001 – TEST ANY COMBINATION OF INPUTS.

Fig. 13 – Noise immunity test circuit.

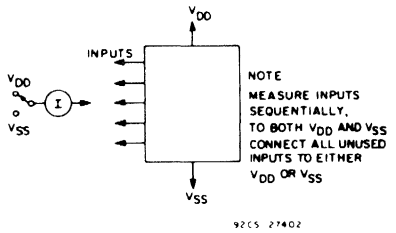


Fig. 14 – Input leakage current test circuit.

CD4006A Types

COS/MOS 18-Stage Static Shift Register

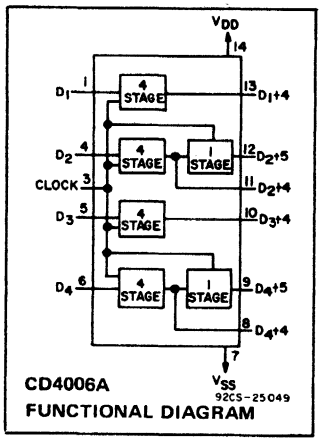
The RCA-CD4006A types are comprised of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

Features:

- **Fully static operation**
- **Shifting rates up to 5 MHz**
- **Permanent register storage with clock line high or low — — no information recirculation required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

The CD4006A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

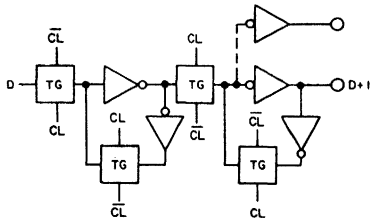
Applications:

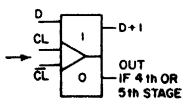
- **Serial shift registers**
- **Time delay circuits**
- **Frequency division**

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	80	–	100	–	ns
	10	40	–	50	–	
Clock Pulse Width, t_W	5	500	–	830	–	ns
	10	200	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	2.5	dc	2	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	15	–	15	μs
	10	–	5	–	5	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.





TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D+1
0	⌞	0
1	⌞	1
X	∫	NC

NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

92CS-17887

Fig. 1 — Logic diagram and truth table (one register stage).

CD4006A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.01	0.5	30	5	0.03	5	70	μA
	–	–	10	1	0.01	1	60	10	0.05	10	40	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.155	0.25	0.125	0.085	0.072	0.25	0.06	0.048	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.15	0.5	0.125	0.1	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.125	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	9.5	–	10	-0.25	-0.3	-0.2	-0.14	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

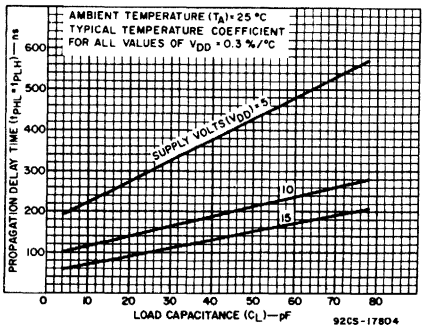


Fig. 2 — Typical propagation delay time vs. load capacitance.

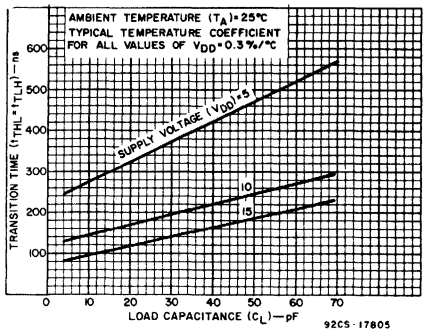


Fig. 3 — Typical transition time vs. load capacitance.

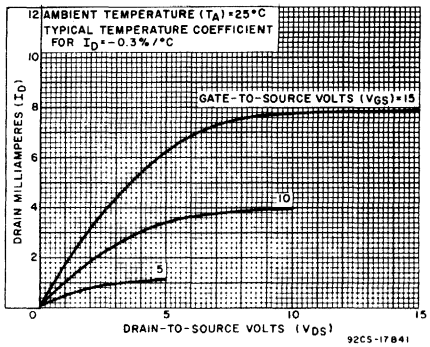


Fig. 5 — Typical output n-channel drain characteristics.

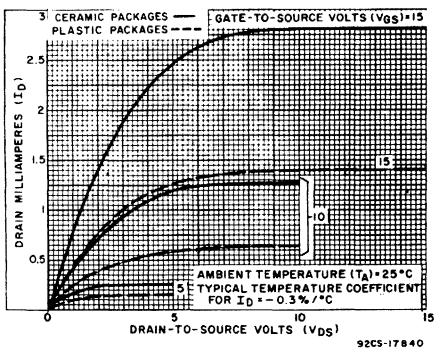


Fig. 6 — Minimum output n-channel drain characteristics.

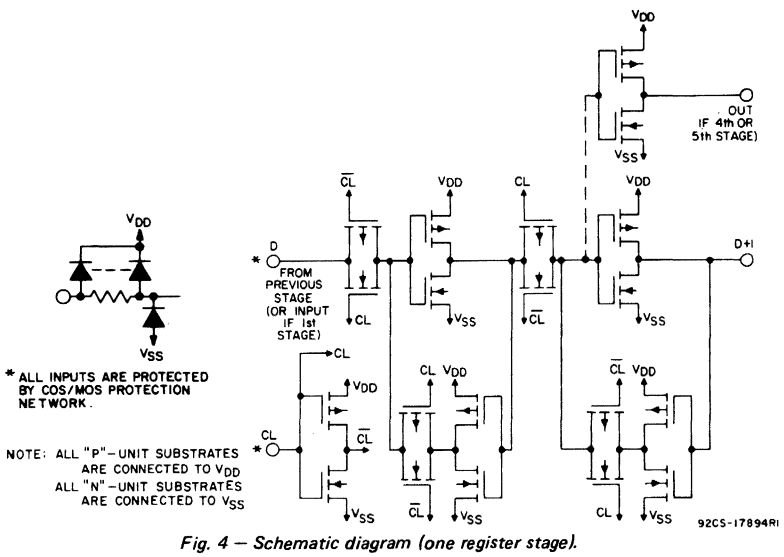


Fig. 4 — Schematic diagram (one register stage).

CD4006A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Transition Time; t_{THL}, t_{TLH}		5	–	250	400	–	250	500	ns
		10	–	125	200	–	125	250	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	2.5	5	–	2	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	200	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Data Set Up Time, t_S		5	–	50	80	–	50	100	ns
		10	–	25	40	–	25	50	
Average Input Capacitance, C_I	Data Input		–	5	–	–	5	–	pF
	Clock Input		–	30	–	–	30	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

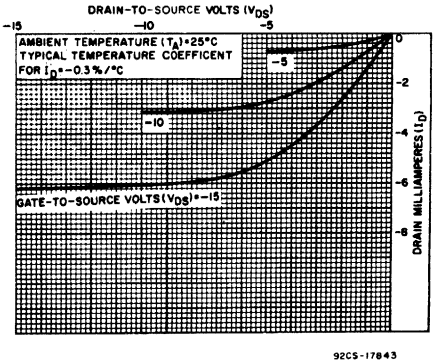


Fig. 7 – Typical output p-channel drain characteristics.

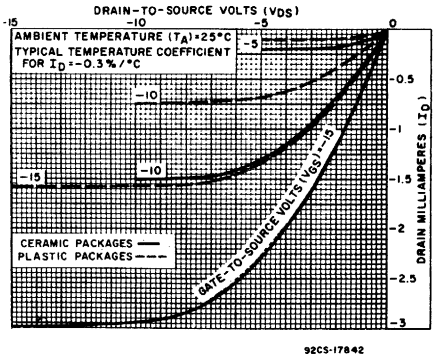


Fig. 8 – Minimum output p-channel drain characteristics.

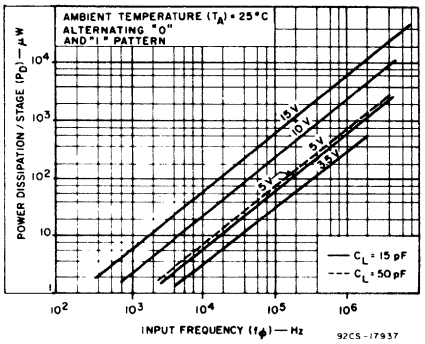


Fig. 9 – Typical dissipation characteristics.

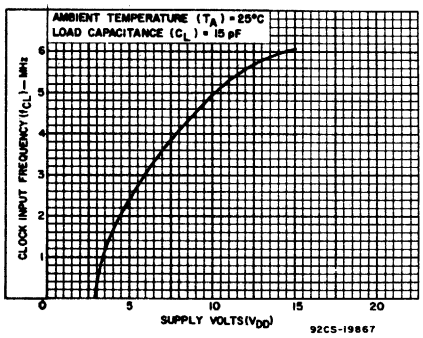


Fig. 10 – Typical clock input frequency vs. supply voltage.

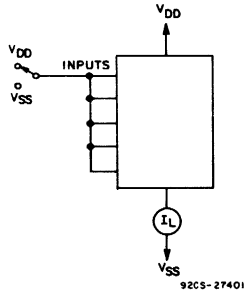


Fig. 11 – Quiescent-device-current test circuit.

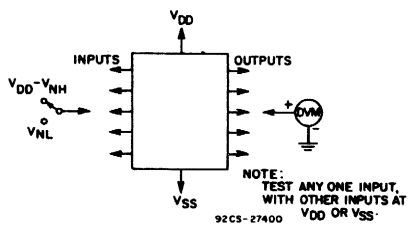


Fig. 12 – Noise-immunity test circuit.

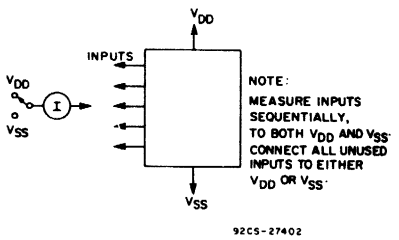


Fig. 13 – Input-leakage-current test circuit.

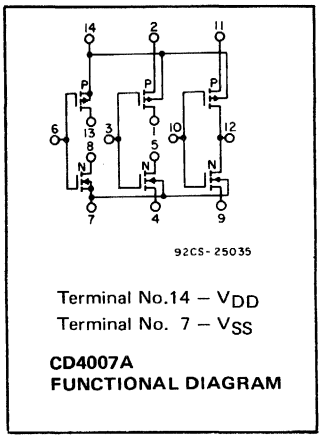
CD4007A Types

COS/MOS Dual Complementary Pair Plus Inverter

The RCA-CD4007A types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007-A Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



Terminal No.14 – V_{DD}
Terminal No. 7 – V_{SS}

CD4007A FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D,F,K,H Packages		E,Y Packages		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
		V_{DD} (V)	D,F,K,H Packages			E,Y Packages			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	35	60	–	35	75	ns
		10	–	20	40	–	20	50	
Transition Time; t_{THL}, t_{TLH}		5	–	50	75	–	50	100	ns
		10	–	30	40	–	30	50	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

Features:

- **Medium-speed operation. . . . t_{PHL} = t_{PLH} = 20 ns (typ.) at C_L = 15 pF, + V_{DD} = 10 V**
- **Low "high" and "low" output impedance. . . . 500 Ω (typ.) at V_{DD} − V_{SS} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Extremely high-input impedance amplifiers**
- **Shapers**
- **Inverters**
- **Threshold detector**
- **Linear amplifiers**

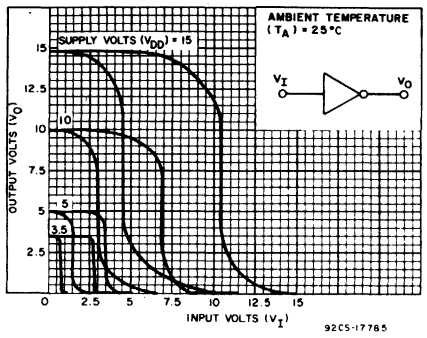


Fig.1 – Minimum and maximum voltage-transfer characteristics for inverter.

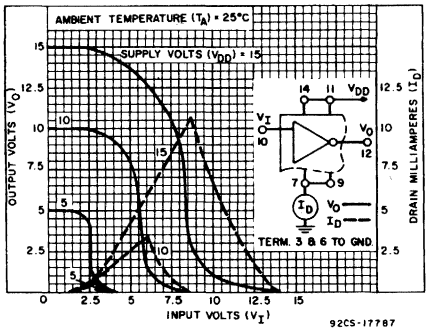


Fig.2 – Typical current and voltage-transfer characteristics for inverter.

CD4007A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current: I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	1	0.005	1	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage Low Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min.	0.5	V_I=	5	0.75	1	0.6	0.4	0.35	1	0.3	0.24	mA
	0.5	V_{DD}	10	1.6	2.5	1.3	0.95	1.2	2.5	1	0.8	
P-Channel (Source): I_DP Min.	4.5	V_I=	5	−1.75	−4	−1.4	−1	−1.3	−4	−1.1	−0.9	
	9.5	V_{DD}	10	−1.35	−2.5	−1.1	−0.75	−0.65	−2.5	−0.55	−0.45	
Input Leakage Current: I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

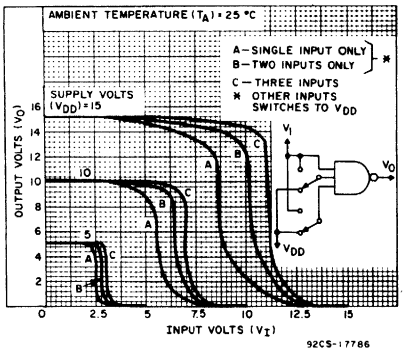


Fig.3 – Typical voltage-transfer characteristics for NAND gate.

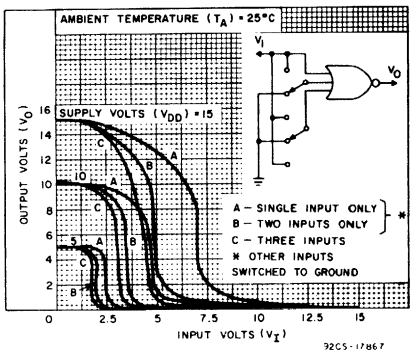


Fig.4 – Typical voltage-transfer characteristics for NOR gate.

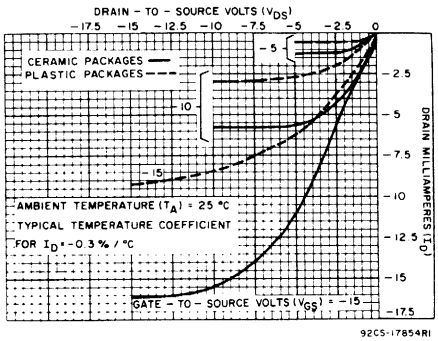


Fig.5 – Minimum output p-channel drain characteristics.

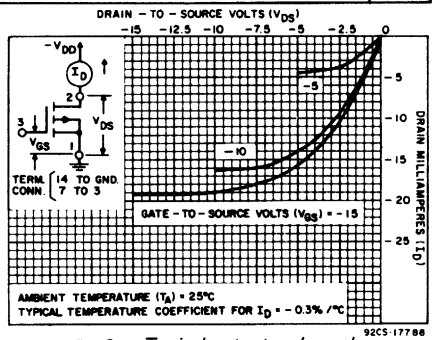


Fig.6 – Typical output p-channel drain characteristics.

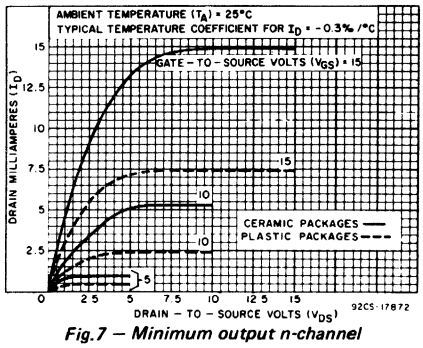


Fig.7 – Minimum output n-channel drain characteristics.

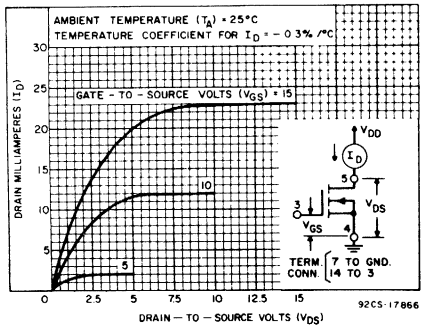


Fig.8 – Typical output n-channel drain characteristics.

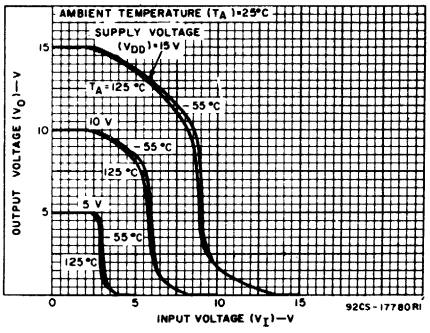


Fig.9 – Typical voltage-transfer characteristics as a function of temperature.

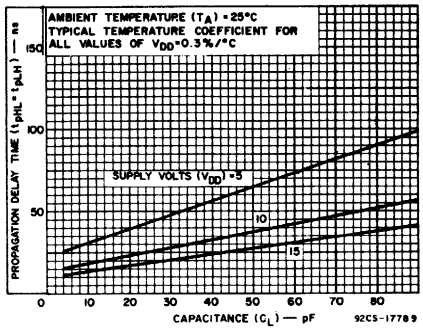


Fig.10 – Typical propagation-delay time vs. load capacitance.

CD4007A Types

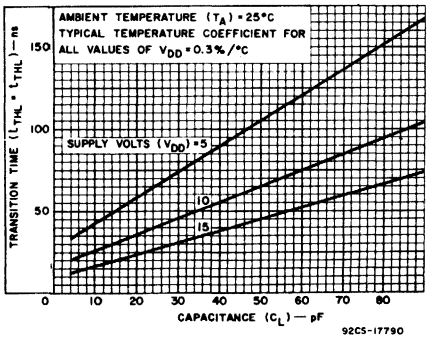


Fig. 11 — Typical transition time vs. load capacitance.

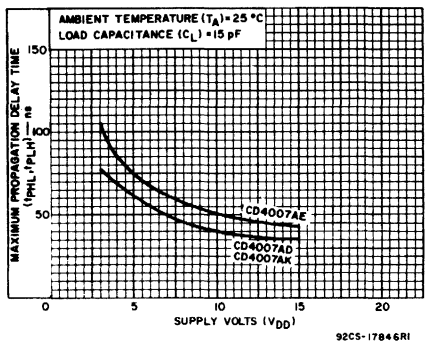


Fig. 12 — Maximum propagation-delay time vs. supply voltage.

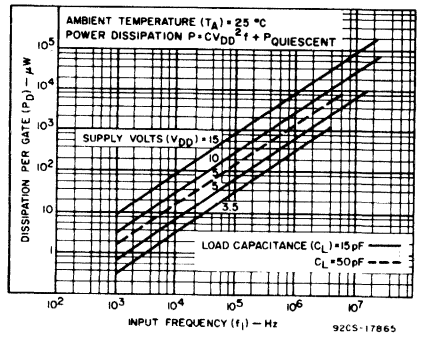
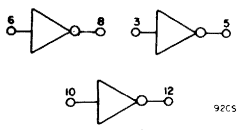
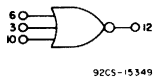


Fig. 13 — Typical dissipation characteristics.



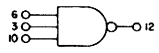
(14,2,11); (8,13); (1,5); (7,4,9)

a) Triple Inverters



(13,2); (1,11); (12,5,8); (7,4,9)

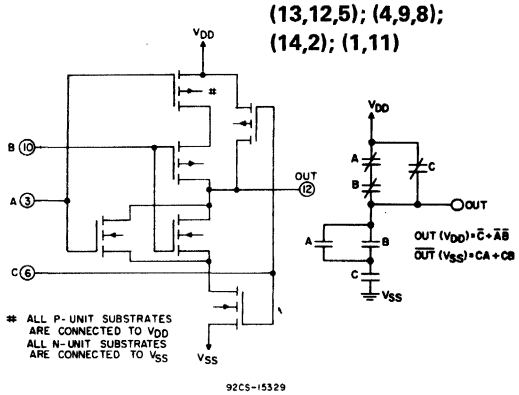
b) 3-Input NOR Gate



(1,12,13); (2,14,11); (4,8); (5,9)

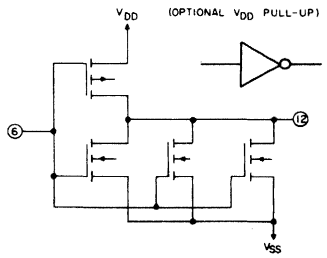
c) 3-Input NAND Gate

(13,12,5); (4,9,8); (14,2); (1,11)



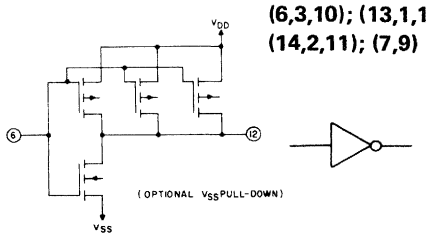
d) Tree (Relay) Logic

(6,3,10); (8.5,12); (11,14); (7,4,9)

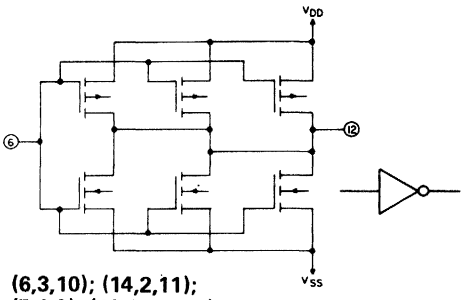


e) High Sink-Current Driver

(6,3,10); (13,1,12); (14,2,11); (7,9)

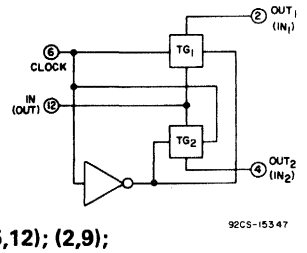


f) High Source-Current Driver



(6,3,10); (14,2,11); (7,4,9); (13,8,1,5,12)

g) High Sink- and Source-Current Driver



(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

h) Dual Bi-Directional Transmission Gating

Fig. 14 — Sample COS/MOS logic circuit arrangements using type CD4007A (Cont'd).

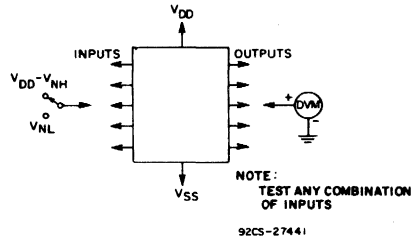


Fig. 15 — Noise-immunity test circuit.

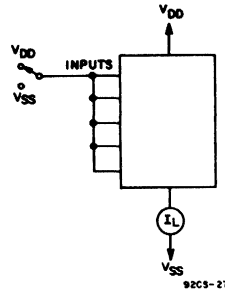


Fig. 16 — Quiescent-device-current test circuit.

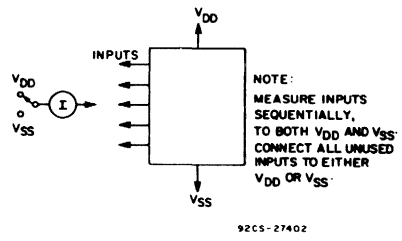


Fig. 17 — Input-leakage-current test circuit.

CD4008A Types

COS/MOS 4-Bit Full Adder

With Parallel Carry Out

The RCA-CD4008A types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008A's. CD4008A inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008A outputs include the four sum bits, S_1 and S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008A section. The CD4008A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications

- **Binary addition/arithmetic units**

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPES E,Y . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS

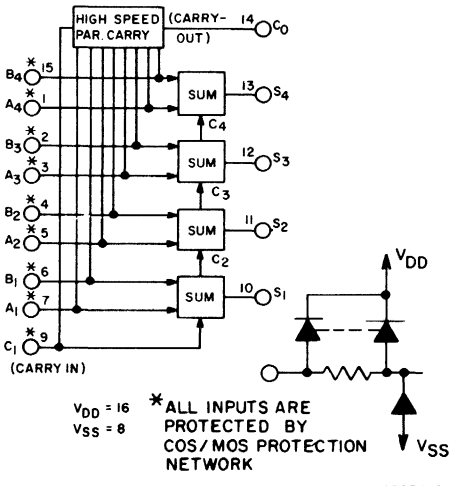
Characteristic		Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	Limits at Indicated Temperatures (°C) D,K,F,H Packages −55	+25 Typ.	+25 Limit	+125	E,Y Packages −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.		—	—	5	5	0.3	5	300	50	0.5	50	700	μA
		—	—	10	10	0.5	10	600	500	1	100	1400	
		—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}		—	0,5	5	0 Typ.; 0.05 Max.								V
		—	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}		—	0,5	5	4.95 Min.; 5 Typ.								
		—	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	—	5	1.5 Min.; 2.25 Typ.								V
		9	—	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}		0.8	—	5	1.5 Min.; 2.25 Typ.								
		1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	—	5	1 Min.								V
		9	—	10	1 Min.								
Inputs High, V_{NMH}		0.5	—	5	1 Min.								
		1	—	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	*	0.5	—	5	0.31	0.5	0.25	0.175	0.155	0.5	0.13	0.105	mA
	*	0.5	—	10	0.93	1.5	0.75	0.53	0.6	1.5	0.5	0.4	
	▲	3	—	5	0.012	0.2	0.01	0.007	0.009	0.2	0.007	0.005	
	▲	3	—	10	0.31	0.5	0.25	0.175	0.24	0.5	0.2	0.16	
p-Channel (Source), I_DP Min.	*	4.5	—	5	-0.31	-0.5	-0.25	-0.175	-0.155	-0.5	-0.13	-0.105	
	*	9.5	—	10	-0.93	-1.5	-0.75	-0.53	-0.6	-1.5	-0.5	-0.4	
	▲	2	—	5	-0.012	-0.2	-0.01	-0.007	-0.008	-0.2	-0.007	-0.005	
	▲	7	—	10	-0.185	-0.3	-0.15	-0.105	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

* Carry Output ▲Sum Output

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A= Full Package-Temp. Range)	3	12	V



92CS-25077R2

Fig. 1 – CD4008A logic diagram.

TRUTH TABLE

A_i	B_i	C_i	C_0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CD4008A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Sum In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Carry In to Sum Out	5	900	1300	900	2000	ns
	10	325	500	325	650	
Sum In to Carry Out	5	320	600	320	800	ns
	10	120	200	120	240	
Carry In to Carry Out	5	100	175	100	200	ns
	10	45	75	45	90	
Transition Time: t_{THL}, t_{TLH} At Sum Outputs	5	1250	2200	1250	2900	ns
	10	550	900	550	1100	
At Carry Output	5	125	225	125	290	ns
	10	45	75	45	90	
Input Capacitance, C_I (Any Input)	—	10	—	10	—	pF

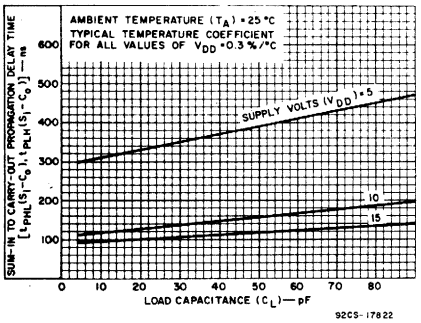


Fig. 2 — Typical sum-in to carry out propagation delay time vs. C_L.

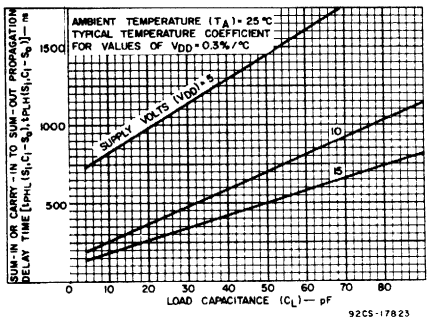


Fig. 3 — Typical sum-in or carry-in to sum-out propagation delay time vs. C_L.

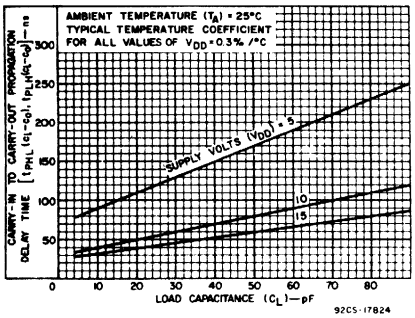


Fig. 4 — Typical carry-in to carry-out propagation delay time vs. C_L.

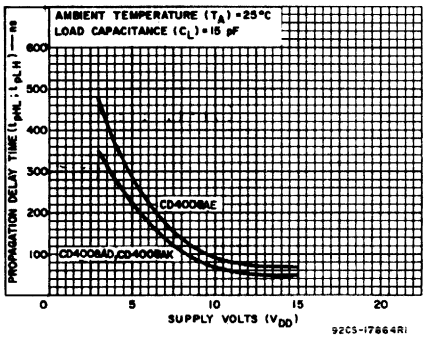


Fig. 5 — Typical maximum propagation delay time vs. V_{DD} for carry-in to carry-out.

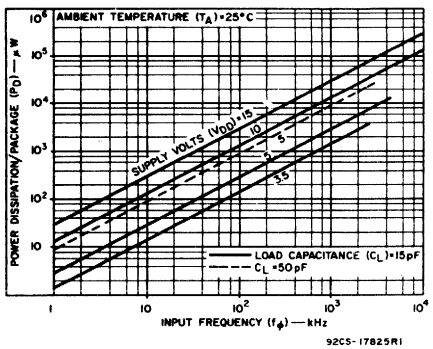


Fig. 6 — Typical dissipation characteristics.

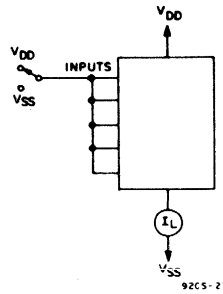


Fig. 7 — Quiescent device current test circuit.

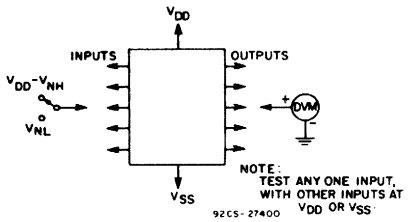


Fig. 8 — Noise immunity test circuit.

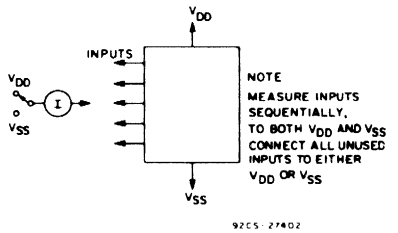


Fig. 9 — Input leakage current test circuit.

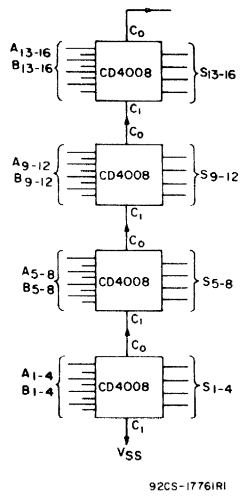


Fig. 10 — Typical connection for a 16-bit adder.

CD4009A, CD4010A Types

COS/MOS Hex Buffers/Converters

Inverting Type: CD4009A
Non-Inverting Type: CD4010A

The RCA-CD4009A and CD4010A Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high sink-current drivers.
The CD4049A and CD4050A are preferred hex buffer replacements for the CD4009A and CD4010A, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069B Hex Inverter is recommended.
The CD4009A and CD4010A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packs (K suffix), and in chip form (H suffix).

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

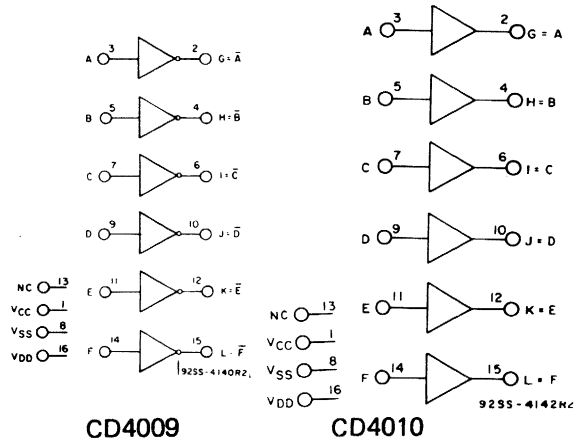


Fig. 1—Logic diagrams.

Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**
- **Multiplexer — 1 to 6 or 6 to 1**

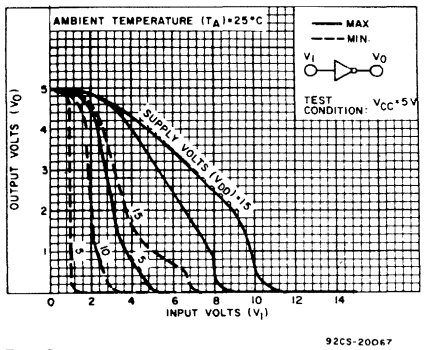


Fig. 2 — Minimum & maximum voltage transfer characteristics — CD4009A.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range : V_{DD} , V_{CC})	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

* The CD4009 and CD4010 have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geqslant V_I \geqslant V_{CC}$.

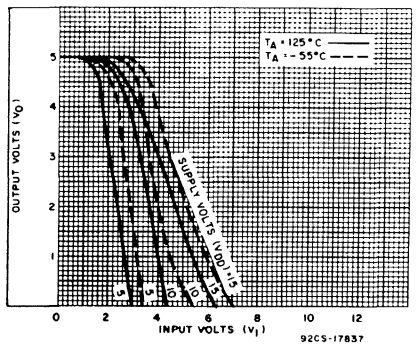


Fig. 3 — Typical voltage transfer characteristics as function of temp. — CD4009A.

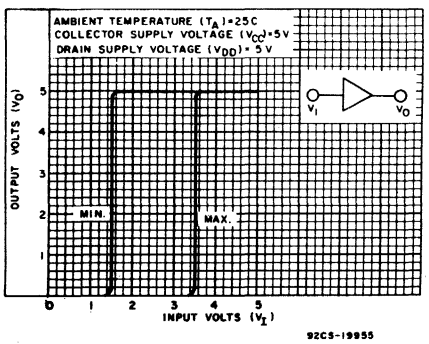


Fig. 4 — Minimum & maximum voltage transfer characteristics (V_{DD} = 5) — CD4010A.

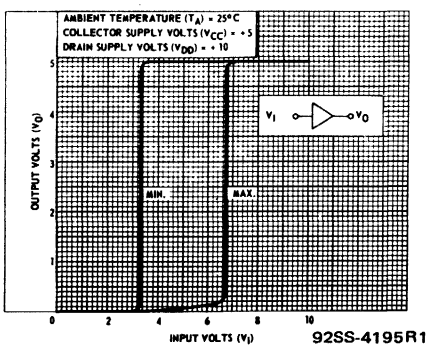


Fig. 5 — Minimum & maximum voltage transfer characteristics (V_{DD} = 10) — CD4010A.

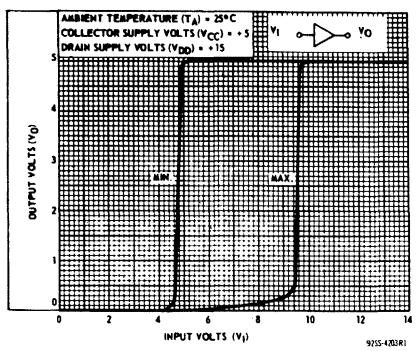


Fig. 6 — Minimum & maximum voltage transfer characteristics (V_{DD} = 15) — CD4010A.

CD4009A, CD4010A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{CC}* (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.5	50	500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
CD4010A	7.2	–	10	.3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
All Types	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL}	3.6	–	5	1 Min.; 1.5 Typ.								
CD4009A	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
CD4010A	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
CD4010A	1	–	10	1 Min.								
Output Drive Current : N-Channel (Sink), I_DN Min.	0.4	–	5	3.75	4	3	2.1	3.6	4	3	2.4	mA
	0.5	–	10	10	10	8	5.6	9.6	10	8	6.4	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.31	-0.5	-0.25	-0.175	-0.3	-0.5	-0.25	-0.2	
	2.5	–	5	-1.85	-1.75	-1.25	-0.9	-1.5	-1.75	-1.25	-1	
	9.5	–	10	-0.9	-0.8	-0.6	-0.4	-0.72	-0.8	-0.6	-0.48	
Input Leakage Current, I_{IL},I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

* $V_{CC} = V_{DD}$

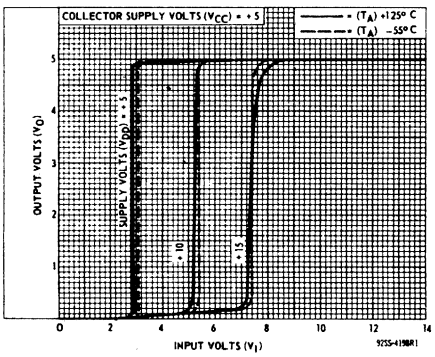


Fig. 7 — Typical voltage transfer characteristics as a function of temperature — CD4010A.

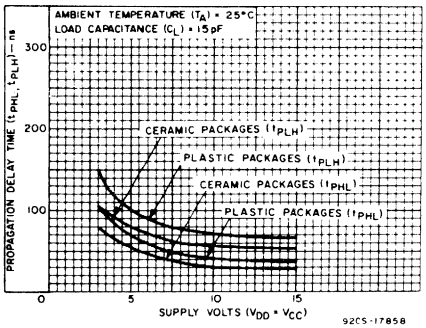


Fig. 8 — Maximum propagation delay time vs. V_{DD} — CD4010A.

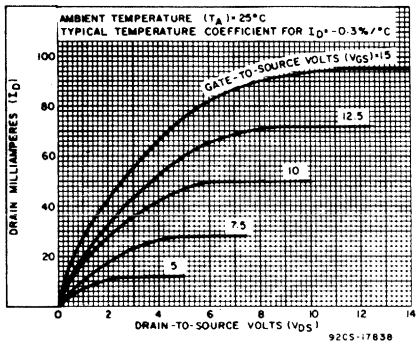


Fig. 9 — Typical n-channel drain characteristics,

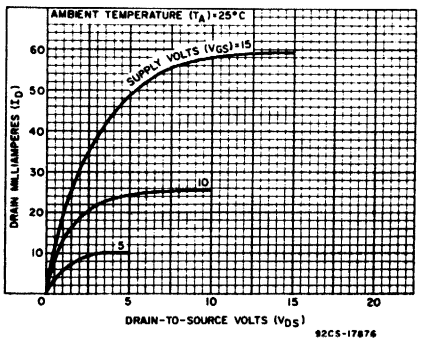


Fig. 10 — Minimum n-channel drain characteristics.

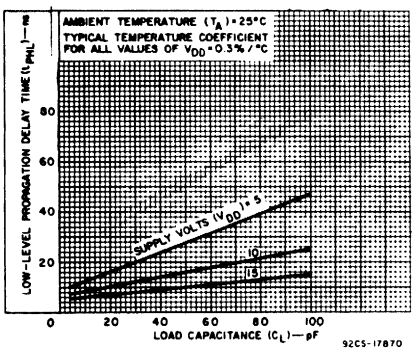


Fig. 11 — Typical high-to-low level propagation delay time vs. C_L.

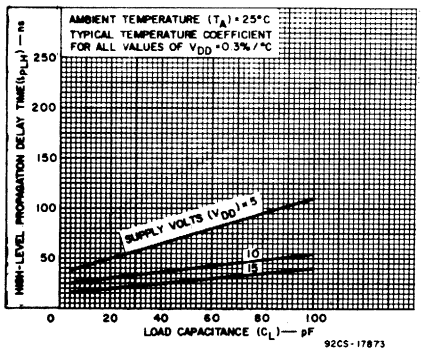


Fig. 12 — Typical low-to-high level propagation delay time vs. C_L.

CD4009A, CD4010A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

CHARACTERISTIC	CONDITION			LIMIT		UNITS
	V_{DD} (V)	V_I (V)	V_{CC} (V)	Typ.	Max.	
D, F, K, H Packages						
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	50	80	ns
	10	10	10	25	55	
	10	10	5	15	30	
High-to-Low, t_{PHL}	5	5	5	15	55	
	10	10	10	10	30	
	10	10	5	10	25	
Transition Time: Low-to-High, t_{TLH}	5	5	5	80	125	ns
	10	10	10	50	100	
High-to-Low, t_{THL}	5	5	5	20	45	
	10	10	10	16	40	
Input Capacitance, C_I CD4009	–	–	–	15	–	pF
CD4010	–	–	–	5	–	
E, Y Packages						
Propagation Delay Time: Low-to-high, t_{PLH}	5	5	5	50	100	ns
	10	10	10	25	70	
	10	10	5	15	40	
High-to-Low, t_{PHL}	5	5	5	15	70	
	10	10	10	10	40	
	10	10	5	10	35	
Transition Time: Low-to-High, t_{PLH}	5	5	5	80	160	ns
	10	10	10	50	120	
High-to-Low, t_{THL}	5	5	5	20	60	
	10	10	10	16	50	
Input Capacitance, C_I CD4009	–	–	–	15	–	pF
CD4010	–	–	–	5	–	

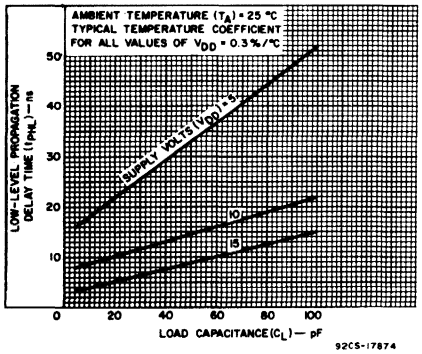


Fig. 13 – Typical high-to-low level propagation delay time vs. C_L (driving TTL, DTL).

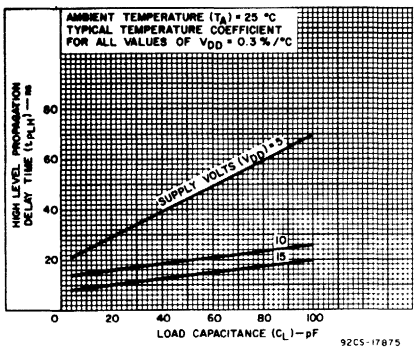


Fig. 14 – Typical low-to-high level propagation delay time vs. C_L (driving TTL, DTL)

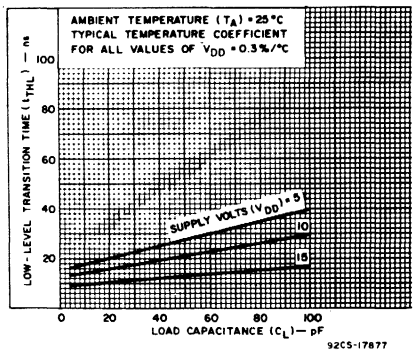


Fig. 15 – Typical high-to-low level transition time vs. C_L.

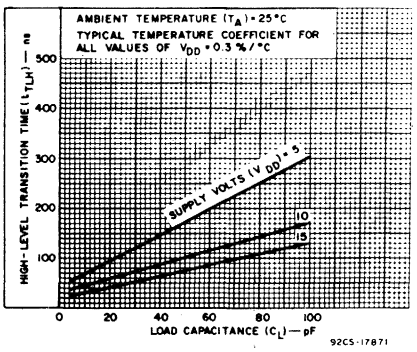


Fig. 16 – Typical low-to-high level transition time vs. C_L.

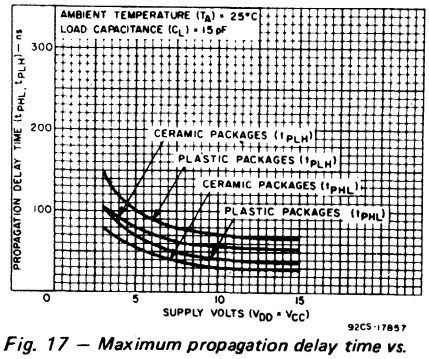


Fig. 17 – Maximum propagation delay time vs. V_{DD} – CD4009A.

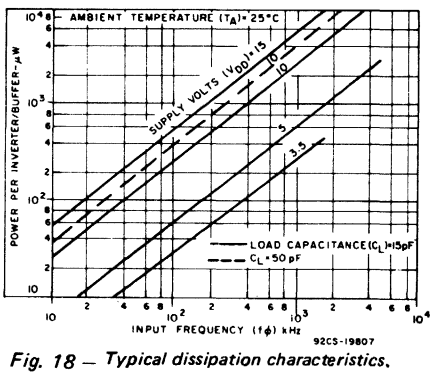


Fig. 18 – Typical dissipation characteristics.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

CD4011A, CD4012A, CD4023A Types

COS/MOS NAND Gates

Features:

- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Quad 2 Input – CD4011A
Dual 4 Input – CD4012A
Triple 3 Input – CD4023A

The RCA-CD4011A, CD4012A, and CD-4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

The CD4011A, CD4012A, and CD4023A types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

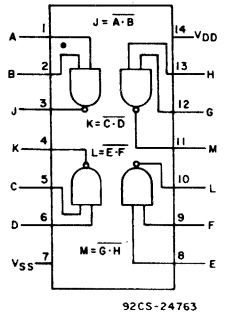
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

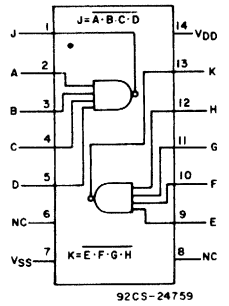
Characteristic	Min.	Max.	Units
Supply Voltage Range (over full package temperature range)	3	12	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

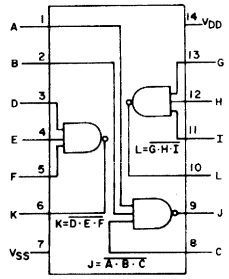
STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E,Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C



CD4011A



CD4012A



CD4023A

Fig. 1 – Functional diagrams.

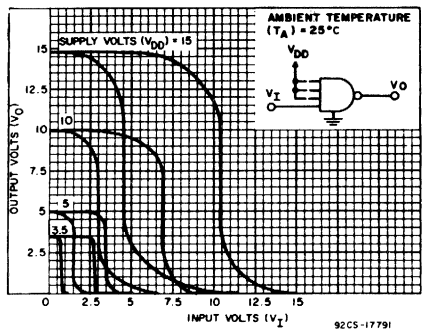


Fig. 2 – Minimum & maximum voltage transfer characteristics.

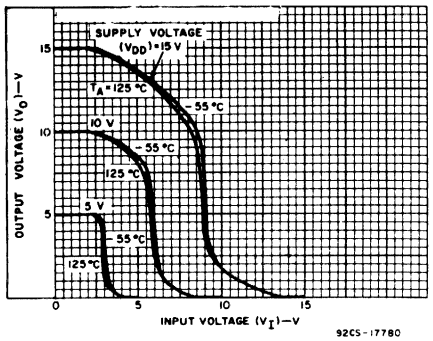


Fig. 3 – Typical voltage transfer characteristics as a function of temperature.

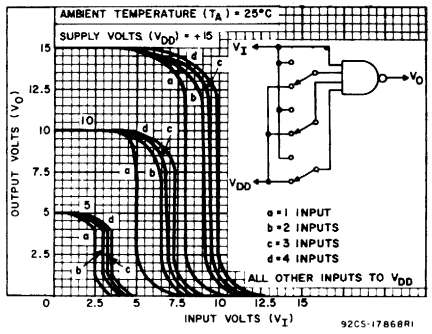


Fig. 4 – Typical multiple input switching transfer characteristics for CD4012A.

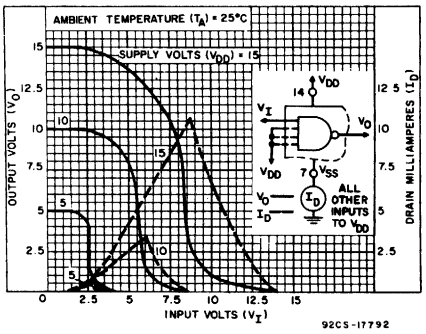


Fig. 5 – Typical current & voltage transfer characteristics.

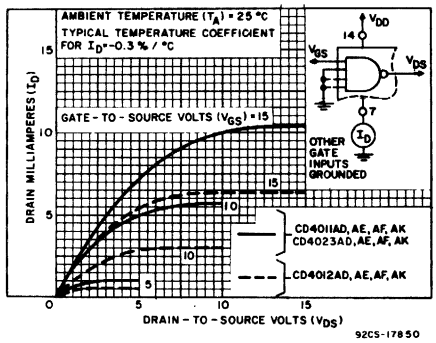


Fig. 6 – Typical n-channel drain characteristics.

CD4011A, CD4012A, CD4023A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	–	–	10	0.1	0.001	0.1	6	5	0.005	5	30	
	–	–	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low-Level V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.;								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_{DN} Min. CD4011A	0.5	–	5	0.31	0.5	0.25	0.175	0.145	0.5	0.12	0.095	mA
CD4023A	0.5	–	10	0.62	0.6	0.5	0.35	0.3	0.6	0.25	0.2	
CD4012A	0.5	–	5	0.15	0.25	0.12	0.085	0.072	0.25	0.06	0.05	
	0.5	–	10	0.31	0.6	0.25	0.175	0.155	0.6	0.13	0.105	
P-Channel (Source), I_{DP} Min. All Types	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.75	-1.2	-0.6	-0.4	-0.35	-1.2	-0.3	-0.24	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

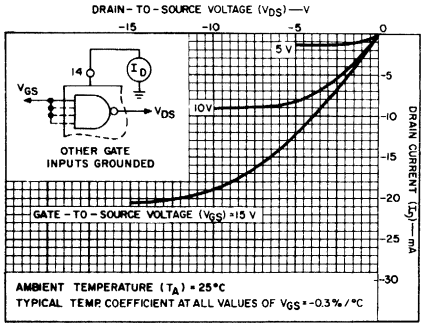


Fig. 7 – Typical p-channel drain characteristics.

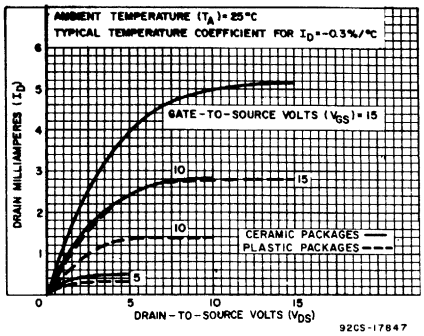


Fig. 8 – Minimum n-channel drain characteristics –CD4011A & CD4023A.

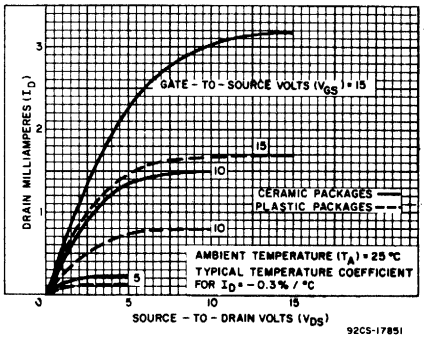


Fig. 9 – Minimum n-channel drain characteristics – CD4012A.

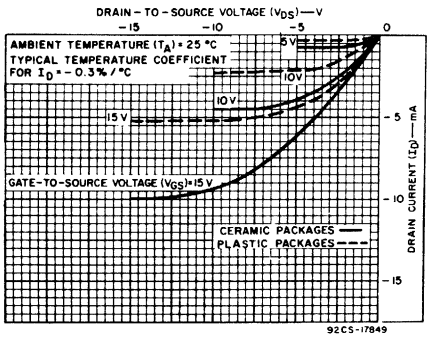


Fig. 10 – Minimum p-channel drain characteristics.

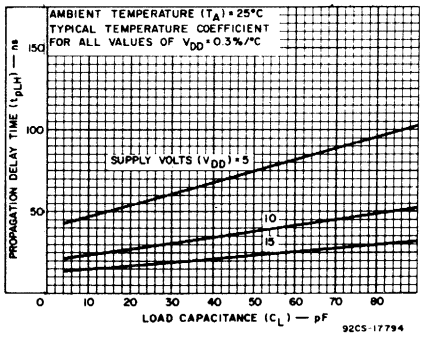


Fig. 11 – Typical low-to-high level propagation delay time vs. C_L.

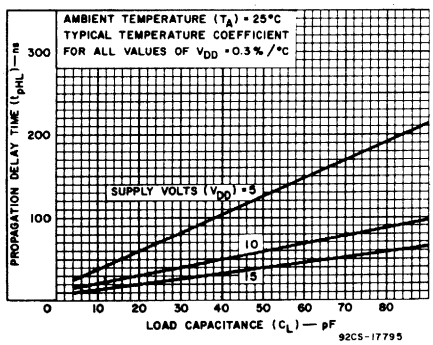


Fig. 12 – Typical high-to-low level propagation delay time vs. C_L – CD4011A, & CD4023A.

CD4011A, CD4012A, CD4023A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 15 pF, Input t_r, t_f = 20 ns, R_L = 200 KΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS				UNITS
			D,F,K,H Packages		*E,Y Packages*		
		V_{DD} (V)	Typ.	Max.	Typ.	Max.	
Propagation Delay Time: Low-to-High Level, t_{PLH}		5	50	75	50	100	ns
		10	25	40	25	50	
High-to-Low Level, t_{PHL} CD4011A and CD4023A		5	50	75	50	100	ns
		10	25	40	25	50	
CD4012A		5	100	150	100	200	ns
		10	50	75	50	100	
Transition Time: Low-to-High Level, t_{TLH}		5	75	100	75	125	ns
		10	40	60	40	75	
High-to-Low Level, t_{THL} CD4011A and CD4023A		5	75	125	75	150	ns
		10	50	75	50	100	
CD4012A		5	250	375	250	500	ns
		10	125	200	125	250	
Input Capacitance, C_I	Any Input		5	—	5	—	pF

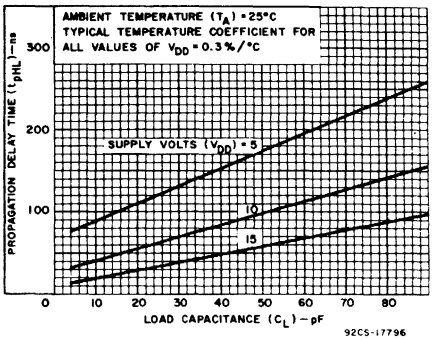


Fig. 13 – Typical high-to-low level propagation delay time vs. C_L – CD4012A.

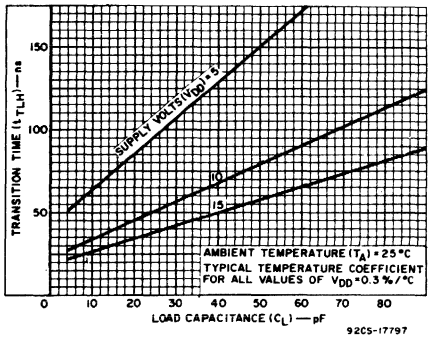


Fig. 14 – Typical low-to-high transition time vs. C_L.

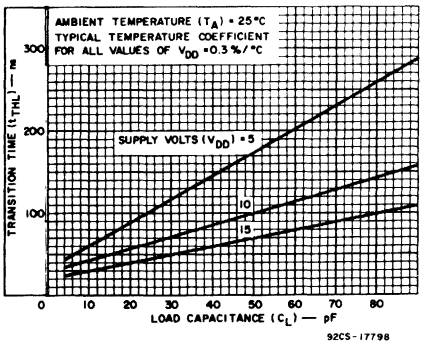


Fig. 15 – Typical high-to-low level transition time vs. C_L – CD4011A & CD4023A.

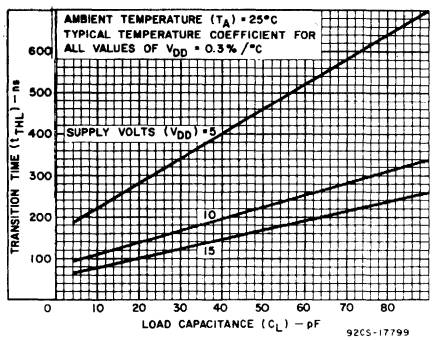


Fig. 16 – Typical high-to-low level transition time vs. C_L – CD4012A.

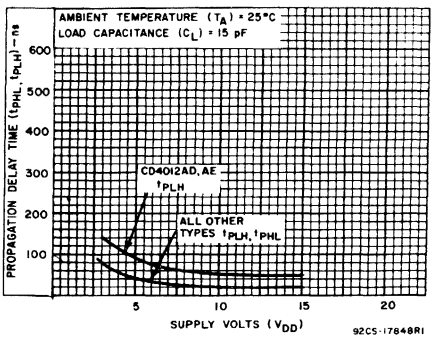


Fig. 17 – Minimum propagation delay time vs. V_{DD}.

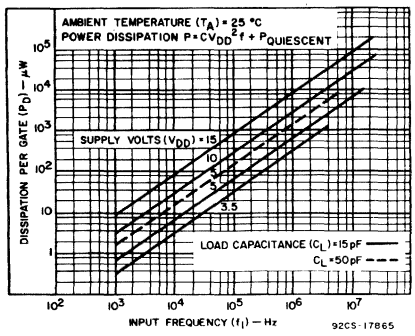


Fig. 18 – Typical dissipation characteristics.

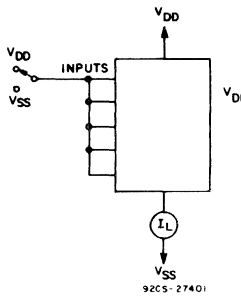


Fig. 19 – Quiescent device current test circuit.

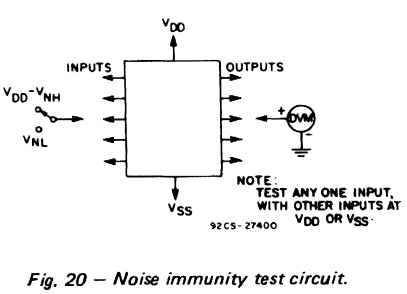


Fig. 20 – Noise immunity test circuit.

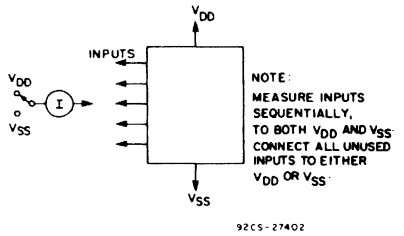


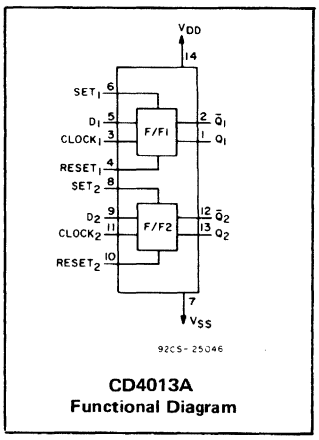
Fig. 21 – Input leakage current test circuit.

CD4013A Types

Dual 'D'-Type Flip-Flop

The RCA-CD4013A consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4013A
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation — 10 MHz (typ.) clock toggle rate at 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Registers, counters, control circuits**

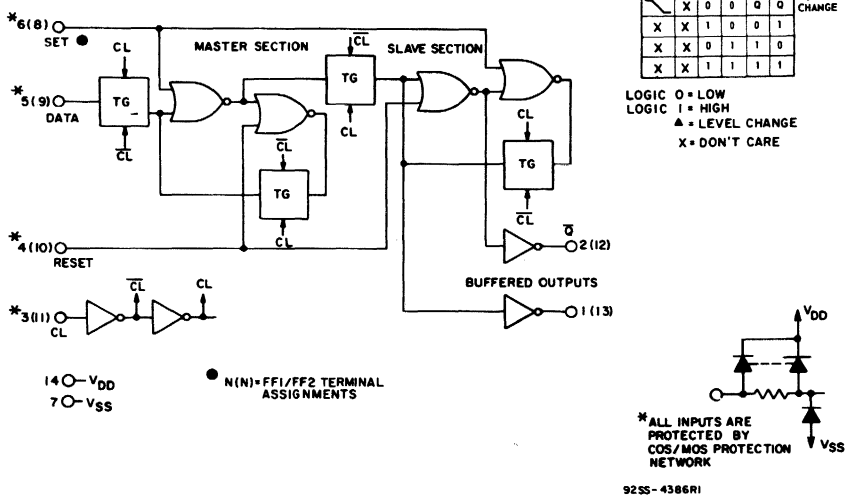


Fig. 1 — Logic diagram and truth table for CD4013A (one of two identical flip flops).

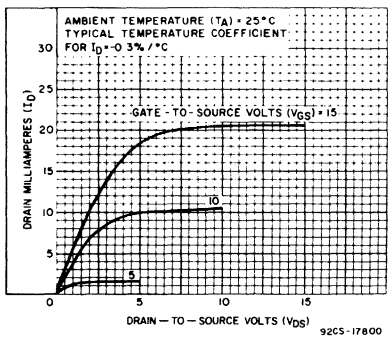


Fig.2 — Typical n-channel drain characteristics.

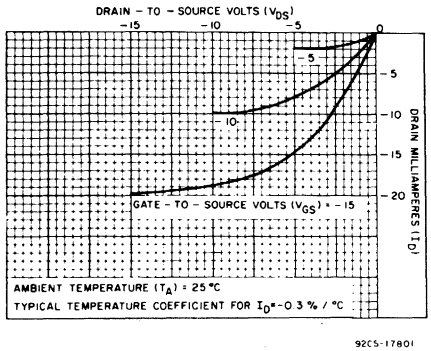


Fig.3 — Typical p-channel drain characteristics.

CD4013A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges –

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	LIMITS D,F,K,H Packages Max.	LIMITS E,Y Packages Min.	LIMITS E,Y Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Data Setup Time t_S	5	40	–	50	–	ns
	10	20	–	25	–	
Clock Pulse Width t_W	5	200	–	500	–	ns
	10	80	–	100	–	
Clock Input Frequency f_{CL}	5		2.5		1	MHz
	10	dc	7	dc	5	
Clock Rise or Fall Time t_rCL*, t_fCL	5	–	15	–	15	μs
	10	–	5	–	5	
Set or Reset Pulse Width	5	250	–	500	–	ns
	10	100	–	125	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

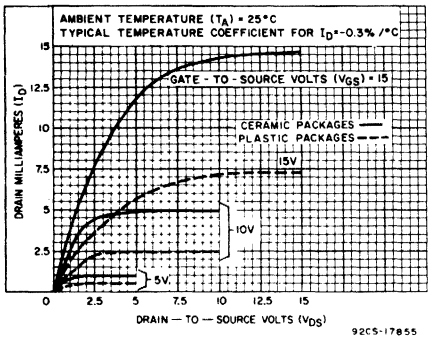


Fig.4 – Minimum n-channel drain characteristics.

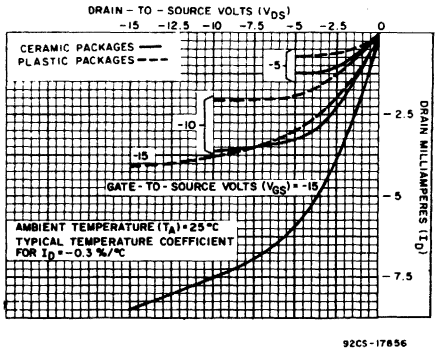


Fig.5 – Minimum p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	Typ.	Max.	LIMITS E,Y Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	350	ns
	10	–	75	110	–	75	125	
Set to Q or Reset to $\bar{Q}$ t_{PLH}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Set to $\bar{Q}$ or Reset to Q t_{PHL}	5	–	175	300	–	175	350	ns
	10	–	75	110	–	75	125	
Transition Time, t_{THL}, t_{TLH}	5	–	75	125	–	75	150	ns
	10	–	50	70	–	50	75	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4	–	1	4	–	MHz
	10	7	10	–	5	10	–	
Minimum Clock Pulse Width, t_W	5	–	125	200	–	125	500	ns
	10	–	50	80	–	50	100	
Minimum Set or Reset Pulse Width, t_W	5	–	125	250	–	125	500	ns
	10	–	50	100	–	50	125	
Minimum Data Setup Time, t_S	5	–	20	40	–	20	50	ns
	10	–	10	20	–	10	25	
Clock Rise or Fall Time t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

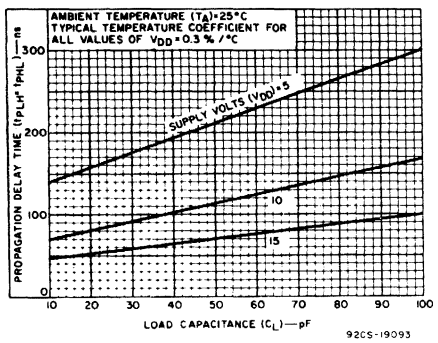


Fig.6 – Typical propagation delay time vs. C_L.

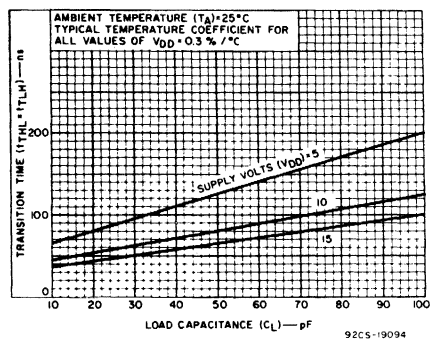


Fig.7 – Typical transition time vs. C_L.

CD4013A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								
	–	0.10	10	10 Typ.; 9.95 Min.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source) I_{DP} Min.	4.5	–	5	−0.31	−0.5	−0.25	−0.175	−0.17	−0.5	−0.14	−0.12	
	9.5	–	10	−0.8	−1.3	−0.65	−0.45	−0.4	−1.3	−0.33	−0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

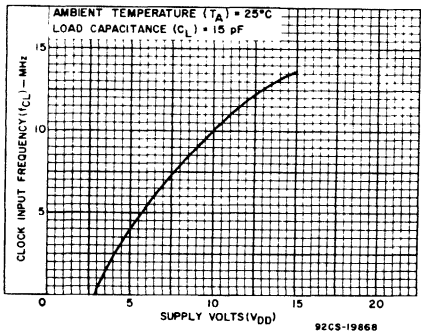


Fig.8 – Typical maximum clock input frequency vs. V_{DD}.

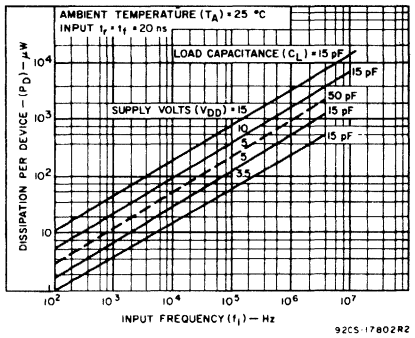


Fig.9 – Typical dissipation characteristics.

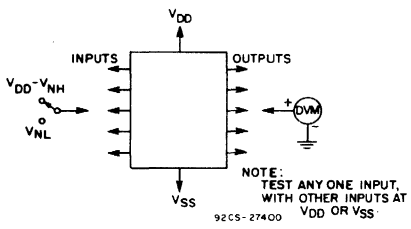


Fig.10 – Noise immunity test circuit.

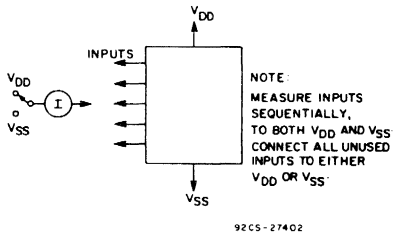


Fig.11 – Input leakage test circuit.

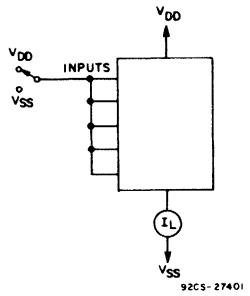


Fig.12 – Quiescent device-current test circuit.

CD4014A Types

COS/MOS 8-Stage Static Shift Register

Synchronous Parallel or
Serial Input/Serial Output

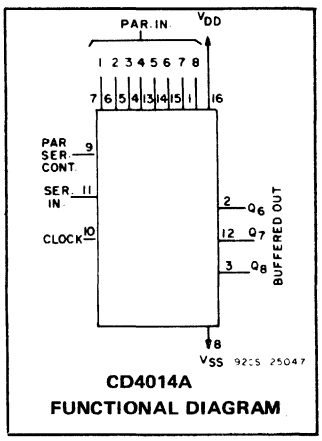
RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A= Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	350	—	500	—	ns
	10	80	—	100	—	
Clock Pulse Width, t_W	5	500	—	830	—	ns
	10	175	—	200	—	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	3	dc	2.5	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	—	15	—	15	μs
	10	—	15	—	15	

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
	D,K,F,H Packages							*E,Y Packages*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	—	—	5	5	0.5	5	300	50	0.5	50	700	μA
	—	—	10	10	1	10	600	100	1	100	1400	
	—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High, V_{NMH}	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	—	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	—	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
p-Channel (Source): I_DP Min.	4.5	—	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	—	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA



CD4014A
FUNCTIONAL DIAGRAM

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

The RCA-CD4014A types are 8-stage parallel-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL INPUTS, a single SERIAL DATA INPUT, and individual parallel "JAM" INPUTS to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronous with the positive clock line transition and under control of the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. Register expansion using multiple CD4014A packages is permitted.

The CD4014A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16- lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

CL ▲	SER. IN	PAR SER CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n
⌐¯	X	1	0	0	0	0
⌐¯	X	1	1	0	1	0
⌐¯	X	1	0	1	0	1
⌐¯	X	1	1	1	1	1
⌐¯	0	0	X	X	0	Q_n-1
⌐¯	1	0	X	X	1	Q_n-1
¯⌐	X	X	X	X	Q_1	Q_n NC

X = DON'T CARE CASE ▲ = LEVEL CHANGE
NC = NO CHANGE

Fig. 1 – Truth table.

CD4014A Types

Features:

- Medium speed operation. . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Synchronous parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E,Y Packages*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}		5	–	150	300	–	150	400	ns
		10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Minimum Data Set Up Time, t_S		5	–	100	350	–	100	500	ns
		10	–	50	80	–	50	100	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

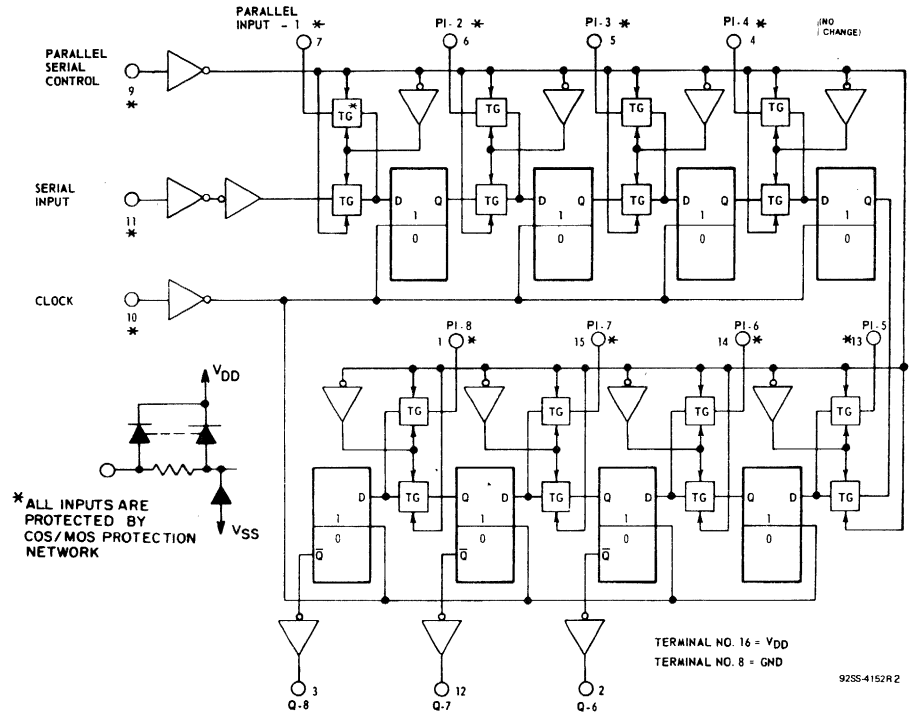


Fig. 5 — Logic block diagram.

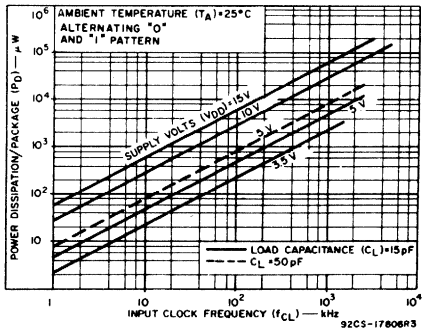


Fig. 2 — Typical dissipation characteristics.

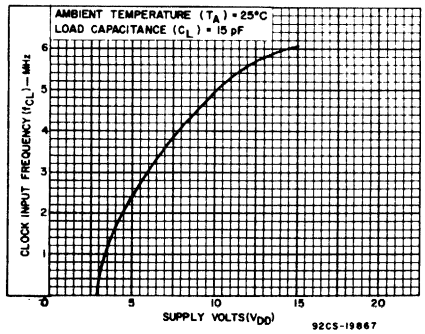


Fig. 3 — Typical clock input frequency vs. supply voltage.

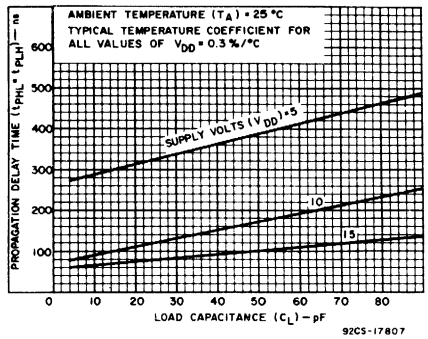


Fig. 4 — Typical propagation delay time vs. load capacitance.

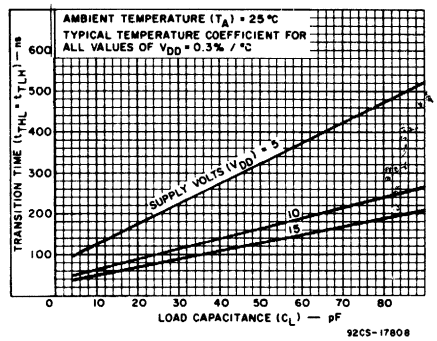


Fig. 6 — Typical transition time vs. load capacitance.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

CD4015A Types

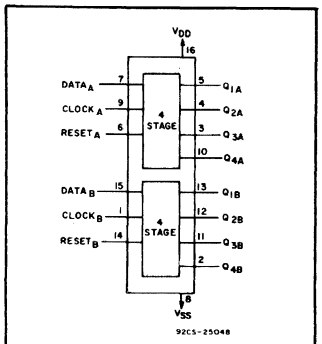
COS/MOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

The RCA-CD4015A consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition.

Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015A package, or to more than 8 stages using additional CD4015A's is possible.

The CD4015A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4015A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to + 60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12mW/°C to 200 mW

FOR T_A = -55 to + 100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = + 100 to +125°C (PACKAGE TYPES D, F, K) . . . .Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 15	– –	15 15	μs
Clock Reset Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Features:

- **Medium speed operation . . . . . 5 MHz (typ.) clock rate at $V_{DD} - V_{SS}$ = 10V**
- **Fully static operation**
- **8 master-slave flip-flops plus output buffering**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial-input/parallel-output data queueing**
- **Serial to parallel data conversion**
- **General-purpose register**

TRUTH TABLE

CL▲	D	R	Q_1	Q_n
⌐⌐	0	0	0	Q_{n-1}
⌐⌐	1	0	1	Q_{n-1}
⌐⌐	X	0	Q_1	Q_n (NO CHANGE)
X	X	1	0	0

▲= LEVEL CHANGE
X = DON'T CARE CASE

Fig. 1 – Truth table.

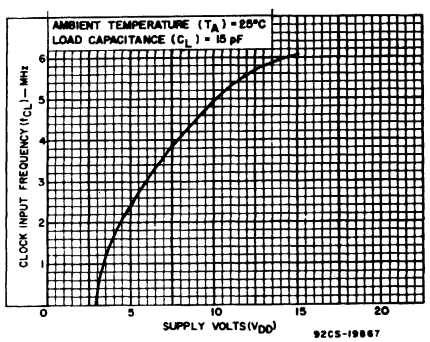


Fig. 2 – Typical clock input frequency vs. supply voltage.

CD4015A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

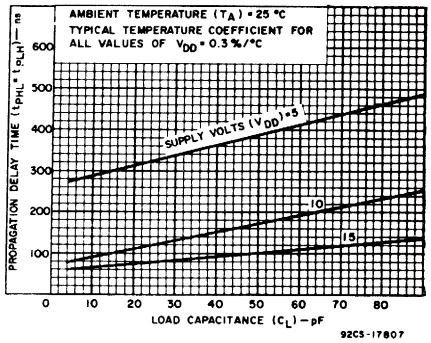


Fig. 3. — Typical propagation-delay time vs. load capacitance.

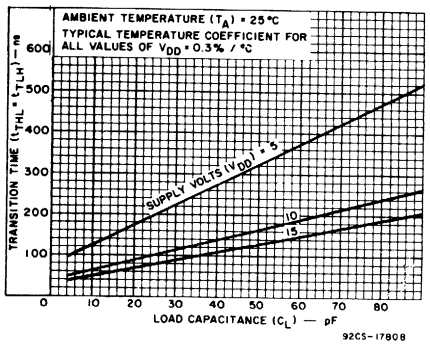


Fig. 4 — Typical transition time vs load capacitance.

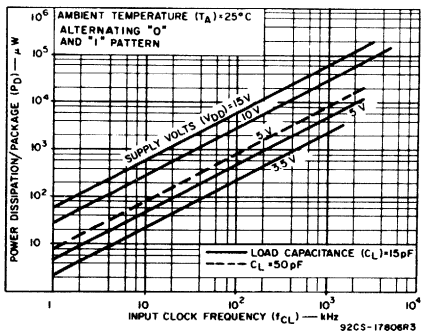


Fig. 5 — Typical dissipation characteristics.

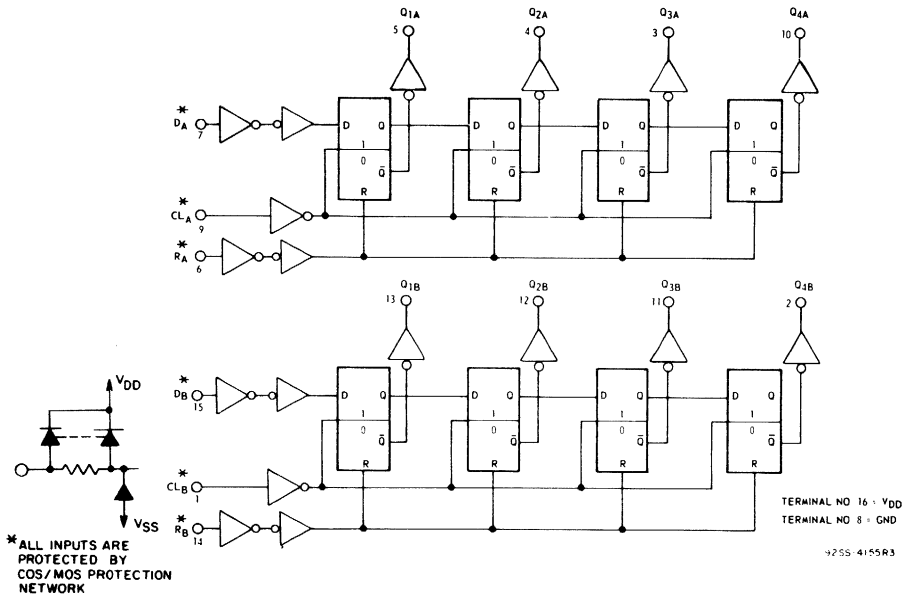


Fig. 6 — Logic diagram.

CD4015A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MIN.	
CLOCKED OPERATION								
Propagation Delay Time; T_{PLH}, T_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	300	
Transition Time; t_{THL}, t_{TLH}	5	–	150	300	–	150	400	ns
	10	–	75	125	–	75	150	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL, t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Data Set-up Time, t_S	5	–	100	350	–	100	500	ns
	10	–	50	80	–	50	100	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2.5	5	–	
Average Input Capacitance, C_I		–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time, T_{PLH}, T_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	300	
Minimum Set and Reset Pulse Widths t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitve load.

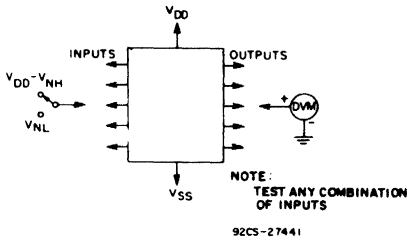


Fig. 7 — Noise-immunity test circuit.

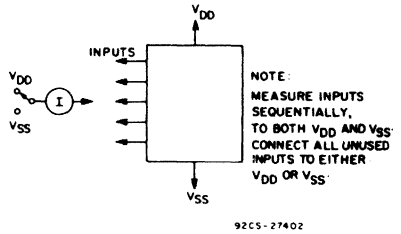
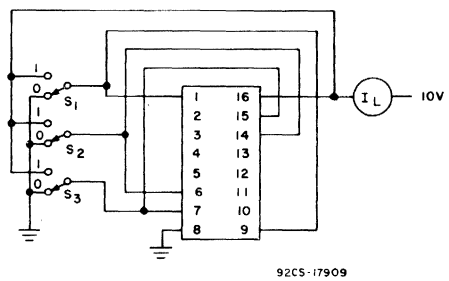


Fig. 8 — Input-leakage-current test circuit.



Test performed with the following sequence of "1's" and "0's"

	S_1	S_2	S_3
Test	0	1	0
Don't Test	0	0	1
Don't Test	1	0	1
Don't Test	0	0	0
Don't Test	1	0	0
Don't Test	0	0	1
Test	1	0	1
Don't Test	0	0	0
Test	1	0	0

Fig. 9 — Quiescent-device-current test circuit.

CD4016A Types

COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

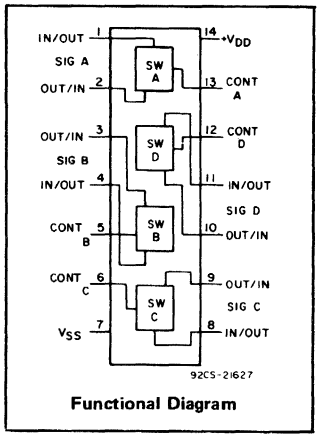
The RCA-CD4016A Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

The CD4016 "A" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F,Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **280-Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq 10$ V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: −50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.



Functional Diagram

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON}(max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
R_{ON}(max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON}(max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from a perfect switch, R_{ON} = 0Ω.

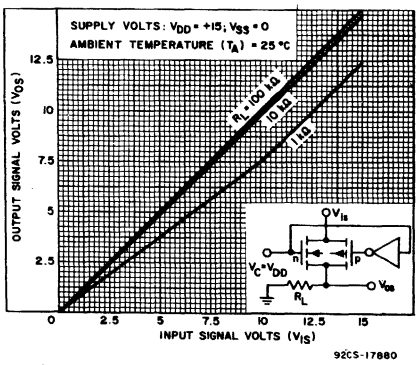


Fig.1 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

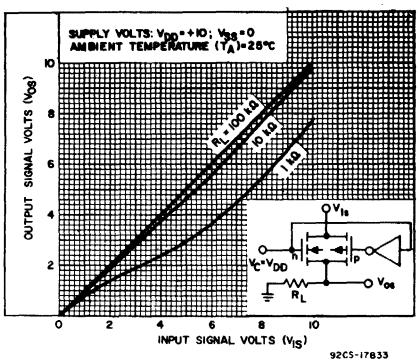


Fig.2 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

CD4016A Types

ELECTRICAL CHARACTERISTICS (All inputs. . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). .3 to 15 V)

Characteristic	Test Conditions *All Voltage Values are in Volts*		Limits *Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E,Y Packages*						Unit
		V_{DD} (V)	−55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	
Quiescent Device Current, I_L max (All switches ON or all Switches OFF) D,F,K,H Pkgs.		5	0.25	–	–	10	0.01	0.25	μA
		10	0.5	–	–	20	0.01	0.5	
		15	2	–	–	40	0.01	2	
E,Y Pkgs.		5	–	0.25	5	–	–	0.25	μA
		10	–	0.5	10	–	–	0.5	
		15	–	2	20	–	–	2	
Signal Inputs (V_{is}) and Outputs (V_{os})									
ON Resistance, R_{ON}	$V_C=V_{DD}$	V_{SS}	V_{is}	Typ/Max	Typ/Max	Typ/Max	Typ/Max			Ω
	R_L = 10 kΩ●								
	+7.5	-7.5	+7.5	120/360	130/370	260/520	300/600	200	400	
			−7.5	120/360	130/370	260/520	300/600	200	400	
			±0.25	130/775	160/790	400/1080	470/1230	280	850	
	+5	−5	+5	130/600	150/610	340/840	400/960	250	660	
			−5	130/600	150/610	340/840	400/960	250	660	
			±0.25	325/1870	370/1900	770/2380	900/2600	580	2000	
	+15	0	+15	120/360	130/370	260/520	300/600	200	400	
			+0.25	120/360	130/370	260/520	300/600	200	400	
			+9.3	150/775	180/790	400/1080	490/1230	300	850	
	+10	0	+10	130/600	150/610	340/840	400/960	250	660	
			+0.25	130/600	150/610	340/840	400/960	250	660	
			+5.6	300/1870	350/1900	750/2380	880/2600	560	2000	
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	R_L = 10 kΩ●									Ω
	+7.5	-7.5	±7.5	–	–	–	–	10	–	
	+5	−5	±5	–	–	–	–	15	–	
Sine Wave Response (Distortion)	+5	−5	5 p-p▲							%
	R_L = 10 kΩ, f_{is} = 1 kHz			–	–	–	–	0.4	–	
Frequency Response Switch ON (Sine-Wave Input)	V_{DD}=+5, $V_C=V_{SS}$=−5		−5 p-p							MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB			–	–	–	–	40	–	
Feedthrough Switch OFF	+5	−5	−5 p-p							MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB			–	–	–	–	1.25	–	
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C=V_{SS}$	±7.5	–	–	–	–	±100	–	pA
	+7.5	−7.5								
	+5	−5	±5	–	–	–	–	$\pm 10 \times 10^{-3}$	±125*	nA

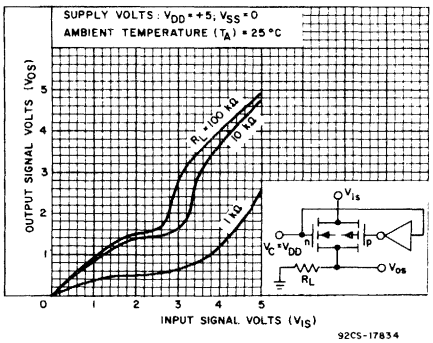


Fig.3 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

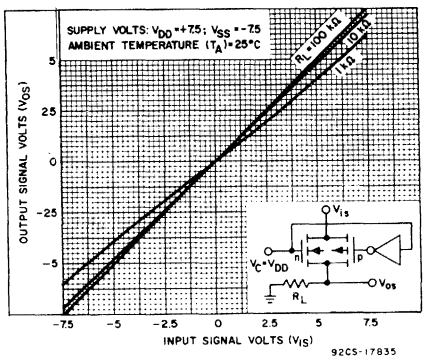


Fig.4 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

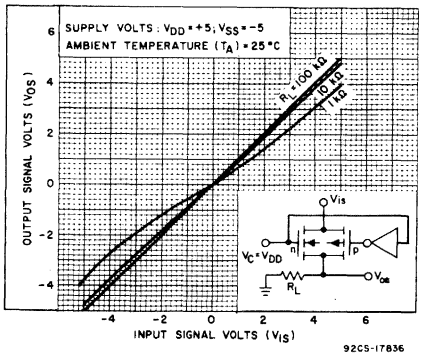


Fig.5 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

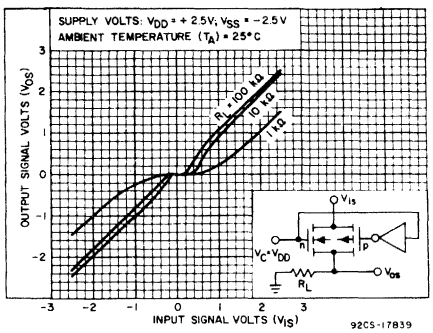


Fig.6 – Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

CD4016A Types

ELECTRICAL CHARACTERISTICS (Cont'd) . . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). .3 to 15 V)

Characteristic	Test Conditions *All Voltage Values are in Volts*	V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages* *Values at −40°C,+25°C,+85°C Apply to E,Y Packages* −55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Crosstalk Between Any 2 of 4 Switches (f = −50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$, $V_{is}(A)$ = 5 p-p, R_L=1 kΩ, $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB		–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ = 10, V_{SS} = GND, C_L = 50 pF, V_{is} = 10 Sq. Wave, t_r, t_f = 20 ns	V_{DD} 5					20	50	ns
		10					10	25	
Capacitance: Input, C_{is}	V_{DD}=+5		–	–	–	–	4	–	pF
Output, C_{os}	$V_{CC}=V_{SS}=-5$		–	–	–	–	4	–	
Feedthrough, C_{ios}			–	–	–	–	0.2	–	
Control (V_C)									
Switch Threshold Voltage, V_{TH}	$V_{is}\leq V_{DD}$, I_{is}=10μA, $V_{DD}-V_{SS}$=15,10,5		0.7min 2.9max	– –	– –	0.2min 2.4max	0.5min 2.7	1.5	V
Input Leakage Current, I_{IL} max	$V_{is}\leq V_{DD}$	V_{DD} =15	±10^{-5} typ; ±1 max.						μA
Crosstalk (Control Input to Signal Output)	V_C=10 (Sq.Wave), t_r,t_f=20 ns, R_L=10 kΩ	V_{DD} =10	–	–	–	–	50	–	mV
Turn-On Propagation Delay, t_p dc	$V_{DD}-V_{SS}$=10, V_C =10 (See Fig.25), t_r,t_f=20 ns, C_L=15 pF, R_L= 1 kΩ	V_{DD} 5	–	–	–	–	20	40	ns
		10	–	–	–	–	10	20	
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1 kΩ, C_L=15 pF, V_{CC}=10(Sq.Wave), t_r,t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage current measurement for automatic testing.

▲ Symmetrical about 0 volts.

● For all test conditions.

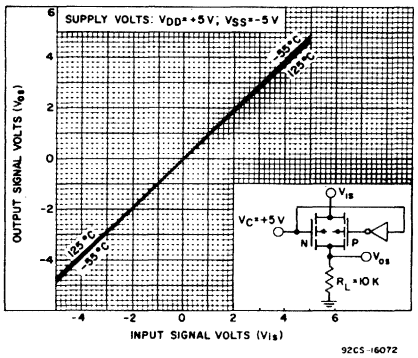


Fig.7 – Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

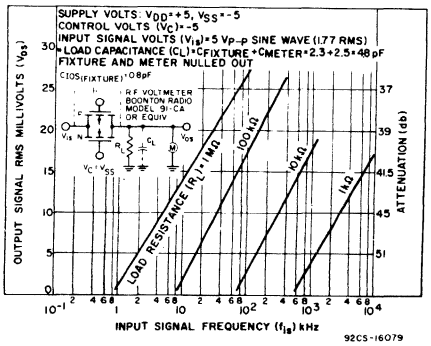


Fig.8 – Typ. feedthru vs. frequency – switch "OFF".

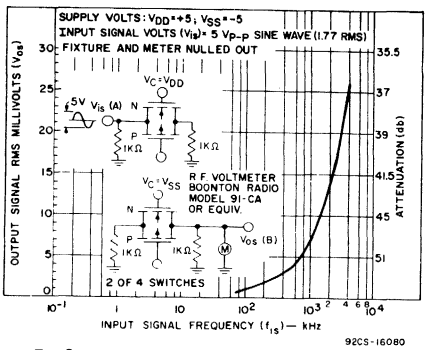


Fig.9 – Typical crosstalk between switch circuits in the same package.

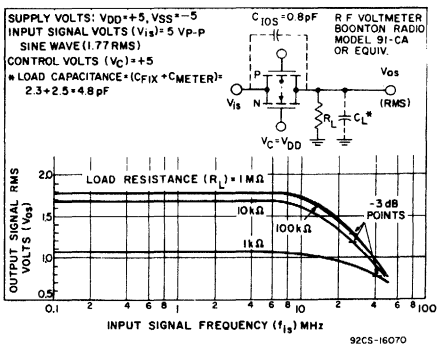


Fig.10 – Typical switch frequency response – switch "ON".

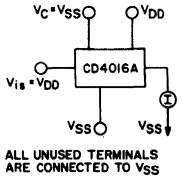


Fig.11 – "OFF" switch input or output leakage current test circuit.

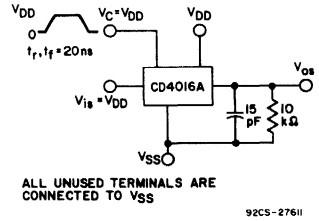


Fig.12 – Test circuit for square-wave response.

CD4016A Types

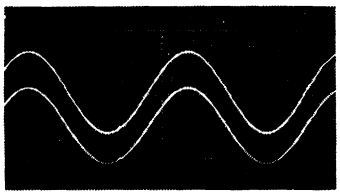


Fig.13 Typical sine wave response of V_{DD} = +7.5 V, V_{SS} = −7.5 V.

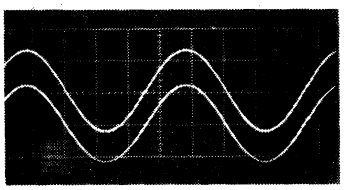


Fig.14 — Typical sine wave response of V_{DD} = +5 V, V_{SS} = −5 V.

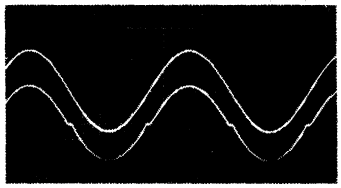


Fig.15 — Typical sine wave response of V_{DD} = +2.5 V, V_{SS} = −2.5 V.

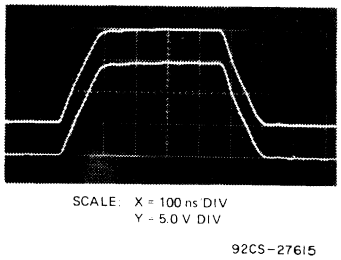


Fig.16 — Typical square wave response at $V_{DD} = V_C$ = +15 V, V_{SS} = Gnd.

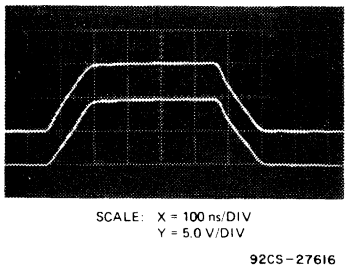


Fig.17 — Typical square wave response at V_{DD} = V_C = +10 V, V_{SS} = Gnd.

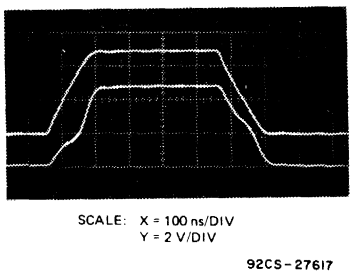


Fig.18 — Typical square wave response at V_{DD} = V_C = +5 V, V_{SS} = Gnd.

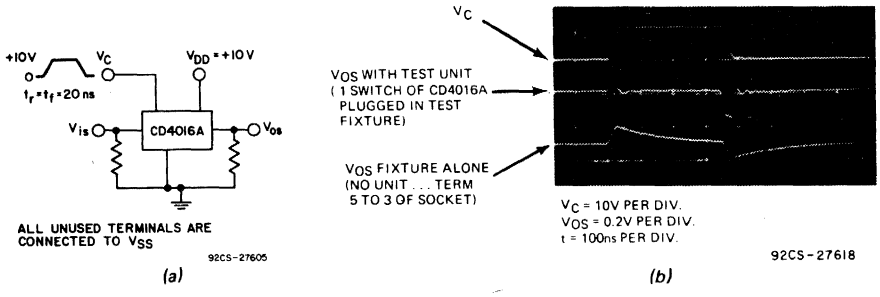


Fig.19 — Crosstalk-control input to signal output.

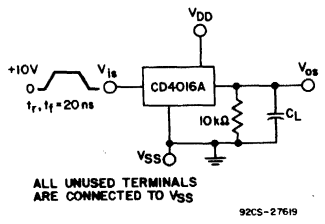


Fig.20 — Propagation delay time signal input (V_{IS}) to signal output (V_{OS}).

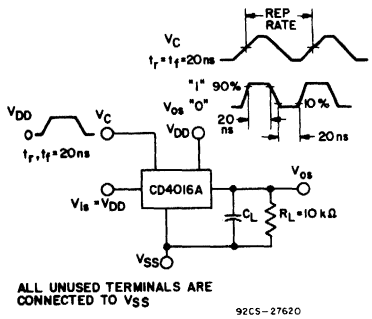


Fig.21 — Max. allowable control-input repetition rate.

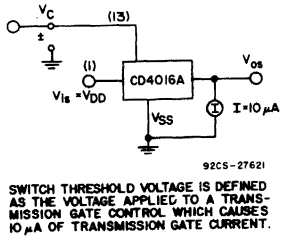


Fig.22 — Switch threshold voltage.

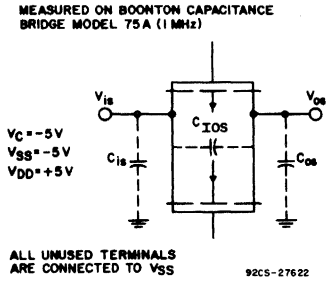


Fig.23 — Capacitance C_{IOS} and C_{OS}.

CD4017A Types

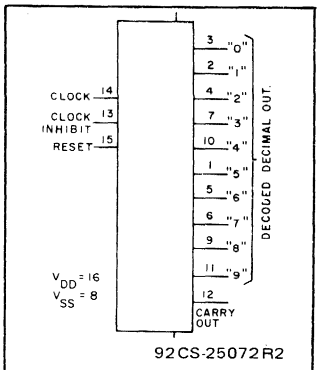
COS/MOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

The RCA-CD4017A consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal.

The decade counter is advanced one count at the positive clock signal transition If the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the clock INHIBIT signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decimal time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The CD4017A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4017A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to + 85°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to 100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Features:

- Synchronous decade counter plus 10 decoded outputs
- Fully static operation
- Medium speed operation. . .
  . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range range)
- 1-V noise margin (full package-temperature range)

Applications:

- Decade counter/decimal decode display
- Frequency division
- Counter control/timers
- Divide by N counting
  N = 2 – 10 with one CD4017A and one one CD4001A
  N > 10 with multiple CD4017A's
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design & Applications"

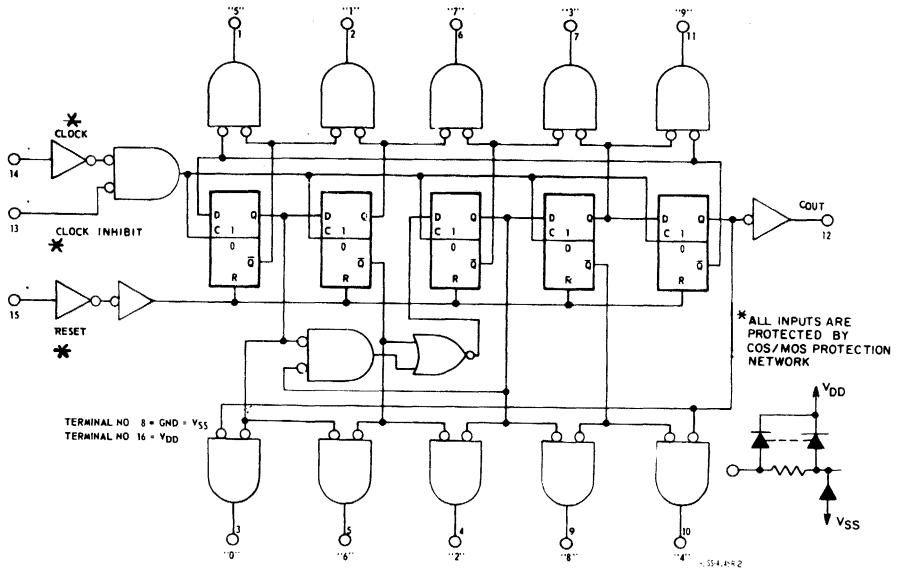


Fig. 1– Logic diagram.

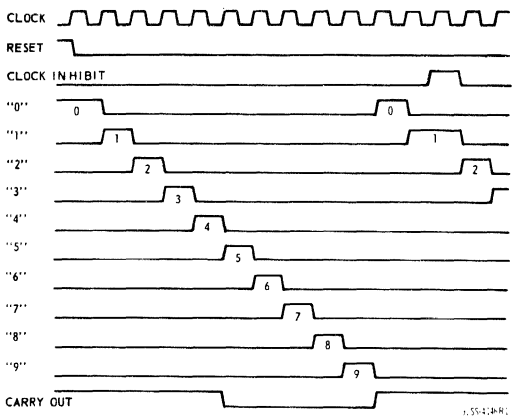


Fig. 2 – Timing diagram.

CD4017A Types

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

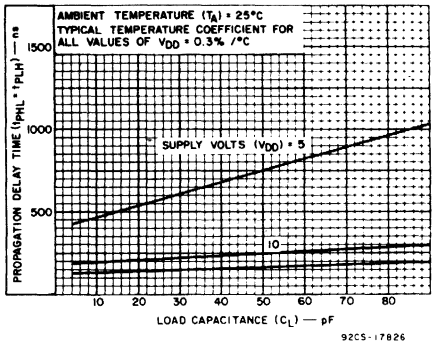


Fig. 3 – Typical propagation delay time vs. C_L for decoded outputs.

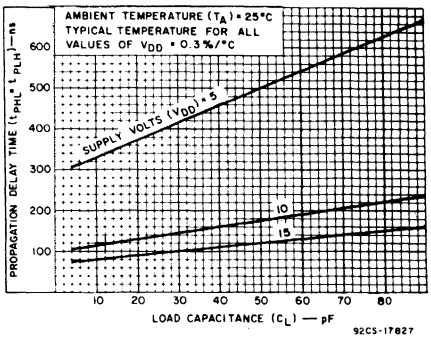


Fig. 4 – Typical propagation delay time vs. C_L for carry output.

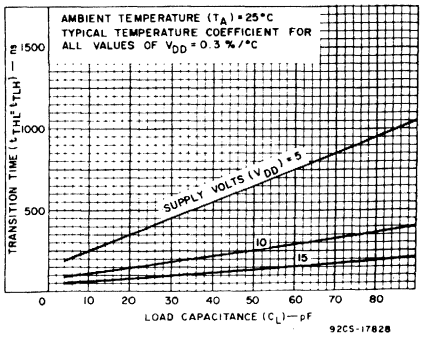


Fig. 5 – Typical transition time vs. C_L for decoded outputs.

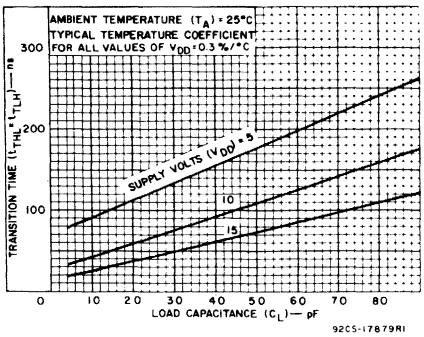


Fig. 6 – Typical transition time vs. C_L for carry output.

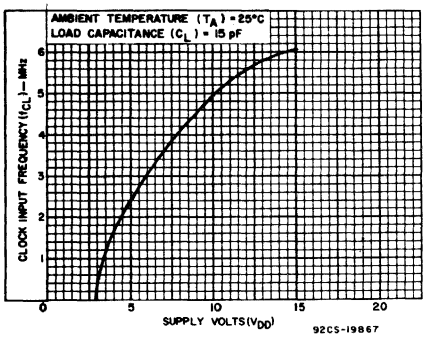


Fig. 7 – Typical clock input frequency vs. V_{DD}.

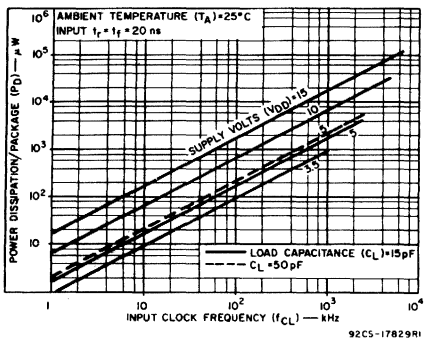
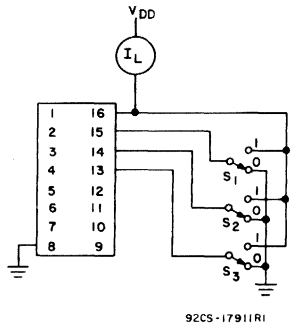


Fig. 8 – Typical dissipation characteristics.



Test performed with the following sequence of "1's and "O's" at each switch.

S_1	S_2	S_3	S_1	S_2	S_3
1	1	1	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
			0	1	0

Fig. 9 – Quiescent device current test circuit.

CD4017A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink)												mA
I_{DN} Min Decoded Outputs	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	0.5	–	10	0.12	0.4	0.1	0.07	0.085	0.4	0.07	0.055	
I_{DN} Min Carry Output	0.5	–	5	0.185	0.4	0.15	0.105	0.095	0.4	0.08	0.065	
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
P-Channel (Source)												
I_{DP} Min Decoded Outputs	4.5	–	5	-0.0375	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
	9.5	–	10	-0.12	-0.2	-0.1	-0.07	-0.085	-0.2	-0.07	-0.055	
I_{DP} Min Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
	9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.20	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

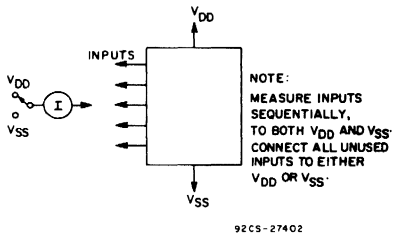


Fig. 10 – Input-leakage-current test circuit.

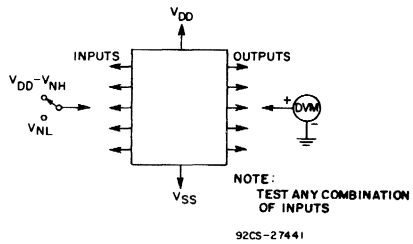


Fig. 11 – Noise-immunity test circuit.

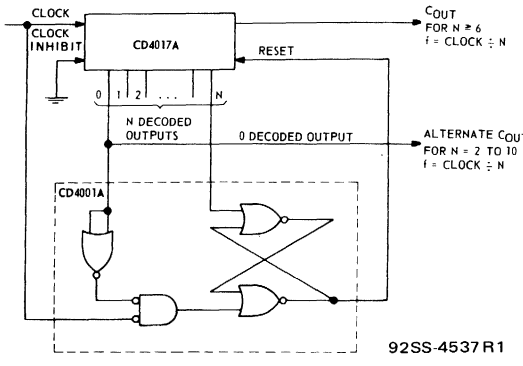


Fig. 12 – Divide by N counter ($N \leq 10$) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017A. If the N^{th} decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

CD4017A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLOCKED OPERATION								
Propagation Delay Time; t_{PHL} t_{PLH} Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
Decode Out Lines	5	–	500	1200	–	500	1600	
	10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} Carry Out Line	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
Decode Out Lines	5	–	300	900	–	300	1200	
	10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}*	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2	5	–	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Clock Inhibit Data Set-Up Time, t_s	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time; t_{PHL} To Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Decode Out Lines	5	–	450	1200	–	450	1600	
	10	–	200	400	–	200	500	
Minimum Reset Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	165	–	100	250	
Minimum Reset Removal Time	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	275	

*Measured with respect to carry output line

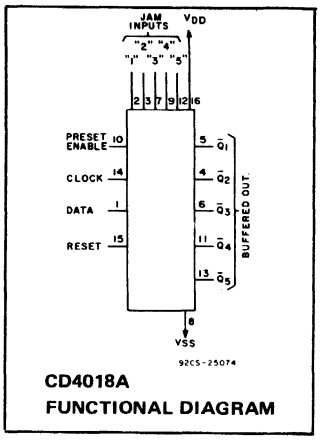
CD4018A Types

COS/MOS Presettable Divide-By-'N' Counter

The RCA-CD4018A types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the DATA input.

Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

The CD4018A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4018A
FUNCTIONAL DIAGRAM

Features:

- **Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters**
- **Fixed and programmable counters greater than 10**
- **Programmable decade counters**
- **Divide-by-"N" counters/frequency synthesizers**
- **Frequency division**
- **Counter control/timers**

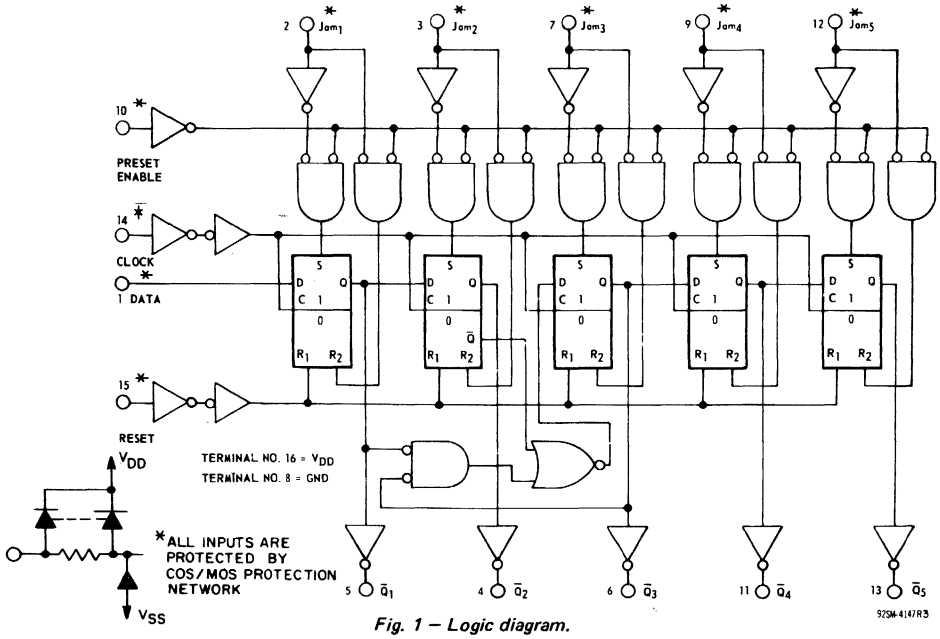


Fig. 1 – Logic diagram.

("DATA" INPUT TIED TO $\overline{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

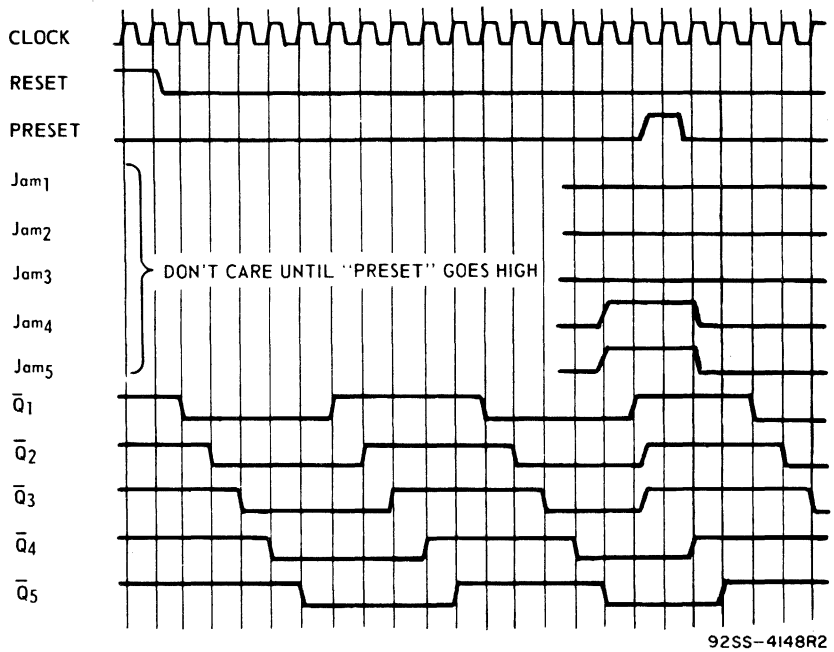


Fig. 2 – Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10	$\overline{Q}_5$	CONNECTED BACK TO "DATA"	NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 8	$\overline{Q}_4$		
DIVIDE BY 6	$\overline{Q}_3$		
DIVIDE BY 4	$\overline{Q}_2$		
DIVIDE BY 2	$\overline{Q}_1$		

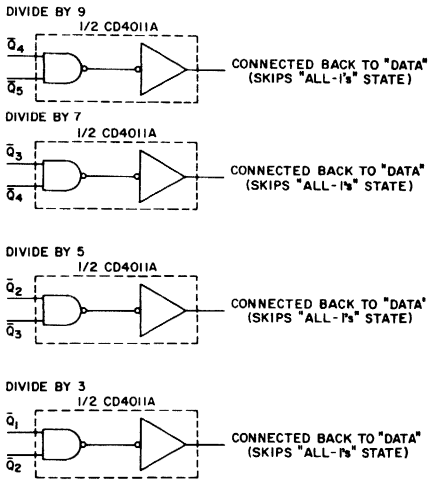


Fig. 3 – External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4018A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPES E, Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E,Y Packages*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time; t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Other Outputs		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} To $\overline{Q}_5$ Output		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
To Other Outputs		5	–	300	900	–	300	1200	ns
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Min. Data Input Set-Up Time, t_S		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
PRESET* OR RESET OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Other Outputs		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Min. Preset or Reset Pulse Width t_W		5	–	200	500	–	200	830	ns
		10	–	100	165	–	100	250	
Min. Preset or Reset Removal Time		5	–	300	750	–	300	1000	
		10	–	100	225	–	100	275	

* At PRESET ENABLE OR JAM Inputs.

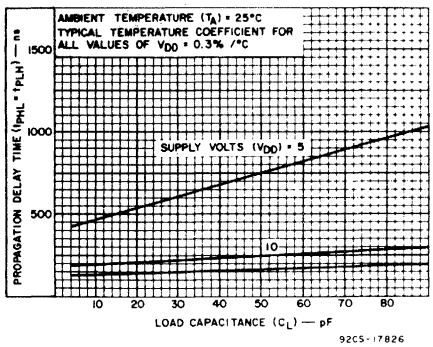


Fig. 4 – Typical propagation delay time vs. load capacitance for decoded outputs.

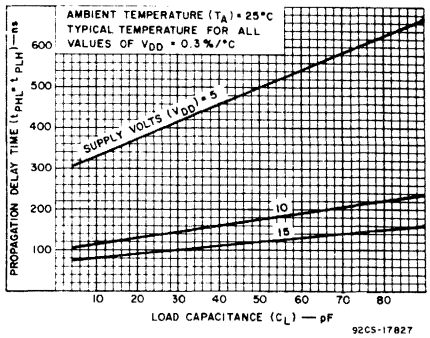


Fig. 5 – Typical propagation delay time vs. load capacitance for $\overline{Q}_5$ output.

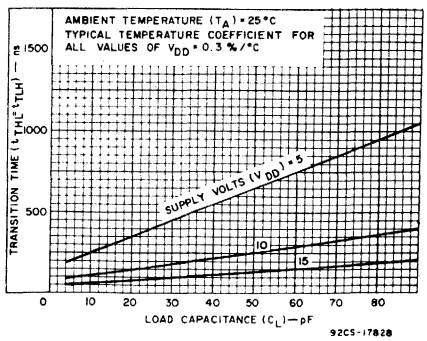


Fig. 6 – Typical transition time vs. load capacitance for decoded outputs.

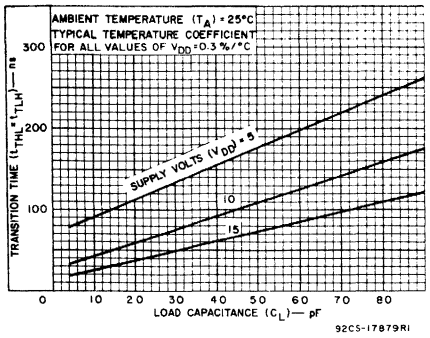


Fig. 7 – Typical transition time vs. load capacitance for $\overline{Q}_5$ output.

CD4018A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Preset or Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Preset or Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

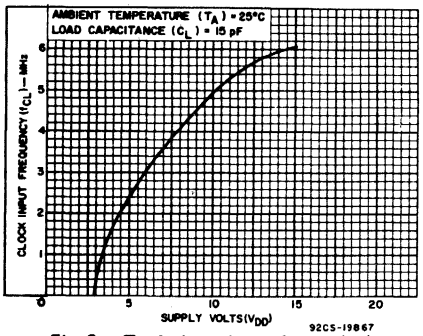


Fig. 8 – Typical maximum input clock frequency vs. supply voltage.

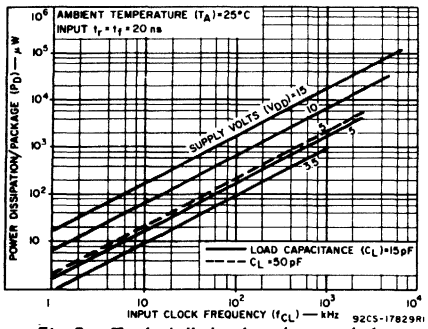


Fig. 9 – Typical dissipation characteristics

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H packages				*E,Y Packages*				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	$\bar{Q}_5$	0.5	–	5	0.18	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
		0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
	$\bar{Q}_1,\bar{Q}_2$	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	$\bar{Q}_3,\bar{Q}_4$	0.5	–	10	0.25	0.4	0.2	0.14	0.18	0.4	0.15	0.12	
p-Channel (Source) I_DP Min.	$\bar{Q}_5$	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.25	-0.2	
	$\bar{Q}_1,\bar{Q}_2$	4.5	–	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
	$\bar{Q}_3,\bar{Q}_4$	9.5	–	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input											μA
		–	–	15	±10^{-5} Typ., ±1 Max.								

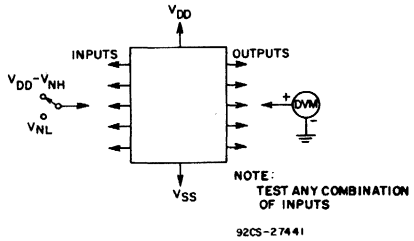
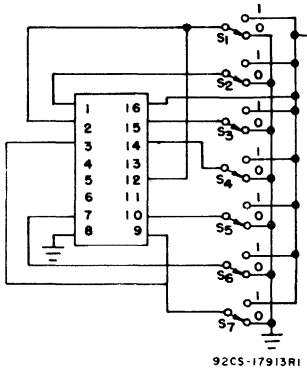


Fig. 10 – Noise-immunity test circuit



Test performed with the following sequence of "1's" and "O's" at each switch.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 11 – Quiescent-device-current test circuit.

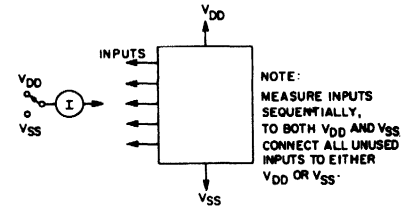


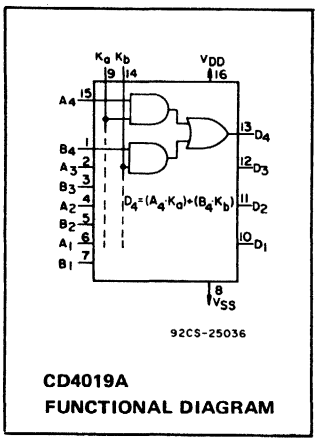
Fig. 12 – Input-leakage-current test circuit.

CD4019A Types

COS/MOS Quad AND/OR Select Gate

The RCA-CD4019A types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4019A
FUNCTIONAL DIAGRAM

Features:

- Medium-speed operation . . . . . . $t_{PHL} = t_{PLH}$ = 50 ns (typ.) at C_L = 15 pF, V_{DD} = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H. . . . . –55 to +125°C
PACKAGE TYPES E,Y. . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	

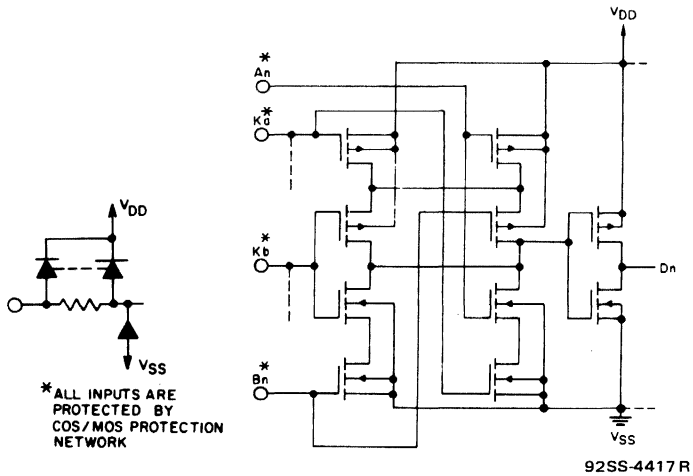


Fig. 1 – Schematic diagram for 1 of 4 identical stages.

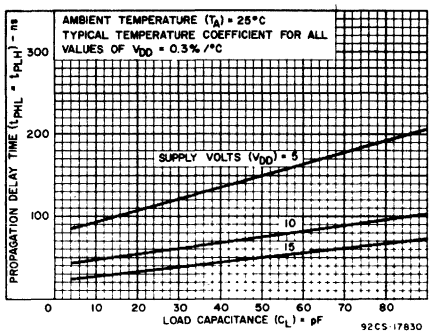


Fig. 2 – Typical propagation delay time vs. load capacitance.

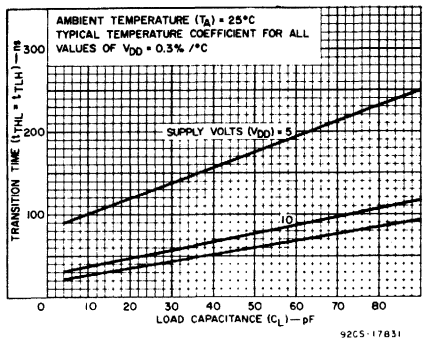


Fig. 3 – Typical transition time vs. load capacitance.

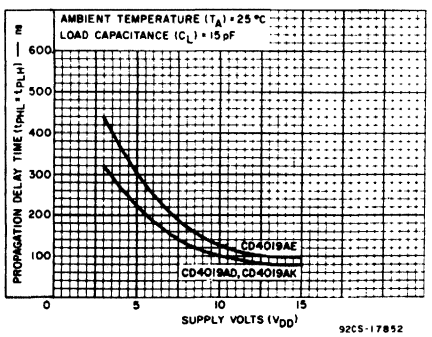


Fig. 4 – Maximum propagation delay time vs. supply voltage.

CD4019A Types

STATIC ELECTRICAL CHARACTERISTCS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.5	–	5	0.6	0.9	0.45	0.3	0.37	1	0.3	0.23	mA
	0.5	–	10	0.9	1.5	0.75	0.55	0.8	1.5	0.65	0.5	
p-Channel (Source): I_DP Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	–	10	-0.95	-1.5	-0.7	-0.5	-0.6	-1.5	-0.5	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

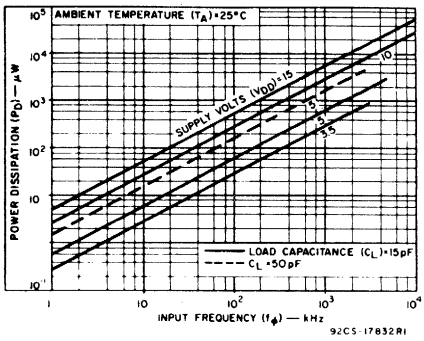


Fig. 5 — Typical dissipation characteristics. (per output).

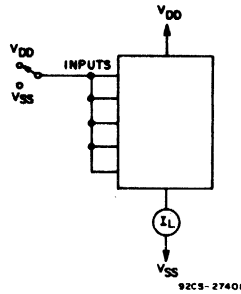


Fig. 6 — Quiescent-device-current test circuit.

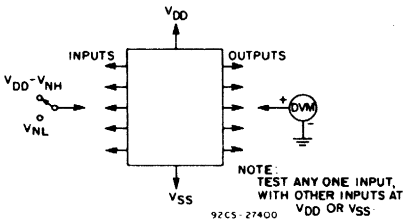


Fig. 7 — Noise-immunity test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	100	225	–	100	300	ns
		10	–	50	100	–	50	125	
Transition Time; t_{THL}, t_{TLH}		5	–	100	200	–	100	275	ns
		10	–	40	65	–	40	80	
Average Input Capacitance, C_I	All A and B Inputs		–	5	–	–	5	–	pF
	K_a and K_b Inputs		–	12	–	–	12	–	pF

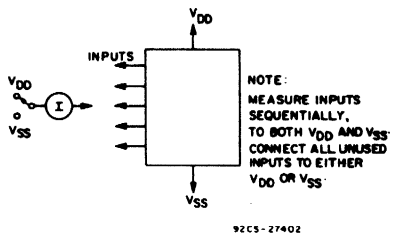


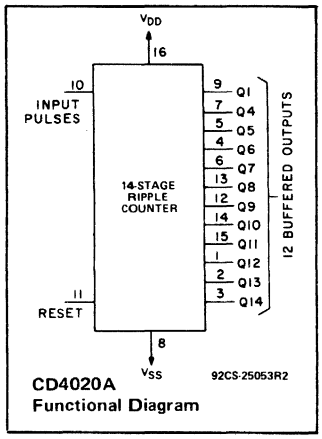
Fig. 8 — Input-leakage-current test circuit.

CD4020A Types

COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4020 consists of a PULSE INPUT shaping circuit, RESET line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1 and 4 through 14. The counter is reset to its all-zeroes state by a high level on the RESET inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each INPUT PULSE.

The CD4020A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4020A
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Min.	LIMITS D,F,K,H Packages Max.	LIMITS E,Y Packages Min.	LIMITS E,Y Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Pulse Width, t_W	5	335	–	500	–	ns
	10	125	–	165	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	4	dc	3	
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	–	15	μs
	10	–	15	–	15	
Reset Pulse Width, t_W	5	2500	–	3000	–	ns
	10	475	–	550	–	

Features:

- Medium speed operation . . . 7 MHz (typ.) at $V_{DD}-V_{SS}$ = 10 V
- Low output impedance
- Common reset
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

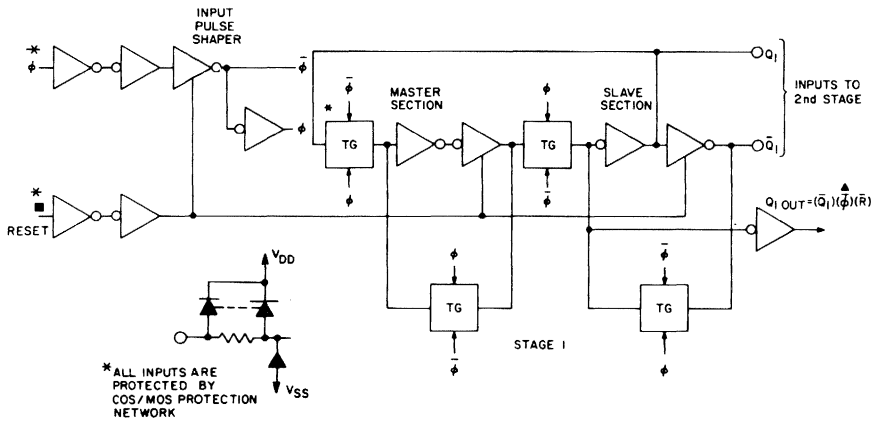


Fig. 1—Logic diagram for 1 of 14 binary stages.

CD4020A Types

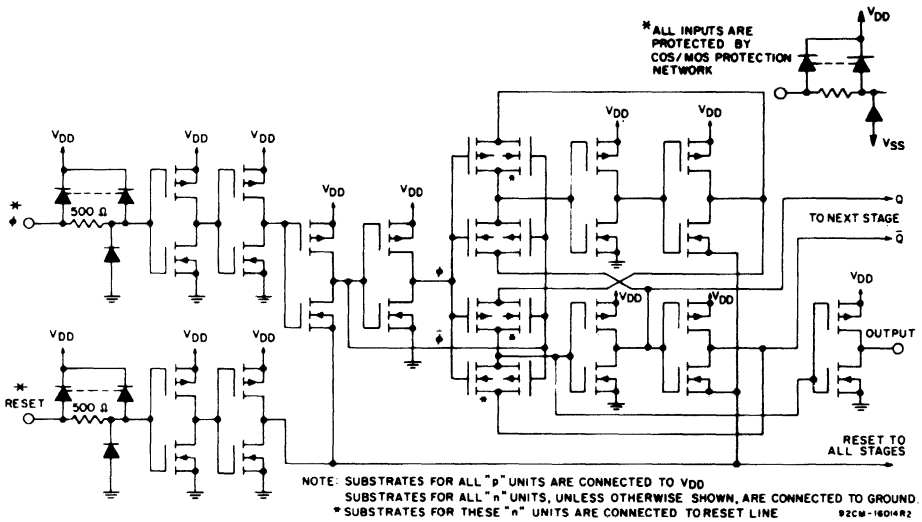


Fig. 2—Schematic diagram of pulse shapers and 1 of 14 binary stages.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.09	0.2	0.075	0.05	0.09	0.33	0.08	0.065	mA
	0.5	–	10	0.185	0.4	0.15	0.105	0.16	0.5	0.10	0.10	
P-Channel (Source) I_DP Min.	4.5	–	5	−0.11	−0.25	−0.09	−0.065	−0.09	−0.25	−0.06	−0.05	
	9.5	–	10	−0.25	−0.5	−0.20	−0.14	−0.18	−0.5	−0.15	−0.12	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

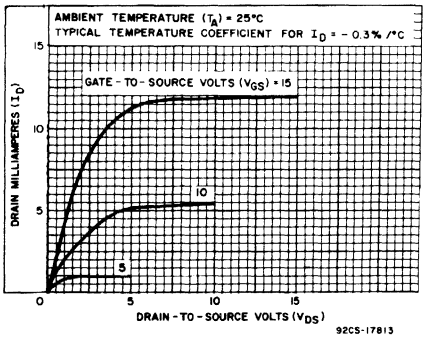


Fig. 3—Typical output n-channel drain characteristics.

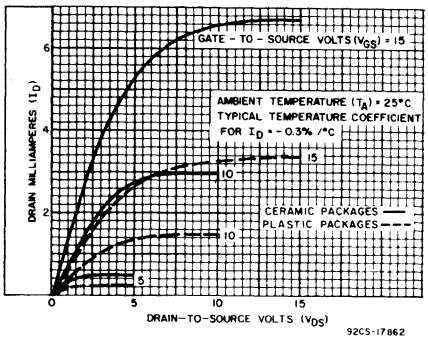


Fig. 4—Minimum output n-channel drain characteristics.

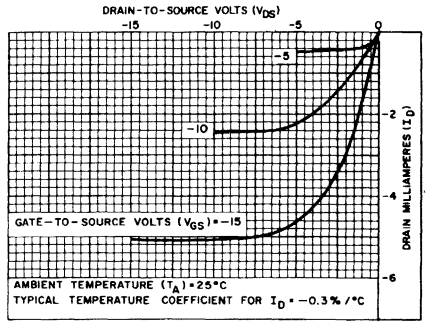


Fig. 5—Typical output p-channel drain characteristics.

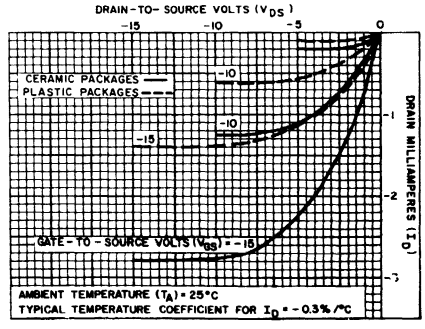


Fig. 6—Minimum output p-channel drain characteristics.

CD4020A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Clocked Operation									
Propagation Delay Time,* t_{PLH}, t_{PHL}		5	–	450	600	–	450	650	ns
		10	–	150	225	–	150	250	
Transition Time, t_{THL}, t_{TLH}		5	–	450	600	–	450	650	ns
		10	–	200	300	–	200	350	
Maximum Clock Input Frequency, f_{CL}		5	1.5	2.5	–	1	2.5	–	MHz
		10	4	7	–	3	7	–	
Minimum Clock Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	70	125	–	70	165	
Clock Rise & Fall Time, t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input		–	–	5	–	–	5	pF
Reset Operation									
Propagation Delay Time,* t_{PHL}		5	–	2000	3000	–	2000	3500	ns
		10	–	500	775	–	500	300	
Minimum Reset Pulse Width, t_W		5	–	1800	2500	–	1800	3000	ns
		10	–	300	475	–	300	550	

* Propagation delay is from clock input to Q_1 output.

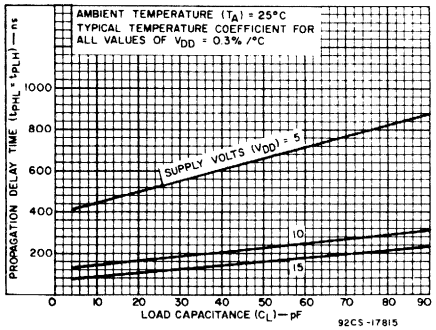


Fig. 7—Typical propagation delay time vs. C_L.

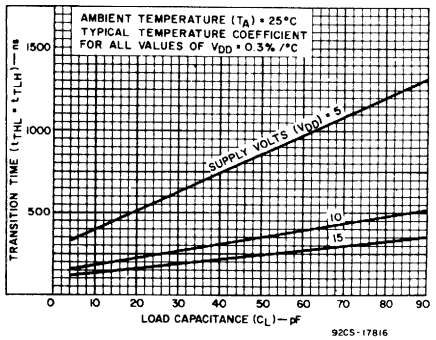


Fig. 8—Typical transition time vs. C_L.

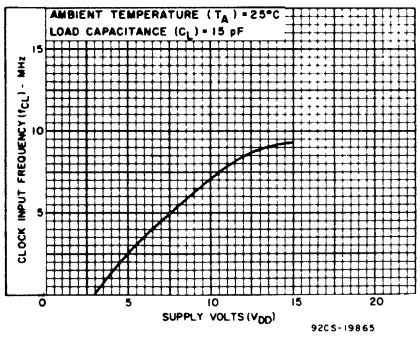


Fig. 9—Typical clock input frequency vs. V_{DD}.

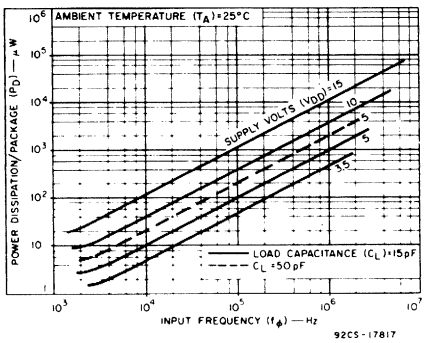


Fig. 10—Typical dissipation characteristics.

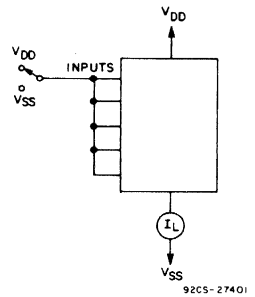


Fig. 11—Quiescent-device-current test circuit.

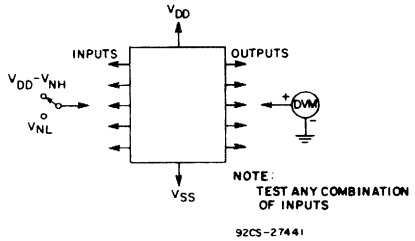


Fig. 12—Noise-immunity test circuit.

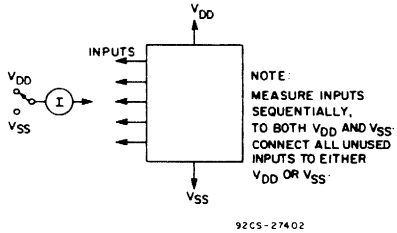


Fig. 13—Input-leakage-current test circuit.

CD4021A Types

COS/MOS 8-Stage Static Shift Register

Asynchronous Parallel Input/Serial Output,
Synchronous Serial Input/Serial Output

The RCA-CD4021A types are 8-stage parallel or serial-input/serial-output shift registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL DATA input, and individual parallel Jam inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. Q outputs are available from the sixth, seventh, and eighth stages.

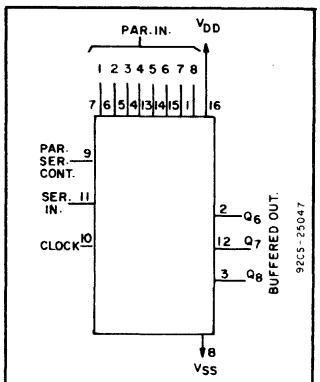
When the PARALLEL/SERIAL CONTROL input is low, data are serially shifted into the 8-stage register synchronously with the positive-going transition of the CLOCK pulse.

Features:

- **Asynchronous parallel or synchronous serial operation under control of parallel/serial control-input**
- **Individual JAM inputs to each register stage**
- **Master-slave flip-flop register stages**
- **Fully static operation. . . . . DC to 5 MHz**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

When the PARALLEL/SERIAL CONTROL input is high, data are jammed into the 8-stage register via the parallel input lines asynchronously with the clock line.

Register expansion is possible using additional CD4021A packages.



CD4021A
FUNCTIONAL DIAGRAM

The CD4021A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Parallel to serial data conversion**
- **Asynchronous parallel input/serial output data queueing**
- **General purpose register**

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.5	5	300	50	0.5	50	700	μA
	–	–	10	10	1	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity; Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.15	0.3	0.12	0.085	0.072	0.3	0.06	0.05	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.12	0.5	0.1	0.08	
P-Channel (Source) I_DP Min.	4.5	–	5	-0.1	-0.16	-0.08	-0.055	-0.06	-0.16	-0.05	-0.04	
	9.5	–	10	-0.25	-0.44	-0.20	-0.14	-0.12	-0.44	-0.1	-0.08	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.								

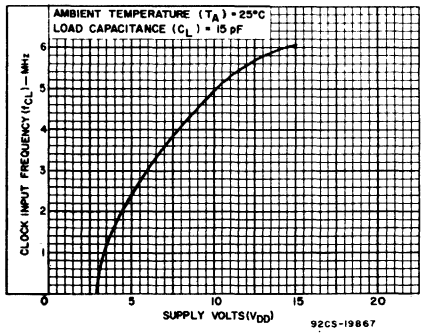


Fig. 1 — Typical clock input frequency vs. supply voltage.

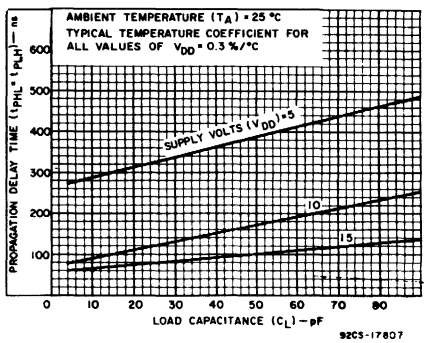


Fig. 2 — Typical propagation delay time vs. load capacitance.

CD4021A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A)\

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPES E, Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = –40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

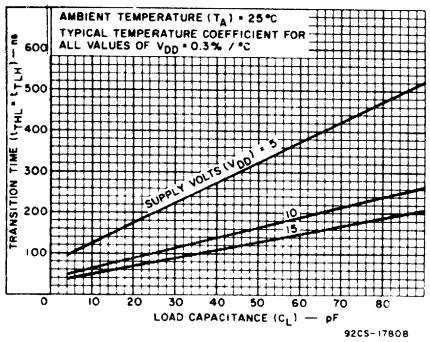


Fig. 3 – Typical transition time vs. load capacitance.

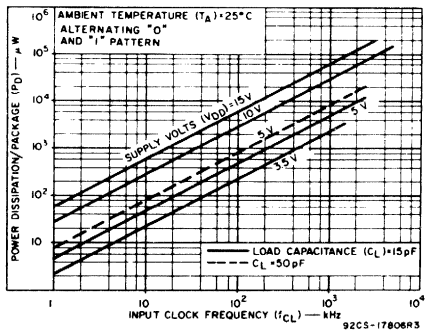


Fig. 4 – Typical dissipation characteristics.

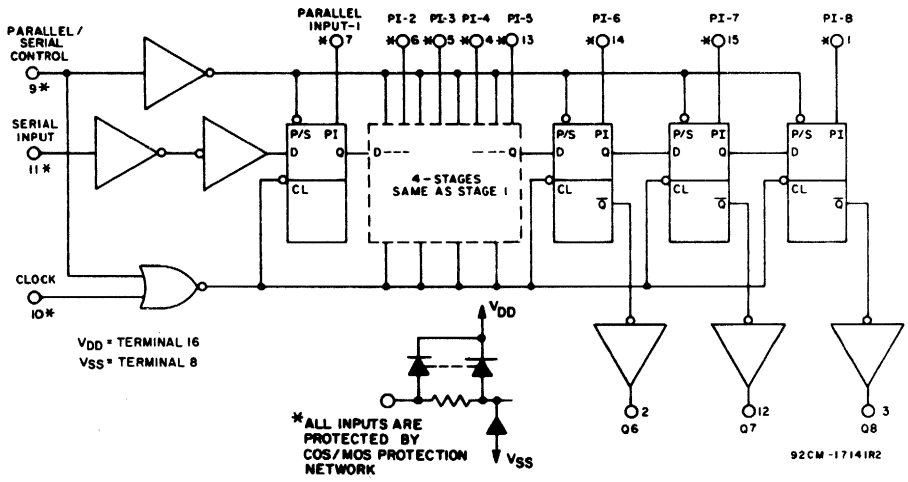


Fig. 5 – Logic diagram.

TRUTH TABLE

CL▲	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
⎍	0	0	X	X	0	Q_{n-1}
⎍	1	0	X	X	1	Q_{n-1}
⎎	X	0	X	X	Q_1	Q_n*

▲ = LEVEL CHANGE X = DON'T CARE CASE

* NO CHANGE

92CS-17141R3

Fig. 6 – Truth table.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	350 80	– –	500 100	– –	ns
Clock Pulse Width, t_W	5 10	500 175	– –	830 200	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2.5	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5 10	– –	15 15	– –	15 15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

CD4021A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time,** t_{PLH}, t_{PHL}	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	300	300	
Transition Time; t_{THL}, t_{TLH}	5	–	150	300	–	150	400	ns
	10	–	75	125	–	75	150	
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	–	0.6	2.5	–	MHz
	10	3	5	–	2.5	5	–	
Minimum Clock Pulse Width, t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Clock Rise & Fall Time; t_rCL & t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Data Set Up Time, t_S	5	–	100	350	–	100	500	ns
	10	–	50	80	–	50	100	
Minimum High-Level Parallel/Serial Control Pulse Width t_W	5	–	200	500	–	200	830	ns
	10	–	100	175	–	100	200	
Input Capacitance C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

**From Clock or Parallel/Serial Control Input

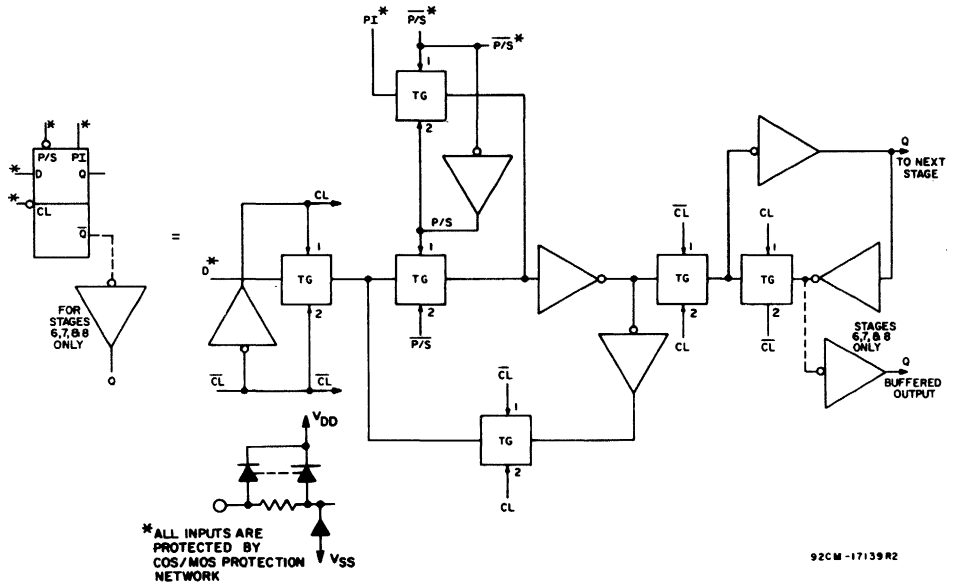


Fig. 10 – One typical stage and its equivalent detailed circuit.

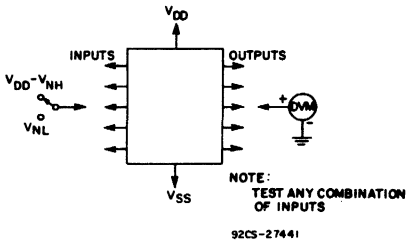


Fig. 7 – Noise-immunity test circuit.

Test performed with the following sequence of "One's" and "Zero's".

S_1	S_2	S_3	S_4	S_5
0	0	1	0	0
1	0	1	1	1
1	0	1	0	1
0	1	1	1	1
0	1	0	0	0

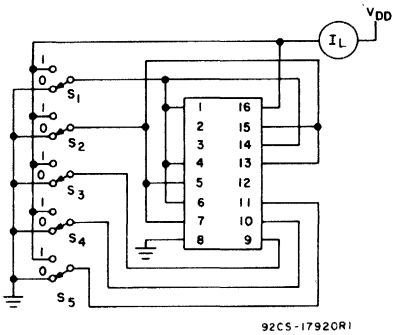


Fig. 8 – Quiescent device current test circuit.

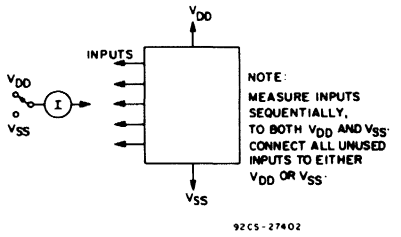


Fig. 9 – Input-leakage-current test circuit.

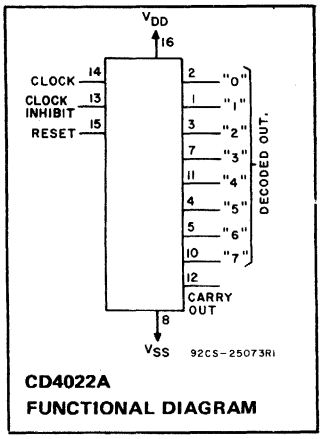
CD4022A Types

COS/MOS Divide-By-8 Counter/Divider With 8 Decoded Outputs

The RCA-CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associate decode output gating and a CARRY-OUT BIT. The counter is cleared to its zero count by a high RESET signal. The counter is advanced on the positive CLOCK-signal transition provided the CLOCK INHIBIT signal is low.

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally low and go high only at their respective decoded time slot. Each decode gate output remains high for one full clock cycle. The CARRY-OUT signal completes one cycle every 8 CLOCK-INPUT cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system.

The CD4022A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4022A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
  PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
  FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y). . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	175 75	– –	175 75	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width	5 10	300 150	– –	600 300	–	ns
Reset Removal Time	5 10	752 225	– –	1000 275	– –	ns

Features:

- Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V
- Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A package
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Binary counting/decoding
- Binary frequency division
- Binary counter control/timers

CD4022A Types

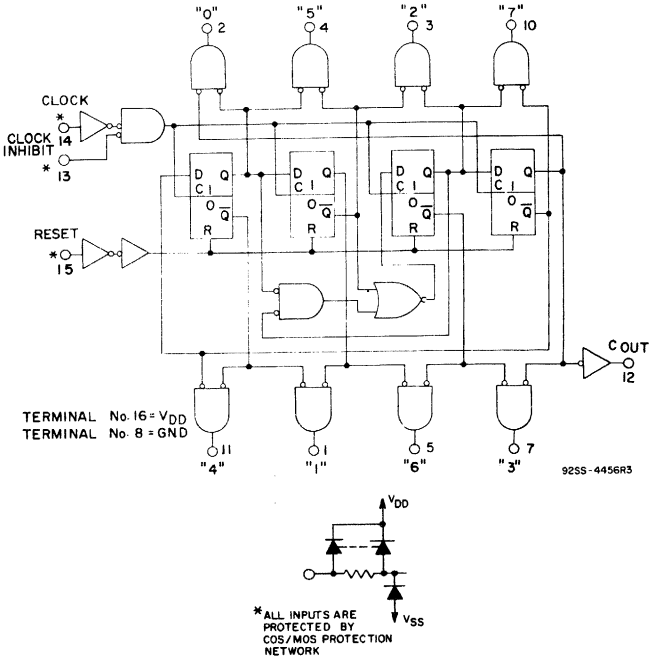


Fig. 1 – Logic diagram.

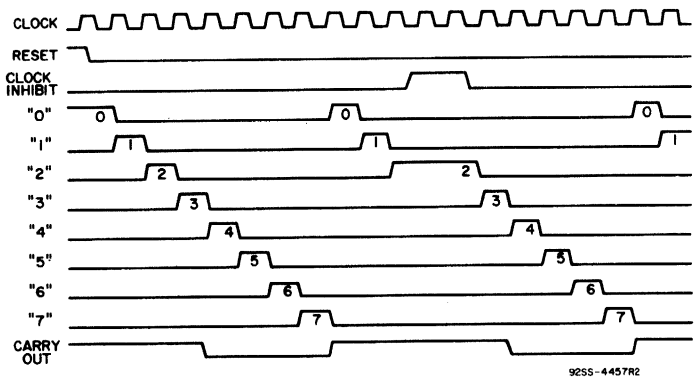


Fig. 2 – Timing diagram.

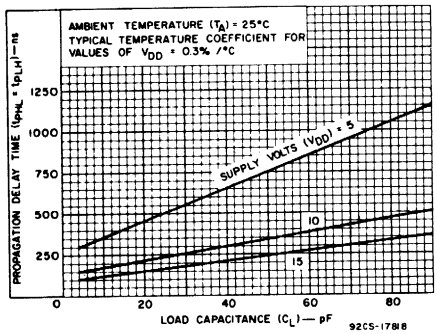


Fig. 3 – Typical propagation delay time vs. load capacitance for decoded outputs.

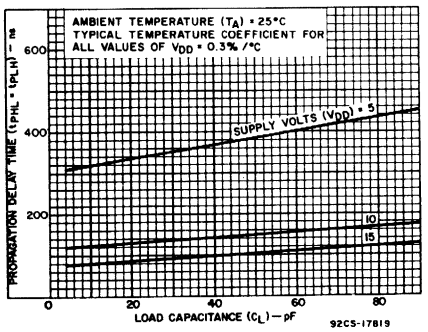


Fig. 4 – Typical propagation delay time vs. load capacitance for carry output.

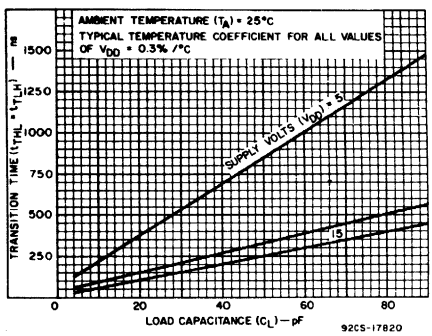


Fig. 5 – Typical transition time vs. load capacitance for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H Packages				E,Y Packages				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) IDN Min.	Decoded Outputs	0.5	–	5	0.062	0.15	0.05	0.035	0.03	0.15	0.025	0.02	mA
		0.5	–	10	0.12	0.3	0.1	0.07	0.06	0.3	0.05	0.04	
	Carry Output	0.5	–	5	0.185	0.5	0.15	0.105	0.095	0.5	0.08	0.065	
		0.5	–	10	0.375	1	0.3	0.21	0.155	1	0.13	0.105	
p-Channel (Source): I_D^P Min.	Decoded Outputs	4.5	–	5	-0.038	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
		9.5	–	10	-0.12	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.375	-0.8	-0.3	-0.21	-0.155	-0.8	-0.13	-0.105	
Input Leakage Current, I_{IL}, I_{IH}		Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4022A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r , t_f = 20 ns,
C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages.			*E,Y Packages*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time: t_{PHL} , t_{PLH} Carry-Out Line		5	–	325	1000	–	325	300	ns
		10	–	125	250	–	125	500	
Decode Out Lines		5	–	400	1200	–	400	1600	ns
		10	–	200	400	–	200	800	
Transition Time: t_{THL} , t_{TLH} Carry-Out Line		5	–	85	300	–	85	340	ns
		10	–	50	100	–	50	200	
Decode-Out Lines		5	–	300	900	–	300	1200	ns
		10	–	125	250	–	125	500	
Min. Clock Pulse Width, t_W		5	–	250	500	–	250	830	ns
		10	–	85	170	–	85	250	
Clock Rise and Fall Time, t_{rCL} , t_{fCL}		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Min. Clock Inhibit Set-Up Time, t_S		5		175	350		175	700	ns
		10		75	150		75	300	
Max. Clock Input Frequency, f_{CL}*		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PHL} , t_{PLH} Carry-Out Line		5	–	300	900	–	300	1200	ns
		10	–	125	250	–	125	500	
Decode-Out Line		5	–	500	1250	–	500	2500	ns
		10	–	200	400	–	200	800	
Min. Reset Pulse Width, t_W		5	–	150	300	–	150	600	ns
		10	–	75	150	–	75	300	
Min. Reset Removal Time		5	–	300	752	–	300	1000	ns
		10	–	100	225	–	100	275	

* Measured with respect to carry output line

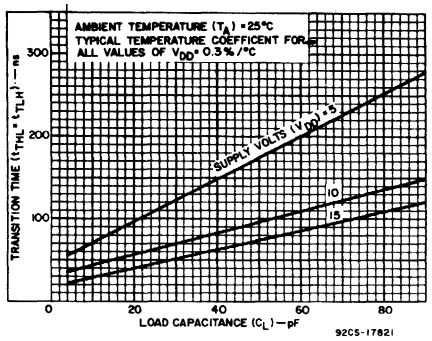


Fig. 6 – Typical transition time vs. load capacitance for carry output.

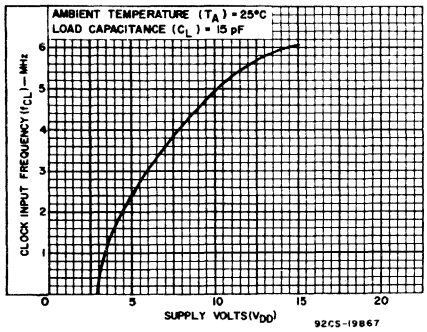


Fig. 7 – Typical clock input frequency vs. supply voltage.

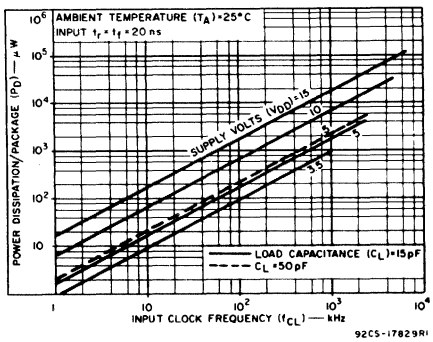


Fig. 8 – Typical dissipation characteristics.

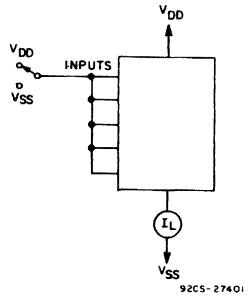


Fig. 9 – Quiescent-device-current test circuit.

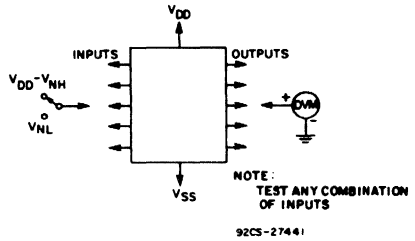


Fig. 10 – Noise-immunity test circuit.

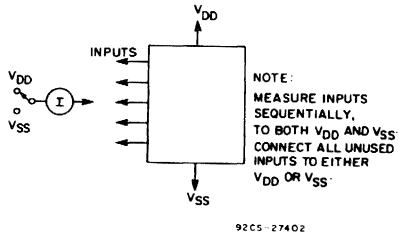


Fig. 11 – Input-leakage-current test circuit.

CD4024A Types

COS/MOS 7-Stage Binary Counter

With Buffered Reset

The RCA-CD4024A consists of an INPUT PULSE shaping circuit, RESET line driver circuitry, and seven binary counter stages. The counter is reset to "zero" by a high level on the RESET input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each INPUT PULSE.

The CD4024A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), 12-lead hermetic TO-5 packages (T suffix), and in chip form (H suffix).

Applications:

- **Frequency-dividing circuits**
- **Time-delay circuits**
- **Counter control**
- **D/A counter and switch on one chip**

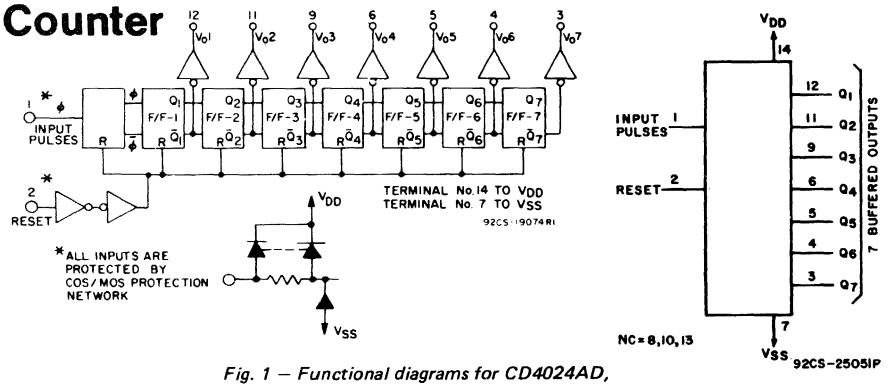


Fig. 1 – Functional diagrams for CD4024AD, AE, AF, AK, AY.

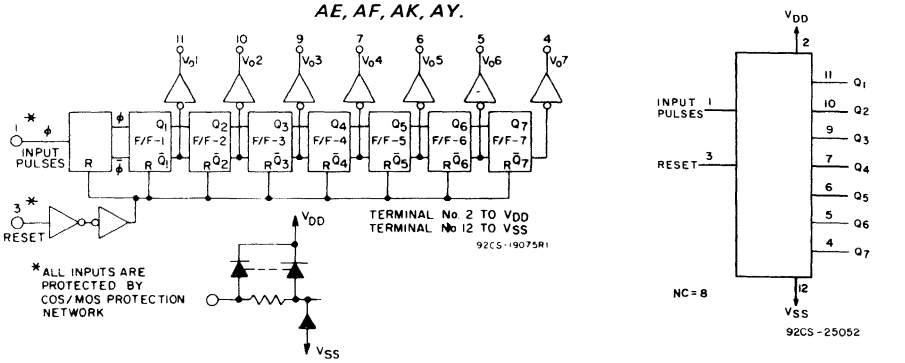


Fig. 2 – Functional diagrams for CD4024AT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H, T . . . . . –55 to +125°C

PACKAGE TYPES E, Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y). . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K, T) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K, T) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H,T Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Pulse Width, t_W	5	330	–	500	–	ns
	10	125	–	165	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	4	dc	3	
Clock Rise or Fall Time, t_rCL, t_fCL	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	500	–	600	–	ns
	10	300	–	350	–	

Features:

- **Medium-speed operation . . . . . 7-MHz (typ.) input pulse rate at $V_{DD} - V_{SS}$ = 10 V**
- **Low high-and-low level output impedance . . . . . 700Ω and 500Ω (typ.), respectively at $V_{DD} - V_{SS}$ = 10 V**
- **Fully static operation**
- **Common reset**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

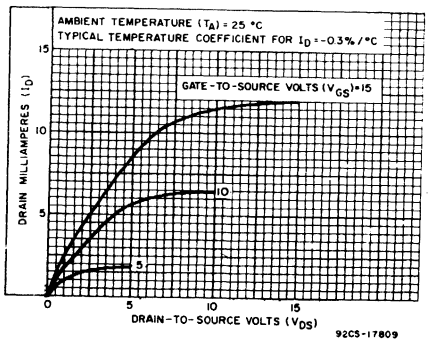
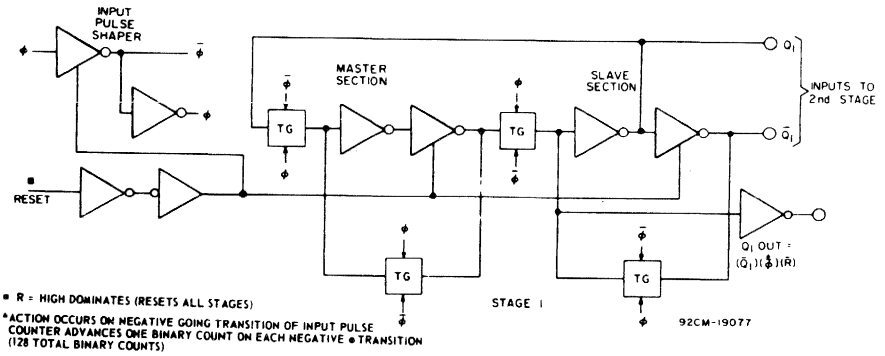


Fig. 3 – Typical output n-channel drain characteristics.

CD4024A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H,T Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	—	—	5	5	0.3	5	300	50	0.5	50	700	μA
	—	—	10	10	0.5	10	600	100	1	100	1400	
	—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High, V_{NMH}	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	—	5	0.31	0.5	0.25	0.175	0.15	0.5	0.12	0.095	mA
	0.5	—	10	0.62	1	0.5	0.35	0.31	1	0.25	0.2	
p-Channel (Source) I_DP Min.	4.5	—	5	-0.19	-0.3	-0.15	-0.105	-0.145	-0.3	-0.12	-0.095	
	9.5	—	10	-0.45	-0.7	-0.35	-0.25	-0.31	-0.7	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	—	—	15	$\pm 10^{-5}$ Typ.; ±1 Max.								



■ R = HIGH DOMINATES (RESETS ALL STAGES)

*ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE • TRANSITION (128 TOTAL BINARY COUNTS)

EQUATIONS FOR STAGES 2 TO 7

$Q_{2OUT} = (\bar{Q}_2)(Q_1)(\overset{\blacktriangle}{\bullet})(R)$ $\quad Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\overset{\blacktriangle}{\bullet})(\bar{R})$

$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\overset{\blacktriangle}{\bullet})(\bar{R})$ $\quad Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\overset{\blacktriangle}{\bullet})(\bar{R})$

$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\overset{\blacktriangle}{\bullet})(\bar{R})$ $\quad Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\overset{\blacktriangle}{\bullet})(\bar{R})$

Fig. 7 — Logic block diagram (pulse shaper and 1 binary stage).

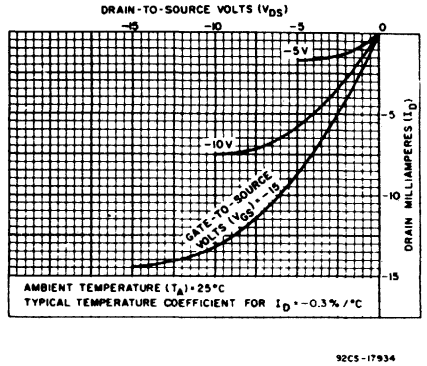


Fig. 4 — Typical output p-channel drain characteristics.

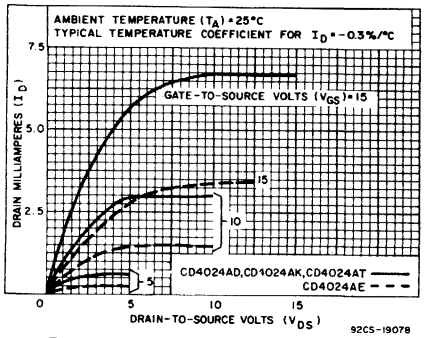


Fig. 5 — Minimum output n-channel drain characteristics.

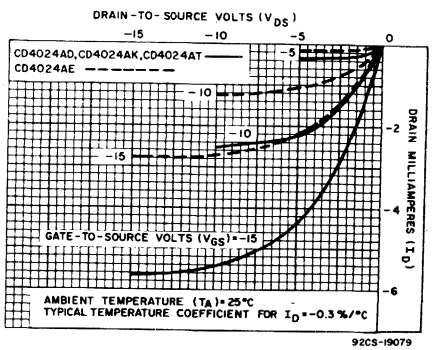


Fig. 6 — Minimum output p-channel drain characteristics.

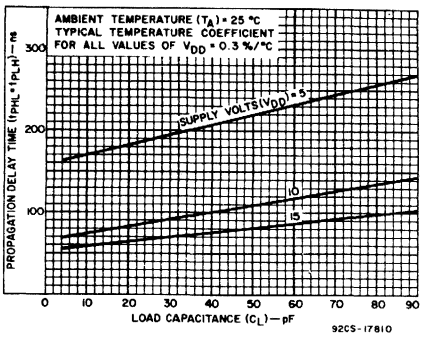


Fig. 8 — Typical propagation delay time vs. C_L.

CD4024A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H,T Packages			*E,Y Packages*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
φ INPUT OPERATION									
Propagation Delay Time;* t_{PLH}, t_{PHL}		5	–	175	350	–	175	400	ns
		10	–	80	125	–	80	150	
Transition Time; t_{THL}, t_{TLH}		5	–	175	225	–	175	250	ns
		10	–	80	125	–	80	150	
Maximum Clock Input Frequency, f_{CL}		5	1.5	2.5	–	1	2.5	–	MHz
		10	4	7	–	3	7	–	
Minimum Clock Pulse Width, t_W		5	–	200	330	–	200	500	ns
		10	–	140	125	–	140	165	
Clock Rise & Fall Time; t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time; T_{PLH}, T_{PHL}		5	–	500	700	–	500	800	ns
		10	–	250	350	–	250	400	
Minimum Reset Pulse Width; t_W		5	–	375	500	–	375	600	ns
		10	–	200	300	–	200	350	

* Propagation delay time is from clock input to Q_1 output.

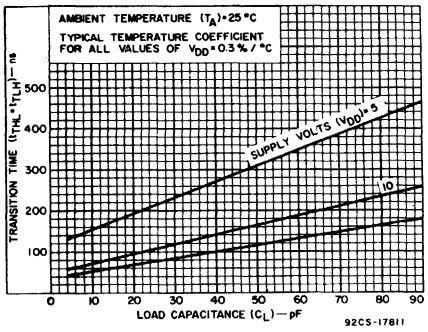


Fig. 9 – Typical transition time vs. C_L.

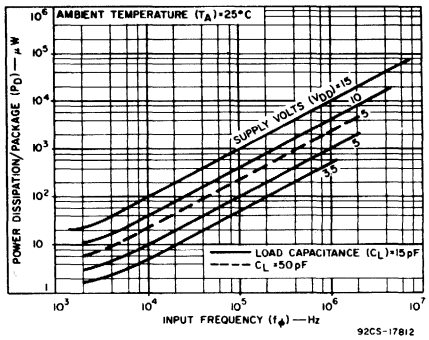


Fig. 10 – Typical dissipation characteristics.

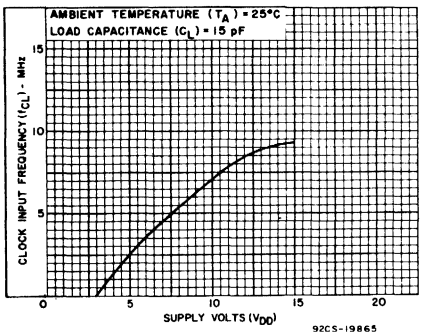


Fig. 11 – Typical input pulse frequency vs. V_{DD}.

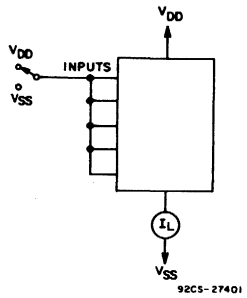


Fig. 12 – Quiescent-device-current test circuit.

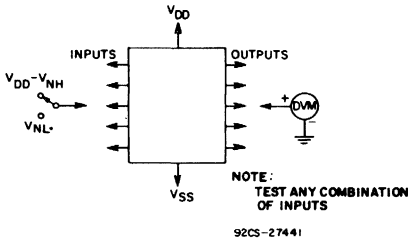
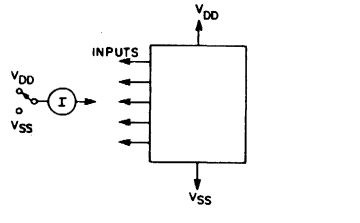


Fig. 13 – Noise-immunity test circuit.

CD4024AD, AK, AE, AF, AY



NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

CD4024AT

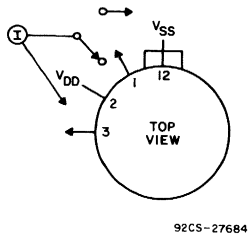


Fig. 14 – Input-leakage-current test circuit.

CD4026A, CD4033A Types

COS/MOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:
Display Enable – CD4026A
Ripple Blanking – CD4033A

The RCA–CD4026A and CD4033A each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033 are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transistion if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033A; in the CD4026A theses outputs go high only when the DISPLAY ENABLE IN is high.

CD4026A

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED"C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a low level voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

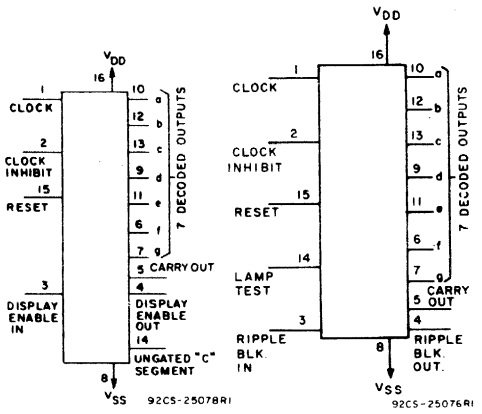
In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage(instead of to the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

The CD4026A- and CD4033A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4026A CD4033A

FUNCTIONAL DIAGRAMS

Features:

- **Counter and 7-segment decoding in one packag**
- **Easily interfaced with 7-segment display types**
- **Fully static counter operation: DC to 2.5 MHz (typ.)**
- **Ideal for low-power displays**
- **Display Enable Output (CD4026A)**
- **"Ripple Blanking" and Lamp Test (CD4033A)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Decade counting/7-segment decimal display**
- **Frequency division/7-segment decimal displays**
- **Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)**
- **Counter/display driver for meter applications**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

CD4026A, CD4033A Types

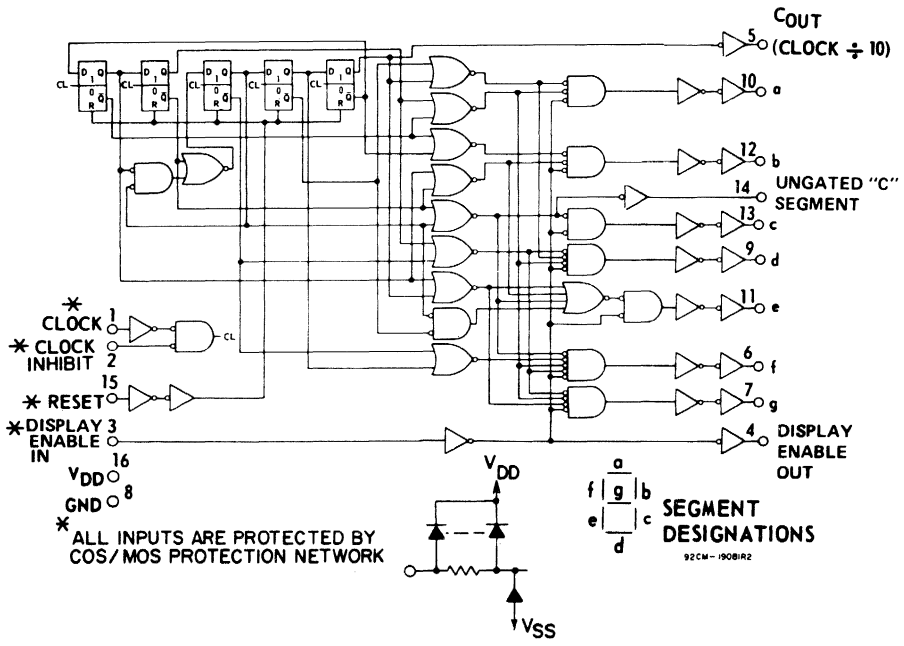


Fig. 1 – CD4026A logic diagram.

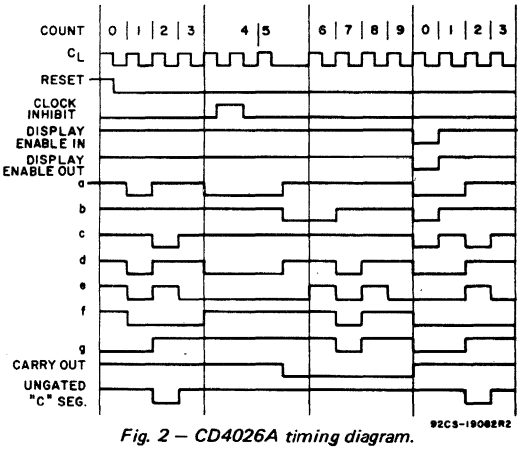


Fig. 2 – CD4026A timing diagram.

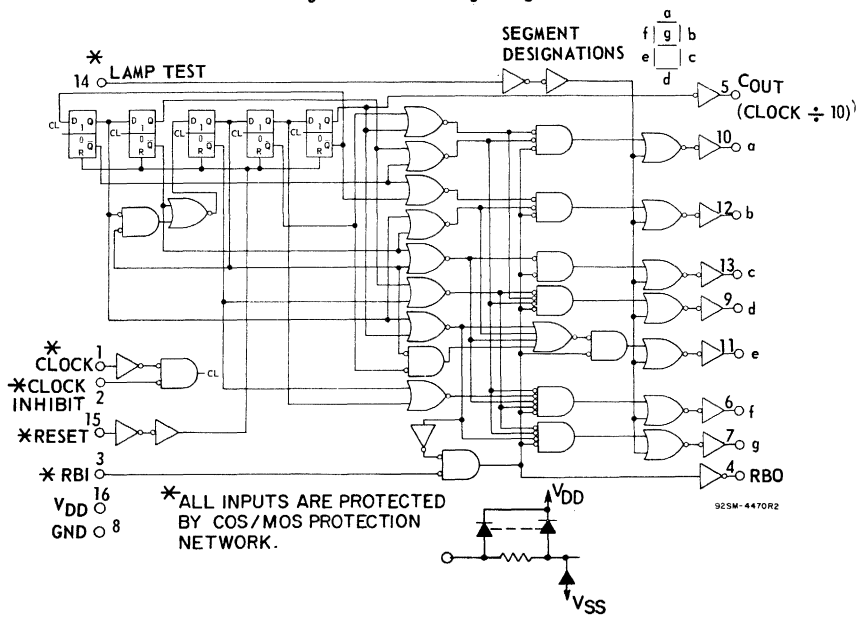


Fig. 3 – CD4033A logic diagram.

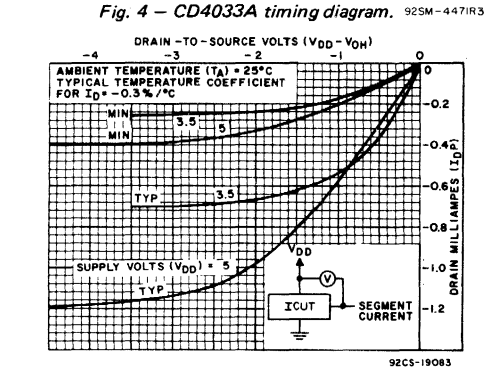


Fig. 4 – CD4033A timing diagram. 92SM-4471R3

Fig. 5 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=3.5 & 5 V.

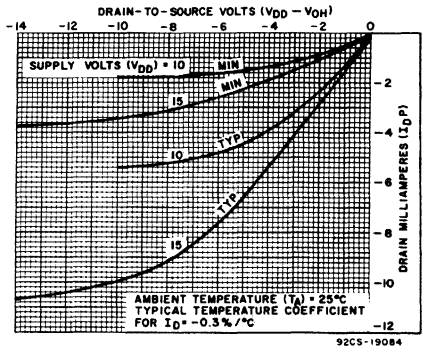


Fig. 6 – Minimum and typical output p-channel decoded drain characteristics @ V_{DD}=10 & 15 V.

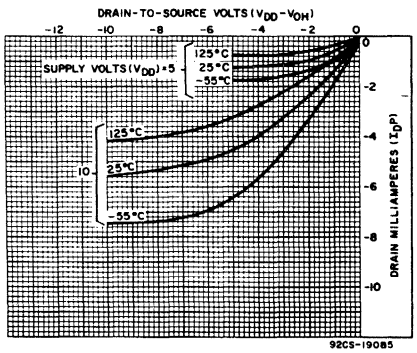


Fig. 7 – Typical output p-channel decoded drain characteristics as a function of temperature.

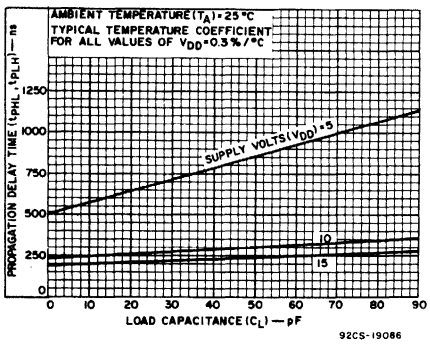


Fig. 8 – Typical propagation delay time vs. C_L for decoded outputs.

CD4026A, CD4033A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	— —	700 300	— —	ns
Clock Pulse Width, t_W	5 10	330 170	— —	500 250	— —	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	— —	15 15	— —	15 15	μs
Reset Pulse Width, t_W	5 10	330 165	— —	550 250	— —	ns
Reset Removal Time	5 10	750 225	— —	1000 275	— —	ns

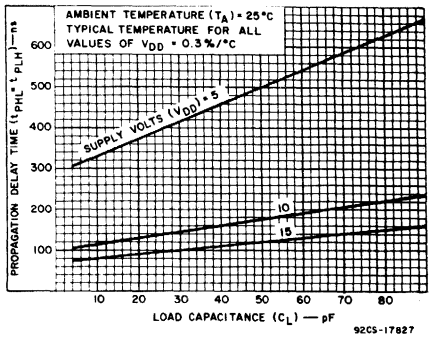


Fig. 9 – Typical propagation delay time vs. C_L for carry outputs.

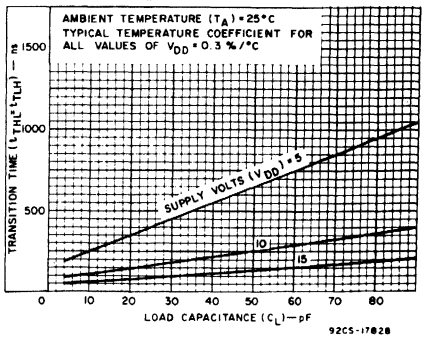


Fig. 10 – Typical transition time vs. C_L for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D,K,F,H Packages				*E,Y Packages*				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		—	—	5	5	0.3	5	300	50	0.5	50	700	μA
		—	—	10	10	0.5	10	600	100	1	100	1400	
		—	—	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}		—	5	5	0 Typ.; 0.05 Max.								V
		—	10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}		—	0	5	4.95 Min.; 5 Typ.								
		—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}			—	5	1.5 Min.; 2.25 Typ.								V
			—	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}			—	5	1.5 Min.; 2.25 Typ.								
				10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	—	5	1 Min.								V
		9	—	10	1 Min.								
Inputs High, V_{NMH}		0.5	—	5	1 Min.								
		1	—	10	1 Min.								
Output Drive Current n-Channel (Sink), I_DN Min.	Decoded Outputs	0.5	—	5	0.15	0.24	0.12	0.09	0.08	0.24	0.06	0.05	mA
		0.5	—	10	0.32	0.5	0.25	0.18	0.15	0.5	0.12	0.1	
	Carry Output	0.5	—	5	0.12	0.4	0.15	0.1	0.095	0.4	0.08	0.06	
		0.5	—	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
p-Channel (Source), I_DP Min.	Decoded Outputs	4.5	—	5	-0.21	-0.28	-0.14	-0.1	-0.09	-0.28	-0.07	-0.06	
		9.5	—	10	-0.45	-0.6	-0.3	-0.22	-0.2	-0.6	-0.15	-0.13	
	Carry Output	4.5	—	5	-0.12	-0.4	-0.15	-0.1	-0.095	-0.4	-0.08	-0.06	
		9.5	—	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.2	
Input Leakage Current, I_{IL}, I_{IH}		Any Input											μA
		—	—	15	$\pm 10^{-5}$ Typ., ±1 Max.								

CD4026A, CD4033A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D,F,K,H Packages			*E,Y Packages*			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION								
Propagation Delay Time; t_{PLH}, t_{PHL} Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
Decode Out Lines	5	–	600	1700	–	600	2200	ns
	10	–	250	500	–	250	700	
Transition Time; t_{THL}, t_{TLH} Carry Out Line	5	–	100	300	–	100	350	ns
	10	–	50	150	–	50	200	
Decode Out Lines	5	–	300	900	–	300	1200	ns
	10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL} ▲	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W	5	–	200	330	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Min. Clock Inhibit Set Up Time, t_S	5	–	175	500	–	175	700	ns
	10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
RESET OPERATION								
Propagation Delay Time: t_{PLH}, t_{PHL} To Carry Out Line	5	–	350	1000	–	350	1300	ns
	10	–	125	250	–	125	300	
To Decode Out Lines	5	–	550	1400	–	550	1900	ns
	10	–	240	500	–	240	600	
Min. Reset Pulse Width t_W	5	–	200	330	–	200	500	ns
	10	–	100	165	–	100	250	
Min. Reset Removal Time	5	–	300	750	–	300	1000	ns
	10	–	100	225	–	100	275	

▲ Measured with respect to carry out line.

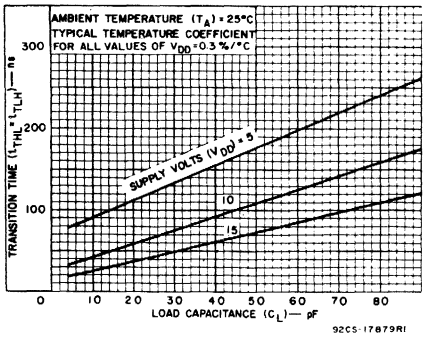


Fig. 11 – Typical transition time vs. C_L for carry output.

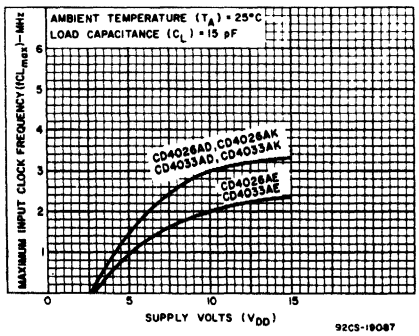


Fig. 12 – Maximum input clock frequency vs. V_{DD}.

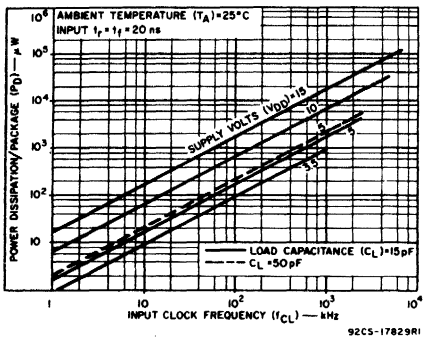


Fig. 13 – Typical dissipation characteristics.

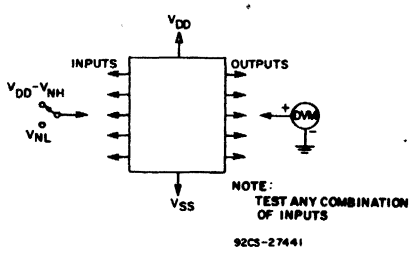


Fig. 14 – Noise immunity test circuit.

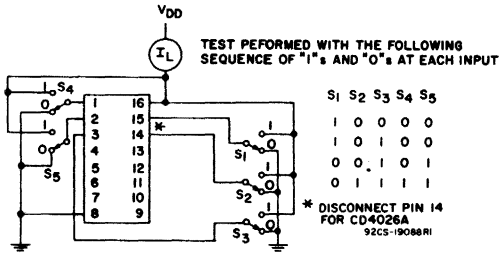


Fig. 15 – Quiescent-device-current test circuit.

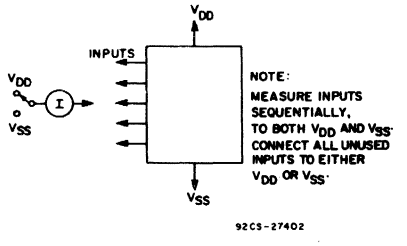


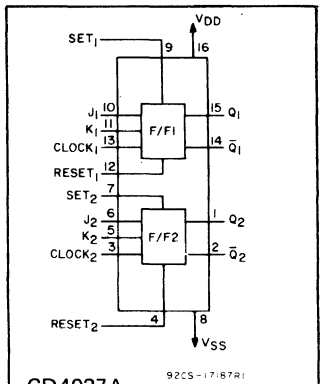
Fig. 16 – Input-leakage-current test circuit.

CD4027A Types

COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013A dual D-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.



CD4027A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	150 50	— —	200 75	— —	ns
Clock Pulse Width, t_W	5 10	330 110	— —	500 165	— —	ns
Clock Input Frequency (Toggle Mode) f_{CL}	5 10	dc	1.5 4.5	dc	1 3	MHz
Clock Rise or Fall Time, t_rCL,* t_fCL	5 10	—	15 5	—	15 5	μs
Set or Reset Pulse Width, t_W	5 10	200 80	—	300 120	—	ns

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

The CD4027A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation—retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation—10 MHz (typ.) clock toggle rate at 10V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications

- Registers, counters, control circuits

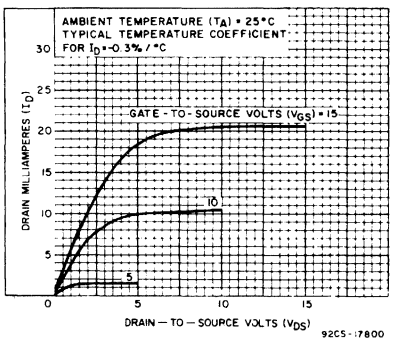
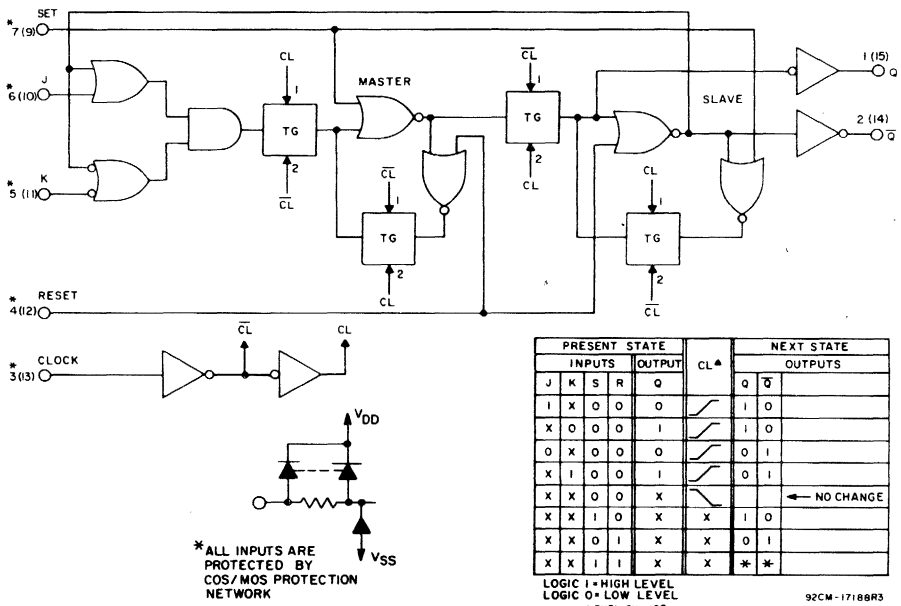


Fig. 1 — Typical n-channel drain characteristics.

CD4027A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, K, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E, Y PACKAGES -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.			5	1	0.005	1	60	10	0.01	10	140	μA
			10	2	0.005	2	120	20	0.05	20	280	
			15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max								V
	–	0.10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0.5	5	5 Typ.; 4.95 Min.								
	–	0.10	10	10 Typ.; 9.95 Min.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25 Typ.; 1.5 Min.								V
	9	–	10	4.5 Typ.; 3 Min.								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink), I_DN Min.	0.5	–	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	–	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source): I_DP Min.	4.5	–	5	−0.31	−0.5	−0.25	−0.175	−0.17	−0.5	−0.14	−0.12	
	9.5	–	10	−0.8	−1.3	−0.65	−0.45	−0.4	−1.3	−0.33	−0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



PRESENT STATE INPUTS J	K	S	R	OUTPUT Q	CL▲	NEXT STATE OUTPUTS Q	Q̄	
1	x	0	0	0	↑	1	0	
x	0	0	0	1	↑	1	0	
0	x	0	0	0	↑	0	1	
x	1	0	0	1	↑	0	1	
x	x	0	0	x	↓			← NO CHANGE
x	x	1	0	x	x	1	0	
x	x	0	1	x	x	0	1	
x	x	1	1	x	x	*	*	

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
▲ – LEVEL CHANGE
X – DON'T CARE

92CM-17188R3

Fig. 2–Logic diagram & truth table for CD4027A (one of two identical J-K flip flops).

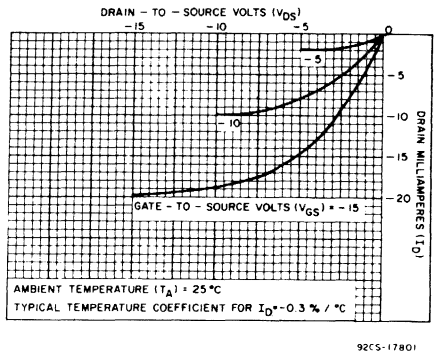


Fig.3 – Typical p-channel drain characteristics.

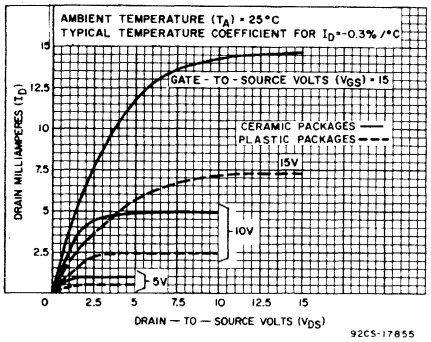


Fig.4 – Minimum n-channel drain characteristics.

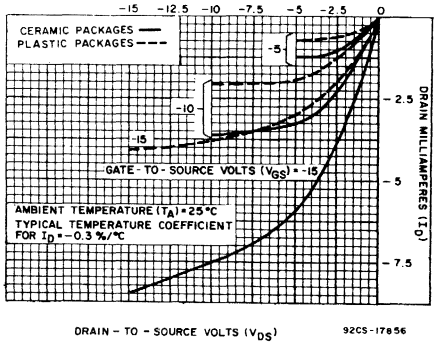


Fig.5 – Minimum p-channel drain characteristics.

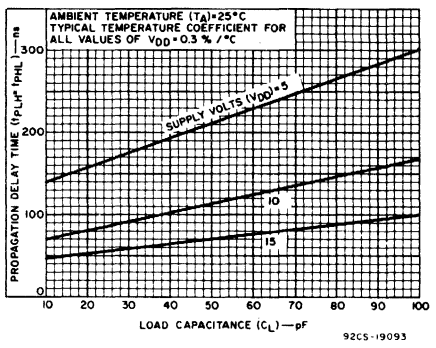


Fig.6 – Typical propagation delay time vs. C_L

CD4027A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	400	ns
	10	–	75	110	–	75	150	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Transition Time t_{THL}, t_{TLH}	5	–	75	125	–	75	250	ns
	10	–	50	70	–	50	140	
Maximum Clock Input Frequency (Toggle Mode) f_{CL}	5	1.5	3	–	1	3	–	MHz
	10	4.5	8	–	3	8	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	–	165	500	ns
	10	–	65	110	–	65	165	
Minimum Set or Reset Pulse Width, t_W	5	–	125	200	–	125	300	ns
	10	–	50	80	–	50	120	
Minimum Data Setup Time, t_S	5	–	70	150	–	70	200	ns
	10	–	25	50	–	25	75	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	us
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

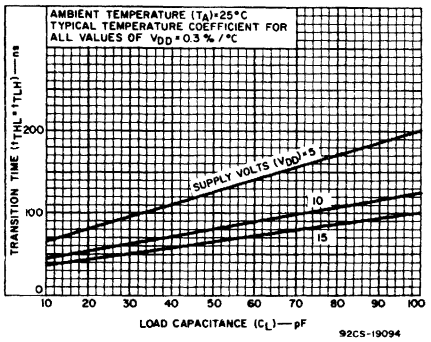


Fig.7 – Typical transition time vs. C_L.

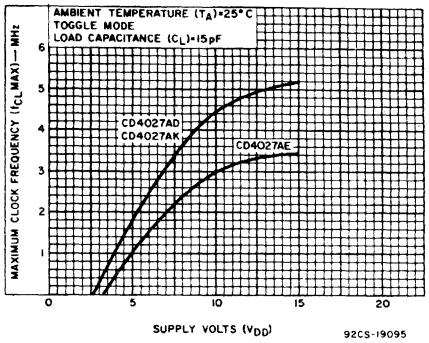


Fig.8 – Typical maximum clock input frequency vs. supply voltage.

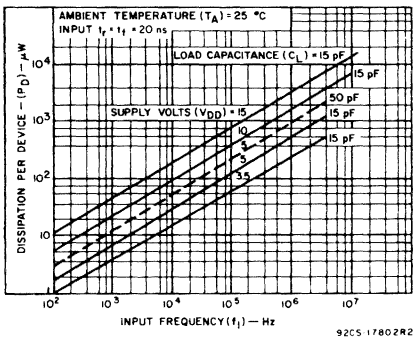


Fig.9 – Typical dissipation characteristics.

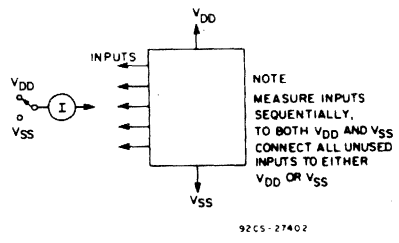


Fig. 11 – Input leakage current test circuit.

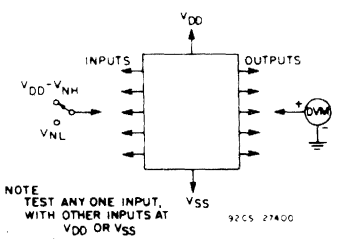


Fig. 10 – Noise immunity test circuit.

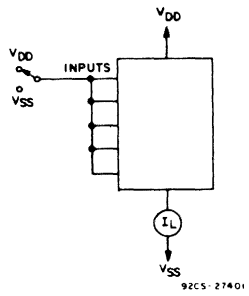


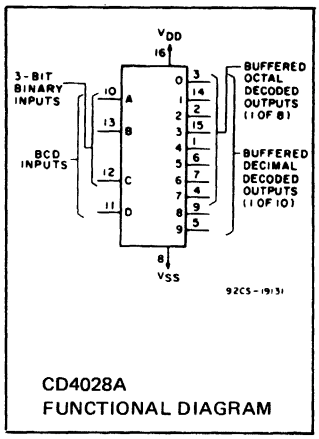
Fig. 12 – Quiescent device current test circuit.

CD4028A Types

COS/MOS BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

The CD4028A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4028A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages references to V_{SS} Terminal) . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V

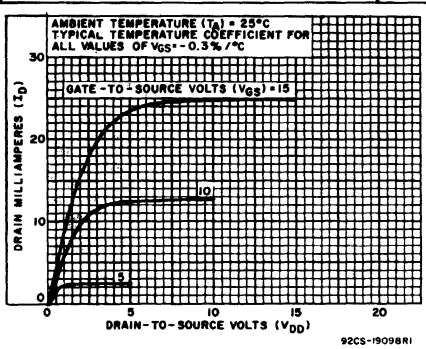


Fig. 1 – Typical output n-channel drain characteristics.

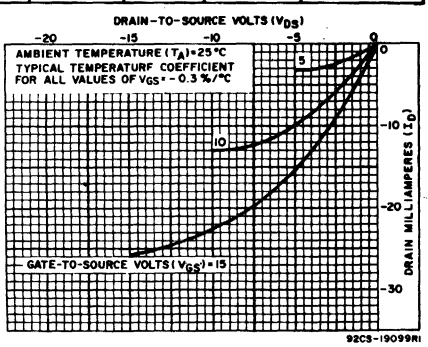


Fig. 2 – Typical output p-channel drain characteristics.

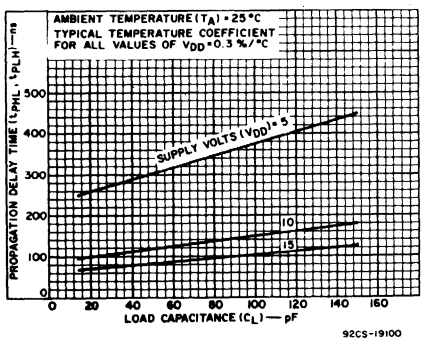


Fig. 3 – Typical propagation delay time vs. C_L.

Features:

- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability. . . . . 8 mA (typ.) sink or source
- "Positive logic" inputs and outputs. . . . . decoded outputs go high on selection
- Medium-speed operation . . . . t_{THL}, t_{TLH} = 30 ns (typ.) @ V_{DD} = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Code conversion
- Address decoding—memory selection control
- Indicator-tube decoder

CD4028A Types

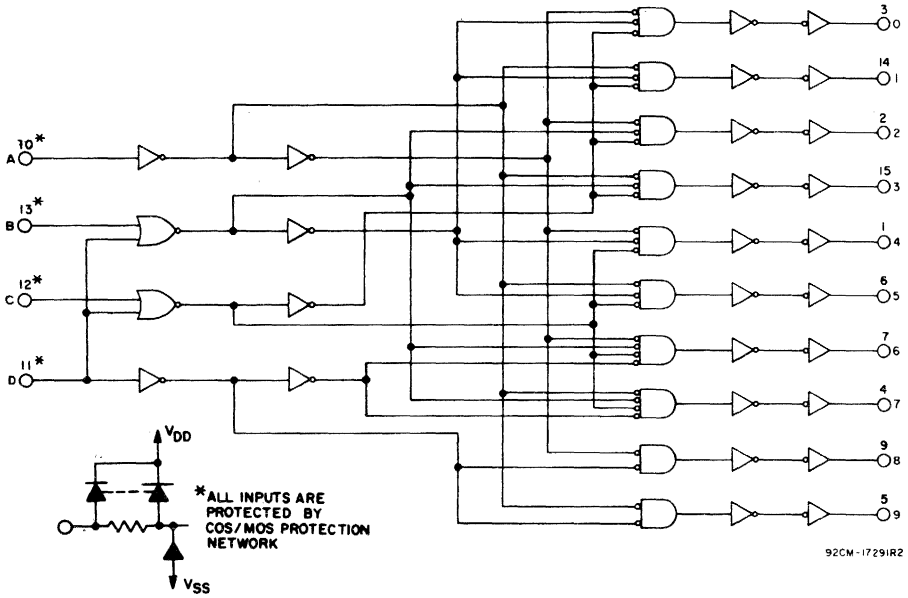


Fig. 4 – Logic diagram.

TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY STATES

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.5	5	300	50	5	50	700	μA
	–	–	10	10	1	10	600	100	10	100	1400	
	–	–	15	50	1	50	2000	500	10	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_{DN} Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P-Channel (Source), I_DP Min.	4.5	–	5	-0.7	-0.9	-0.45	-0.32	-0.32	-0.9	-0.22	-0.18	
	9	–	10	-1.4	-1.9	-0.95	-0.65	-0.65	-1.9	-0.48	-0.4	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

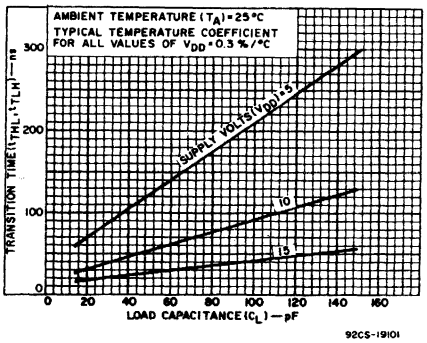


Fig. 5 – Typical transition time vs. C_L.

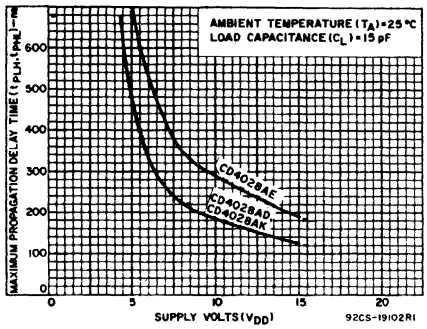


Fig. 6 – Maximum propagation delay time vs. V_{DD}.

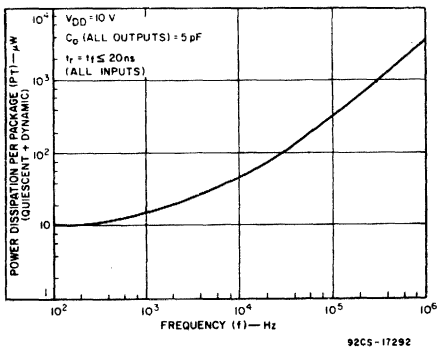


Fig. 7 – Dissipation vs. input frequency.

CD4028A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^oC$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H PACKAGES			E, Y PACKAGES			
		V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	250	480	–	250	700	ns
		10	–	100	180	–	100	290	
Transition Time; t_{THL}, t_{TLH}		5	–	60	150	–	60	300	ns
		10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

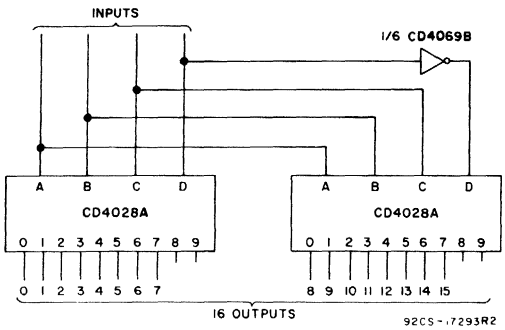
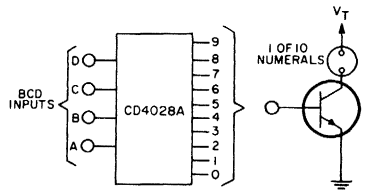


Fig. 8 – Code conversion circuit.

The circuit shown in Fig. 9 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.



▲ (Trademark) Burroughs Corp.

TUBE REQUIREMENTS:

Type	V_T (Vdc)	mA/numeral
Burroughs B4081	170	1.4
B4336/718	170	2
B4032	170	1.4
B4021	120	1.4

TRANSISTOR CHARACTERISTICS:
Leakage with transistor cutoff ≤ 0.05mA
$V_{(BR)CEO}$ ≥ 70V

Fig. 9 – Neon readout (Nixie Tube▲) display application.

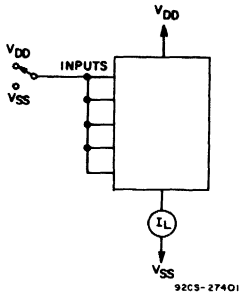


Fig. 10 – Quiescent-device-current test circuit.

TABLE II – CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER																
				Hexa-Decimal		Decimal																				
D	C	B	A	4-BIT BINARY	4-BIT GRAY	EXCESS-3	EXCESS-3 GRAY	AIKEN	4-2-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	3	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

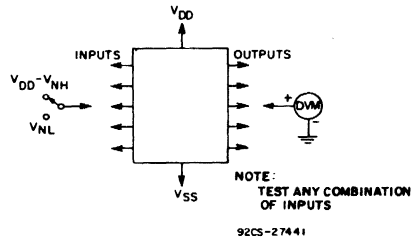


Fig. 11 – Noise-immunity test circuit.

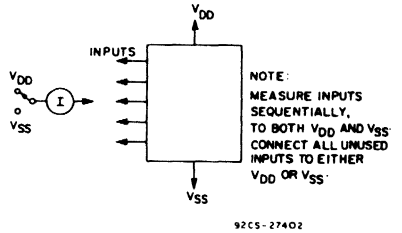


Fig. 12 – Input-leakage-current test circuit.

CD4029A Types

COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

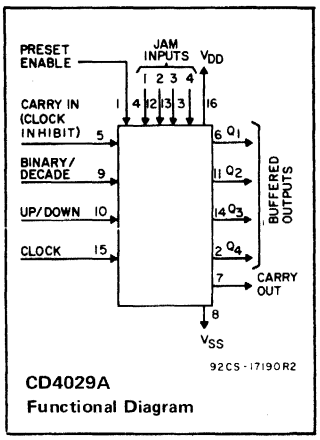
The CD4029A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium speed operation . . . 5 MHz (typ.) @ C_L=15 pF and $V_{DD}-V_{SS}$=10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



CD4029A
Functional Diagram

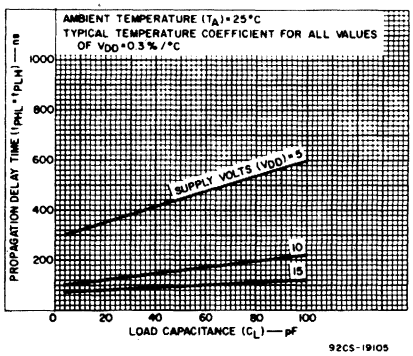


Fig. 1— Typical propagation delay time vs. C_L for Q outputs.

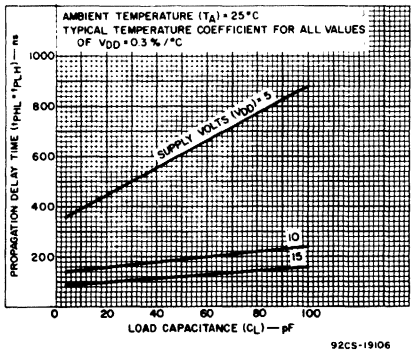


Fig. 2— Typical propagation delay time vs. C_L for carry output.

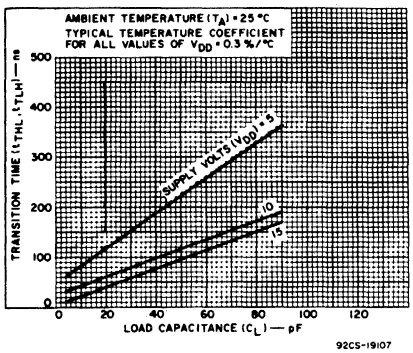


Fig. 3— Typical transition time vs. C_L for Q outputs.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		E,Y Packages		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t_S*	5	650	–	1300	–	ns
	10	230	–	460	–	
Clock Pulse Width, t_W	5	340	–	500	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	dc	1	MHz
	10	dc	3	dc	2	
Clock Rise or Fall Time, t_rCL,t_fCL**	5	–	15	–	15	μs
	10	–	15	–	15	
Preset Enable Pulse Width, t_W	5	330	–	660	–	ns
	10	160	–	320	–	

*From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.

**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

CD4029A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,K,H ..... −55 to +125°C
PACKAGE TYPES E,Y ..... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A=−40 to +60°C (PACKAGE TYPES E,Y) ..... 500 mW
FOR T_A=+60 to +85°C (PACKAGE TYPES E,Y) ..... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A=−55 to +100°C (PACKAGE TYPES D,F,K) ..... 500 mW
FOR T_A=+100 to +125°C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,K,H Packages Min.	Typ.	Max.	LIMITS E,Y Packages Min.	Typ.	Max.	UNITS
Clocked Operation								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Transition Time: t_{THL}, t_{TLH} Q Outputs	5	–	100	200	–	100	400	ns
	10	–	50	100	–	50	200	
Carry Output	5	–	200	400	–	200	800	
	10	–	100	200	–	100	400	
Minimum Clock Pulse Width, t_W	5	–	200	340	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Setup Times, t_S*	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
Preset Enable								
Propagation Delay Time: t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Minimum Preset Enable Pulse Width, t_W	5	–	115	330	–	115	660	ns
	10	–	80	160	–	80	320	
Minimum Preset Enable Removal Time	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Input								
Propagation Delay Time: t_{PHL}, t_{PLH} Carry Output	5	–	175	350	–	175	700	ns
	10	–	50	100	–	50	200	

For footnotes, see Recommended Operating Conditions.

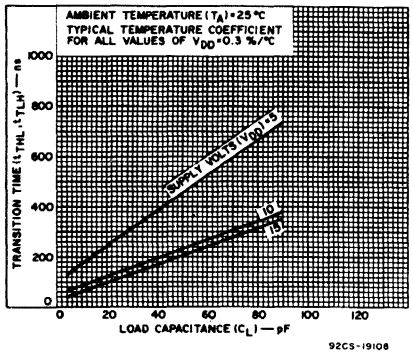


Fig. 4—Typical transition time vs. C_L for carry output.

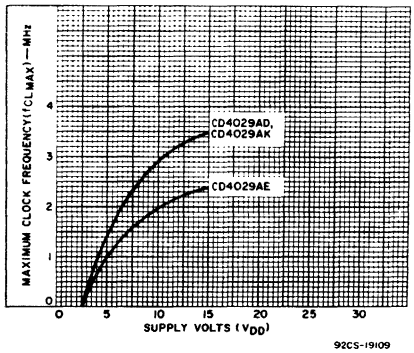


Fig. 5—Maximum clock input frequency vs. V_{DD}.

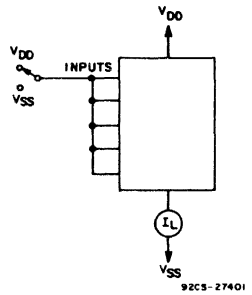


Fig. 6—Quiescent-device-current test circuit.

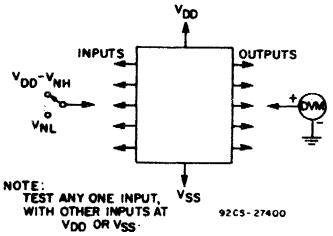


Fig. 7—Noise-immunity test circuit.

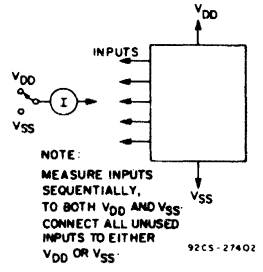


Fig. 8—Input-leakage-current test circuit.

CD4029A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min. Q Outputs	0.5	–	5	0.5	0.8	0.4	0.28	0.24	0.8	0.2	0.16	mA
	0.5	–	10	0.74	1.2	0.6	0.42	0.36	1.2	0.3	0.24	
Carry Output	0.5	–	5	0.1	0.16	0.08	0.06	0.05	0.16	0.04	0.03	
	0.5	–	10	0.4	0.64	0.32	0.22	0.19	0.64	0.16	0.13	
P-Channel (Source), I_DP Min. Q Outputs	4.5	–	5	−0.18	−0.24	−0.12	−0.08	−0.07	−0.24	−0.06	−0.05	
	9.5	–	10	−0.3	−0.4	−0.2	−0.14	−0.14	−0.4	−0.1	−0.08	
Carry Output	4.5	–	5	−0.09	−0.12	−0.06	−0.04	−0.04	−0.12	−0.03	−0.02	
	9.5	–	10	−0.15	−0.2	−0.1	−0.07	−0.07	−0.2	−0.05	−0.04	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

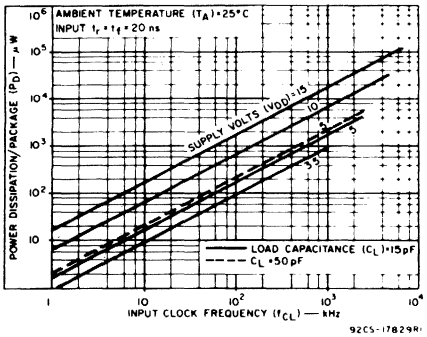


Fig. 9—Typical dissipation characteristics.

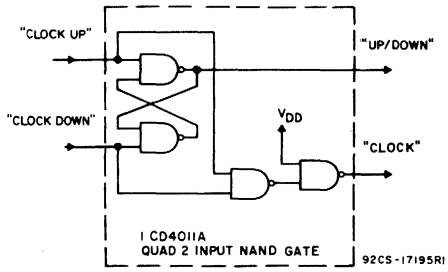


Fig. 10—Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029A CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029A CLOCK and UP/DOWN inputs can easily be realized by use of the circuit shown below.

CD4029A changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

* TRUTH TABLE FOR F-F No 1

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
⌞	1	1	X	$\bar{Q}$	Q
X	X	0	1	1	Q
⌞	0	1	X	Q	$\bar{Q}$ NC
⌜	X	1	X	Q	$\bar{Q}$ NC

NC-NO CHANGE TE-TOGGLE ENABLE

** TRUTH TABLE FOR F-F'S 2,3,4

CLOCK	TE	PE	J	Q	$\bar{Q}$
X	X	0	0	0	1
⌞	0	1	X	$\bar{Q}$	Q
X	X	0	1	1	0
⌞	1	1	X	Q	$\bar{Q}$ NC
⌜	X	1	X	Q	$\bar{Q}$ NC

X-DON'T CARE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK INHIBIT)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

92CL-17191R2

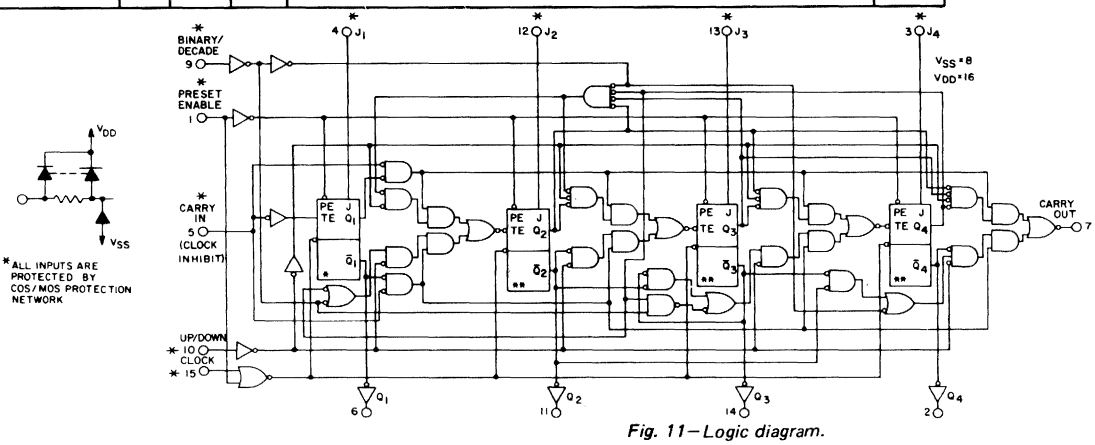


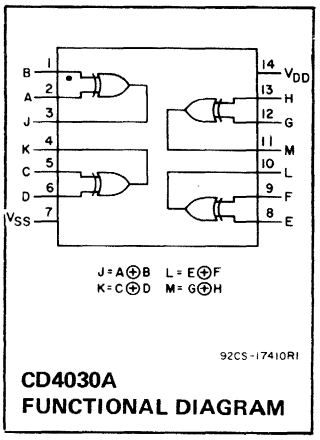
Fig. 11—Logic diagram.

CD4030A Types

COS/MOS
Quad Exclusive-OR Gate

The RCA-CD4030A types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

The CD4030A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4030A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A)

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

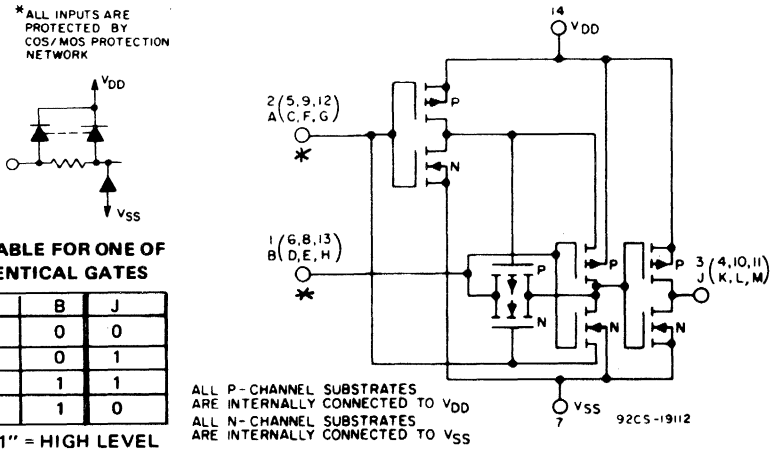
LEAD TEMPERATURE (DURING SOLDERING)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C,

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D,F,K,H Packages		E,Y Packages		
	Min.	Max.	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	3	12	V



TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL

Fig.1 — Schematic diagram for 1 of 4 identical exclusive-OR gates.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

Features:

- **Medium speed operation. . . . . $t_{PHL} = t_{PLH}$ = 40 ns (typ.) @ C_L = 15 pF and $V_{DD}-V_{SS}$ = 10 V**
- **Low output impedance. . . . . 500 Ω (typ.) @ $V_{DD}-V_{SS}$ = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (Full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Even and odd-parity generators and checkers**
- **Logical comparators**
- **Adders/subtractors**
- **General logic functions**

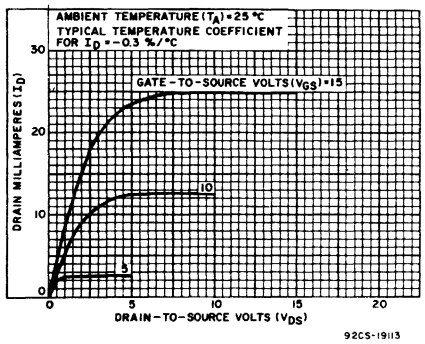


Fig.2 — Typical output n-channel drain characteristics.

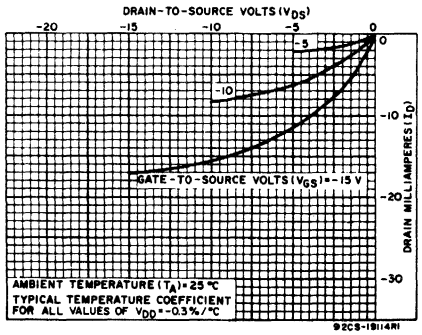


Fig.3 — Typical output p-channel drain characteristics.

CD4030A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	0.5	0.005	0.5	30	5	0.05	5	70	μA
	–	–	10	1	0.01	1	60	10	0.1	10	140	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N Channel (Sink) I_DN Min.	0.5	–	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	–	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
P Channel (Source): I_DP Min.	4.5	–	5	−0.45	−0.6	−0.3	−0.21	−0.21	−0.6	−0.15	−0.12	
	9.5	–	10	−0.95	−1.3	−0.65	−0.45	−0.45	−1.3	−0.32	−0.25	
Input Leakage Current I_{IL}, I_{IH}	Any Input		15	±10⁻⁵ Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions		LIMITS						Units
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: t_{PLH}, t_{PHL}		5	–	100	200	–	100	300	ns
		10	–	40	100	–	40	150	
Transition Time: High-to-Low Level, t_{THL}		5	–	70	150	–	70	300	ns
		10	–	25	75	–	25	150	
Low-to-High Level, t_{TLH}		5	–	80	150	–	80	300	
		10	–	30	75	–	30	150	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

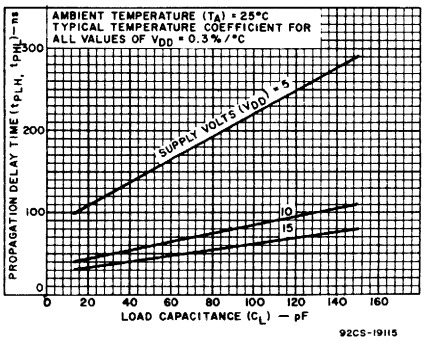


Fig.4 – Typical propagation-delay time vs. load capacitance.

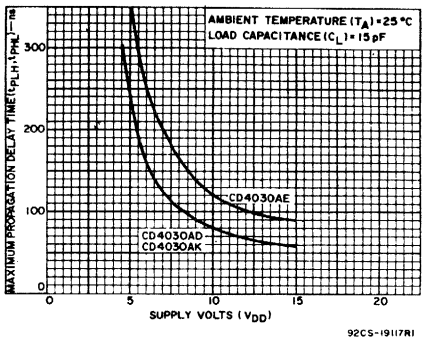


Fig.5 – Maximum propagation-delay time vs. supply voltage.

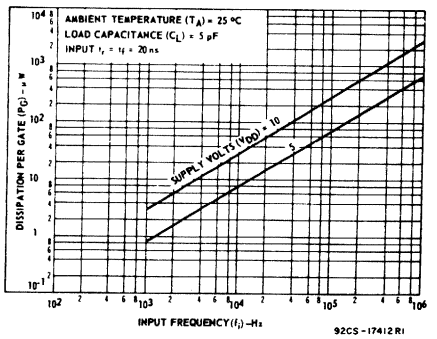


Fig.6 – Typical dynamic power dissipation characteristics.

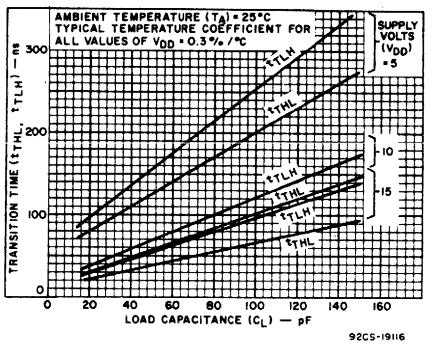


Fig.7 – Typical transition time vs. load capacitance.

CD4031A Types

COS/MOS 64-Stage Static Shift Register

The RCA-CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

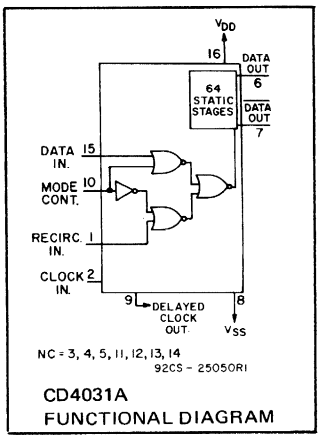
The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 4 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031A has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements.

Data (Q) and $\overline{Data}$ ($\overline{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of drving one TTL or DTL load.

The CD4031A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation: DC to 4 MHz typ. @ $V_{DD} - V_{SS} = 10$ V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.) for ceramic packages; 100 μW (typ.) for plastic packages**



CD4031A
FUNCTIONAL DIAGRAM

- **Single phase clocking requirements**
- **Recirculation capability**
- **Data compatible with TTL-DTL**
- **Two cascading modes:**
  - **Direct clocking for high-speed operation**
  - **Delayed clocking for reduced clock drive requirements**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time delay circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
  PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
  FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Hold Time, t_H	5	100	–	100	–	ns
	10	200	–	200	–	
Clock Pulse Width, t_W	5	0.62	–	1.3	–	μs
	10	1.25	–	0.5	–	
Clock Input Frequency, f_{CL}	5	dc	0.8	dc	0.4	MHz
	10	dc	2	dc	1	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	2	–	2	μs
	10	–	1	–	1	

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

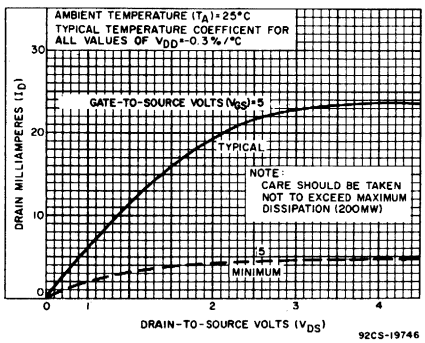


Fig. 1

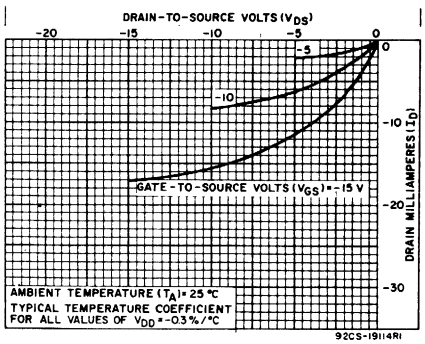
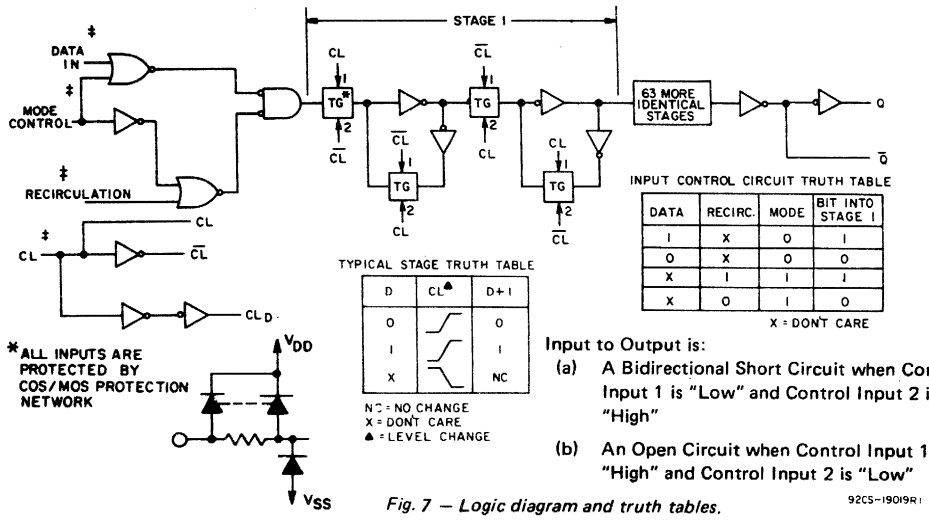


Fig. 2 – Typical output p-channel drain characteristics for Q output.

CD4031A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	10	0.5	10	600	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	1.6	2.6	1.3	1.05	mA
		0.5	–	10	5	8	4	3.2	5	8	4	3.2	
	$\overline{Q}$	0.5	–	5	0.11	0.18	0.09	0.06	0.05	0.18	0.045	0.037	
		0.5	–	10	0.24	0.4	0.2	0.14	0.12	0.4	0.1	0.08	
	CL_D	0.5	–	5	0.48	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
		0.5	–	10	1.5	2.4	1.2	0.84	0.75	2.4	0.6	0.5	
P- Channel (Source): I_DP Min.	Q	4.5	–	5	-0.4	-0.64	-0.32	-0.22	-0.20	-0.64	-0.16	-0.13	
		9.5	–	10	-0.85	-1.4	-0.70	-0.49	-0.42	-1.4	-0.35	-0.29	
	$\overline{Q}$	4.5	–	5	-0.11	-0.18	-0.09	-0.06	-0.05	-0.18	-0.045	-0.037	
		9.5	–	10	-0.24	-0.4	-0.20	-0.14	-0.12	-0.4	-0.10	-0.08	
	CL_D	4.5	–	5	-0.48	-0.8	-0.40	-0.28	-0.24	-0.8	-0.20	-0.16	
		9.5	–	10	-1	-1.6	-0.80	-0.56	-0.5	-1.6	-0.40	-0.32	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



TYPICAL STAGE TRUTH TABLE

D	CL▲	D+1
0		0
1		1
X		NC

NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

X = DON'T CARE

Input to Output is:

(a) A Bidirectional Short Circuit when Control Input 1 is "Low" and Control Input 2 is "High"

(b) An Open Circuit when Control Input 1 is "High" and Control Input 2 is "Low"

Fig. 7 – Logic diagram and truth tables. 92CS-19019R1

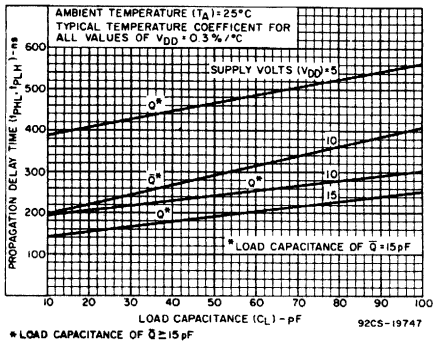


Fig. 3 – Typical propagation delay time vs. load capacitance for data outputs.

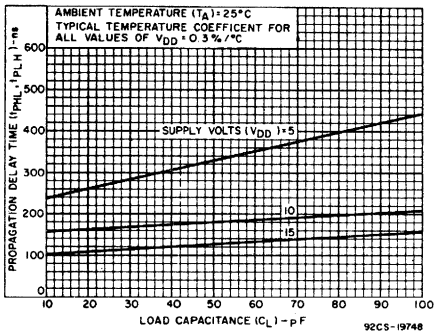


Fig. 4 – Typical propagation delay vs. load capacitance for delayed clock output.

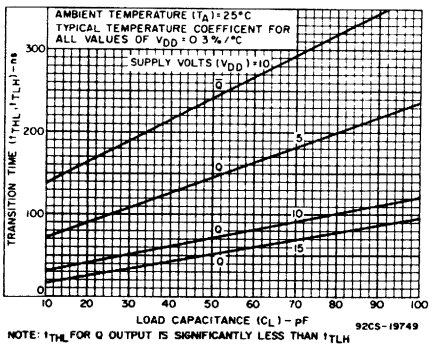


Fig. 5 – Typical transition time vs. load capacitance for data outputs.

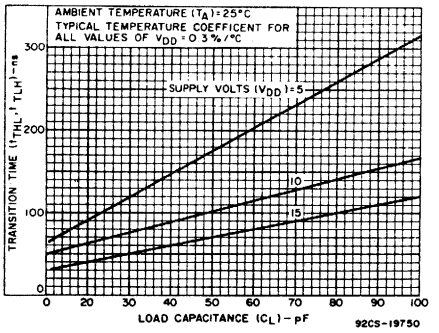


Fig. 6 – Typical transition time vs. load capacitance for delayed clock output.

CD4031A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF (unless otherwise specified), R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D, F, K, H MIN.	D, F, K, H TYP.	D, F, K, H MAX.	E, Y MIN.	E, Y TYP.	E, Y MAX.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	400	800	–	400	1600	ns
Clock to Data Output Q & $\overline{Q}$*		10	–	200	400	–	200	800	
Clock to CL_D	C_L = 60 pF	5	–	400	800	–	400	1600	
		10	–	200	400	–	200	800	
Transition Time; t_{THL}, t_{TLH} Q Output		5	–	75	150	–	75	300	ns
		10	–	30	60	–	30	120	
$\overline{Q}$ Output		5	–	300	600	–	300	1200	
		10	–	150	300	–	150	600	
CL_D Output	C_L = 60 pF	5	–	200	400	–	200	800	
		10	–	100	200	–	100	400	
Clock Rise and Fall Time; t_rCL, t_fCL**		5	–	–	2	–	–	2	μs
		10	–	–	1	–	–	1	
Minimum Data Set-Up Time, t_S		5	–	200	400	–	200	800	ns
		10	–	50	100	–	50	200	
Maximum Clock Input Frequency, f_{CL}***		5	0.8	2	–	0.4	2	–	MHz
		10	2	4	–	1	4	–	
Minimum Data Hold Time, t_H		5	–	50	100	–	50	100	ns
		10	–	100	200	–	100	250	
Minimum Clock Pulse Width, t_W		5	–	1.3	0.62	–	2.6	1.3	μs
		10	–	2.5	1.25	–	1	0.5	
Average Input Capacitance, C_I Clock			–	60	–	–	60	–	pF
All Others			–	5	–	–	5	–	

* Capacitive loading on $\overline{Q}$ output affects propagation delay of Q output. These limits apply for $\overline{Q}$ load $C_L \leq 15$ pF.

** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

*** Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature –

$$f_{max} = \frac{1}{(n-1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$

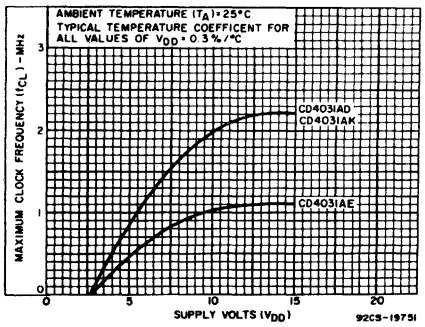


Fig. 8 – Maximum clock input frequency vs. supply voltage.

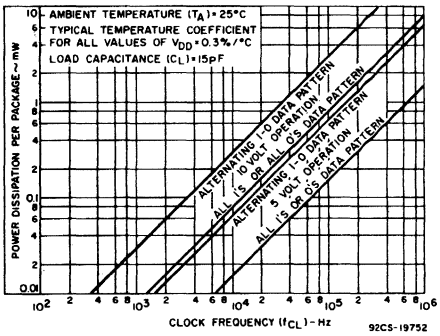


Fig. 9 – Typical power dissipation vs. frequency.

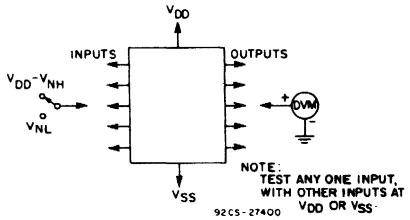


Fig. 10 – Noise-immunity test circuit.

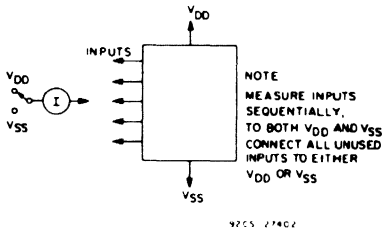
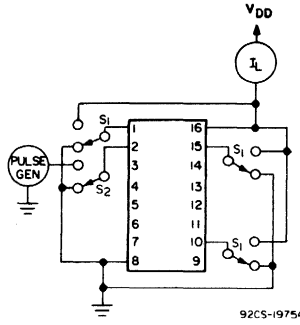
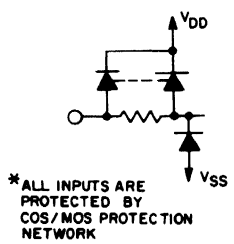


Fig. 11 – Input-leakage-current test circuit.



WITH S_1 AT GROUND, CLOCK UNIT 64 TIMES BY CONNECTING S_2 TO PULSE GENERATOR. RETURN S_2 TO GND AND MEASURE LEAKAGE CURRENT. REPEAT WITH S_1 AT V_{DD}.

Fig. 13 – Quiescent-device-current test circuit.



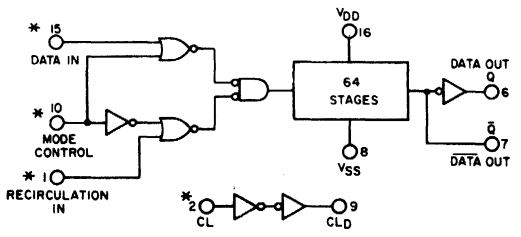


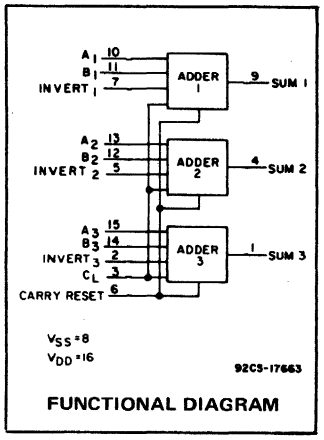
Fig. 12 – Functional diagram.

CD4032A, CD4038A Types

COS/MOS Triple Serial Adders

Positive Logic Adder – CD4032A

Negative Logic Adder – CD4038A



FUNCTIONAL DIAGRAM

Features:

- **Invert inputs on all adders for sum complementing applications**
- **Fully static operation. . . . . dc to 5 MHz (typ.)**
- **Buffered outputs**
- **Single-phase clocking**
- **Microwatt quiescent power dissipation. . . . 5 μW (typ.)**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

The RCA-CD4032A and CD4038A types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the CD4032A or at the negative-going clock for the CD4038A, thus, for spike free operation the input data transitions should occur as soon as possible after the triggering edge.

The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one bit-position before the application of the first bit of the next word. Figs. 2 and 4 show definitive waveforms for all input and output signals.

The CD4032A and CD4038A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip from (H suffix).

Applications:

- **Serial arithmetic units**
- **Digital correlators**
- **Digital datalink computers**
- **Flight control computers**
- **Digital servo control systems**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATINT GEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPES E, Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . –0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = –40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D, F, K, H Packages Min.	LIMITS D, F, K, H Packages Max.	LIMITS E, Y Packages Min.	LIMITS E, Y Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Setup Time, t_S	5 10	t_rCL	–	t_rCL	–	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs

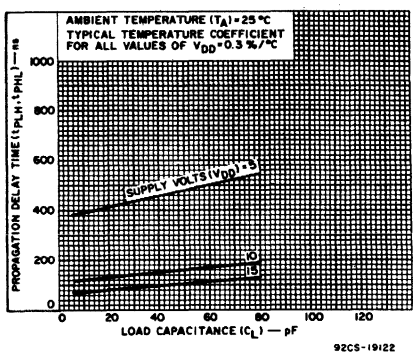


Fig. 1 – Typical propagation delay time vs. load capacitance for A, B, or INVERT inputs to sum outputs.

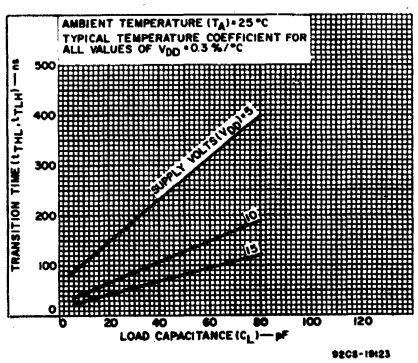


Fig. 2 – Typical transition time vs.load capacitance for sum outputs.

CD4032A, CD4038A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	LIMITS E, Y Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PLH}, t_{PHL} A, B, or Invert Inputs to Sum Outputs	5	–	400	1100	–	400	1400	ns
	10	–	125	250	–	125	300	
Clock Input to Sum Outputs	5	–	800	2200	–	800	2400	
	10	–	250	500	–	250	600	
Transition Time; t_{THL}, t_{TLH} (Sum Outputs)	5	–	125	375	–	125	425	ns
	10	–	50	150	–	50	200	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Clock Rise & Fall Time; t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Input Set Up Time, t_S*	5	–	–	t_rCL	–	–	t_rCL	ns
	10							
Average Input Capacitance, C_I		–	5	–	–	5	–	pF

*This characteristic refers to the minimum time required for the A, B, or Reset Inputs to change state following a positive clock transition (CD4032A) or negative transition (CD4038A).

**If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

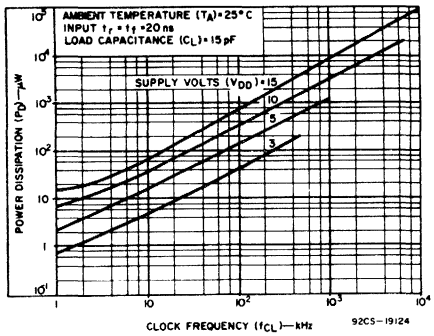


Fig. 3 – Typical dissipation characteristics.

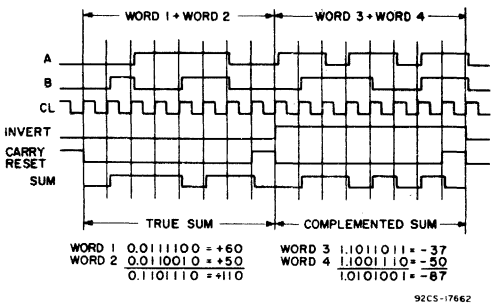


Fig. 4 – CD4032A timing diagram.

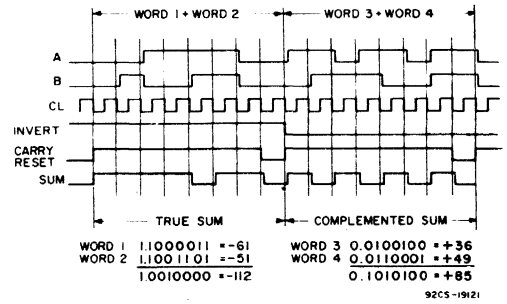


Fig. 5 – CD4038A timing diagram.

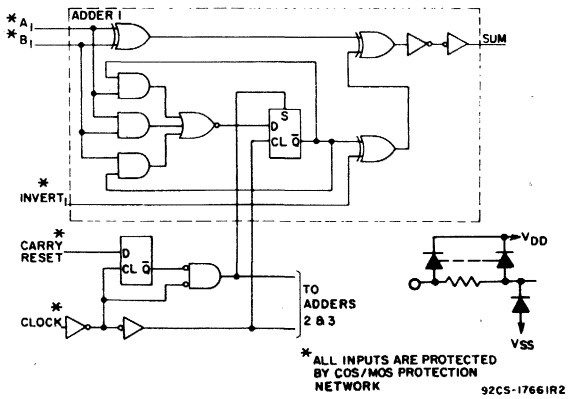


Fig. 6 – CD4032A logic diagram of one of three serial adders.

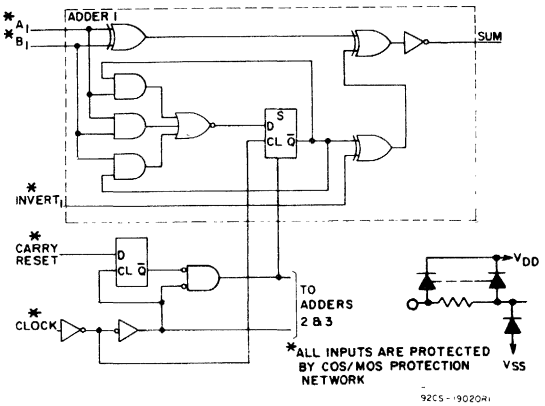


Fig. 7 – CD4038A logic diagram of one of three serial adders.

CD4032A, CD4038A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, K, F, H Packages				E, Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_DN Min.	0.5	–	5	0.6	0.9	0.5	0.3	0.25	0.9	0.2	0.14	mA
	0.5	–	10	0.75	2.4	0.7	0.6	0.6	2.4	0.5	0.4	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.21	−0.4	−0.15	−0.075	−0.14	−0.4	−0.1	−0.095	
	9.5	–	10	−0.7	−7.2	−0.55	−0.35	−0.3	−1.2	−0.27	−0.22	
Input Leakage Current, I_{IL}, I_{IH}	Any Input			±10⁻⁵ Typ., ±1 Max.								μA
	–	–	15									

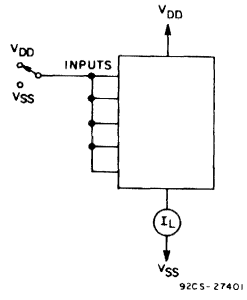


Fig. 8 – Quiescent-device-current test circuit.

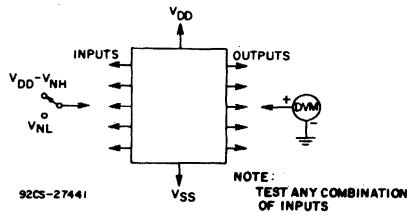


Fig. 9 – Noise-immunity test circuit.

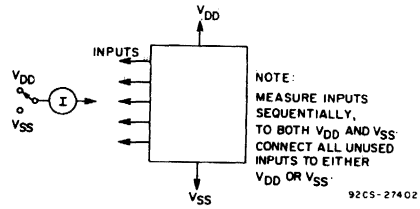


Fig. 10 – Input-leakage-current test circuit.

CD4034A Types

COS/MOS MSI 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

The RCA-CD4034A is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/2B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034A packages.

The CD4034A-Series types are supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

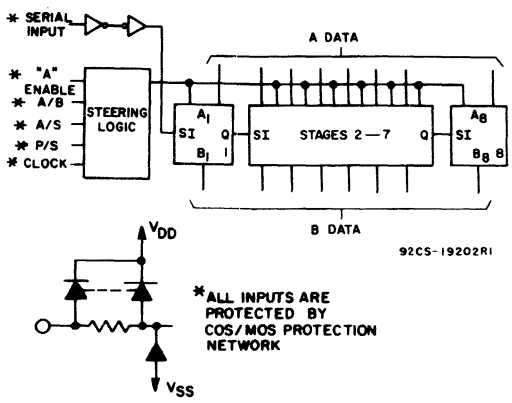


Fig. 1 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to + 150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H . . . . . -55 to +125°C

PACKAGE TYPE E. . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to +60°C (PACKAGE TYPE E). . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E). . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	500 200	– –	ns
Clock Pulse Width, t_W	5 10	400 175	– –	400 175	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1.5 3	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5,10	–	15	–	15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

CD4034A Types

Table I — Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) At $V_{DD}-V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

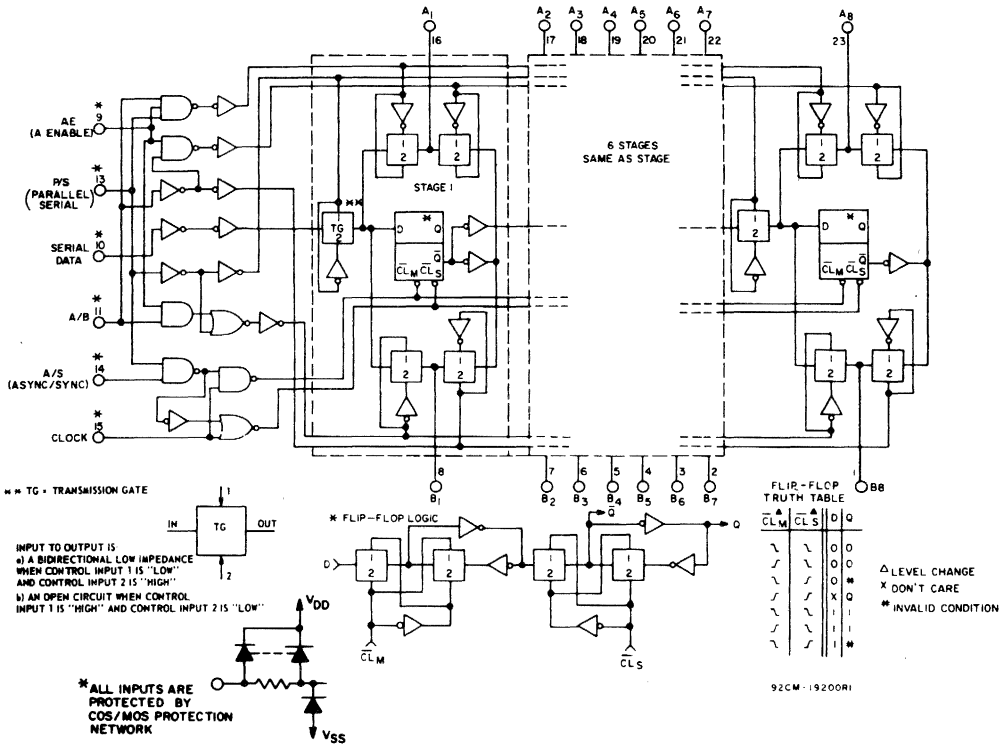


Fig.2 — Logic diagram.

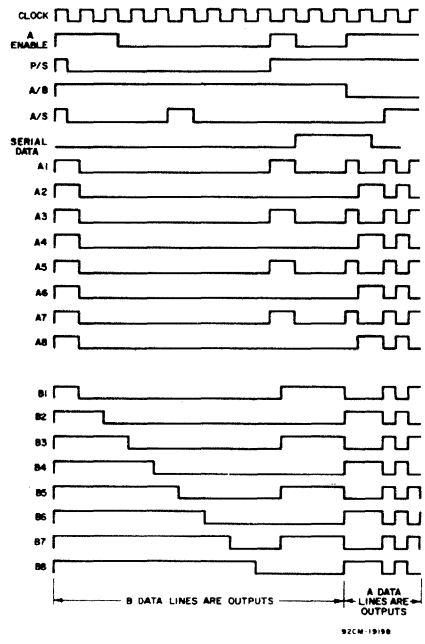


Fig.3 - Timing diagram.

CD4034A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.124	0.2	0.1	0.07	0.124	0.2	0.1	0.07	mA
	0.5	–	10	0.31	0.5	0.25	0.175	0.31	0.5	0.25	0.175	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.075	-0.1	-0.05	-0.035	-0.075	-0.1	-0.05	-0.035	
	9.5	–	10	-0.188	-0.25	-0.125	-0.088	-0.188	-0.25	-0.125	-0.088	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

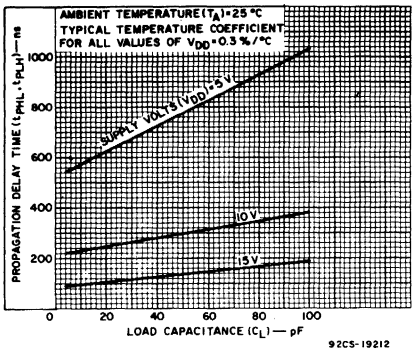


Fig.4 – Typical propagation delay time vs. load capacitance.

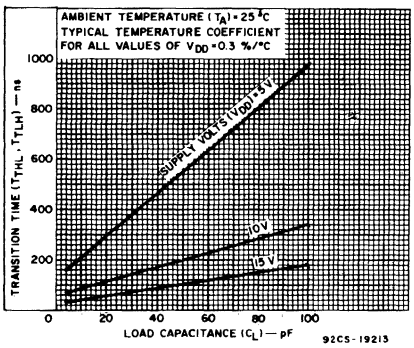


Fig.5 – Typical transition time vs. load capacitance.

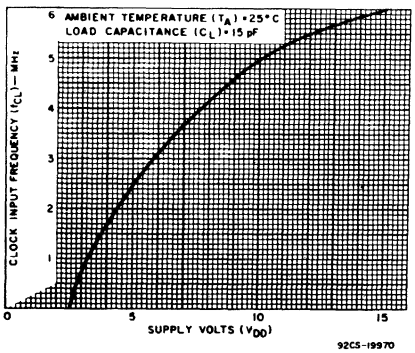


Fig.6 – Typical clock input frequency vs. supply voltage.

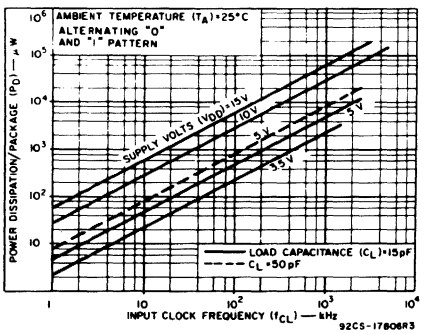


Fig.7 – Typical dissipation characteristics.

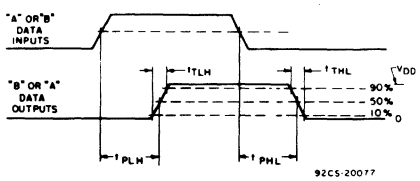


Fig.8 – Asynchronous operation propagation delay time and transition time.

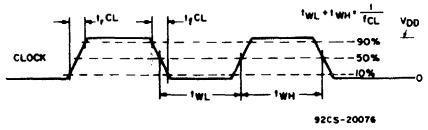


Fig.9 – Clock pulse rise and fall times.

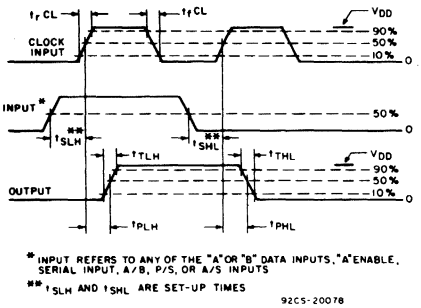


Fig.10 – Synchronous operation propagation delay times, transition times, and set-up times.

CD4034A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20ns, C_L = 15 pF, RL = 200kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, K, H PACKAGES MIN.	D, K, H PACKAGES TYP.	D, K, H PACKAGES MAX.	E PACKAGES MIN.	E PACKAGES TYP.	E PACKAGES MAX.	UNIT
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	600	1200	–	600	1200	ns
	10	–	240	480	–	240	480	
Transition Time; t_{THL}, t_{TLH}	5	–	250	750	–	250	750	ns
	10	–	100	300	–	100	300	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1.5	2.5	–	MHz
	10	3	5	–	3	5	–	
Clock Pulse Width, t_W	5	–	200	400	–	200	400	ns
	10	–	100	175	–	100	175	
Min. High-Level AE, P/S, A/S Pulse Width	5	–	240	480	–	240	480	ns
	10	–	85	195	–	85	195	
Clock Rise & Fall Time t_rCL, t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Data Set-Up Time, t_S	5	–	250	500	–	250	500	ns
	10	–	100	200	–	100	200	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

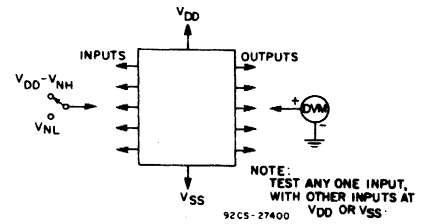


Fig. 11 – Noise-immunity test circuit.

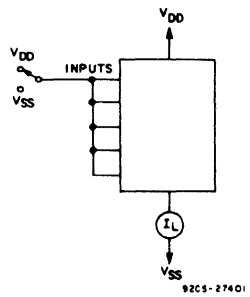


Fig. 12 – Quiescent-device-current test circuit.

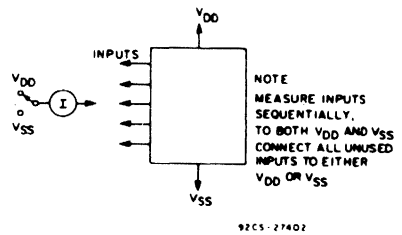


Fig. 13 - Input-leakage-current test circuit.

APPLICATIONS

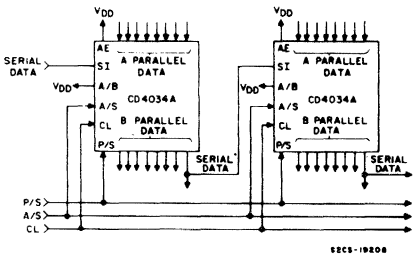


Fig. 14 – 16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

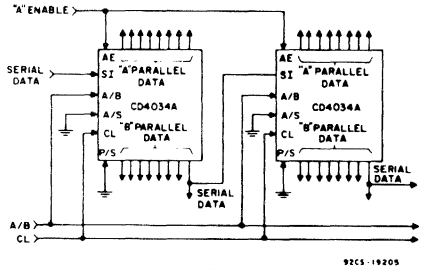


Fig. 15 – 16-Bit serial in/gated parallel out register.

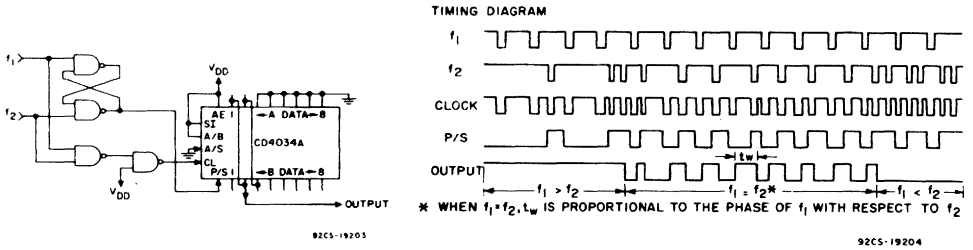


Fig. 16 – Frequency and phase comparator.

CD4035A Types
COS/MOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/Complement Outputs

Features:

- 4-Stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- J$\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Static flip-flop operation; Master-slave configuration
- Reset control
- Buffered outputs
- Low power dissipation — 5μW typ. (ceramic)
- High speed — to 5 MHz
- Quiescent current specified to 15 V
- Maximum input leakage current of 1μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

The RCA-CD4035A is a four-stage clocked signal serial register with provision for SYNCHRONOUS PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry via the D line of each register stage is permitted only when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

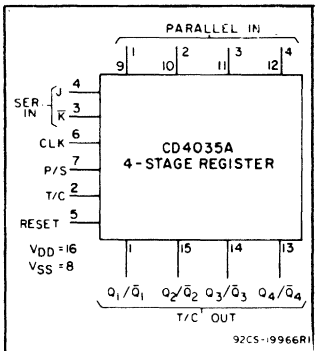
When the TRUE/COMPLEMENT control is high, the TRUE contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications

- Counters, Registers
  - Arithmetic-unit registers
  - Shift left — shift right registers
  - Serial-to-parallel/parallel-to-serial conversions
- Sequence generation
- Control circuits
- Code conversion



CD4035A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −66 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . −55 to +125°C

PACKAGE TYPES E, Y . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). 100mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5V

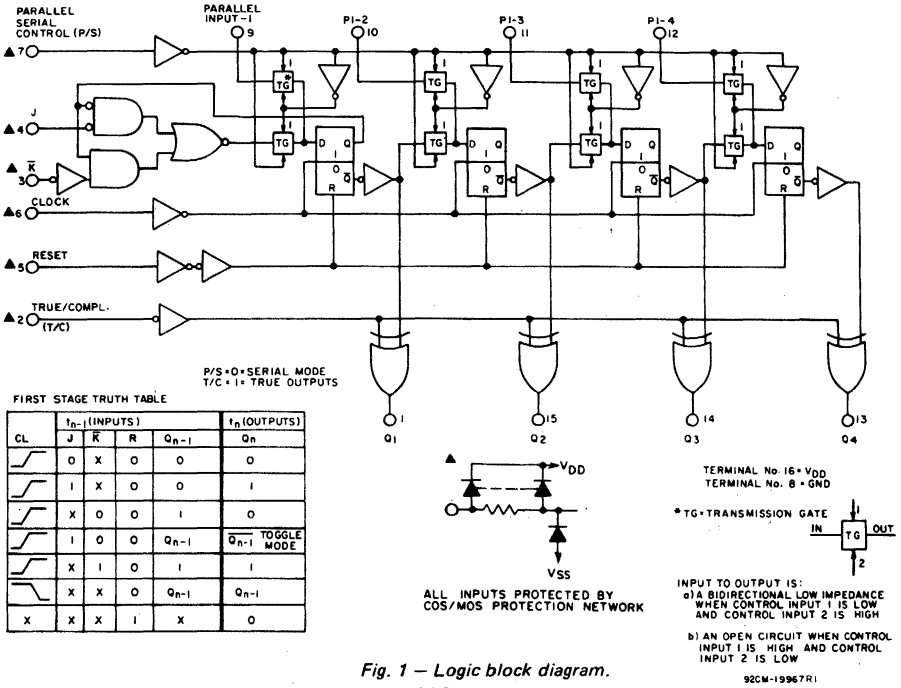
LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, except as noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range		3	12	3	12	V
Data Setup Time, t_S:						
J/$\overline{K}$ Lines	5	500	–	750	–	ns
	10	200	–	250	–	
Parallel-In Lines	5	350	–	500	–	
	10	80	–	100	–	
Clock Pulse Width, t_W	5	335	–	500	–	ns
	10	165	–	250	–	
Clock Rise and Fall Time, t_rCL,t_fCL	5	–	15	–	15	μs
	10	–	5	–	5	
Reset Pulse Duration, t_W	5	400	–	500	–	ns
	10	175	–	200	–	

CD4035A Types



FIRST STAGE TRUTH TABLE

CL	t_{n-1} (INPUTS) J	K	R	Q_{n-1}	t_n (OUTPUTS) Q_n
⌐	0	X	0	0	0
⌐	1	X	0	0	1
⌐	X	0	0	1	0
⌐	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⌐	X	1	0	1	1
⌐	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Fig. 1 – Logic block diagram.

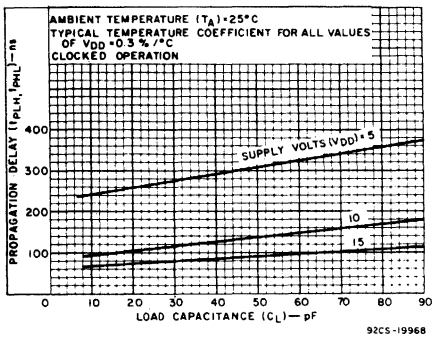


Fig. 2 – Typical propagation delay time vs. load capacitance.

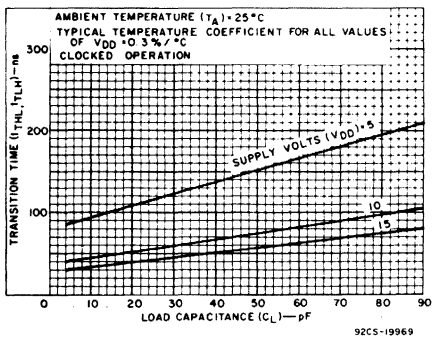


Fig. 3 – Typical transition time vs. load capacitance.

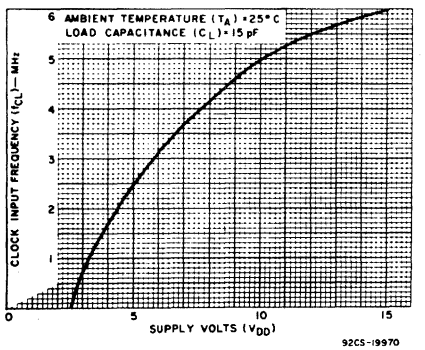


Fig. 4 – Typical clock input frequency vs. supply voltage.

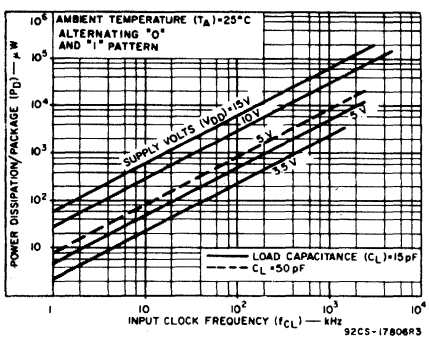


Fig. 5 – Typical dynamic power dissipation characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, K, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E, Y PACKAGES -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.62	1	0.5	0.35	0.43	1	0.35	0.24	mA
	0.5	–	10	1.55	2.5	1.25	0.87	1.05	2.5	0.85	0.59	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.31	-0.5	-0.25	-0.17	-0.2	-0.5	-0.18	-0.12	
	9.5	–	10	-0.81	-1.3	-0.65	-0.45	-0.56	-0.31	-0.45	-0.31	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4035A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^oC$, Input $t_r, t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTICS	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H PACKAGES			E, Y PACKAGES			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Min.	
CLOCKED OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Transition Time: t_{THL}, t_{TLH}		5	–	100	200	–	100	300	ns
		10	–	50	100	–	50	150	
Minimum Clock Pulse Width, t_W		5	–	200	335	–	200	500	ns
		10	–	100	165	–	100	250	
Maximum Clock Rise & Fall Time t_{rCL}, t_{fCL}*		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Minimum Setup Time: J/$\overline{K}$ Lines		5	–	250	500	–	250	750	ns
		10	–	100	200	–	100	250	
Parallel-In Lines		5	–	100	350	–	100	500	
		10	–	50	80	–	50	100	
Maximum Clock Frequency, f_{CL}		5	1.5	2.5	–	1	2.5	–	MH_z
		10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	–	250	700	ns
		10	–	100	200	–	100	300	
Minimum Reset Pulse Width, t_W		5	–	200	400	–	200	500	ns
		10	–	100	175	–	100	200	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

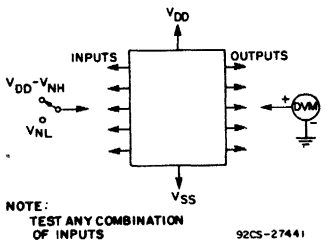


Fig. 6 – Noise-immunity test circuit.

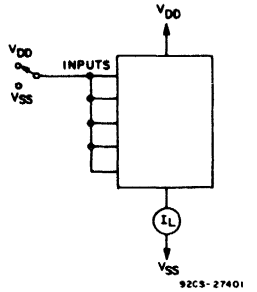


Fig. 7 – Quiescent-device-current test circuit.

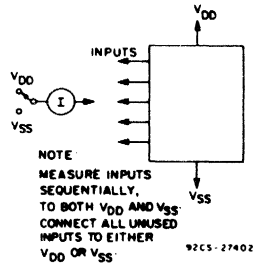


Fig. 8 – Input-leakage-current test circuit.

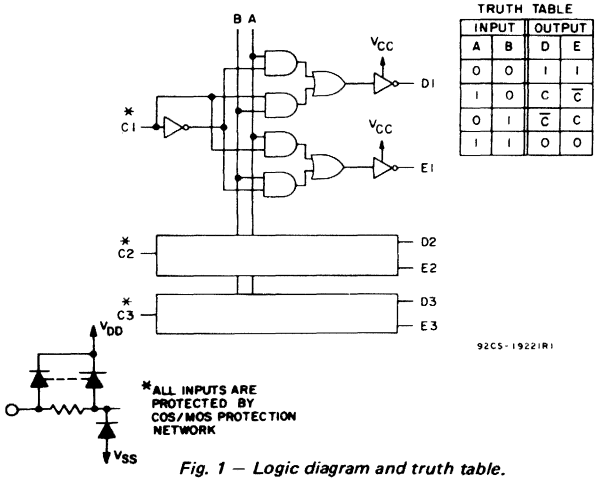
CD4037A Types

COS/MOS Triple AND/OR Bi-Phase Pairs

The RCA-CD4037A consists of three AND/OR pairs driven by common control signals A and B.

Each circuit has a data input (C), and two output terminals (D and E) that provide outputs in accordance with the truth table shown in Fig. 1. The circuit is useful for coding or decoding signals for split-phase (Bi-phase) communication systems, magnetic recording, and plated wire and core memory systems. A separate V_{CC} terminal is provided to allow level conversion to any voltage from 3 volts to V_{DD}.

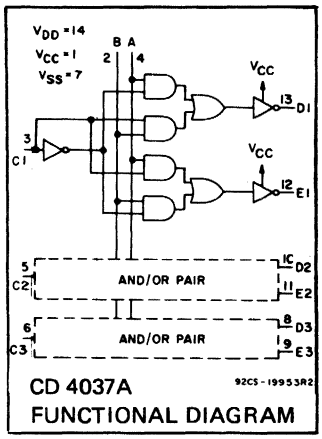
The CD4037A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TRUTH TABLE

INPUT		OUTPUT	
A	B	D	E
0	0	1	1
1	0	C	$\overline{C}$
0	1	$\overline{C}$	C
1	1	0	0

Fig. 1 – Logic diagram and truth table.



RECOMMENDED OPERATING CONDITIONS. For maximum reliability, nominal operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E, Y PACKAGES		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

CAUTION: V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V_{DD}

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E, Y PACKAGES			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: A and B Inputs t_{PHL}, t_{PLH}	5	–	225	450	–	325	650	ns
	10	–	75	150	–	100	200	
C Inputs t_{PHL}	5	–	250	500	–	350	700	ns
	10	–	75	150	–	100	200	
t_{PLH}	5	–	225	450	–	325	650	
	10	–	90	180	–	125	250	
Transition Time: High-to-Low Level, t_{THL}	5	–	40	80	–	60	120	ns
	10	–	15	30	–	20	40	
Low-to-High Level, t_{TLH}	5	–	75	150	–	100	200	ns
	10	–	60	120	–	90	180	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

Features:

- **Outputs compatible with low-power TTL systems.**
- **High sink and source current (1.6 mA typ.) capability at $V_{DD} = V_{CC}$ = 10V and V_{DS} = 0.5 V.**
- **Microwatt quiescent power dissipation: P_D = 0.5 μW/ceramic pkg. (typ.), P_D = 2 μW/plastic pkg. (typ.) at V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Split-phase (Bi-Phase) communication systems.**
- **Disc, drum, and tape digital recording systems.**
- **Plated wire and core memory systems.**
- **High-to-low logic level converter.**

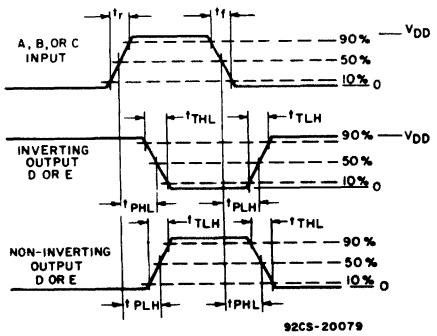


Fig.2 – Waveforms for measurement of dynamic characteristics.

CD4037A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . -55 to +125° C

PACKAGE TYPES E, Y . . . . . -40 to +85° C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60° C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85° C (PACKAGE TYPES E, Y) . . . Derate Linearly at 12 mW/° C to 200 mW

FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES D, F, K)Derate Linearly at 12 mW/° C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265° C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, K, F, H PACKAGES				E, Y PACKAGES				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.85	0.7	1.2	0.45	0.4	0.35	0.7	0.3	mA
	0.5	–	10	1.3	1.1	2	0.7	0.65	0.55	1.1	0.45	
P-Channel (Source): I_DP Min.	4.5	–	5	-0.65	-0.55	-1	-0.35	-0.35	-0.3	-0.55	-0.2	
	9.5	–	10	-0.9	-0.75	-1.6	-0.45	-0.5	-0.4	-0.75	-0.3	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

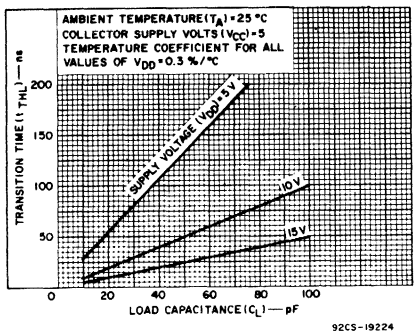


Fig.3 – Typical transition time vs. load capacitance.

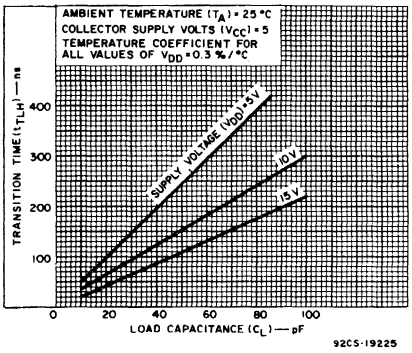


Fig.4 – Typical transition time vs. load capacitance.

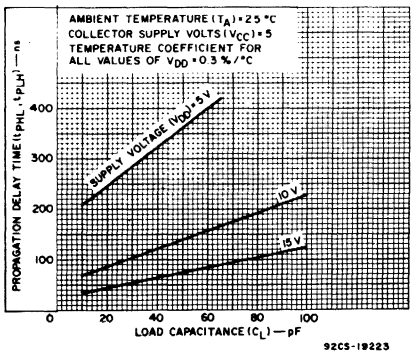


Fig.5 – Typical propagation delay time vs. load capacitance.

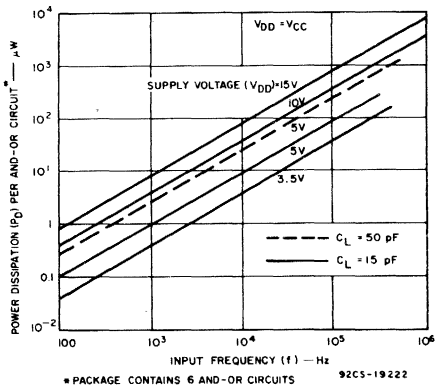


Fig.6 – Typical dissipation characteristics.

CD4040A Types

COS/MOS 12-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

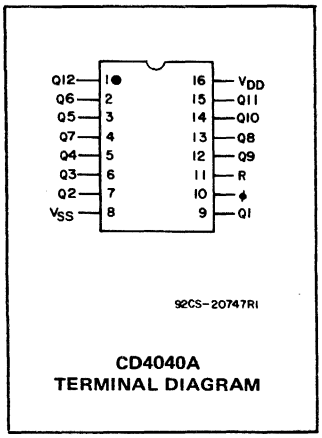
The CD4040A-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation . . . 5 MHz (typ.) input pulse rate at $V_{DD} - V_{SS} = 10$ V
- Low output impedance . . . 750 Ω (typ.) at $V_{DD} - V_{SS} = 10$ V and $V_{DS} = 0.5$ V
- Common reset
- Fully static operation
- All 12 buffered outputs available
- Low-power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Control counters



CD4040A
TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITONS at $T_A = 25^oC$, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges :

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		E,Y Packages		
		Min.	Max.	Min.	Max.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Frequency, f_ϕ	5	dc	1	dc	0.9	MHz
	10	dc	3.5	dc	3.25	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

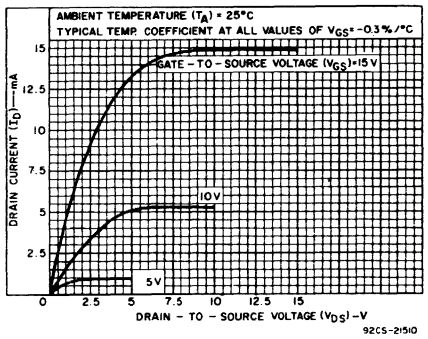


Fig.2 – Typical output n-channel drain characteristics.

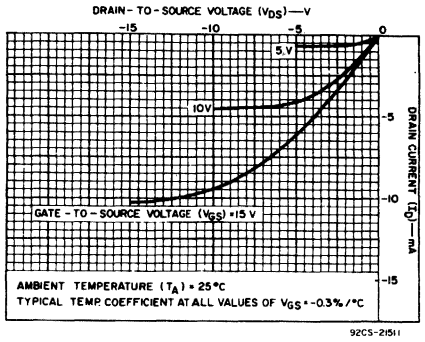


Fig.3 – Typical output p-channel drain characteristics.

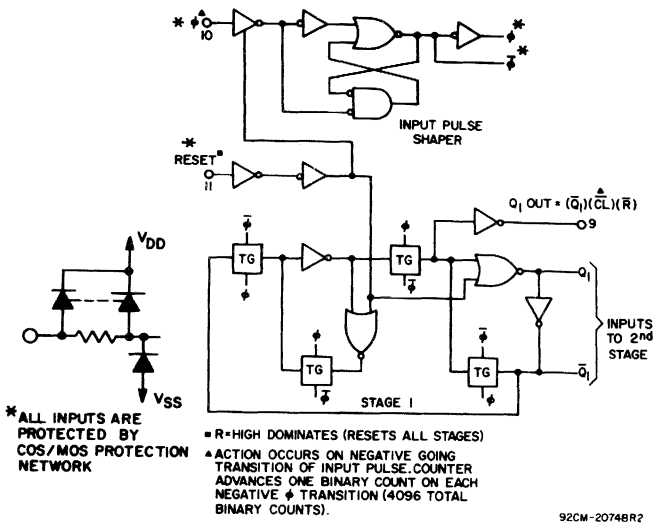


Fig.1 – Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

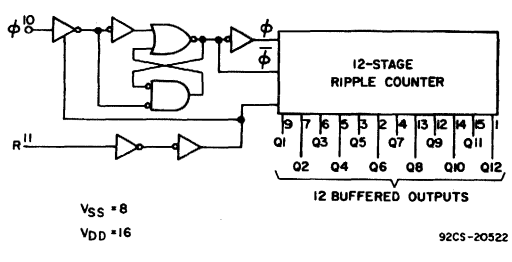


Fig.4 – Functional diagram.

CD4040A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

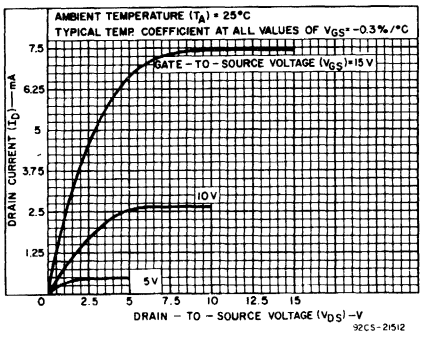


Fig.5 – Minimum output n-channel drain characteristics.

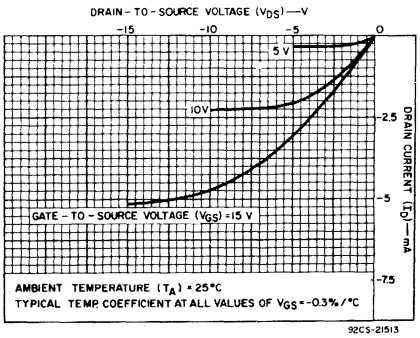


Fig.6 – Minimum output p-channel drain characteristics.

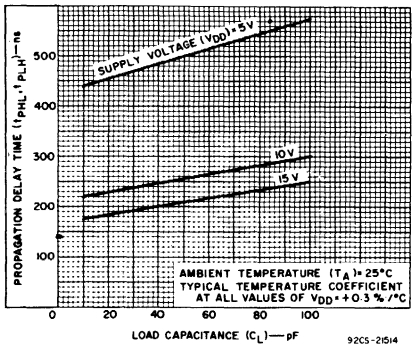


Fig.7 – Typical propagation delay time vs. load capacitance (per stage).

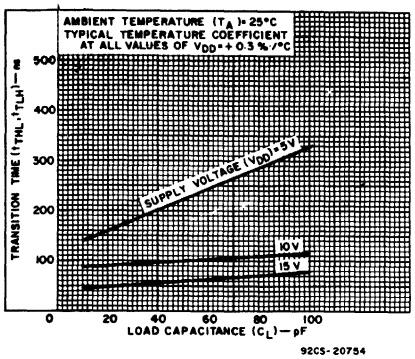


Fig.8 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink). I_DN Min.	0.5	–	5	0.22	0.36	0.145	0.102	0.21	0.36	0.08	0.056	mA
	0.5	–	10	0.44	0.75	0.4	0.250	0.42	0.75	0.2	0.14	
P-Channel (Source): I_DP Min.	4.5	–	5	−0.15	−0.25	−0.1	−0.07	−0.45	−0.25	−0.06	−0.04	
	9.5	–	10	−0.03	−0.5	−0.25	−0.175	−0.29	−0.5	−0.15	−0.1	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4040A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions		LIMITS						Units
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation									
Propagation Delay Time, t_{PLH}, t_{PHL}●		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Maximum Input-Pulse Frequency, f_ϕ		5	1	1.75	–	0.9	1.75	–	MHz
		10	3.5	5	–	3.25	5	–	
Minimum Input-Pulse Width, t_W	f=100 kHZ	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$▲		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}*		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

● Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

▲ Maximum input rise or fall time for functional operation.

* Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

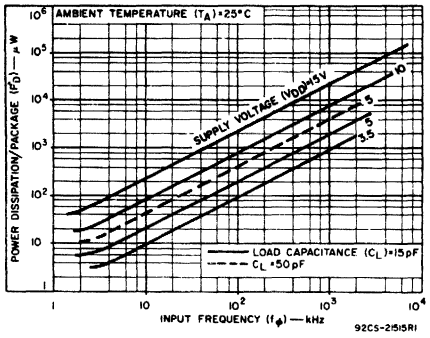


Fig. 9 – Typical dissipation characteristics.

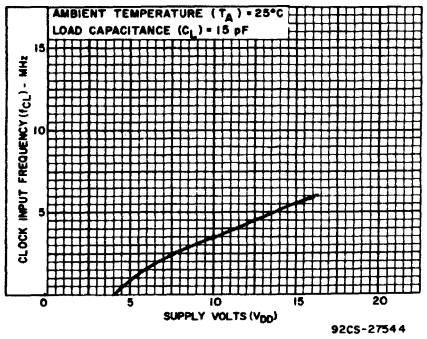


Fig.10 – Typical input-pulse frequency vs. supply voltage.

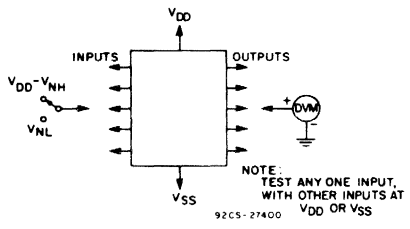


Fig.11 – Noise-immunity test circuit.

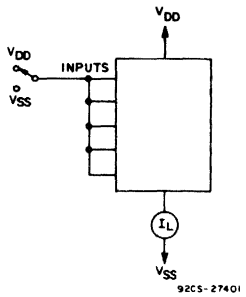


Fig.12 – Quiescent-device-current test circuit.

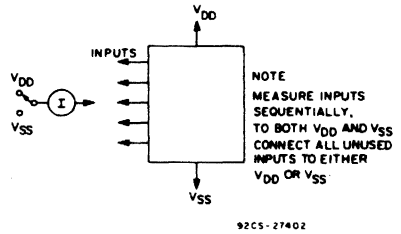


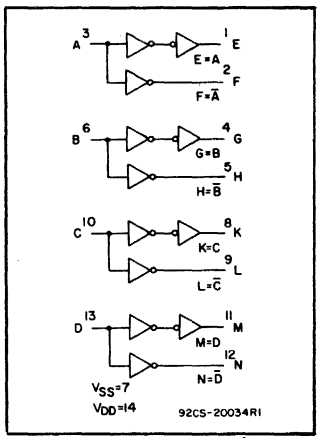
Fig.13 – Input-leakage-current test circuit.

CD4041A Types

COS/MOS Quad True/Complement Buffer

The RCA-CD4041A types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041A is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

The CD4041A types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4041A
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	12	V

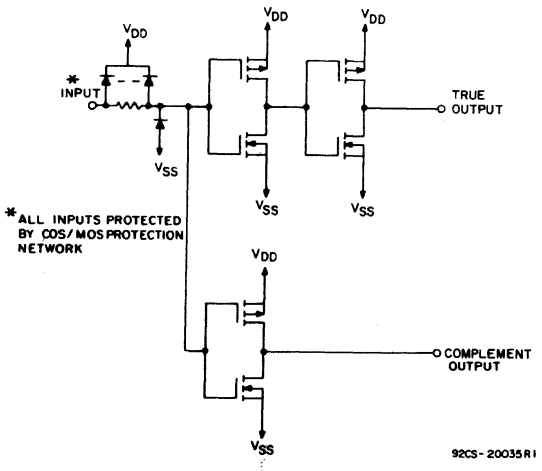


Fig. 1 – CD4041A schematic diagram.

Features:

True Output

- **High current source and sink capability**
  8 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  3.2 mA (typ.) @ V_{DS} = 0.4 V, V_{DD} = 5 V
  (two TTL loads)

Complement Output

- **Medium current source and sink capability**
  3.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V
  1.6 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 5 V
- **Quiescent current specified to 15 V**
- **Maximum input peakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package temperature range)**

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

CD4041A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0.5	5	0 Typ.; 0.05 Max.								V
	–	0.10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0.5	5	4.95 Min.; 5 Typ.								
	–	0.10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	True	5	2.1	3.2	1.6	1.2	1	3.2	0.8	0.7	mA
	0.5		10	6.25	10	5	3.5	3	10	2.5	2.2	
	0.5	Comp.	5	1	1.6	0.8	0.55	0.5	1.6	0.4	0.35	
	0.5		10	2.5	4	2	1.4	1.2	4	1	0.9	
P-Channel (Source) I_{DP} Min.	4.5	True	5	−1.75	−2.8	−1.4	−1	−0.85	−2.8	−0.7	−0.6	
	9.5		10	−5	−8	−4	−2.8	−2.4	−8	−2	−1.8	
	4.5	Comp.	5	−0.75	−1.2	−0.6	−0.4	−0.35	−1.2	−0.3	−0.27	
	9.5		10	−2.25	−3.6	−1.8	−1.25	−1.1	−3.6	−0.9	−0.8	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								μA

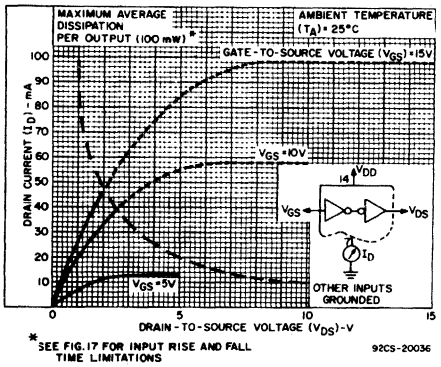


Fig.2 – Typical output n-channel drain characteristics – true output.

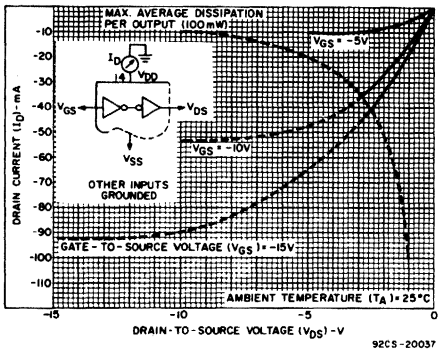


Fig.3 – Typical output p-channel drain characteristics – true output.

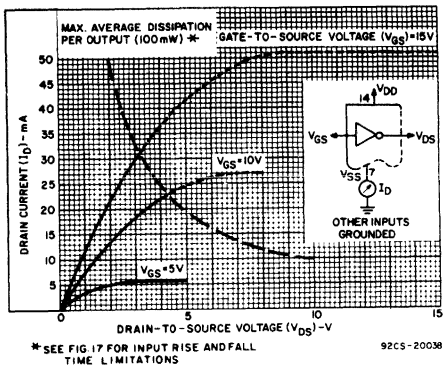


Fig.4 – Typical output n-channel drain characteristics – complement output.

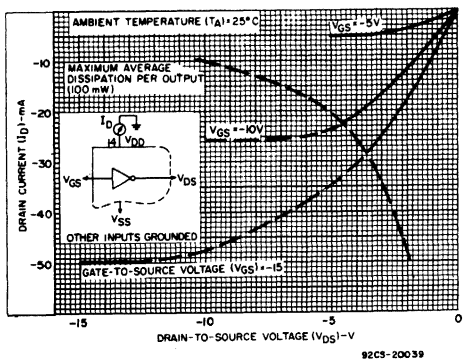


Fig.5 – Typical output p-channel drain characteristics – complement output.

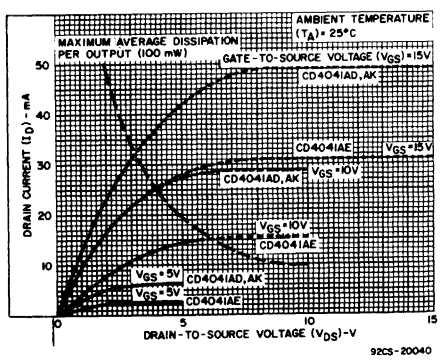


Fig.6 – Minimum output n-channel drain characteristics – true output.

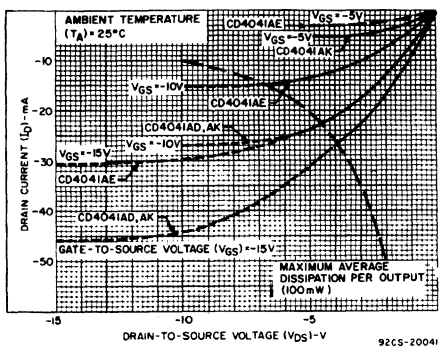


Fig.7 – Minimum output p-channel drain characteristics – true output.

CD4041A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (Volts)	LIMITS D,F,K,H Packages TYP.	LIMITS D,F,K,H Packages MAX.	LIMITS E,Y Packages TYP.	LIMITS E,Y Packages MAX.	UNITS
Propagation Delay Time: High-to-Low Level t_{PHL}	True Output	5	65	115	65	140	ns
		10	40	75	40	100	
	Comp. Output	5	55	100	55	125	ns
		10	30	45	30	65	
Low-to-High Level t_{PLH}	True Output	5	75	125	75	150	ns
		10	45	75	45	100	
	Comp. Output	5	45	100	45	125	ns
		10	25	40	25	60	
Transition Time: High-to-Low Level t_{THL}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	40	60	40	80	ns
		10	25	40	25	50	
Low-to-High Level t_{TLH}	True Output	5	20	40	20	60	ns
		10	13	25	13	40	
	Comp. Output	5	35	55	35	75	ns
		10	25	40	25	50	
Input Capacitance C_I	Any Input		15	—	15	—	pF

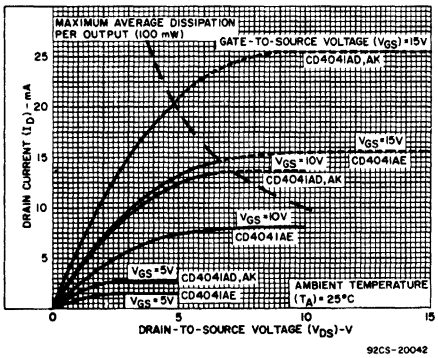


Fig.8 — Minimum output n-channel drain characteristics —complement output.

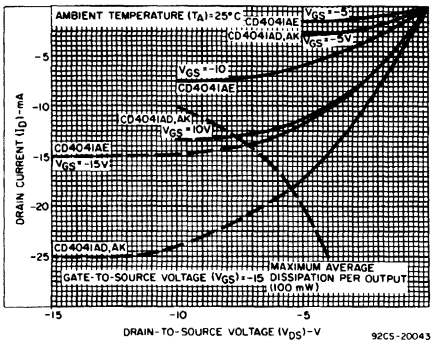


Fig.9 — Minimum output p-channel drain characteristics — complement output.

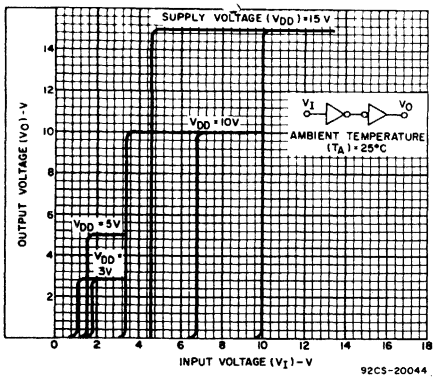


Fig.10 — Minimum and maximum transfer characteristics — true output.

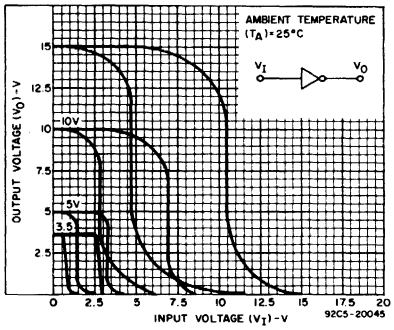


Fig.11 — Minimum and maximum transfer characteristics — complement output.

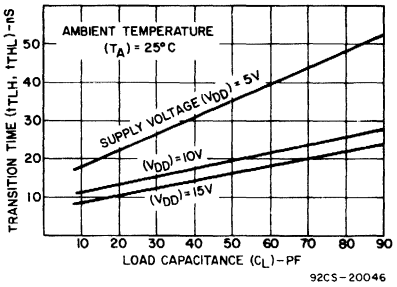


Fig.12 — Typical transition time vs. C_L — true output.

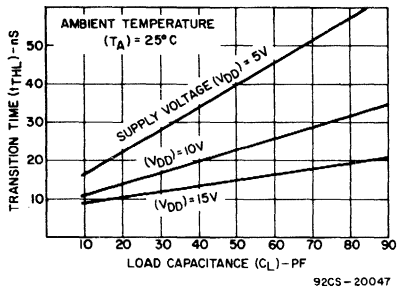


Fig.13 — Typical high-to-low level transition time vs. C_L — complement output.

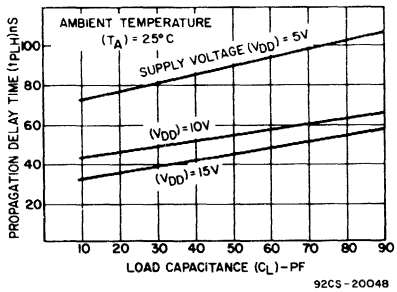


Fig.14 — Typical low-to-high level propagation delay time vs. C_L — true output.

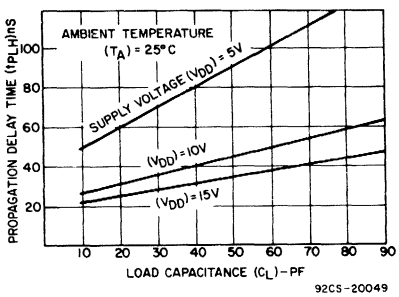


Fig.15 — Typical low-to-high level propagation delay time vs. C_L — complement output.

CD4041A Types

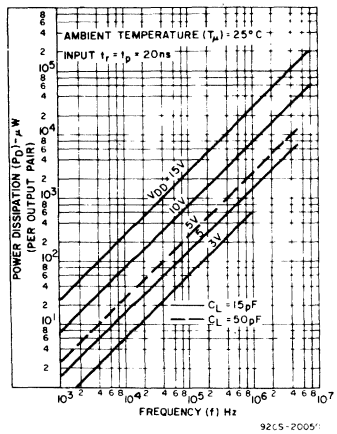


Fig.16 – Typical power dissipation vs. frequency per output pair.

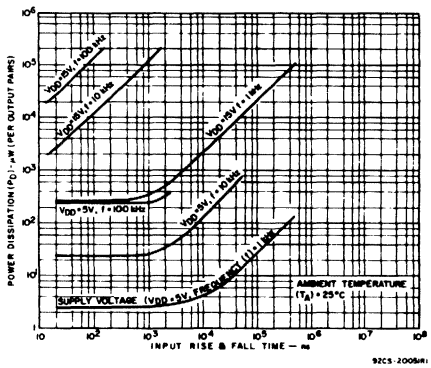


Fig.17 – Typical power dissipation vs. input rise & fall time per output pair.

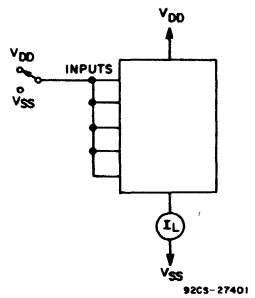


Fig.18 – Quiescent device current test circuit.

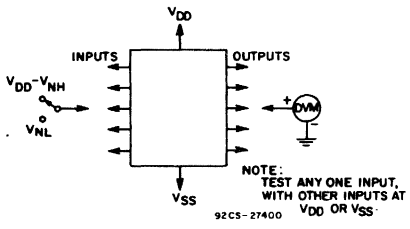


Fig.19 – Noise immunity test circuit.

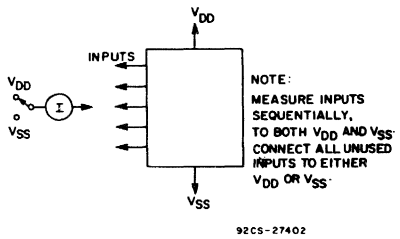


Fig.20 – Input leakage current test circuit.

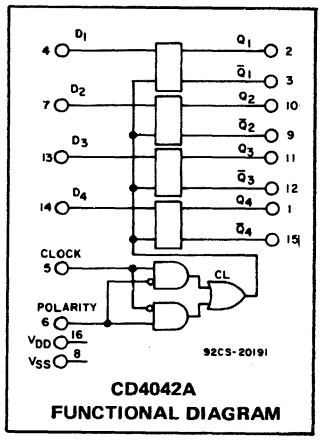
CD4042A Types

COS/MOS Quad Clocked "D" Latch

The RCA-CD4042A types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4042A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E,Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 KΩ

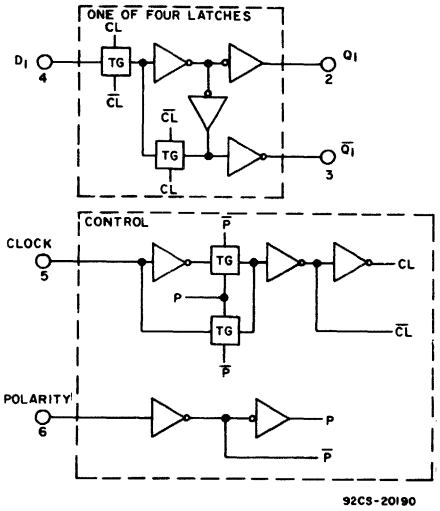
CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	150	300	150	400	ns
	10	75	150	75	200	
Data In to $\overline{Q}$	5	250	500	250	600	ns
	10	100	200	100	250	
Clock to Q	5	300	600	300	750	ns
	10	125	250	125	300	
Clock to $\overline{Q}$	5	400	800	400	1000	ns
	10	175	350	175	400	
Transition Time: t_{THL}, t_{TLH}	5	100	200	100	300	ns
	10	50	100	50	150	
Minimum Clock Pulse Width, t_W	5	175	250	175	350	ns
	10	60	120	60	175	
Minimum Hold Time, t_H	5	150	300	150	350	ns
	10	60	120	60	150	
Minimum Setup Time, t_S	5	0	50	0	50	ns
	10	0	30	0	30	
Minimum Clock Rise or Fall Time: t_r, t_f	5	Not rise or fall time sensitive.				μs
	10					
Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

Features:

- **Clock polarity control**
- **Q and $\overline{Q}$ outputs**
- **Common clock**
- **Low power TTL compatible**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Buffer storage**
- **Holding register**
- **General digital logic**



CLOCK	POLARITY	Q
0	0	D
↗	0	LATCH
1	1	D
↘	1	LATCH

Fig. 1 – Logic block diagram & truth table.

CD4042A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	12	3	12	V
Clock Pulse Width, t_W	5	350	–	250	–	ns
	10	175	–	120	–	
Setup Time, t_S	5	50	–	50	–	ns
	10	30	–	30	–	
Hold Time, t_H	5	350	–	300	–	ns
	10	150	–	120	–	
Clock Rise or Fall Time: t_r, t_f	5 10	Not rise or fall time sensitive.				μs

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E,Y Packages*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_{DN} Min.	0.5	–	5	0.5	1	0.4	0.27	0.24	1	0.2	0.18	mA
	0.5	–	10	1.25	2	1	0.7	0.6	2	0.5	0.45	
p-Channel (Source), I_{DP} Min.	4.5	–	5	-0.45	-1	-0.35	-0.25	-0.2	-1	-0.175	-0.15	
	9.5	–	10	-1.15	-2	-0.9	-0.6	-0.34	-2	-0.45	-0.4	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ.; 1 Max.								μA

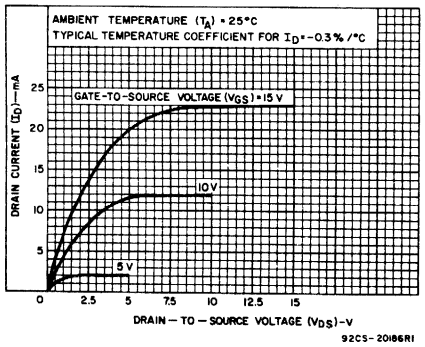


Fig. 2 – Typical output n-channel drain characteristics.

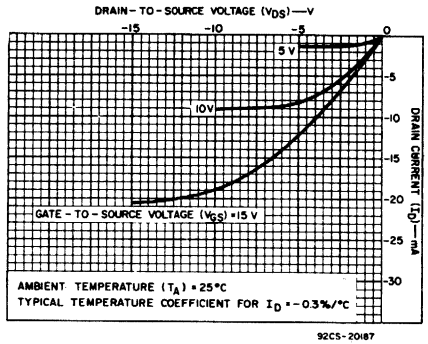


Fig. 3 – Typical output p-channel drain characteristics.

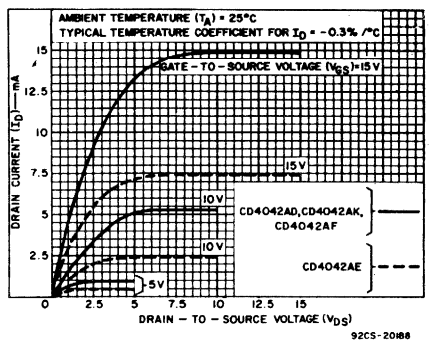


Fig. 4 – Minimum n-channel drain characteristics.

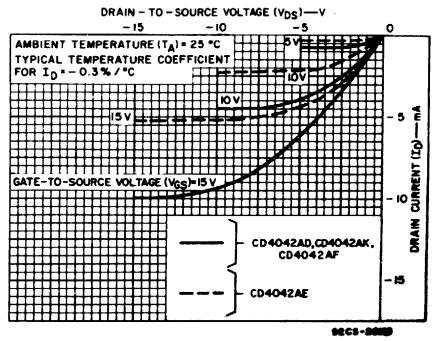
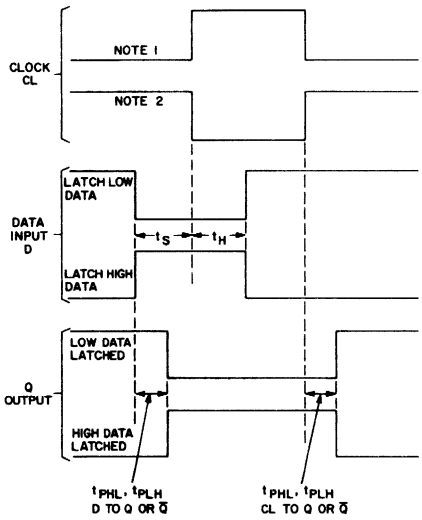


Fig. 5 – Minimum p-channel drain characteristics.

CD4042A Types



NOTES:
1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

Fig. 6 – Dynamic test parameters.

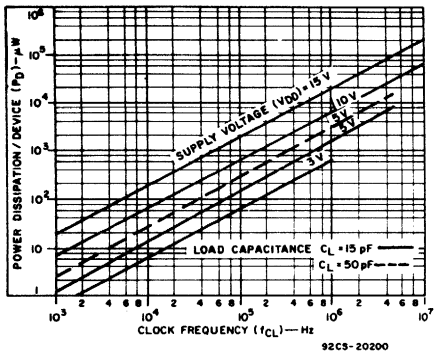


Fig. 11 – Typical dissipation characteristics.

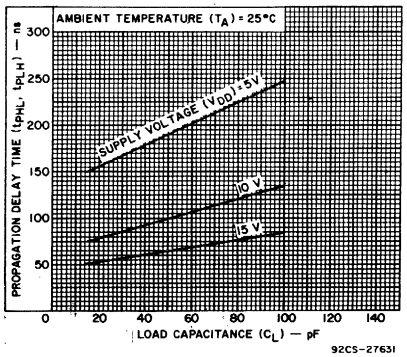


Fig. 7 – Typical propagation delay time vs. load capacitance– data to Q.

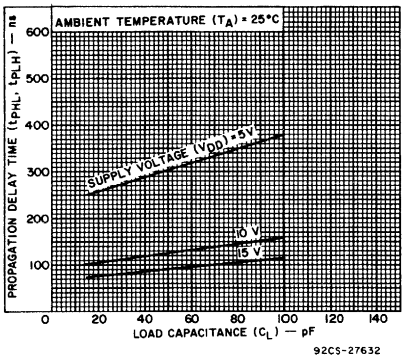


Fig. 8 – Typical propagation delay time vs. load capacitance – data to $\overline{Q}$.

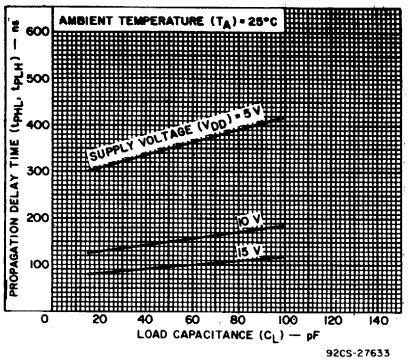


Fig. 9 – Typical propagation delay time vs. load capacitance – clock to Q.

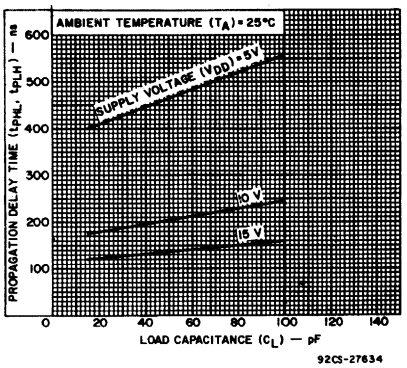


Fig. 10 – Typical propagation delay time vs. load capacitance – clock to $\overline{Q}$.

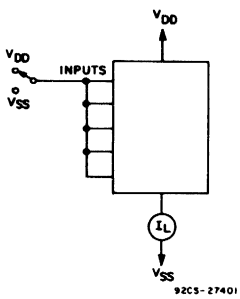


Fig. 12 – Quiescent device current test circuit.

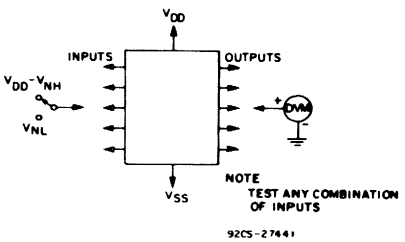


Fig. 13– Noise immunity test circuit.

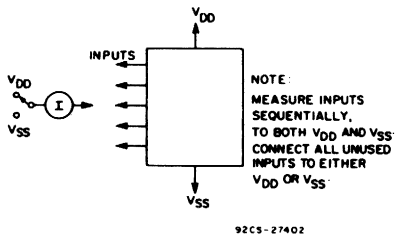


Fig. 14 – Input leakage current test circuit.

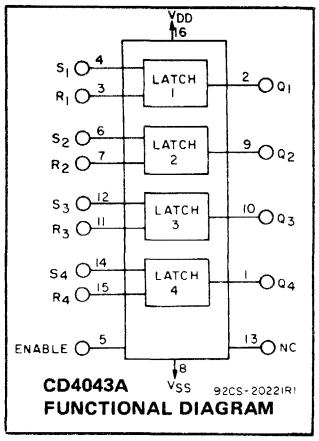
CD4043A, CD4044A Types

COS/MOS Quad 3-State R/S Latches

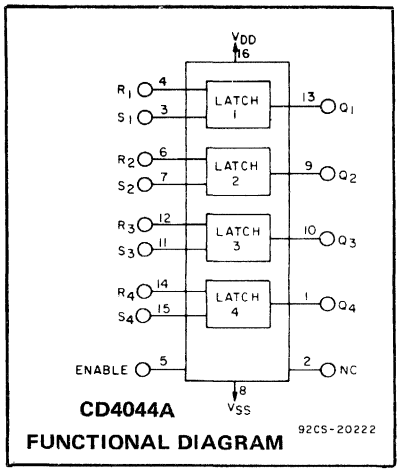
Quad NOR R/S Latch – CD4043A
Quad NAND R/S Latch – CD4044A

The RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044A types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table shown in Fig. 1.

The CD4043A and CD4044A types are supply in 16-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4043A
FUNCTIONAL DIAGRAM



CD4044A
FUNCTIONAL DIAGRAM

Applications:

- Holding register in multi-register system
- Four bits of independent storage with output ENABLE
- Strobed register
- General digital logic

Features:

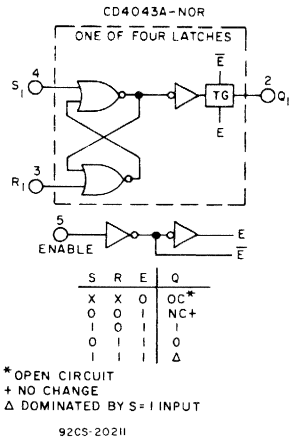
- 3-Level outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
  PACKAGE TYPES E,Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range	–	3	12	3	12	V
Set or Reset Pulse Width, t_W	5	200	–	225	–	ns
	10	100	–	110	–	



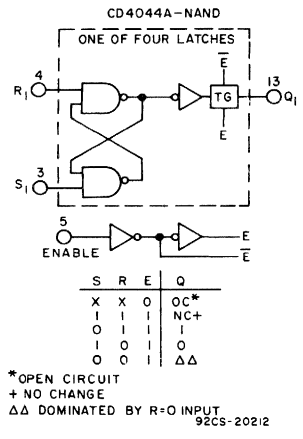


Fig. 1 — Logic diagrams and truth tables.

CD4043A, CD4044A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.005	2	120	20	0.02	20	280	
	–	–	15	25	0.25	25	1000	250	2.5	250	2500	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0 Typ.; 0.05 Max.								V
	–	0,10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	–	0,5	5	4.95 Min.; 5 Typ.								
	–	0,10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.;								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink), I_DN Min.	0.5	–	5	0.25	0.5	0.2	0.19	0.12	0.5	0.1	0.09	mA
	0.5	–	10	0.61	1	0.5	0.35	0.3	1	0.25	0.22	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.22	-0.5	-0.175	-0.12	-0.11	-0.5	-0.09	-0.08	
	9.5	–	10	-0.5	-1	-0.4	-0.28	-0.24	-1	-0.2	-0.18	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,K,H Packages Typ.	LIMITS D,F,K,H Packages Max.	LIMITS E,Y Packages Typ.	LIMITS E,Y Packages Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	175	350	175	400	ns
	10	75	175	75	200	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	100	200	100	200	ns
	10	50	100	50	100	
t_{PLZ}, t_{PZL}	5	80	160	80	160	ns
	10	40	80	40	80	
Transition Time: t_{THL}, t_{PLH}	5	100	200	100	250	ns
	10	50	100	50	125	
Minimum SET or RESET Pulse Width, t_W	5	80	200	80	225	ns
	10	40	100	40	110	
Average Input Capacitance, C_I (Any Input)	–	5	–	5	–	pF

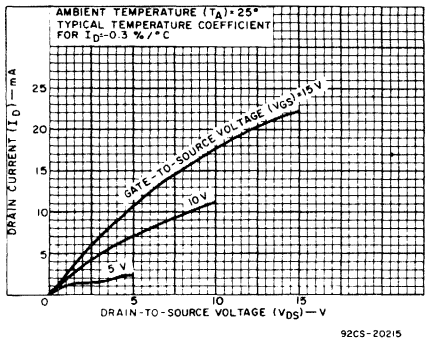


Fig. 2 — Typical output n-channel drain characteristics.

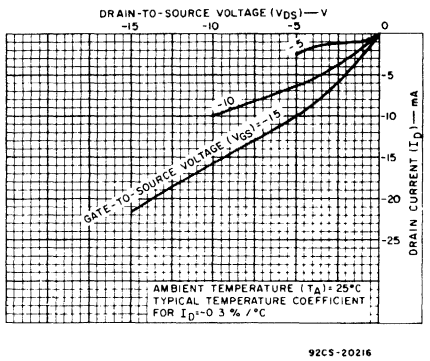


Fig. 3 — Typical output p-channel drain characteristics.

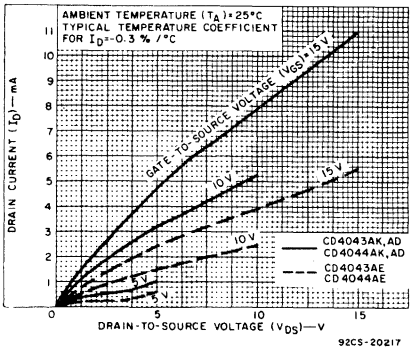


Fig. 4 — Minimum n-channel drain characteristics.

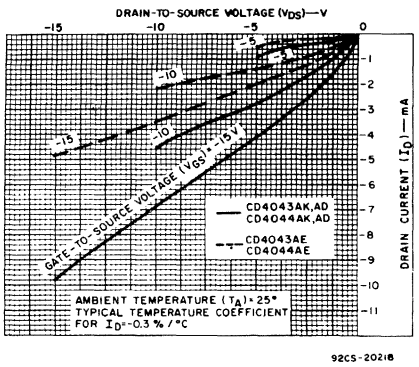


Fig. 5 — Minimum p-channel drain characteristics.

CD4043A, CD4044A Types

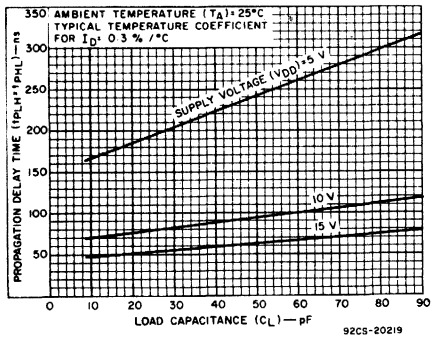


Fig. 6 — Typical propagation delay time vs. C_L.

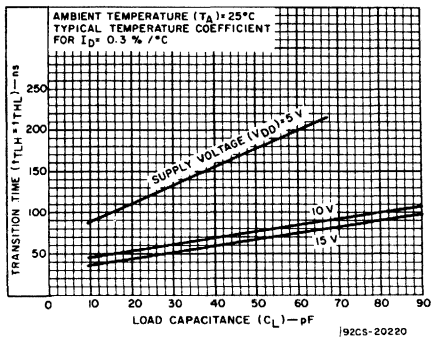


Fig. 7 — Typical transition time vs. C_L.

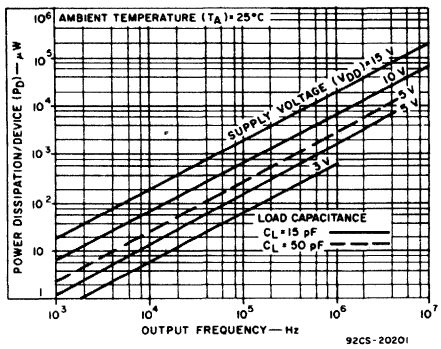


Fig. 8 — Typical dissipation characteristics.

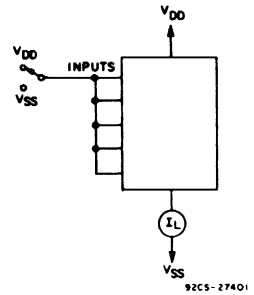


Fig. 9 — Quiescent device current test circuit.

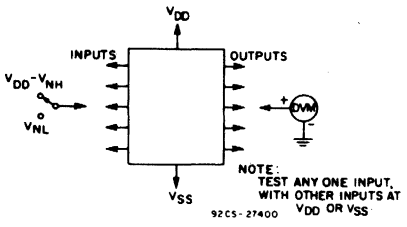


Fig. 10 — Noise immunity test circuit.

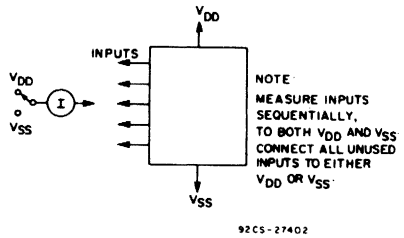


Fig. 11 — Input leakage current test circuit.

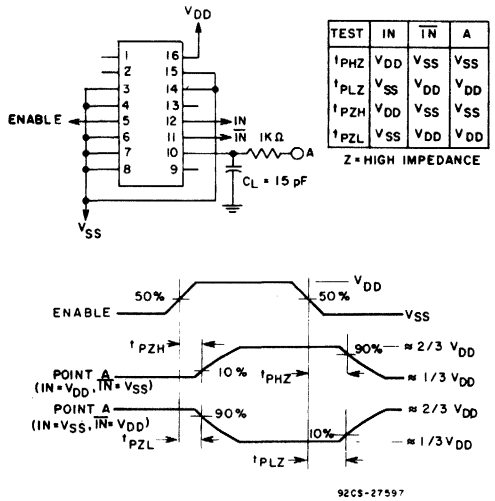


Fig. 12 — ENABLE propagation delay time test circuit and waveforms.

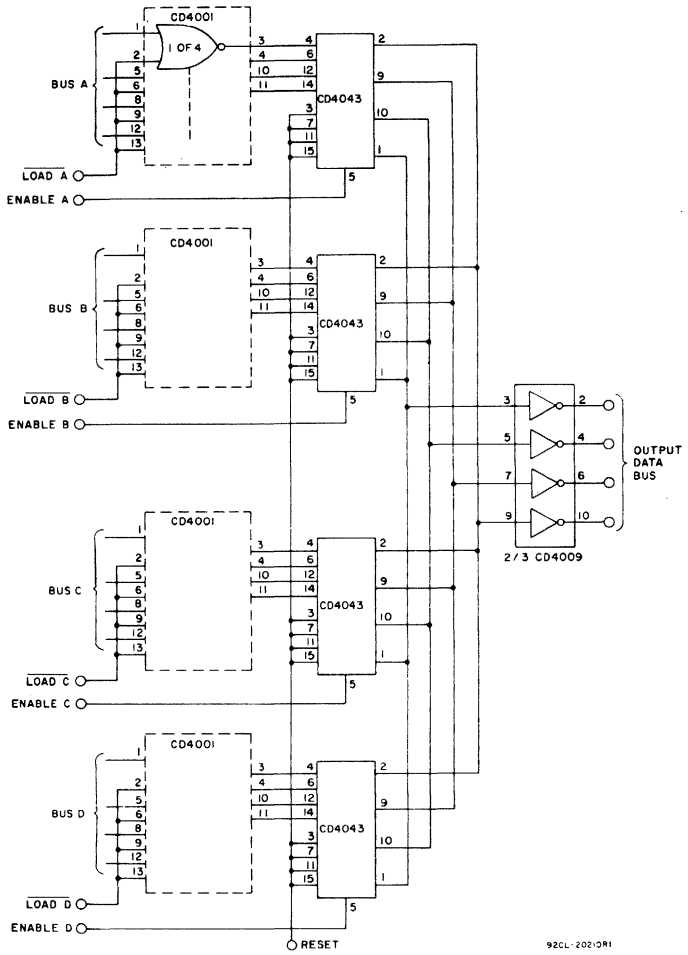


Fig. 14 — Multiple bus storage.

APPLICATIONS

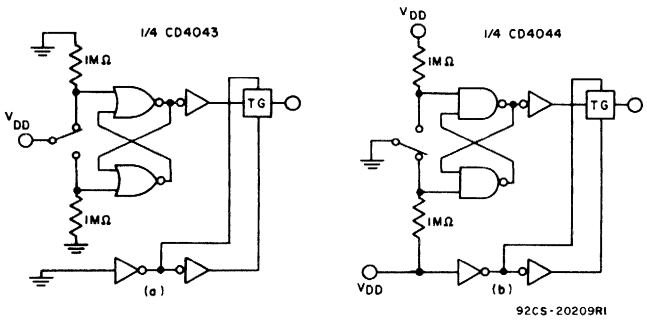


Fig. 13 — Switch bounce eliminator.

CD4045A Types

COS/MOS 21-Stage Counter

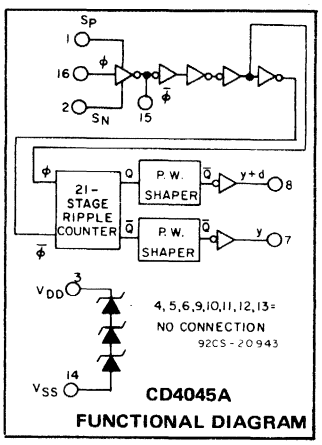
The RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 3.

The CD4045A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**



CD4045A
FUNCTIONAL DIAGRAM

Features:

- **Microwatt quiescent dissipation . . . . . 2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V**
- **Very low operating dissipation . . . . . 1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink) 5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)**
- **Medium speed (typ.) . . . . . fϕ = 5 MHz @ V_{DD} = 5 V fϕ = 10 MHz @ V_{DD} = 10 V**
- **16.5 V zener diode transient protection on chip for automotive use**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPES E, Y . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W	5	115	–	140	–	ns
	10	60	–	75	–	
Input-Pulse Frequency, fϕ	5	dc	4.4	dc	3.5	MHz
	10	dc	8.5	dc	6.5	
Input-Pulse Rise or Fall Time, $t_r\phi$, $t_f\phi$	5	–	15	–	15	μs
	10	–	10	–	10	

NOTE 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for $V_{DD} > 13$ V.

NOTE 2: Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

CD4045A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: ϕ to y or y+d out t_{PLH}, t_{PHL}		5	–	2.2	4.4	–	2.2	5.5	μs
		10	–	1.2	2.4	–	1.2	3.3	
Transition Time: t_{THL}, t_{TLH}		5	–	450	800	–	450	900	ns
		10	–	375	650	–	375	750	
Maximum Input-Pulse Frequency, $f_{m\phi}$		5	4.4	5	–	3.5	5	–	MHz
		10	8.5	10	–	6.5	10	–	
Minimum Input-Pulse Width, t_W		5	–	100	115	–	100	140	ns
		10	–	50	60	–	50	75	
Input-Pulse Rise & Fall Time; $t_r\phi$, $t_f\phi$		5	–	–	15	–	–	15	μs
		10	–	–	10	–	–	10	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

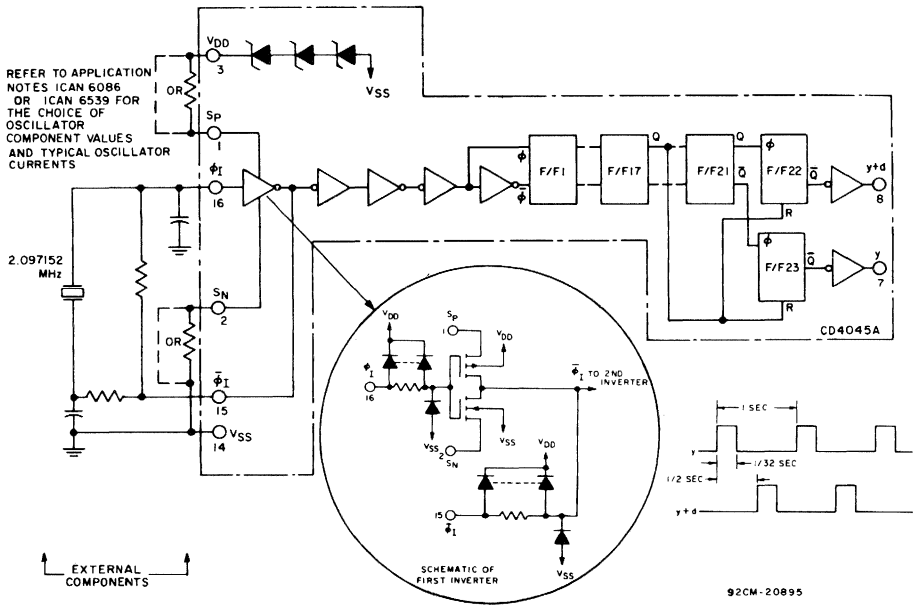


Fig. 3 – CD4045A and outboard components in a typical 21-stage counter application.

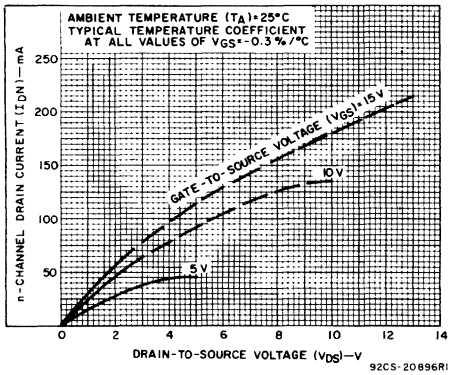


Fig. 1 – Typical output n-channel drain characteristics.

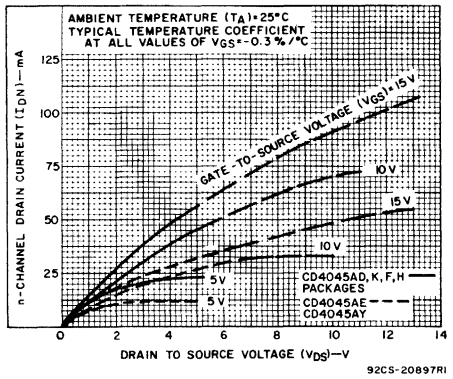


Fig. 2 – Minimum output n-channel drain characteristcs.

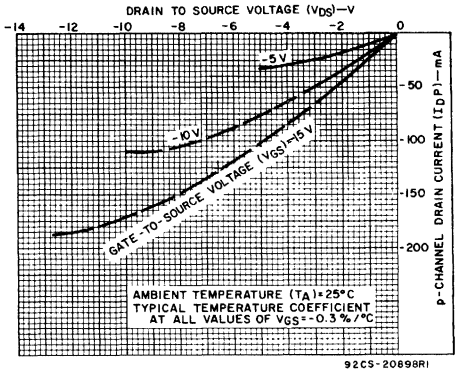


Fig. 4 – Typical output p-channel drain characteristics.

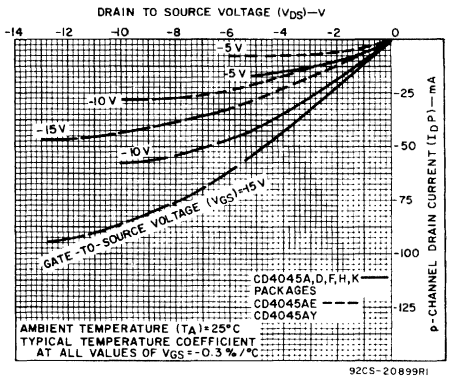


Fig. 5 – Minimum output p-channel drain characteristics.

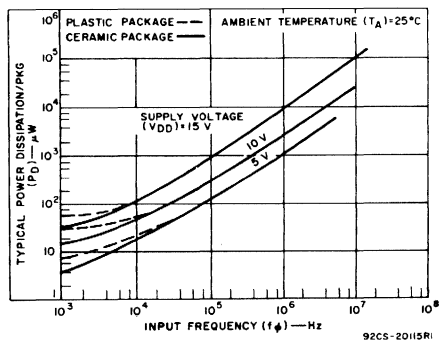


Fig. 6 – Typical dissipation vs input frequency (21 counting stages).

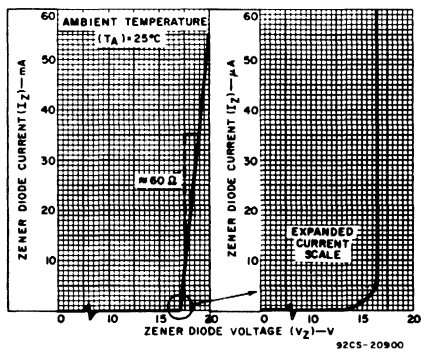


Fig. 7 – Typical zener diode characteristics.

CD4045A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.5	–	5	4.4	7	3.5	2.5	2.2	7	1.8	1.3	mA
	0.5	–	10	6.9	11	5.5	3.9	3.5	11	2.8	2	
p-Channel (Source): I_DP Min.	4.5	–	5	−3.1	−5	−2.5	−1.8	−1.6	−5	−1.3	−0.9	
	9.5	–	10	−5.6	−9	−4.5	−3.2	−2.8	−9	−2.3	−1.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA
Zener Breakdown Voltage, $V_{(BR)Z}$	1–100 μA		Min.	13.3	–	13.5	13.7	13.3	–	13.5	13.6	V
			Typ.	–	16.5	–	–	–	16.5	–	–	
			Max.	17.8	–	18	18.2	17.8	–	18	18.1	

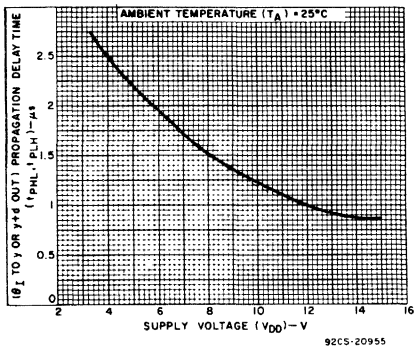


Fig. 8 – Typical propagation delay (ϕ_1 to y or y+d out) vs V_{DD}.

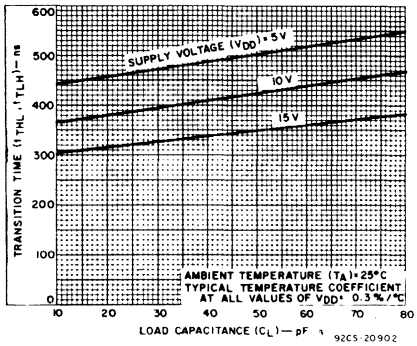


Fig. 9 – Typical transition time vs C_L.

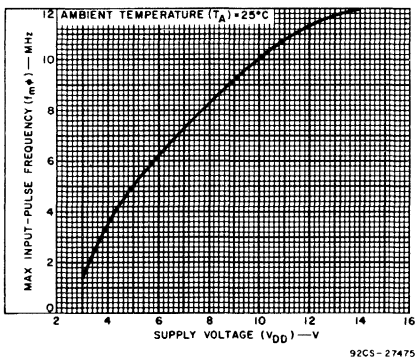


Fig. 10 – Typical maximum input-pulse frequency.

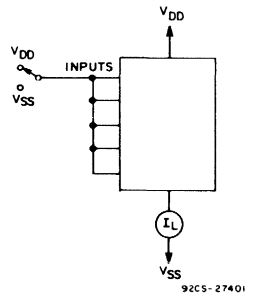


Fig. 11 – Quiescent-device-current test circuit.

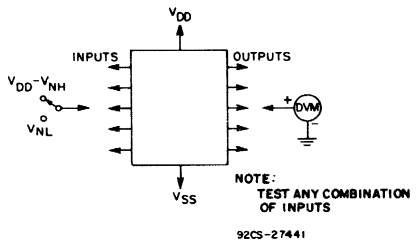


Fig. 12 – Noise-immunity test circuit.

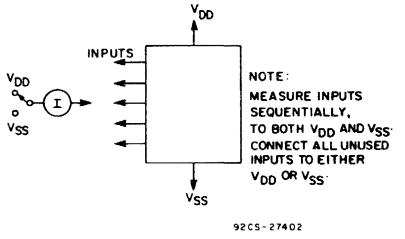


Fig. 13 – Input-leakage-current test circuit.

CD4046A Types

COS/MOS Micropower Phase-Locked Loop

The RCA-CD4046A COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary. The CD4046A is supplied in a 16-lead dual-in-line ceramic package (CD4046AD), a 16-lead dual-in-line plastic package (CD4046AE), and a 16-lead flat pack (CD4046AK). It is also available in chip form (CD4046AH).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" ≤30% ($V_{DD}-V_{SS}$), logic "1" ≥ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic

Features:

- **Very low power consumption: 70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.2 MHz (typ.) at V_{DD} = 10 V**
- **Wide supply-voltage range: $V_{DD} - V_{SS}$ = 5 to 15 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**

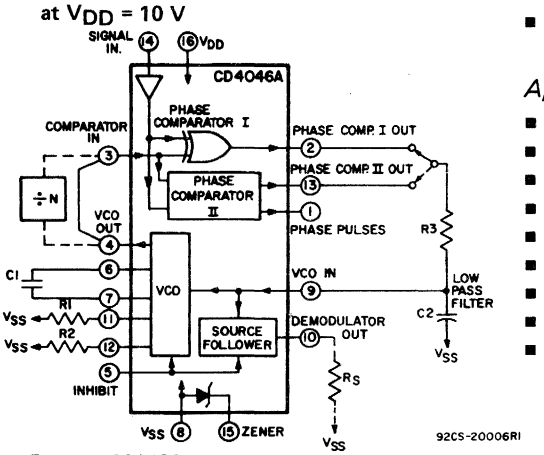


Fig. 1 – COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range	3	12	V

CD4046A Types

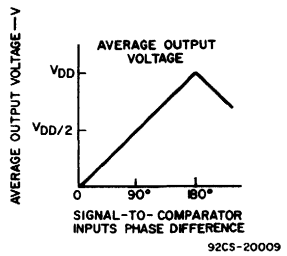


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

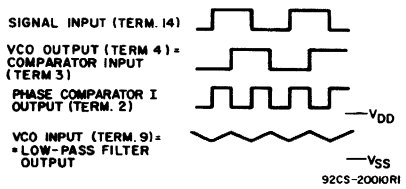


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits All Package Types D,E,F,H,K,Y Min.	Typ.	Max.	Units
Phase Comparator Section							
Operating Supply Voltage, $V_{DD}-V_{SS}$	VCO Operation		–	5	–	15	V
	Comparators only		–	3	–	15	
Total Quiescent Device Current, I_L: Term. 14 Open	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	55	μA
			10	–	200	410	
Term. 14 at V_{SS} or V_{DD}			5	–	5	15	
			10	–	25	60	
			15	–	50	500	
Term. 14 (SIGNAL IN) Input Impedance, Z_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	400	mV
			10	–	400	800	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	–	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.5	–	
	Phase Pulses	0.5	5	0.23	0.47	–	
		0.5	10	0.7	1.4	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II Term. 2 & 13	4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
	Phase Pulses	4.5	5	–0.08	–0.16	–	
		9.5	10	–0.25	–0.5	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	–	$\pm 10^{-5}$	±1	μA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

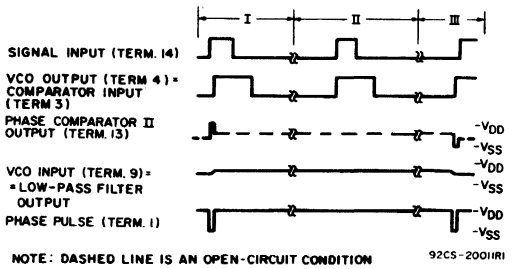


Fig.4 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

CD4046A Types

DESIGN INFORMATION

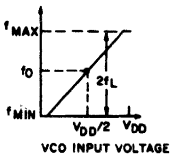
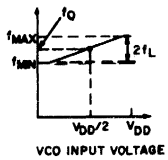
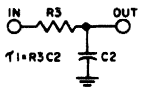
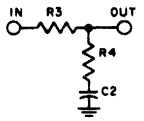
This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leq R1, R2, R_S \leq 1\ M\Omega$

$C1 \geq 100\ pF$ at $V_{DD} \geq 5\ V$;

$C1 \geq 50\ pF$ at $V_{DD} \geq 10\ V$

In addition to the given design information refer to Fig.5 for R1, R2, and C1 component selections.

Characteristics	Phase Comparator Used	Design Information
VCO Frequency	1	VCO WITHOUT OFFSET ($R_2 = \infty$):  VCO WITH OFFSET: 
	2	Same as for No.1
For No Signal Input	1	VCO will adjust to center frequency, f_0
	2	VCO will adjust to lowest operating frequency, f_{min}
Frequency Lock Range, $2f_L$	1	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$
	2	Same as for No.1
Frequency Capture Range, $2f_C$ Loop Filter Component Selection	1	 (1), (2) $2f_C \approx \frac{1}{\pi} \frac{2\pi f_L}{\tau 1}$  For $2f_C$, see Ref. (2)
	2	$f_C = f_L$
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_0) approximating 0° and 180° at ends of lock range ($2f_L$)
	2	Always 0° in lock

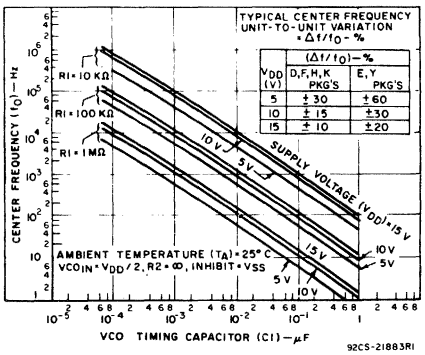


Fig.5(a) — Typical center frequency vs C1 for R1 = 10 kΩ, and 1 MΩ and $f_0 \sim 1/R1\ C1$.

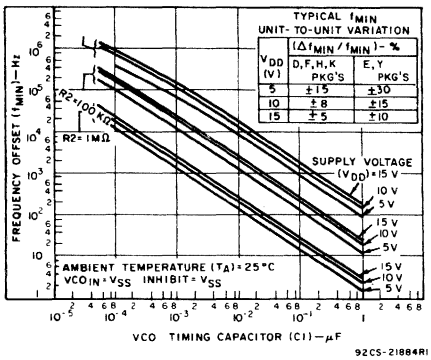


Fig.5(b) — Typical frequency offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ.

NOTE: Lower frequency values are obtainable if larger values of C1 than shown in Figs. 5(a) and 5(b) are used.

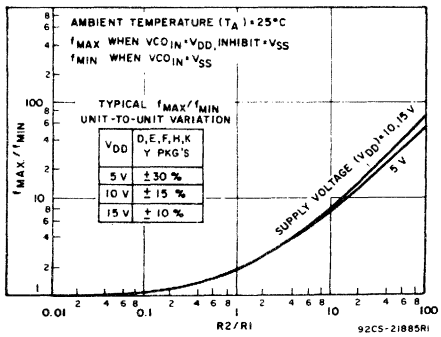


Fig.5(c) — Typical f_{max}/f_{min} vs R2/R1.

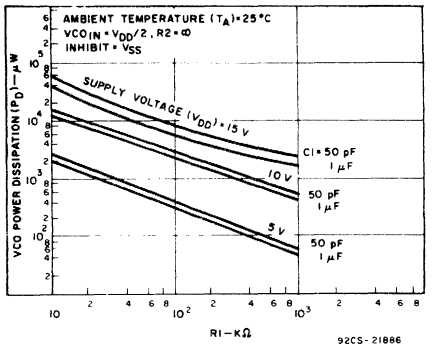


Fig.6(a) — Typical VCO power dissipation at center frequency vs R1.

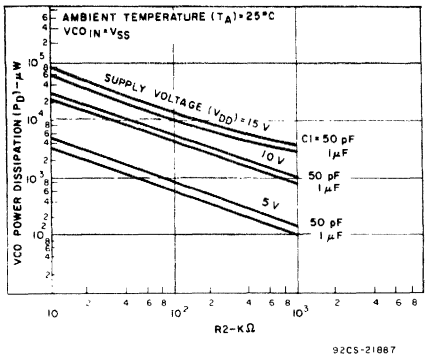


Fig.6(b) — Typical VCO power dissipation at f_{min} vs R2.

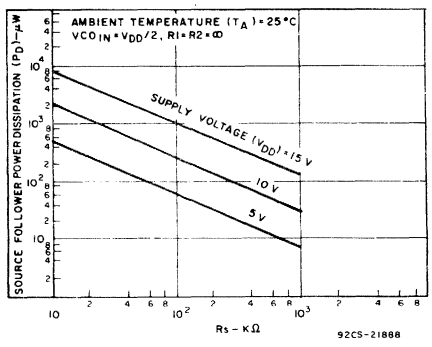


Fig.6(c) — Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S) — Phase Comparator I

P_D (Total) = P_D (f_{MIN}) — Phase Comparator II

CD4046A Types

DESIGN INFORMATION (Cont'd):

Characteristics	Phase Comparator Used	Design Information	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	
VCO Component Selection	1	**VCO WITHOUT OFFSET** $R_2 = \infty$ – Given: f_o – Use f_o with Fig.5a to determine R1 and C1	**VCO WITH OFFSET** – Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1
	2	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

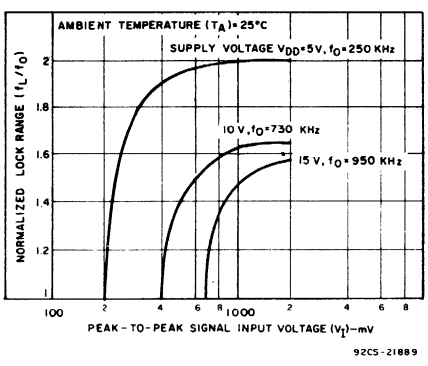
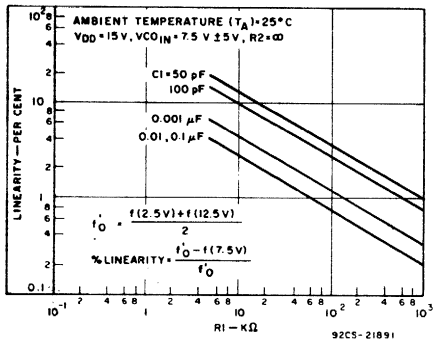


Fig.7 – Typical lock range vs signal input amplitude.



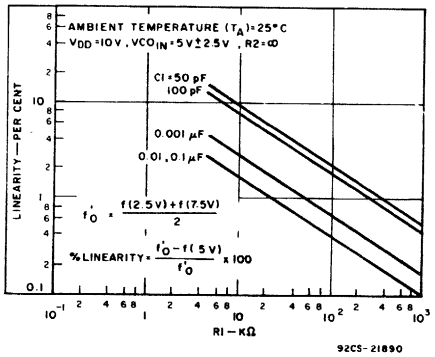


Fig.8(a) and (b) – Typical VCO linearity vs R1 and C1.

CD4046A Types

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits (All Package Types D,E,F,H,K,Y) Min.	Typ.	Max.	Units
VCO Section							
Operating Supply Voltage $V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V
	Phase-lock-loop operation			5	–	15	
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, $R_2 = \infty$, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	μW
			10	–	600	–	
			15	–	2400	–	
Maximum Operating Frequency, f_{max}	R1 = 10 kΩ, $R_2 = \infty$, $VCO_{IN} = V_{DD}$, C1 = 100 pF		5	0.25	0.5	–	MHz
	C1 = 50 pF		10	0.6	1.2	–	
			15	–	1.5	–	
Center Frequency (f_o) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ		5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–	
Temperature-Frequency Stability●: No Frequency Offset $f_{MIN} = 0$	$\%/^oC \propto \frac{1}{f \cdot V_{DD}}$, $R_2 = \infty$		5	–	0.12–0.24	–	%/°C
			10	–	0.04–0.08	–	
			15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	$\%/^oC \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–	
			10	–	0.05–0.1	–	
			15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I			5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving COS/MOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V
High Level, V_{OH}			5	4.99	–	–	
			10	9.99	–	–	
			15	14.99	–	–	
VCO Output Duty Cycle			5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}		V_O Volts	5	–	75	150	ns
			10	–	50	100	
			15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}		0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.6	–	
p-Channel (Source), I_{DP}		4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	R_S > 10 kΩ		5,10	–	1.5	2.2	V
			15	–	1.5	–	
Linearity	R_S>50kΩ, VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
	= 5±2.5 V		10	–	0.6	–	
	= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z): CD4046AD,AF,AK	I_Z = 50 μA			4.7	5.2	5.7	V
CD4046AE,AY				4.5	5.2	6.1	
Zener Dynamic Resistance, R_Z	I_Z = 1 mA			–	100	–	Ω

● Positive coefficient.

CD4047A Types

COS/MOS Low-Power Monostable/Astable Multivibrator

The RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

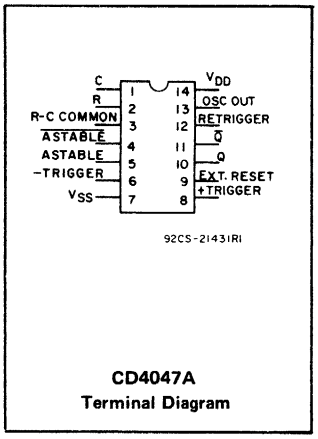
The CD4047A-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**



CD4047A
Terminal Diagram

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  Frequency deviation:
  =±2% + 0.03%/°C @ 100 kHz
  =±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications :

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**
- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**

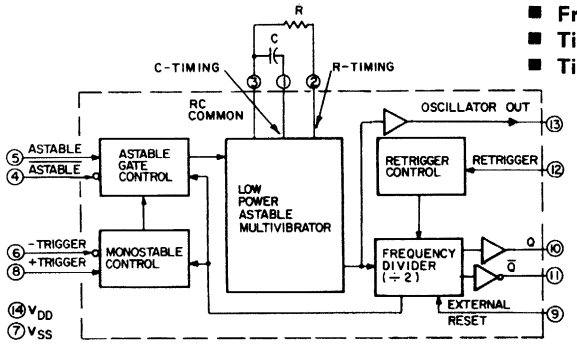


Fig. 1 – CD4047A logic block diagram. 92CS-20026R2

MAXIMUM RATINGS, ***Absolute-Maximum Values:***

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPES E, Y . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

CD4047A Types

RECOMMENDED OPERATING CONDITIONS at T_A= 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD}	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package- Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W (Any Input)	5 10	1000 400	– –	1300 600	– –	ns
Trigger, Retrigger Rise or Fall Time, t_r , t_f	5 10	– –	15 5	– –	15 5	μs

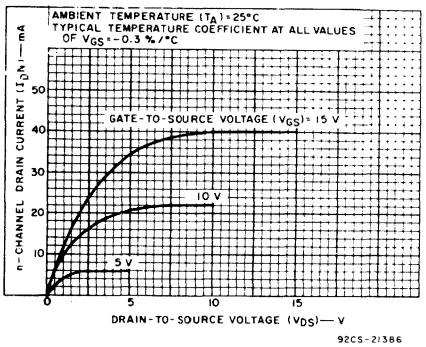


Fig. 2 – Typical output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

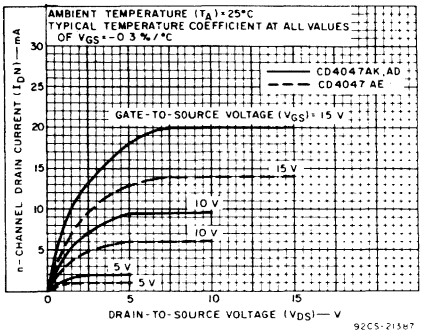


Fig. 3 – Minimum output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E,Y Packages*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	– 40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min., 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5		5	1 Min.								V
	9		10	1 Min.								
Inputs High, V_{NMH}	0.5		5	1 Min.								
	1		10	1 Min.								
Output Drive Current: (Q,$\overline{Q}$ Outputs) n-channel (Sink), I_{DN} Min.	0.5	–	5	0.5	0.8	0.4	0.28	0.34	0.8	0.28	0.23	mA
	0.5	–	10	1.25	2	1	0.7	0.85	2	0.7	0.6	
p-Channel (Source): I_{DP} Min.	4.5	–	5	-0.5	-0.8	-0.4	-0.28	-0.34	-0.8	-0.28	-0.23	
	9.5	–	10	-1.25	-2	-1	-0.7	-0.85	-2	-0.7	-0.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input			$\pm 10^{-5}$ Typ., ±1 Max.								μA
	–	–	15									

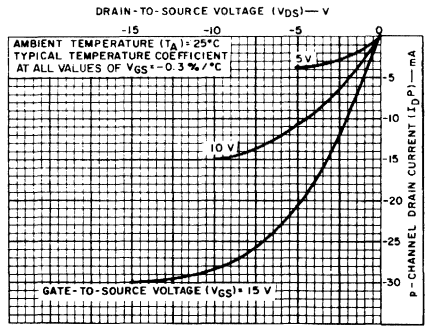


Fig. 4. – Typical output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

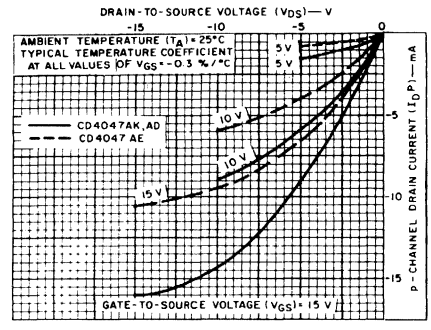


Fig. 5 – Minimum output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

CD4047A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTICS	TEST CONDITIONS	LIMITS							UNITS
			D,F,K,H Packages			E,Y Packages			
		V_{DD} (Volts)	Min.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} Astable, $\overline{\text{Astable}}$ to Osc. Out		5	–	200	400	–	200	550	ns
		10	–	100	200	–	100	275	
Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$		5	–	550	900	–	550	1200	
		10	–	250	500	–	250	650	
+Trigger, –Trigger to Q, $\overline{Q}$		5	–	700	1200	–	700	1600	
		10	–	300	600	–	300	800	
+Trigger, Retrigger to Q, $\overline{Q}$		5	–	300	600	–	300	800	
		10	–	175	300	–	175	400	
External Reset to Q, $\overline{Q}$		5	–	300	600	–	300	800	
		10	–	125	250	–	125	350	
Transition Time: t_{THL}, t_{TLH} Q, $\overline{Q}$		5	–	75	125	–	75	150	ns
		10	–	45	75	–	45	100	
Osc. Out		5	–	75	150	–	75	180	
		10	–	45	100	–	45	130	
Minimum Input Pulse Width (any input), t_W*		5	–	500	1000	–	500	1300	ns
		10	–	200	400	–	200	600	
+Trigger, Retrigger Rise & Fall Time, t_r, t_f		5	–	–	15	–	–	15	μs
		10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	–	5	–	–	5	–	pF

* Input pulse widths below the minimum specified may cause malfunction of the unit. See Application Note ICAN - 6230

CD4047A FUNCTIONAL TERMINAL CONNECTIONS

NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	–	10,11,13	t_A(10,11)=4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A(13)=2.20 RC
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	t_M(10,11)=2.48 RC
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	–	10,11	

* Input Pulse to Reset of External Counting Chip
External Counting Chip Output To Terminal 4

▲ See Text.

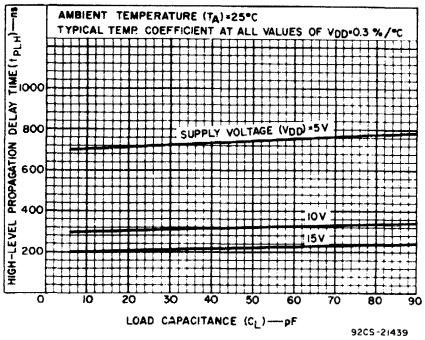


Fig. 6 – Typical low-to-high level propagation delay time vs load capacitance for Q and $\overline{Q}$ buffers.

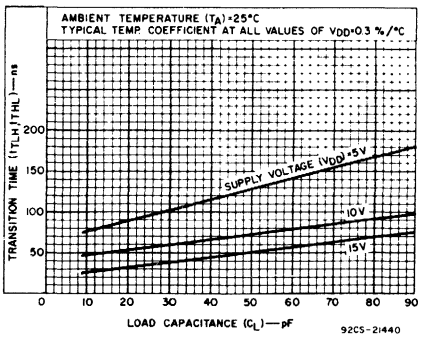


Fig. 7 – Typical transition time vs load capacitance for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations.

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

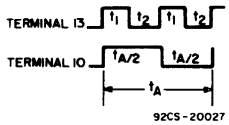


Fig. 8 – Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\,V_{DD}$ $t_A = 4.40\,RC$
Min: $V_{TR} = 0.33\,V_{DD}$ $t_A = 4.62\,RC$
Max: $V_{TR} = 0.67\,V_{DD}$ $t_A = 4.62\,RC$

thus if $\boxed{t_A = 4.40\,RC}$ is used, the maximum variation will be (+5.0%,–0.0%).

CD4047A Types

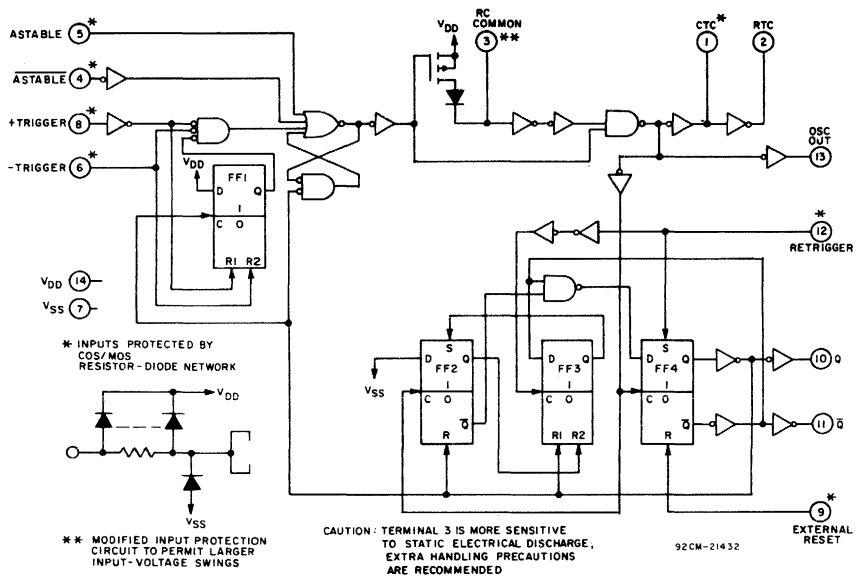


Fig. 9 – CD4047A logic diagram.

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit to unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

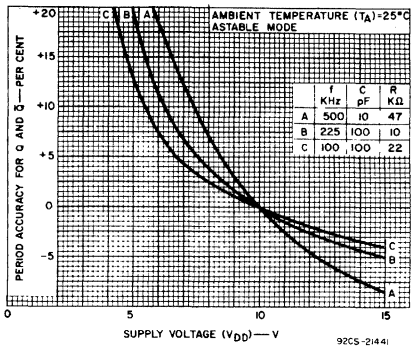


Fig. 10 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (high frequency).

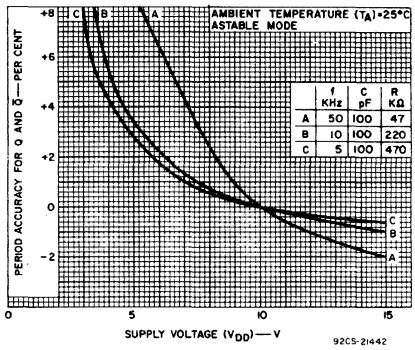


Fig. 11 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (medium frequency)

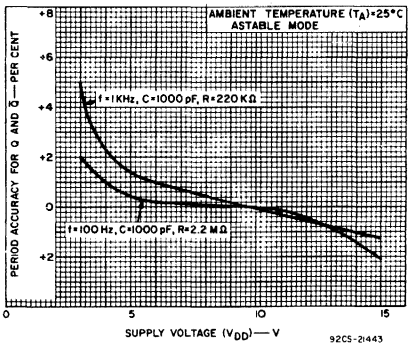


Fig. 12 – Typical Q-and-$\bar{Q}$-period accuracy vs supply voltage (low frequency).

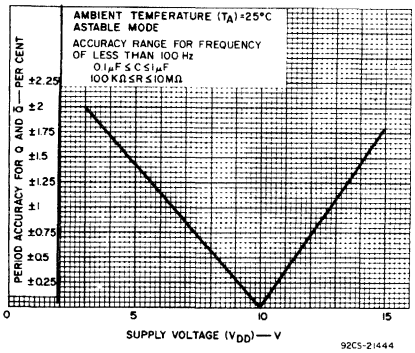


Fig. 13 – Typical Q-and-$\bar{Q}$- period accuracy vs supply voltage (very low frequency).

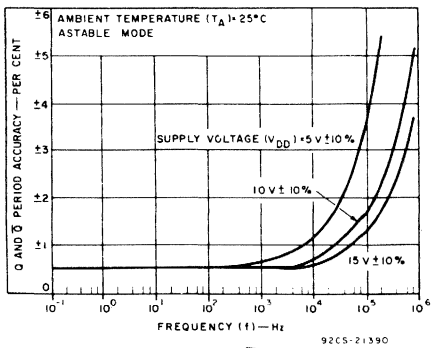


Fig. 14 – Typical Q-and $\bar{Q}$-period accuracy vs frequency for V_{DD} variation of ±10% from value indicated.

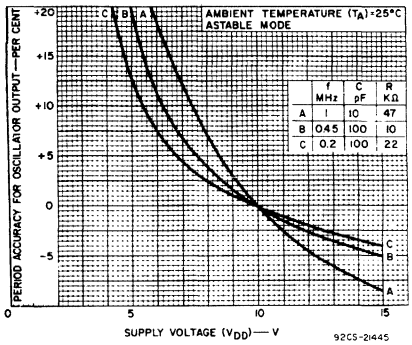


Fig. 15 – Typical oscillator-output-period accuracy vs supply voltage (high frequency).

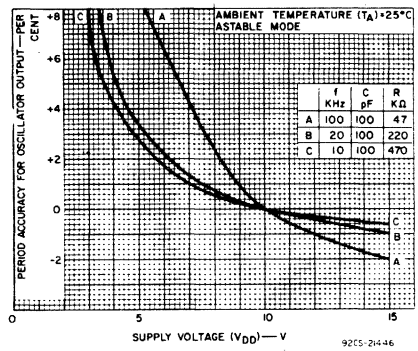


Fig. 16 – Typical oscillator-output-period accuracy vs supply voltage (medium frequency).

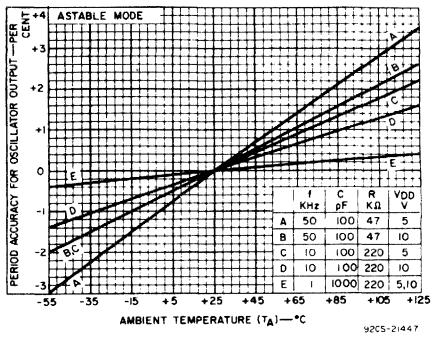


Fig. 17 – Typical Q- and $\bar{Q}$-period accuracy vs temperature (medium frequency).

CD4047A Types

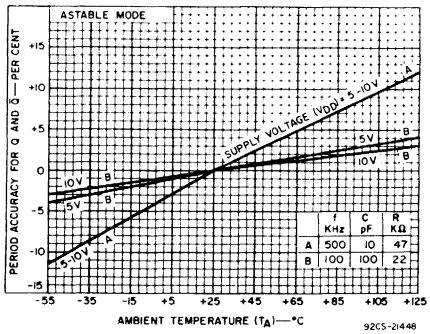


Fig. 18 – Typical Q- and $\overline{Q}$-period accuracy vs temperature (high frequency).

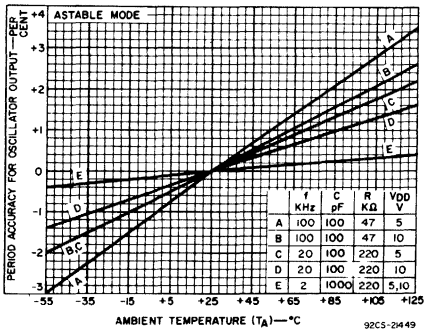


Fig. 19 – Typical oscillator-period accuracy vs temperature (medium frequency).

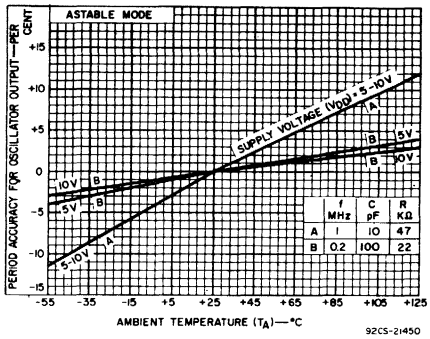


Fig. 20 – Typical oscillator-period accuracy vs temperature (high frequency).

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

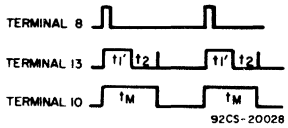


Fig. 21 – Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max. $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, –0.0%).

Note:

In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Fig. 22 to 27 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

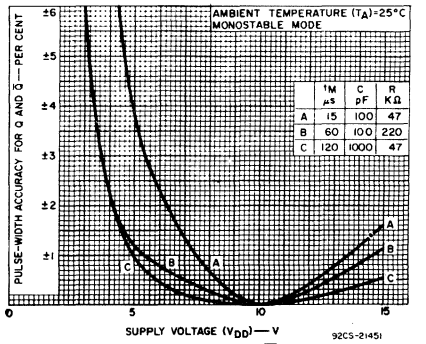


Fig. 22 – Typical Q- and $\overline{Q}$-pulse-width accuracy vs supply voltage (t_M = 15, 60, 120 µs).

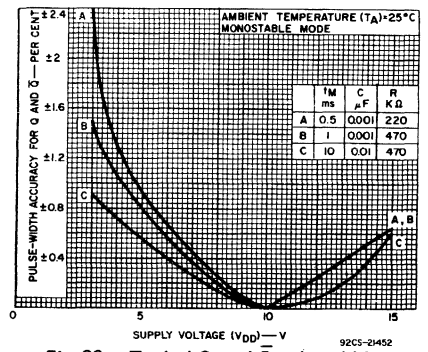


Fig. 23 – Typical Q- and $\overline{Q}$-pulse-width accuracy vs supply voltage (t_M = 0.5, 1, 10 ms).

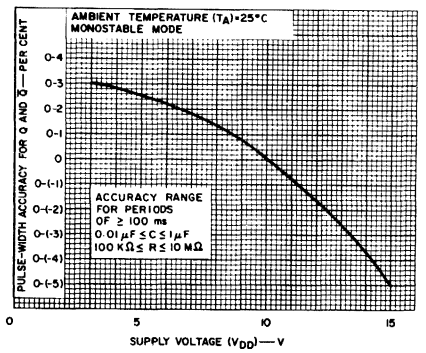


Fig. 24 – Typical Q- and $\overline{Q}$-pulse-width accuracy vs supply voltage ($t_M \geq$ 100 ms).

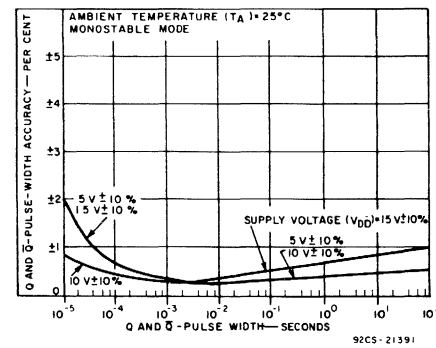


Fig. 25 – Typical Q- and $\overline{Q}$ pulse-width accuracy vs Q and $\overline{Q}$ pulse width for a variation of ±10% from value indicated.

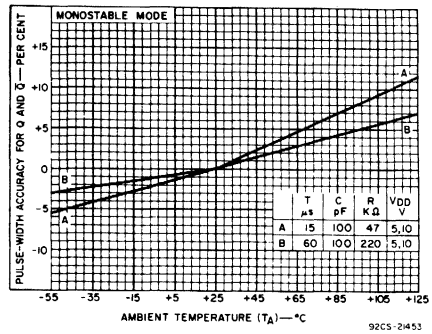


Fig. 26 – Typical Q and $\overline{Q}$ pulse-width accuracy vs temperature (high frequency).

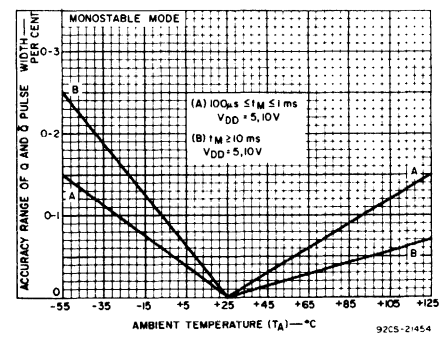


Fig. 27 – Typical Q and $\overline{Q}$ pulse-width accuracy range vs temperature.

CD4047A Types

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 29, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE}=t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT), terminates at some variable time, t_D, after the termination of the last retrigger pulse, t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 9).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 28. The pulse duration at the output is

$$t_{ext} = (N-1)(t_A) + (t_M + t_A/2)$$

where t_{ext}= pulse duration of the circuitry, and N is the number of counts used.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant 100$ pF, up to any practical value, for astable modes;

$C \geqslant 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leqslant R \leqslant 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)
$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

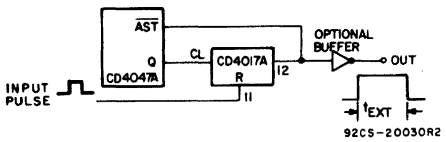


Fig. 28 – Implementation of external counter option.

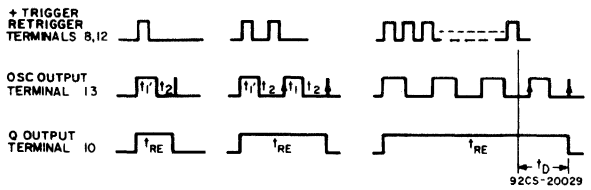


Fig. 29 – Retrigger-mode waveforms.

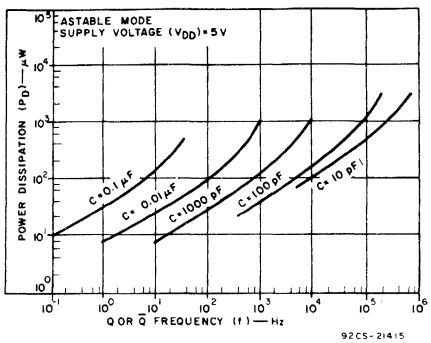


Fig. 30 – Power dissipation vs output frequency (V_{DD} = 5 V).

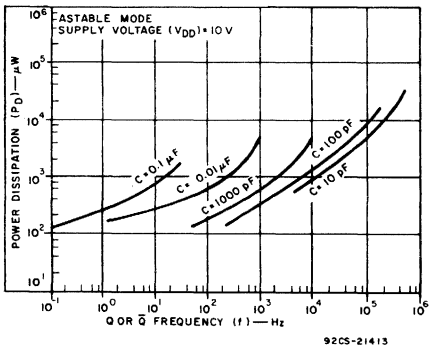


Fig. 31 – Power dissipation vs output frequency (V_{DD} = 10 V).

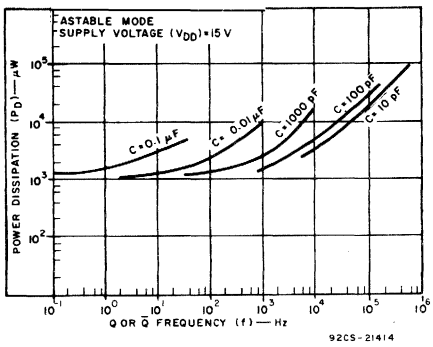


Fig. 32 – Power dissipation vs output frequency (V_{DD} = 15 V).

CD4048A Types

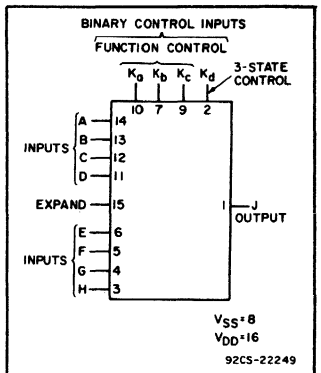
COS/MOS Multi-Function Expandable 8-Input Gate

The RCA- CD4048A is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input –Kd – provides the user with 3-state outputs. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 6). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

The CD4048A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4048A
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

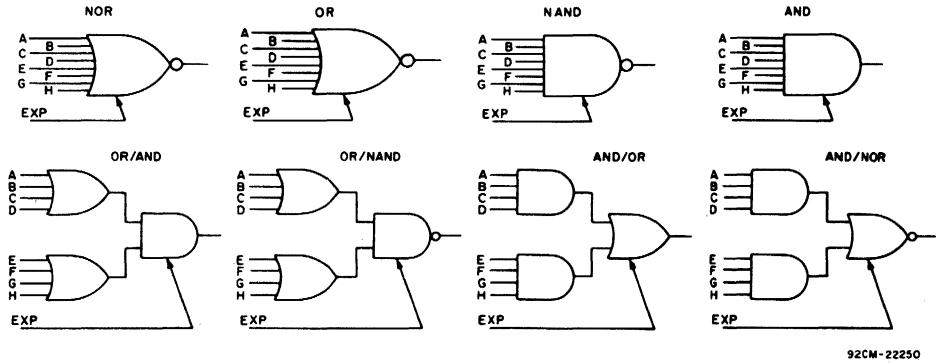


Fig. 1 – Basic logic configurations.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		E,Y Packages		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

Features:

- **Medium-power TTL drive capability**
- **Three-state output**
- **High-current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- **Many logic functions available in one package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - **Decoding**
  - **Encoding**

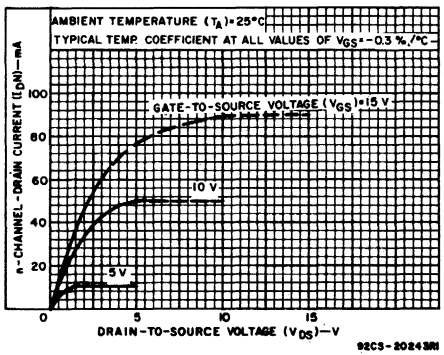


Fig. 2– Typical output n-channel drain characteristics.

CD4048A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.01	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.4	–	4.5	2	3.2	1.6	1.1	1.9	3.2	1.6	1.3	mA
	0.5	–	10	5.6	9	4.5	3.1	5.4	9	4.5	3.7	
p-channel (Source), I_DP Min.	4.6	–	5	−2	−3.2	−1.6	−1.1	−1.9	−3.2	−1.6	−1.3	
	9.5	–	10	−5.6	−9	−4.5	−3.1	−3.8	−9	−3.15	−2.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input											μA
	–	–	15	± 10^{-5} Typ., ± 1 Max.								
3-State Output Leakage Current I_{OL},I_{OH}	Forced (Output Disabled)											μA
	–	–	15	±10^{-4} Typ., ±2 Max.								

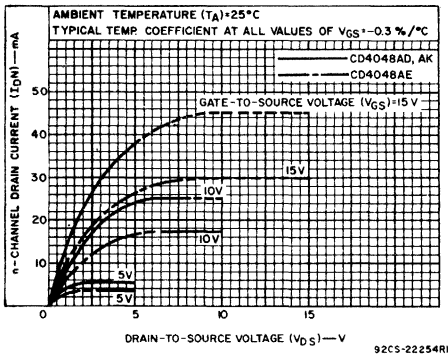


Fig. 3— Minimum output n-channel drain characteristics .

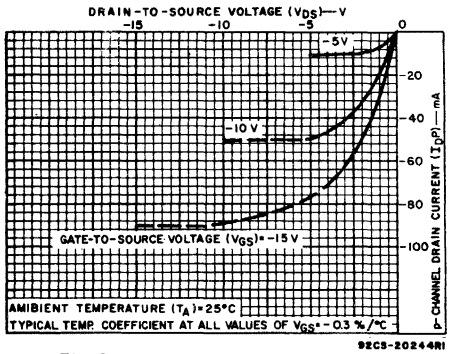


Fig. 4— Typical output p-channel drain characteristics.

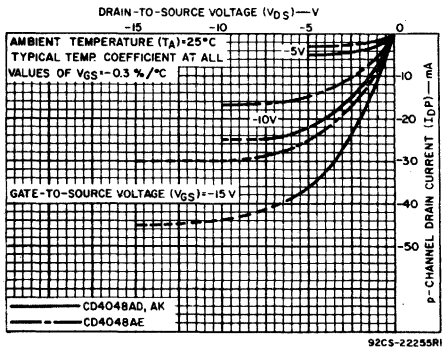


Fig. 5— Minimum output p-channel drain characteristics.

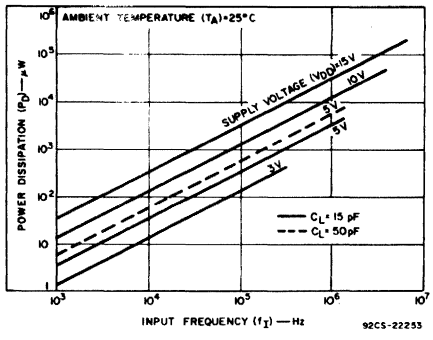


Fig. 6— Typical power dissipation as a function of input frequency.

CD4048A Types

DYNAMIC ELECTRICAL CHARACTERISTCS at T_A = 25°C and C_L = 15 pF and 50 pF,
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C R_L = 200 kΩ

C_L = 15 pF

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
			D,F,K,H Packages		*E,Y Packages*		
		V_{DD} (Volts)	TYP.	MAX.*	TYP.	MAX.*	
Propagation Delay Time t_{PHL}		5	750	1300	750	1600	ns
		10	225	400	225	500	
Transition Time: High-to-Low Level t_{THL}		5	90	140	90	170	ns
		10	30	50	30	65	
Low-to-High Level t_{TLH}		5	130	250	130	300	ns
		10	40	60	40	75	
Input Capacitance C_I	Any Input		5	—	5	—	pF

C_L = 50 pF

Propagation Delay Time t_{PLH},t_{PHL}		5	775	1350	775	1650	ns
		10	240	430	240	530	
Transition Time: High-to-Low Level t_{THL}		5	105	170	105	200	ns
		10	40	70	40	85	
Low-to-High Level t_{TLH}		5	145	280	145	330	ns
		10	50	80	50	95	
Input Capacitance C_I	Any Input		5	—	5	—	pF

* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17.

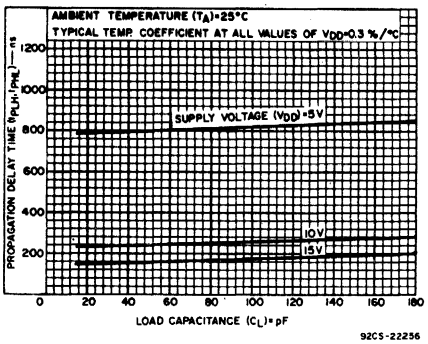


Fig. 7— Typical propagation delay time as a function of load capacitance.

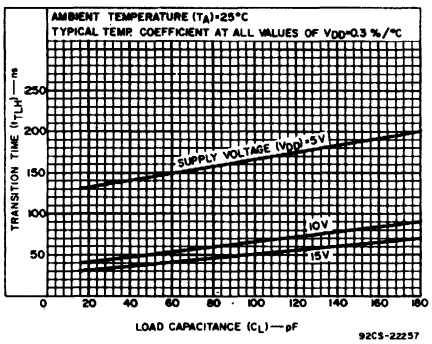


Fig. 8— Typical low-to-high level transition time as a function of load capacitance.

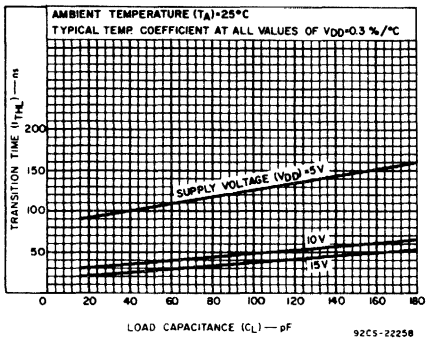


Fig. 9— Typical high-to-low level transition time as a function of load capacitance.

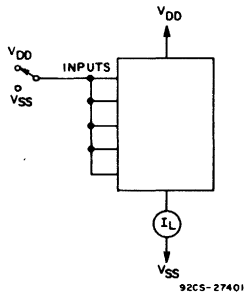


Fig. 10— Quiescent-device-current test circuit.

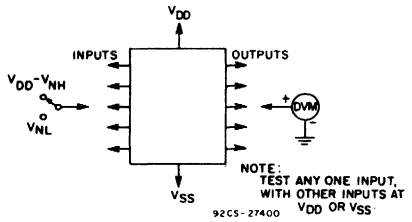


Fig. 11— Noise-immunity test circuit.

TEST CIRCUITS – DYNAMIC MEASURMENTS

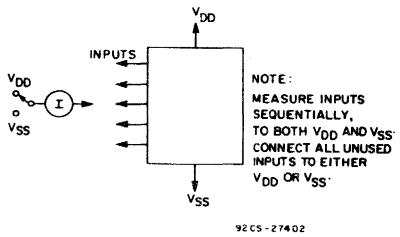
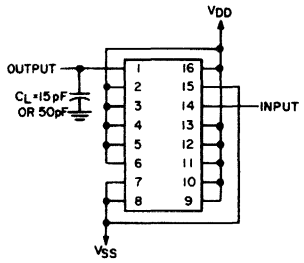


Fig. 12— Input-leakage-current test circuit.



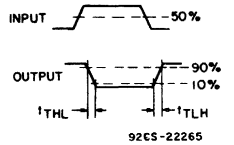
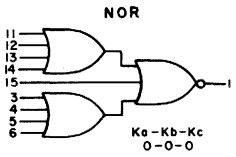
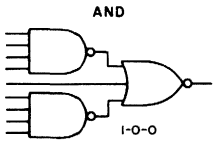
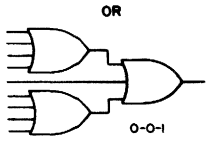


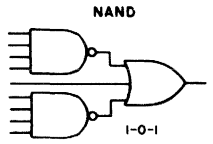
Fig. 13— t_{THL}, t_{TLH} – AND/NOR.

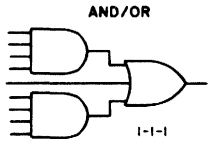
CD4048A Types











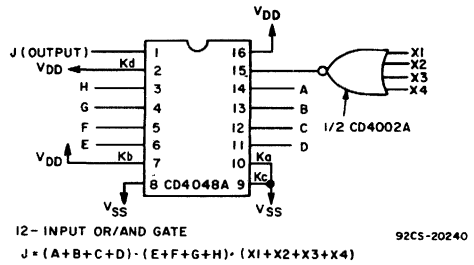


Fig. 14 (a) – 12-input OR/AND gate.

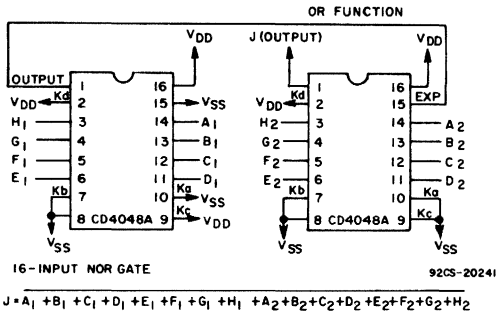


Fig. 14 (b) – 16-input NOR gate.

Applications of Expand Input

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot(EXP)$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot(EXP)}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot(EXP)}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).

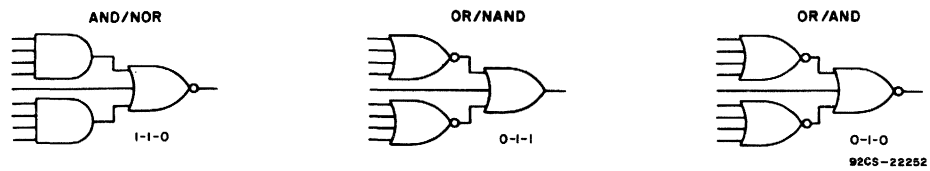
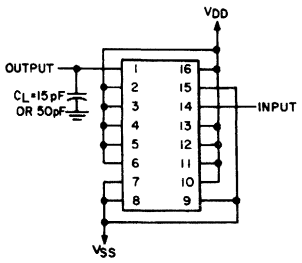


Fig. 14 (c) – Acutal-circuit logic configurations.

Fig. 14 – Expansion logic and truth table.



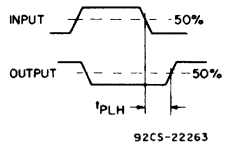
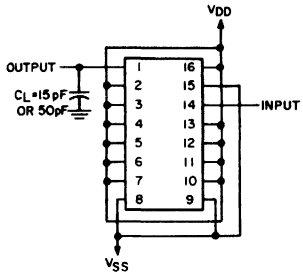


Fig. 15– t_{PLH} – NAND.



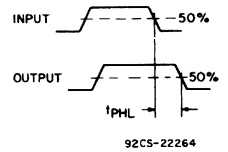
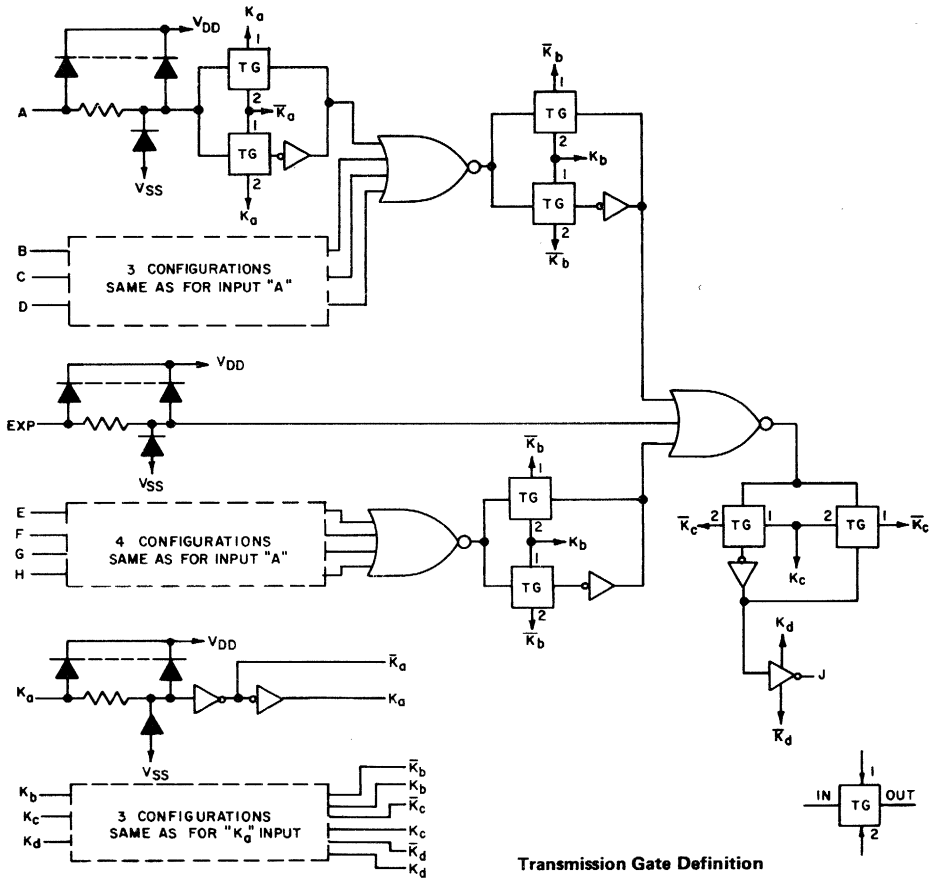


Fig. 16– t_{PHL} – AND.

CD4048A Types



Transmission Gate Definition

TG = Transmission Gate
Input to Output is:

a) A bidirectional low impedance when control input 1 is low and control 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

92CM-22251RI

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

K_d=1 Normal Inverter Action
K_d=0 High Impedance Output

EXPAND Input=0

*See Figs. 1 and 7.

Fig. 17– Logic diagram and truth table.

CD4049A, CD4050A Types

COS/MOS Hex Buffer/Converters

CD4049A—Inverting Type
CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \geqslant$0.4 V, and $I_{DN} \geqslant$3.2 mA.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

The CD4049A and CD4050A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**

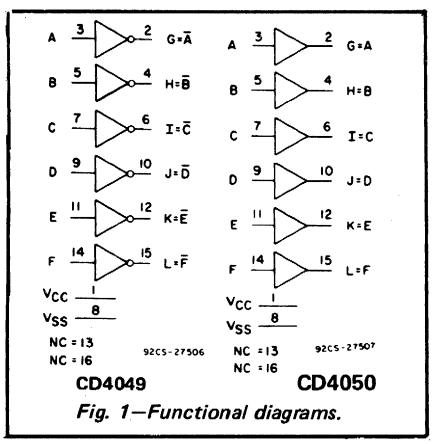


Fig. 1—Functional diagrams.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_I \geqslant V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				*E,Y Packages*				
	V_O (V)	V_{IN} (V)	V_{CC} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max.								V
	–	0, 10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4050A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4049A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} Min. CD4050A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} Min. CD4050A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
	0.4	–	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	–	10	10	16	8	5.6	9.6	16	8	6.6	
P-Channel (Source), I_{DP} Min.	4.5	–	5	−0.62	−1	−0.5	−0.35	−0.6	−1	−0.5	−0.4	
	2.5	–	5	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
	9.5	–	10	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

CD4049A, CD4050A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{CC})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

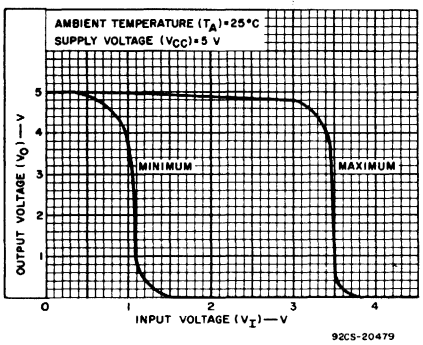


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049A.

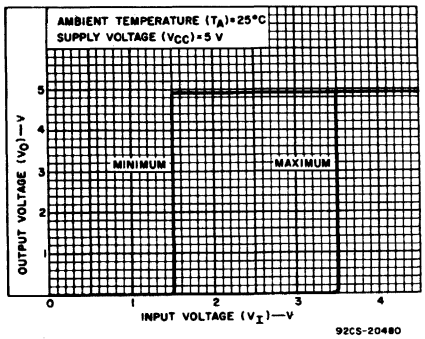


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050A.

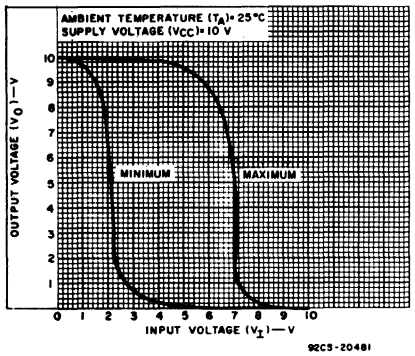


Fig. 4—Minimum and maximum voltage transfer characteristics for CD4049A.

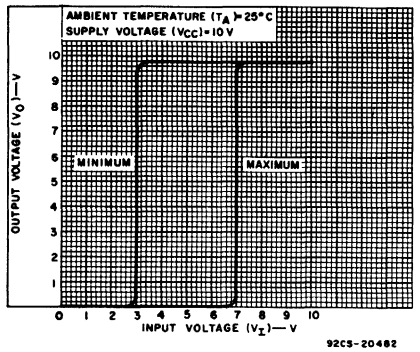


Fig. 5—Minimum and maximum voltage transfer characteristics for CD4050A.

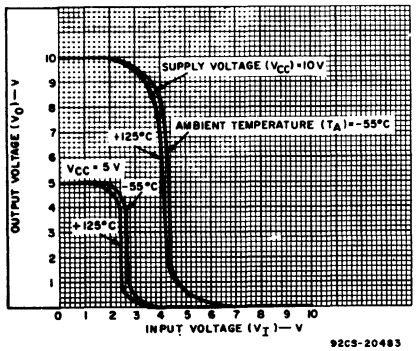


Fig. 6—Typical voltage transfer characteristics as a function of temperature for CD4049A.

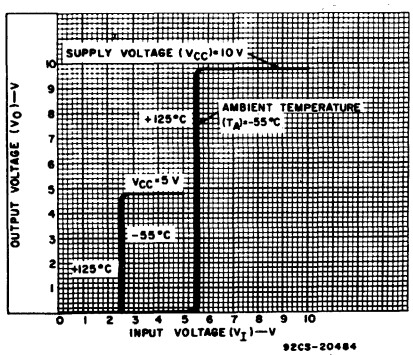


Fig. 7—Typical voltage transfer characteristics as a function of temperature for CD4050A.

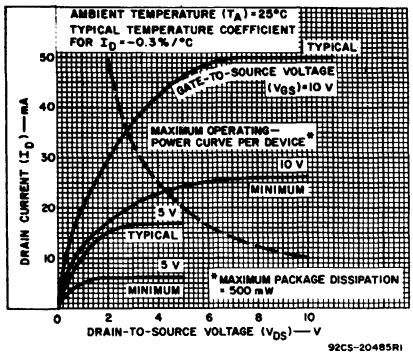


Fig. 8—Typical and minimum n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

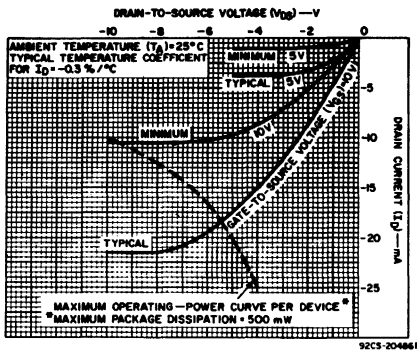


Fig. 9—Typical and minimum p-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

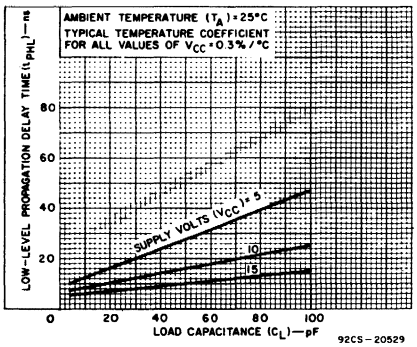


Fig. 10—Typical high-to-low level propagation delay time vs. C_L for CD4049A.

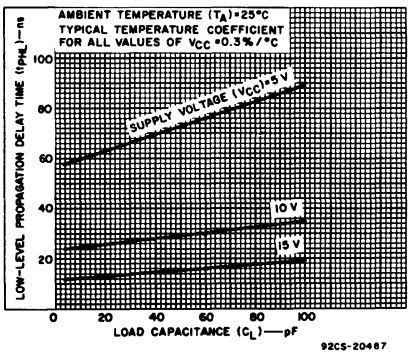


Fig. 11—Typical high-to-low level propagation delay time vs. C_L for CD4050A.

CD4049A, CD4050A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r, t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_I	V_{CC}	Typ.	Max.	
Propagation Delay Time:					
Low-to-High, t_{PLH}					
CD4049A	5	5	50	80	ns
	10	10	25	55	
CD4050A	5	5	75	140	
	10	10	35	85	
High-to-Low, t_{PHL}					
CD4049A	5	5	15	55	ns
	10	10	10	30	
CD4050A	5	5	55	110	
	10	10	25	55	
Transition Time:					
Low-to-High, t_{TLH}	5	5	50	100	ns
	10	10	30	60	
High-to-Low, t_{THL}	5	5	20	45	
	10	10	16	40	
Input Capacitance, C_I					
CD4049A	–	–	15	–	pF
CD4050A	–	–	5	–	

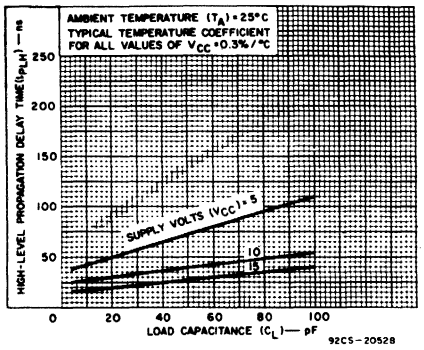


Fig. 12—Typical low-to-high level propagation delay time vs. C_I for CD4049A.

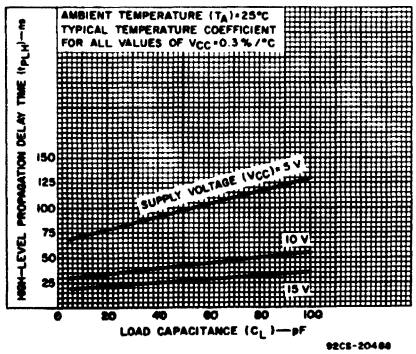


Fig. 13—Typical low-to-high level propagation delay time vs. C_L for CD4050A.

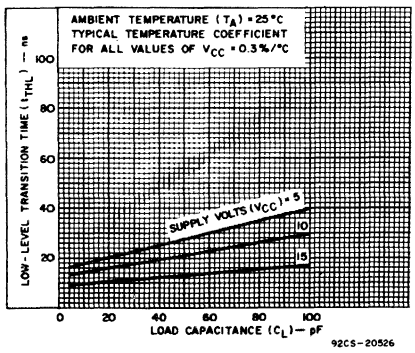


Fig. 14—Typical high-to-low level transition time vs. C_L for CD4049A, CD4050A.

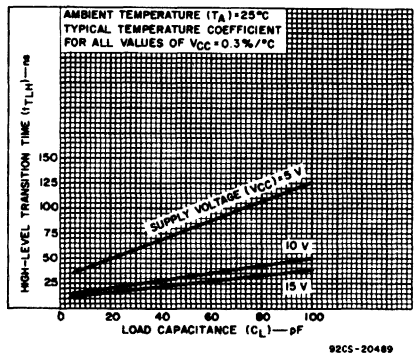


Fig. 15—Typical low-to-high level transition time vs. C_L for CD4049A, CD4050A.

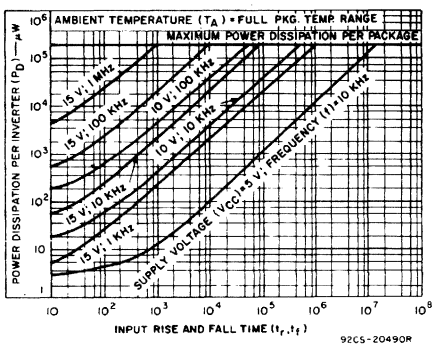


Fig. 17—Typical power dissipation vs. transition time per inverter CD4049A.

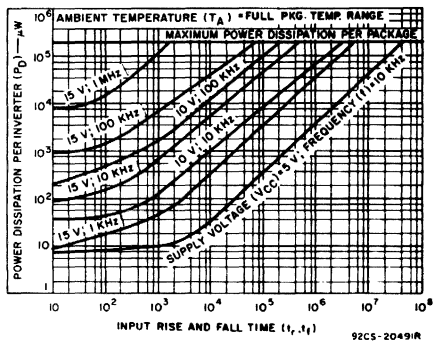


Fig. 18—Typical power dissipation vs. transition time per inverter CD4050A.

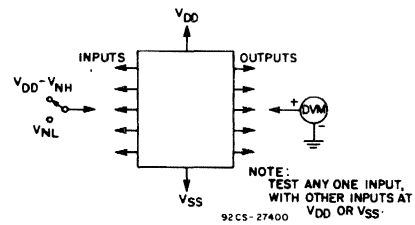


Fig. 19—Noise immunity test circuit.

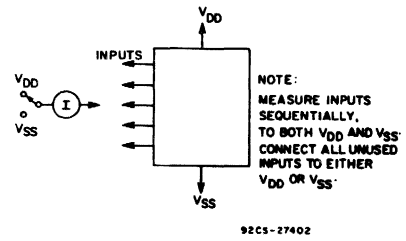


Fig. 20—Input leakage current test circuit.

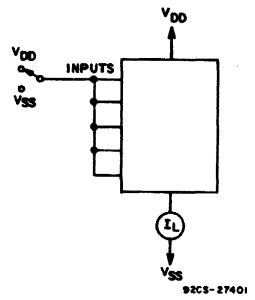


Fig. 21—Quiescent device current test circuit.

CD4057A Types

COS/MOS LSI 4-Bit Arithmetic Logic Unit

The RCA-CD4057A is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in 4^N unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), in a flat-pack (CD4057AK), and in chip form (CD4057AH).

Applications:

- **Parallel Arithmetic Units**
- **Process Controllers**
- **Remote Data Sets**
- **Graphic Display Terminals**

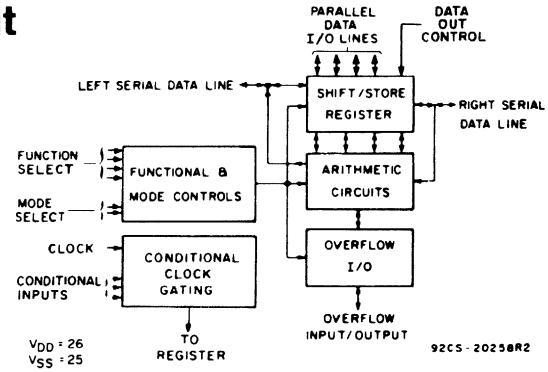


Fig. 1 – Block diagram – CD4057A.

Features:

- **LSI Complexity on a Single Chip**
- **16-Instruction Capability**
  -Add, Subtract, Count
  -AND, OR, Exclusive-OR
  -Right, Left, or Cyclic Shifts
- **Bidirectional Data Busses**
- **Instruction Decoding on Chip**
- **Fully Static Operation**
- **Single-Phase Clocking**
- **Easily Expandable to 8, 12, 16,. . . . Bit Operation**
- **Low Quiescent Device Dissipation . . . . . 10 μW (typ.)**
- **Conditional-Operation Controls on Chip**
- **Add Time (Data In-To Sum Out) =375 ns (typ) at 10V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H ..... −55 to +125°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −55 to +100°C (PACKAGE TYPES D, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	V
Setup Time, t_S DATA	5	40	–	ns
	10	20	–	
OP CODE	5	4590	–	
	10	1320	–	
Clock Pulse Width, t_W	5	1200	–	ns
	10	375	–	
Clock Input Frequency, f_{CL} Count Mode	5	0.13	–	MHz
	10	0.46	–	
Shift Mode	5	0.33	–	
	10	1.4	–	
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	

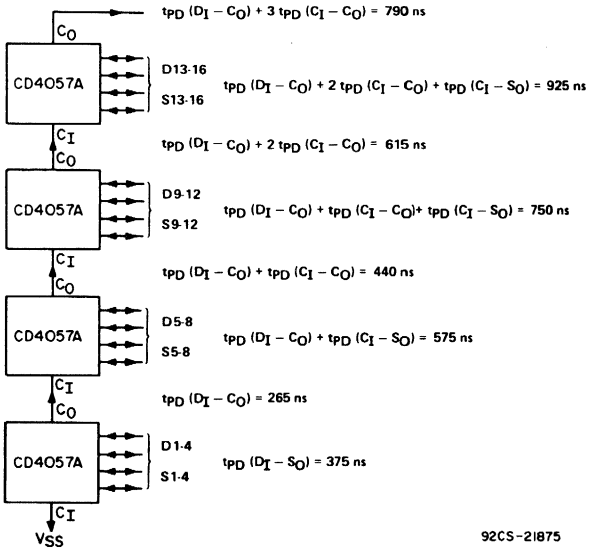


Fig. 2 – Typical speed characteristics of a 16-bit ALU at V_{DD} = 10 V.

CD4057A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits at Indicated Temperatures (°C)							UNITS
				CD4057AD, CD4057AK, CD4057AH							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°C		25°C			125°C		
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current I_L	–	–	5	–	5	–	0.5	5	–	150	μA
	–	–	10	–	10	–	1	10	–	300	
	–	–	15	–	50	–	1	50	–	2000	
Output Voltage; Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.							V
	–	10	10	0 Typ.; 0.05 Max.							
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.							V
	–	0	10	9.95 Min.; 10 Typ.							
Noise Immunity (All Inputs) V_{NL}, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.							V
	1	–	10	3 Min.; 4.5 Typ.							
	4.2	–	5	1.5 Min.; 2.25 Typ.							
	9	–	10	3 Min.; 4.5 Typ.							
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.							V
	9	–	10	1 Min.							
Inputs High, V_{NMH}	0.5	–	5	1 Min.							
	1	–	10	1 Min.							
Output Drive Current: I_DN, I_DP Zero Indicator	0.5	–	5	0.11	–	0.09	0.16	–	0.06	–	mA
n-channel	0.5	–	10	0.12	–	0.10	0.16	–	0.07	–	
p-channel	3	–	5	0.04	–	0.03	0.06	–	0.02	–	
	7	–	10	0.08	–	0.07	0.13	–	0.05	–	
Negative Indicator	0.5	–	5	0.11	–	0.09	0.30	–	0.06	–	
n-channel	0.5	–	10	0.12	–	0.10	0.40	–	0.07	–	
p-channel	4.5	–	5	0.07	–	0.06	0.19	–	0.04	–	
	9.5	–	10	0.12	–	0.10	0.30	–	0.07	–	
Overflow Indicator	0.5	–	5	0.25	–	0.20	0.50	–	0.14	–	
n-channel	0.5	–	10	0.37	–	0.30	0.90	–	0.21	–	
p-channel	4.5	–	5	0.08	–	0.07	0.21	–	0.05	–	
	9.5	–	10	0.12	–	0.10	0.38	–	0.07	–	
All Other Outputs	0.5	–	5	0.11	–	0.09	0.10	–	0.06	–	
n-channel	0.5	–	10	0.06	–	0.05	0.12	–	0.03	–	
p-channel	4.5	–	5	0.02	–	0.02	0.05	–	0.01	–	
	9.5	–	10	0.06	–	0.05	0.08	–	0.03	–	
Input Leakage Current I_{IL}, I_{IH}	Any Input										μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.							

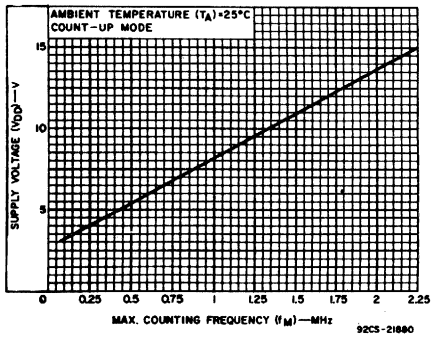


Fig. 3 — Maximum counting frequency vs. supply voltage for a typical CD4057A.

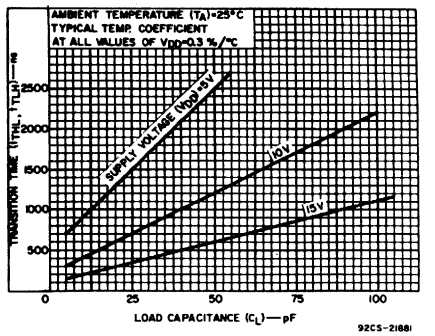


Fig. 4 — Transition time vs. load capacitance for data outputs (D1-D4).

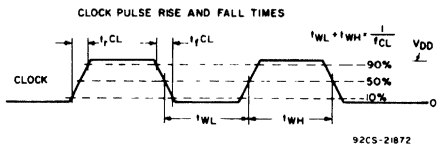


Fig. 5 — Clock pulse rise and fall times.

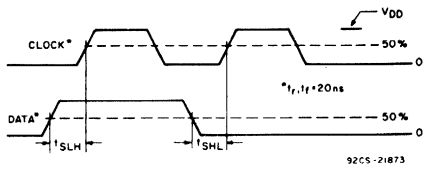


Fig. 6 — Data setup time.

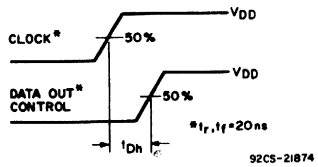


Fig. 7 — Data hold time.

CD4057A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $C_L = 15$ pF, $R_L = 200$ kΩ, $t_r, t_f = 20$ ns

Typical Temperature Coefficient at all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS CD4057AD, CD4057AK			UNITS
	V_{DD}	Min.	Typ.	Max.	
Propagation Delay Time: t_{PLH}, t_{PHL} DATA IN-to-SUM OUT	5	–	1430	3900	ns
	10	–	375	720	
CARRY IN-to-SUM OUT	5	–	915	2550	
	10	–	310	840	
DATA IN-to-CARRY OUT	5	–	950	2580	
	10	–	265	720	
CARRY IN-to-CARRY OUT	5	–	485	1320	
	10	–	175	480	
ZI Input -to- ZI Output	5	–	1980	5400	
	10	–	750	2040	
	5	–	265	720	
	10	–	110	300	
Transition Time: t_{TLH}, t_{THL} ZI Output	5	–	3700	10350	ns
	10	–	1650	4500	
	5	–	420	1140	
	10	–	220	600	
Negative Indicator and Overflow Indicator	5	–	300	825	
	10	–	165	450	
All Other Outputs	5	–	1000	2775	
	10	–	475	1275	
Minimum Clock Pulse Width, t_W	5	–	400	1200	ns
	10	–	125	375	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	15	
Minimum Set Up Time : t_{SLH}, t_{SHL} DATA	5	–	20	40	ns
	10	–	10	20	
OP CODE	5	–	1675	4590	ns
	10	–	485	1320	
Minimum Data Hold Time, t_{HLH}, t_{HHL}	5	–	20	40	ns
	10	–	10	20	
Maximum Clock Frequency: f_{CL} Count Mode	5	0.13	0.36	–	MHz
	10	0.46	1.35	–	
Shift Mode	5	0.33	0.90	–	
	10	1.4	3.8	–	
Input Capacitance, C_I	ANY INPUT	–	5	–	pF

LOGIC DESCRIPTION

OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 8 shows the manner in which the four modes control the data on the serial-data lines.

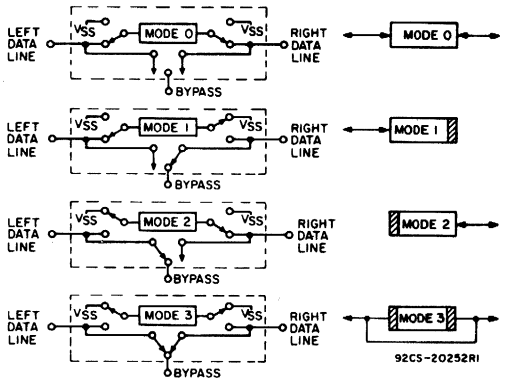


Fig. 8 – Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line.

In MODE 2, data can enter or leave only on the right serial-data line.

In MODE 3, serial data can neither enter nor leave the register, regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I. Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one " hard-wired " combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 10.

CD4057A Types

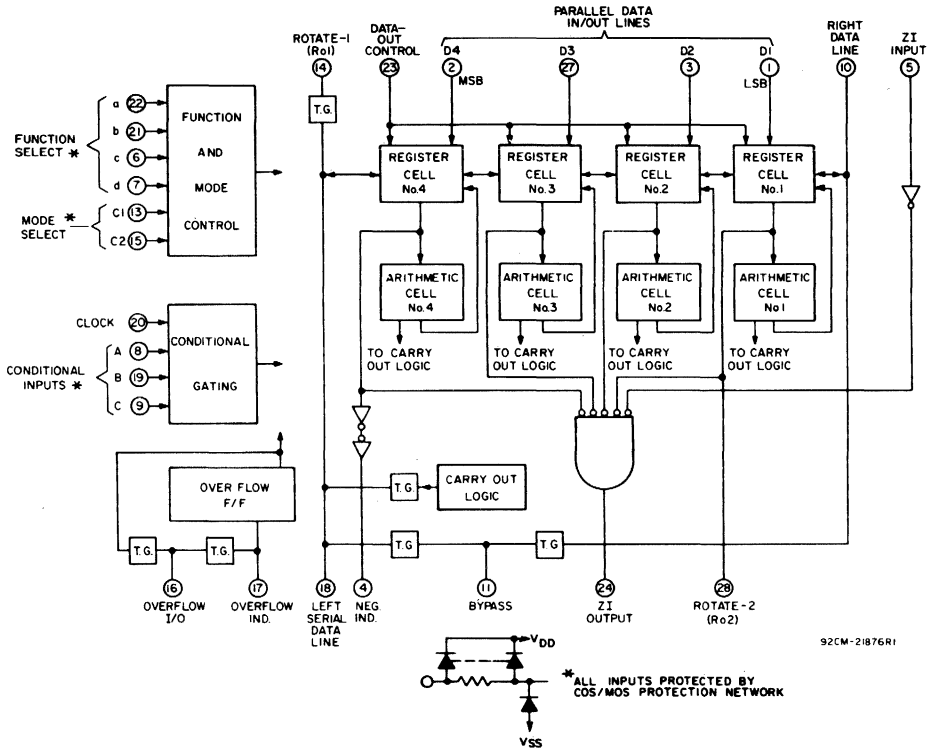


Fig. 9 – Simplified logic diagram.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used, 4^4 combinations (256) are possible. *Fig. 11* shows a diagram of 4 CD4057A's interconnected to form a 16-bit parallel processor.

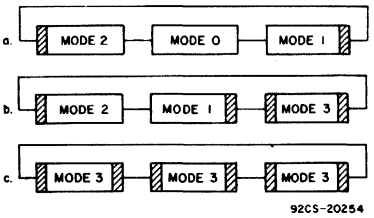


Fig. 10 – "Mode" connections for parallel processor:
(a) 12-bit unit,
(b) one 8-bit and one 4-bit unit
(c) three 4-bit units.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a	b	c	d	
0	0	0	0	NO-OP (Operational Inhibit)
0	0	0	1	AND
0	0	1	0	Count down
0	0	1	1	Count up
0	1	0	0	Subtract Stored number from zero (SMZ)
0	1	0	1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0	1	1	0	Add (AD)
0	1	1	1	Subtract (SUB) (Parallel data lines from stored number)
1	0	0	0	Set to all ones (SET)
1	0	0	1	Clear to all zeroes (CLEAR)
1	0	1	0	Exclusive-OR
1	0	1	1	OR
1	1	0	0	Input Data (From parallel data lines)
1	1	0	1	Left shift
1	1	1	0	Right shift
1	1	1	1	Rotate (cycle) right

All instructions are executed on the positive edge of the clock.

PARALLEL COMMANDS

a. **CLEAR** – sets register to zero.
b. **SET** –sets register to all ones.
c. **OR** –processes contents of register with value on parallel-data lines in a logical OR function.
d. **AND** –processes contents of register with value on parallel-data lines in a logical AND function.
e. **Exclusive-OR** – processes contents of register with data on parallel-data lines in a logical Exclusive-OR function.
f. **IN** –loads data on parallel-data lines into register.
g. **DATA OUT CONTROL** – unloads contents of register and overflow flip-flop onto parallel data lines and overflow I/O independent of all other controls.
h. **SUB:**
   In Mode 0, adds to the contents of the register the one's complement of the data on the parallel-data lines. Carries can enter on the right serial data line and can leave on the left serial data line. The overflow indicator does not change state.
   In Mode 1, adds to the contents of the register the two's complement of the data on the parallel-data lines. Generated carries can leave on the left serial line. The CARRY IN is set to zero. The overflow indicator does not change state.
   In Mode 2, same as Mode 0, except carries cannot leave on the right serial-data line. The absence or presence of an overflow is registered.
   In Mode 3, same as Mode 1, except carries cannot leave on the left serial-date line. The absence or presence of an overflow is registered.
i. **COUNT UP:**
   In Mode 0, adds to the contents of the register the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters the parallel-data lines.
   In Mode 1, internally adds a one to the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.
   In Mode 2, adds to the contents of the register the data on the right serial-data line. No data enters or leaves the left serial-data line.
   In Mode 3, internally adds a one to the contents of the register No data enters or leaves the register on any serial-data or parallel-data line.
   In all modes, with the DATA OUT control high

CD4057A Types

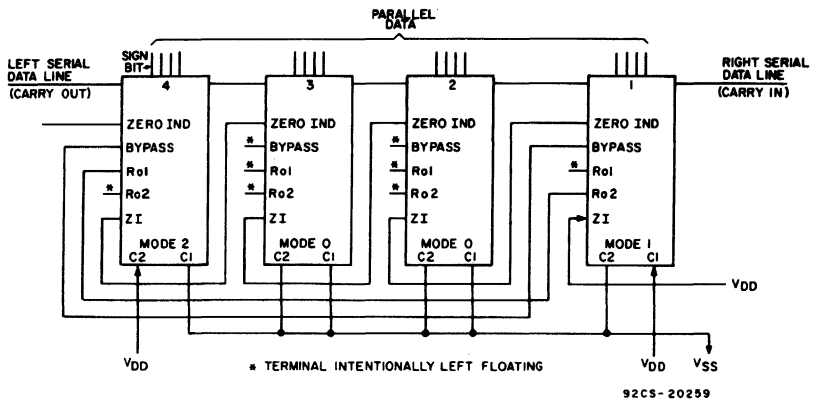


Fig. 11 — Connection for 16-bit arithmetic logic unit.

the count is presented on the parallel data lines (D1-D4).

j. COUNT DOWN:

In Mode 0, subtracts a one (2's complement form) from the contents of the register and adds to this result the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters on the parallel-data lines.

In Mode 1, internally subtracts a one from the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, subtracts a one from the contents of the register and adds to this result the data on the right serial-data line. No data enters or leaves on the left serial-data line.

In Mode 3, internally subtracts a one from the contents of the register. No data enters or leaves on the serial-data lines.

In all modes, with the DATA OUT control high the count is presented on the parallel data lines (D1-D4).

k. ADD(AD):

In Mode 0, adds the contents of the register to the data on the parallel-data lines and the right serial-data line. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, adds the contents of the register to the data on the parallel-data lines and allows any resulting carry to leave on the left serial-data line. The right serial-data line is open-circuited. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, adds the contents of the register to the data on the parallel data lines and the right serial-data line. Any overflow sets the overflow indicator. The left serial-data line is open-circuited. The absence or presence of an overflow is registered.

In Mode 3, adds contents of the register to the data on the parallel-data lines. Any resulting carry sets the overflow indicator. The two serial-data lines are open circuited. The absence or presence of an overflow is registered. The CARRY-IN is set to zero.

l. SM — same operation as AD except the contents of the register are two's complemented during addition in Mode 1 and Mode 3. In Mode 0 or Mode 2, the contents of the register are one's complemented and added to the data on the right serial-data line and the parallel-data lines. Overflows occurring in Mode 1 or Mode 0 do not alter the overflow indicator. The presence or absence of overflows is registered on the overflow indicator in Mode 2 or Mode 3.

m. SMZ:

In Mode 0, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, two's complements the contents of the register and permits any carry to leave on the left serial-data line. No data can enter the right serial-data line. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Carries cannot leave the left serial data line. The absence or presence of an overflow alters the overflow indicator.

In Mode 3, two's complements the contents of the register. Serial data can neither enter the right serial-data line nor leave the left serial-data line. The overflow indicator is at zero. The CARRY-IN is set to zero.

n. NO-OP — no operation takes place, The clock input is inhibited and the state of all registers and indicators remains unchanged.

SERIAL-SHIFT OPERATIONS

a. ROTATE (cycle) RIGHT — This operation is internal. The contents of the register shift to the right, cyclic fashion with the leftmost stage accepting data from the rightmost stage regardless of the mode. Data can leave the register serially on the right data line only while the register is in Mode 1 or Mode 0. Data can enter the left data line serially while the register is in Mode 1 or Mode 0. The Ro1 terminal of the "Most Significant" CD4057A must be connected to the Ro2 terminal of the "Least Significant" CD4057A. All other Ro1 and Ro2 terminals must be left floating. When only one CD4057A is used, Ro1 must be connected to Ro2.

b. RIGHT SHIFT — The contents of the register shift to the right and serial operations are as follows:

In Mode 0, data can enter serially on the left data line, shift through the register, and leave on the right data line.

In Mode 1, data can enter serially on the left data line. The right data line effectively is open - circuited.

In Mode 2, data can leave serially on the right data line. The left data line effectively is open-circuited. Vacant spaces are filled with zeros.

In Mode 3, serial data can neither enter nor leave the register; however,the contents shift to the right and vacated places are filled with zeros.

CD4057A Types

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

c. **LEFT SHIFT** – The contents of the register shift to the left and serial operations are as follows;

In Mode 0, data can enter the right data line, shift through the register, and leave on the left data line.

In Mode 1, data can leave serially on the left data line. The right data line effectively is open-circuited. All vacant positions are filled with zeros.

In Mode 2, data can enter serially on the right data line. The left data line effectively is open-circuited.

In Mode 3, data can neither enter nor leave the register; however, the contents shift to the left, and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

Because the "DATA OUT" control instruction is independent of the other 16 instructions, care must be taken not to activate this control when data are to be loaded into the processor. This instruction should only be activated when the processor is executing a NO-OP, any SHIFT, SMZ, COUNT UP or DOWN, CLEAR, or SET.

If a data line, serial or parallel, is used as an input and the logic state of that line is not defined (i.e., the line is an open circuit),then the result of any operation using that line is undefined.

OPERATIONAL SEQUENCE FOR ARITHMETIC ADD CYCLE

1. Apply IN Instruction and Word A on Parallel Data Lines (D1–D4).
2. Apply CLOCK to load Word A into the register.
3. Apply OP CODE Instruction and Word B on Data Lines.
4. Apply CLOCK to load resulting function of A and B into the register.
5. Apply "DATA OUT" control to present result to Parallel Data Lines.

NOTE: Transitions of Step 2 and Step 3 may occur almost simultaneously; i.e. separated by only one data-hold time.

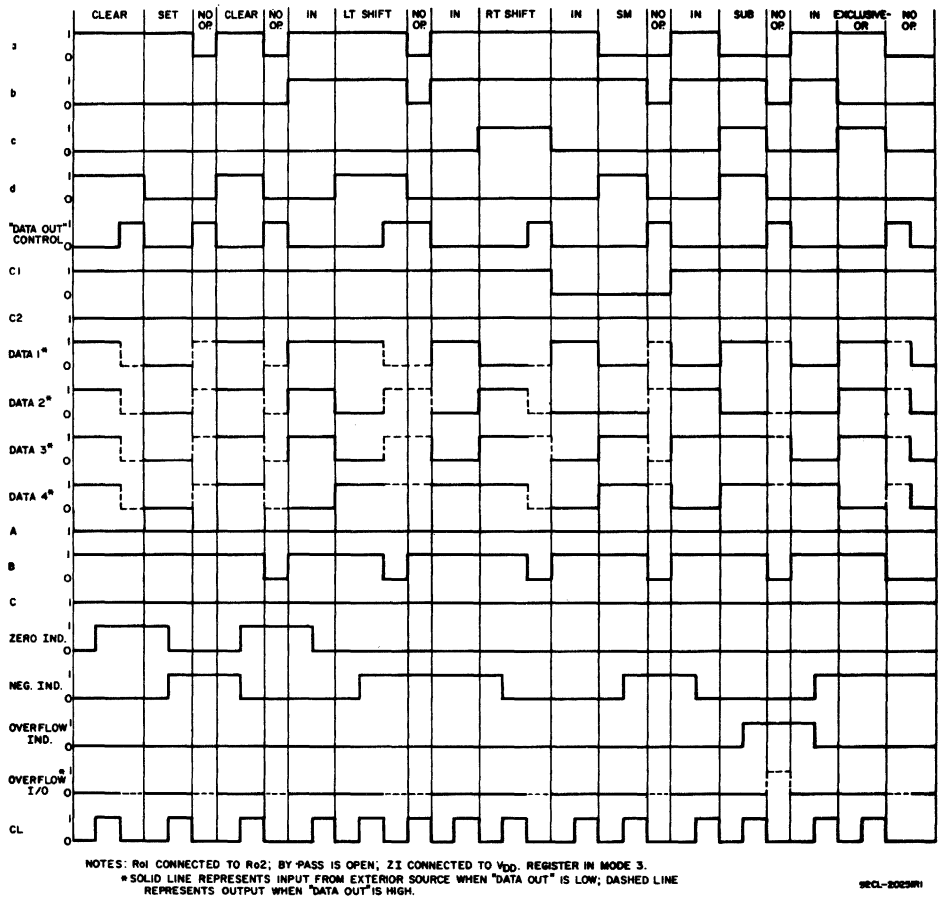


Fig. 12 – Timing diagram.

NEGATIVE-NUMBER DETECTION

The NEG IND terminal of the CD4057A is connected to the output of the flip-flop that is in the most significant bit position. A "1" on the NEG IND terminal indicates a negative number is in the register. This detection is also independent of modes.

ZERO DETECTION

The condition of "all zeros" is indicated by a "1" on the Zero Indicator terminal of the "Most Significant" CD4057A. As shown in Fig. 11, terminal ZI of the CD4057A containing the least significant set of bits is connected to V_{DD}. Zero indication is independent of modes.

COMPLEMENTING NUMBERS

1. One's complement of number in ALU register.
   a) ALU must be in MODE 0 or MODE 2.
   b) Zero on Rt. Data Line.
   c) Execute an SMZ instruction.

(Continued)

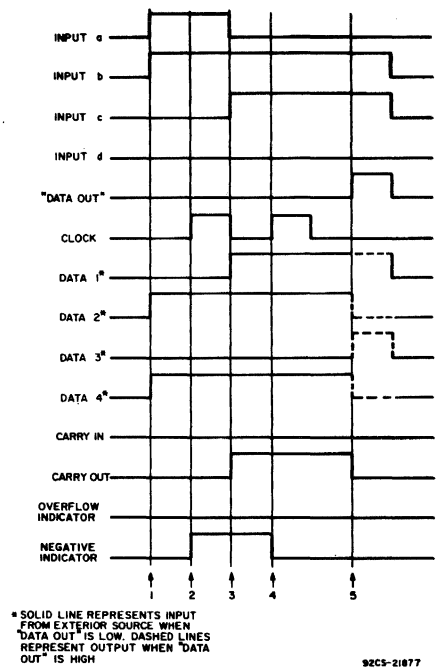


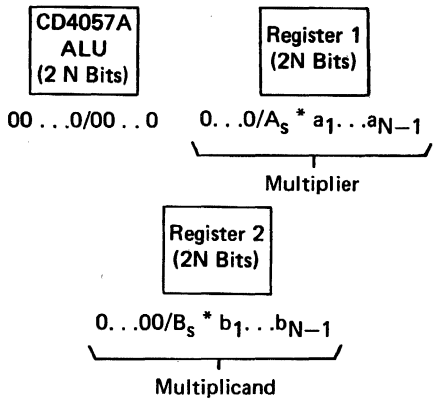
Fig. 13 – Add cycle waveforms.

CD4057A Types

2. One's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 0 or MODE 2.
   c) Execute an SUB instruction.
3. Two's complement of number in ALU register.
   a) ALU must be in MODE 1 or MODE 3.
   b) Execute an SMZ instruction.
4. Two's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 1 or MODE 3.
   c) Execute an SUB instruction.

The following algorithms are given as a general guideline to demonstrate some of the capabilities of the CD4057A.

MULTIPLICATION OF TWO N-BIT NUMBERS

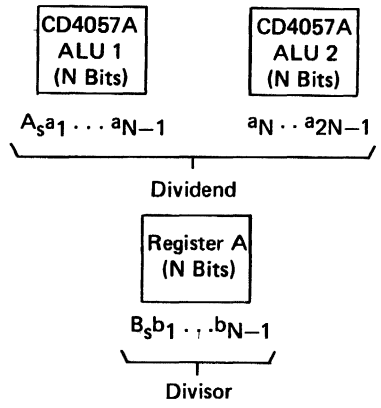


*A_S and B_S are sign bits

Multiplication Algorithm

1. Clear ALU to Zero
2. Store $A_S \oplus B_S$ in External Flip-Flop.
3. If $A_S = 1$, Complement Register 1.
4. If $B_S = 1$, Complement Register 2.
5. Load Register 2 into ALU.
6. Do shift Left on ALU N Times (N = number of bits).
7. Do N Times:
   (1)
   a) If MSB of ALU = 1 (Negative Indicator = High), Then shift ALU left 1 bit; add Register 1 to ALU.
   b) If MSB of ALU = 0 (Negative Indicator = Low) Then shift ALU left 1 bit.
8. If $A_S \oplus B_S = 1$, then Complement ALU.
9. Answer in ALU.

Division Algorithm



1. Store $A_S \oplus B_S$ in External Flip-Flop.
2. If $A_S = 1$, complement ALU 1 and ALU 2.
3. If $B_S = 1$, complement Register A.
4. Check for Divisor = 0
   a) If Divisor = 0; stop, indicates division by 0.
   b) If Divisor $\neq 0$; continue.
5. Apply SUB instruction to ALU 1 and Register A to ALU 1 data lines.
   a) If $C_O = 0$ (Dividend < Divisor), Stop, indicates overflow.
   b) If $C_O = 1$ (Dividend $\geq$ Divisor), Continue.
6. Put a zero on RT data line of ALU 2 and shift ALU 1 & ALU 2 left 1 bit.
7. Do "N" times.
   a) If $C_O = 1$, then clock ALU 1, and put a 1 on right data line of ALU 2.
   b) If $C_O = 0$, then no clock, and put a 0 on right data line of ALU 2.
8. If sign Flip Flop = 1, complement ALU 2.
9. Answer in ALU 2.

CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional input terminals A,B,and C.In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional inputs, truth table, defines the interactions among A,B, and C.

TABLE II – CONDITIONAL-INPUTS TRUTH TABLE

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

1) For the Multiplication Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = negative Indicator
2) For the Division Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = C_O (left data line)

OVERFLOW DETECTION

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

For example:
$$\begin{array}{rr} & 0.011 \\ (+) & \underline{0.110} \\ & 1.001 \end{array}$$

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/O line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/O line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

CD4057A Types

OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

1. DATA-IN-to-CARRY OUT and DATA IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B (data in)
   - E. Apply Clock to load result (sum out)
   - F. Apply DATA OUT CONTROL to look at result

2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B
   - E. Apply CARRY IN (carry in)
   - F. Apply Clock to load result (sum out)
   - G. Apply DATA OUT CONTROL to look at result

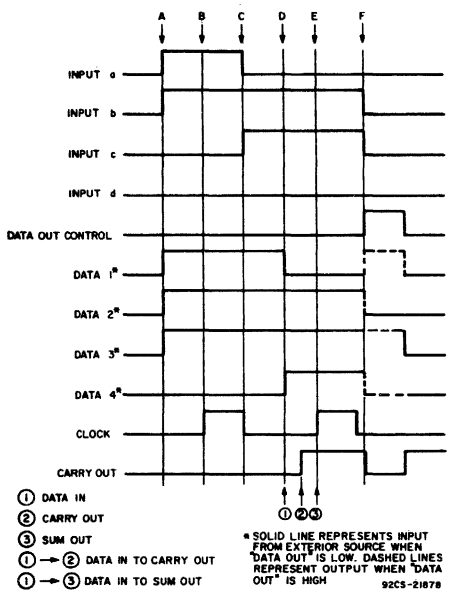


Fig. 14(a) — DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

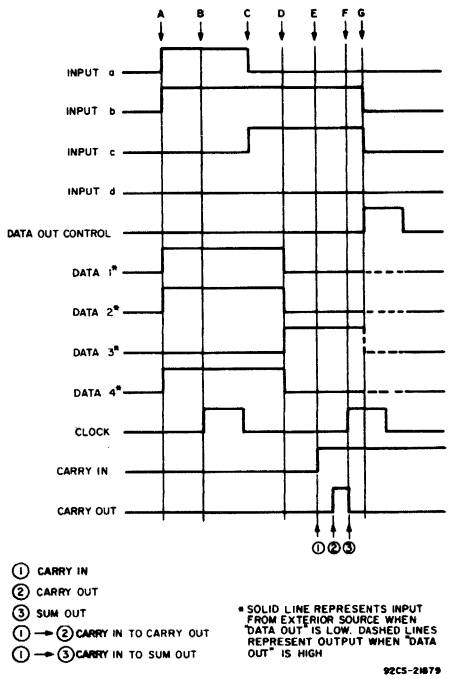


Fig. 14(b) — CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

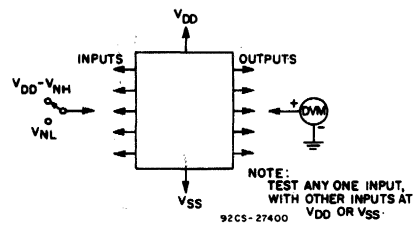


Fig. 15 — Noise-immunity test circuit.

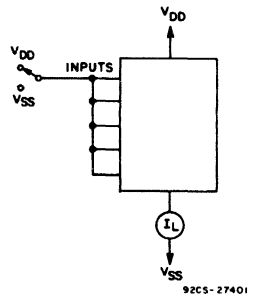


Fig. 16 — Quiescent-device-current test circuit

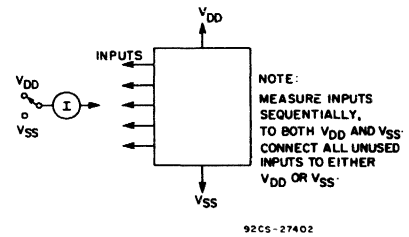


Fig. 17 — Input-leakage-current test circuit.

TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals. The block diagram of Fig. 18 is an example of a computer that processes 8 bits in parallel.

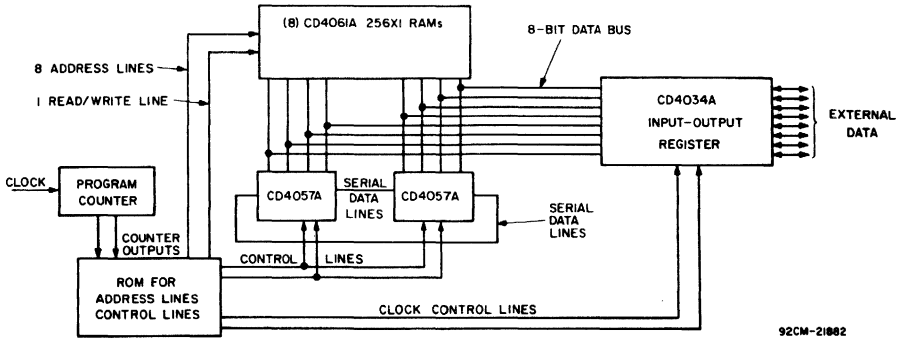


Fig. 18 — Example of computer organization using CD4057A.

CD4059A Types

COS/MOS Programmable Divide-by-"N" Counter

RCA-CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting-down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected. Whenever the master preset mode is used, control signals Kb=0 and Kc=0 must be applied for at least 3 full clock pulses. A "1" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "0". If the Latch Enable is "0", the output pulse will remain high for only 1 cycle of the clock-input signal.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig.1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due.

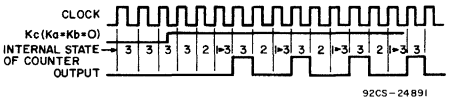
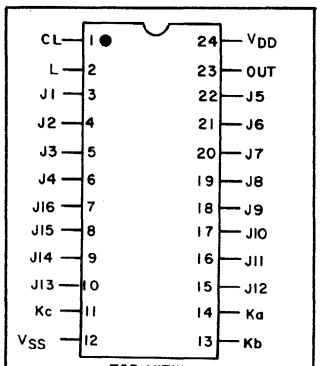


Fig.1 – Total count of 3.

As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. The CD4059A can also be used to perform the synthesizer "Fixed Divide-by-R" counting function. It is also useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.

The CD4059A series types are available in a 24-lead ceramic dual-in-line package, 24-lead dual-in-line plastic package, 24-lead ceramic flat pack, and in chip form.



TERMINAL DIAGRAM

Features:

- **Synchronous Programmable ÷ N Counter: N = 3 to 9999 or 15,999**
- **Presettable down-counter**
- **Fully static operation**
- **Mode-select control of initial decade counting function (÷ 10,8,5,4,2)**
- **T^2L drive capability**
- **Master preset initialization**
- **Latchable ÷ N output**
- **Quiescent current specified to 15 volts**
- **Max. input leakage current of 1 μA at 15 volts, full package-temperature range**
- **1 volt noise margin, full package-temperature range**
- **5-V and 10-V parametric ratings**

Applications

- **Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.**
- **Fixed or programmable frequency division**
- **"Time out" timer for consumer-application industrial controls**
- **Companion Application Note, ICAN-6374, "Application of the COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"**

OPERATING CONDITIONS AT T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	–	3	12	V
Clock Pulse Width	5 10	200 100	– –	ns
Clock Input Frequency	5 10	– –	1.5 3	MHz
Clock Input Rise and Fall Time	5 10	– –	15 5	ns

CD4059A Types

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC		CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES Min.	Typ.	Max.	UNITS
Propagation Delay Time; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	90	180	
Transition Time:	t_{THL}	5	–	35	70	ns
		10	–	20	40	
	t_{TLH}	5	–	100	200	
		10	–	50	100	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	–	MHz
		10	3	6	–	
Average Input Capacitance, C_I (any input)		–	–	5	–	pF

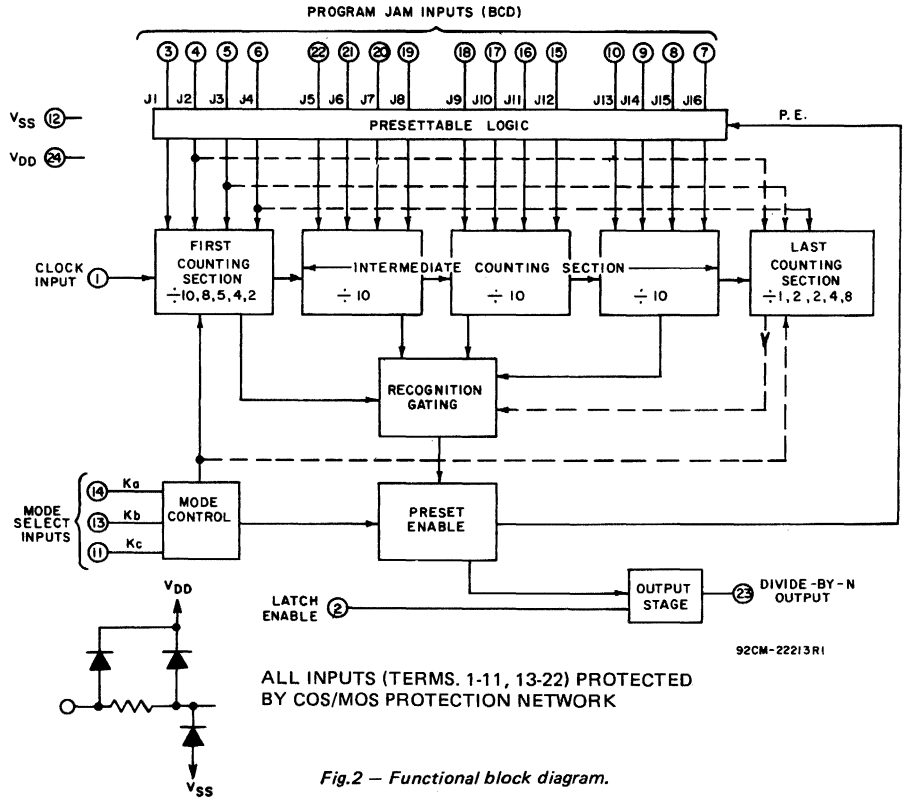


Fig.2 – Functional block diagram.

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{STG}) . . . . . −65 to 150°C

OPERATING-TEMPERATURE RANGE (T_A):
Package Types D,K,H . . . −55 to +125°C
Package Type E . . . . . −40 to + 85°C

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal) . −0.5 to + 15 V

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (Package Type E) . . . . 500 mW
For T_A = +60 to +85°C (Package Type E) Derate Linearly to 200 mW
For T_A = −55 to +100°C (Package Types D,K,H) . . 500 mW
For T_A = +100 to +125°C (Package Types D,K,H) Derate Linearly to 100 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = Full package-temperature range (All package types) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

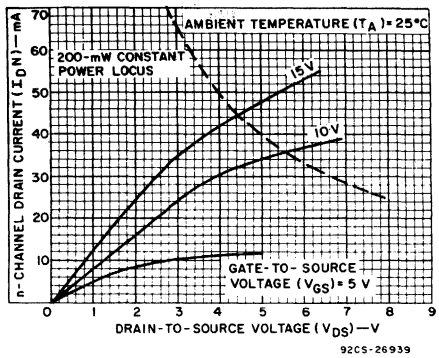


Fig.3 – Minimum output n-channel drain characteristics.

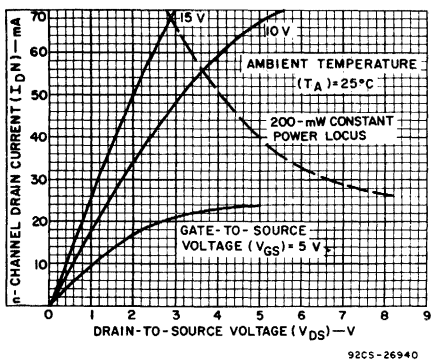


Fig.4 – Typical output n-channel drain characteristics.

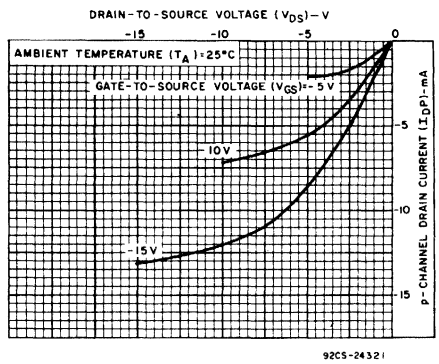


Fig.5 – Minimum output p-channel drain characteristics.

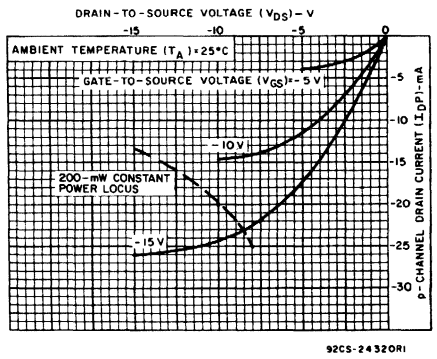


Fig.6 – Typical output p-channel drain characteristics.

CD4059A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E Packages* −55°	−40°	+85°	+125°	+25° Min.	+25° Typ.	+25° Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	–	0.02	10	μA
			10	20	20	200	400	–	0.02	20	
			15	–	–	–	–	–	–	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	–	V
			10	3				3	4.5	–	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	–	
			10	3				3	4.5	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High, V_{NMH} Min.	0.5		5	1							
	1		10	1							
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.4		5	2.5	2.3	1.6	1.4	2	4	–	mA
	0.5		10	5	4.7	3.3	2.8	4	9	–	
P-Channel (Source) I_{DP} Min.	2.5		5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	4.6		5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	9.5		10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
Input Leakage Current:* I_{IL}, I_{IH} Max.			15	±1					$\pm 10^{-5}$	±1	μA

* Any Input

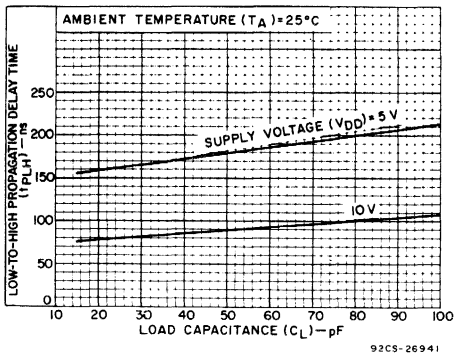


Fig.7 – Typical low-to-high propagation delay time vs. load capacitance.

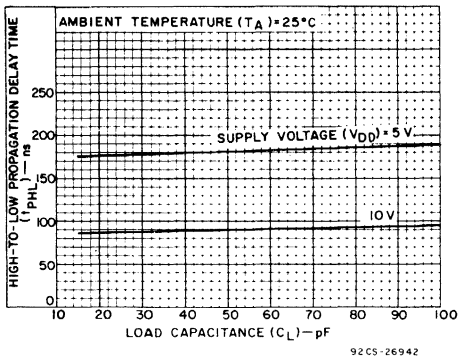


Fig.8 – Typical high-to-low propagation delay time vs. load capacitance.

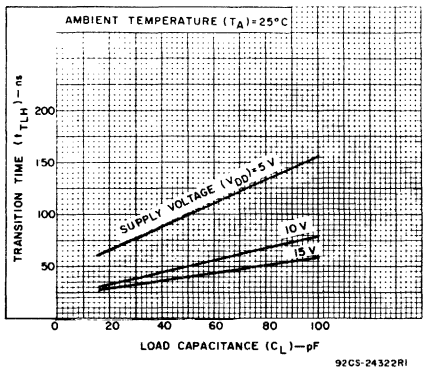


Fig.9 – Typical low-to-high transition time vs. load capacitance.

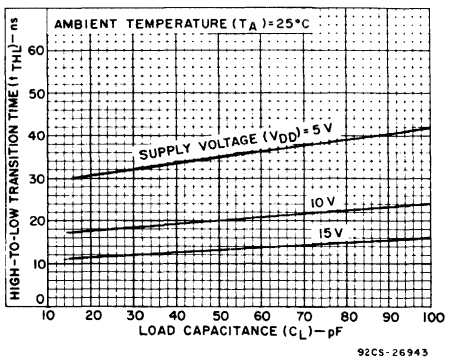


Fig.10 – Typical high-to-low transition time vs. load capacitance.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

CD4059A Types

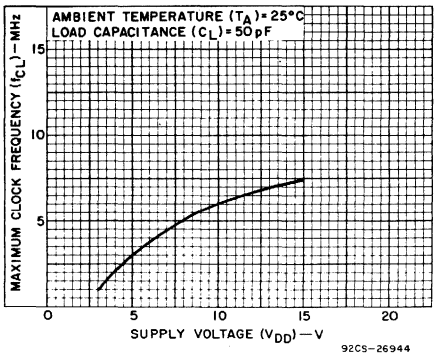


Fig.11 – Typical max. clock frequency vs. supply voltage.

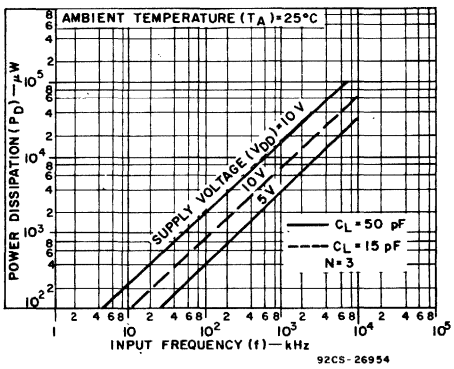


Fig.12 – Typical power dissipation vs. input frequency.

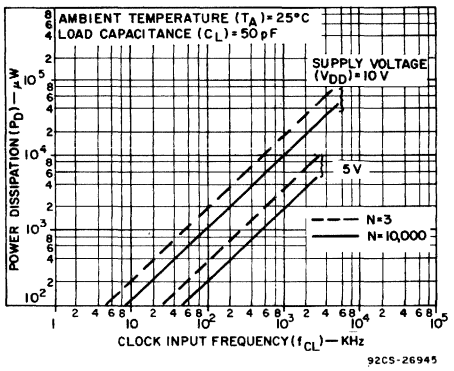


Fig.13 – Typical power dissipation vs. clock input frequency.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

N = [MODE*] [1000 x Decade 5 Preset + 100X Decade 4 Preset + 10X Decade 3 Preset + 1X Decade 2 Preset] + Decade 1 Preset (1)

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \quad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 | 8479

Mode, N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4			1	5			9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

B) N = 12382, Mode = 8

1547 + 6

8 | 12382

MODE SELECT = 8

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6			1	7			4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

C) N = 8479, Mode = 10

0847 + 9

10 | 8479

MODE SELECT = 10

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

9				7			4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

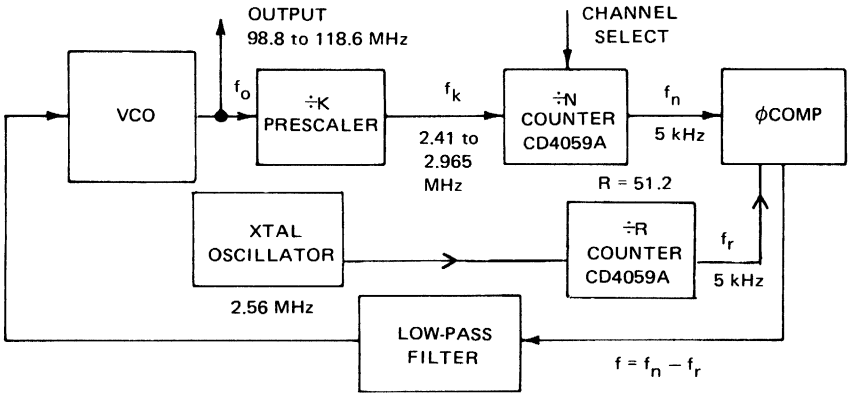
N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

CD4059A Types

APPLICATIONS

1) DIGITAL PLL FOR FM BAND SYNTHESIZER



Calculating Min & Max "N" Values:

Output Freq. Range (f_O) = 98.8 to 118.6 MHz
Channel Spacing Freq. (f_C) = 200 kHz
Division Factor (k) = 40

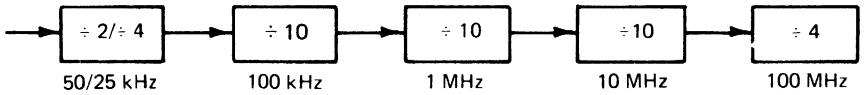
Reference Freq. (fr) $= \frac{f_c}{k} = \frac{200}{40}$ kHz = 5 kHz

$$f_k = \frac{f_o}{40} \qquad f_k Max. = \frac{118.6\ MHz}{40} = 2.965\ MHz; \quad f_k Min = \frac{98.8\ MHz}{40} = 2.47\ MHz$$

$$N = \frac{f_o}{f_c}$$

$$N_{Max} = \frac{118.6\ MHz}{200\ kHz} = 593 \qquad N_{Min} = \frac{98.8\ MHz}{200\ kHz} = 494 \qquad R = \frac{2.56\ MHz}{5\ kHz} = 512$$

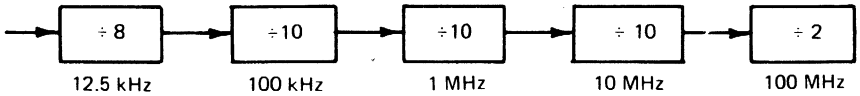
2) ÷N Counter Configuration for UHF – 220 to 400 MHz
Channel Spacing: 50 kHz or25 kHz



$$N_{Max} = \frac{400\ MHz}{25\ kHz} = 16{,}000 \qquad N_{Max} = \frac{400\ MHz}{50\ kHz} = 8{,}000$$

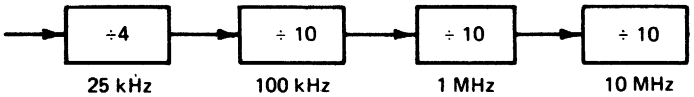
$$N_{Min} = \frac{220\ MHz}{25\ kHz} = 8{,}800 \qquad N_{Min} = \frac{220\ MHz}{50\ kHz} = 4{,}400$$

3) ÷N Counter Configuration for VHF – 116 to 160 MHz
Channel Spacing = 12.5 kHz



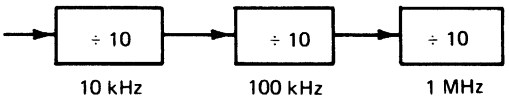
$$N_{Max} = \frac{160\ MHz}{12.5\ kHz} = 12{,}800 \qquad N_{Min} = \frac{116\ MHz}{12.5\ kHz} = 9{,}300$$

4)÷N Counter Configuration for VHF – 30 to 80 MHz
Channel Spacing: 25 kHz



$$N_{Max} = \frac{80\ MHz}{25\ kHz} = 3{,}200 \qquad N_{Min} = \frac{30\ MHz}{25\ kHz} = 1200$$

5)÷N Counter Configuration for AM – 995 to 2055 kHz
Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055\ kHz}{10\ kHz} = 205 \qquad N_{Min} = \frac{995\ kHz}{10\ kHz} = 99$$

CD4059A Types

Fig.14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

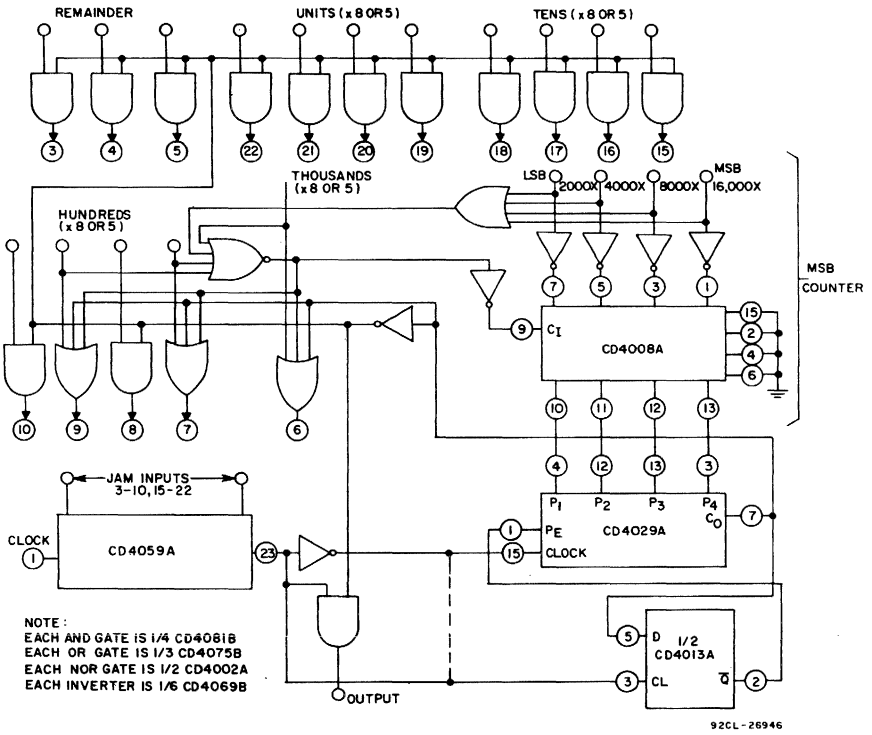


Fig.14 – BCD switch-compatible ÷N system of the most general kind.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I.. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

CD4059A Types

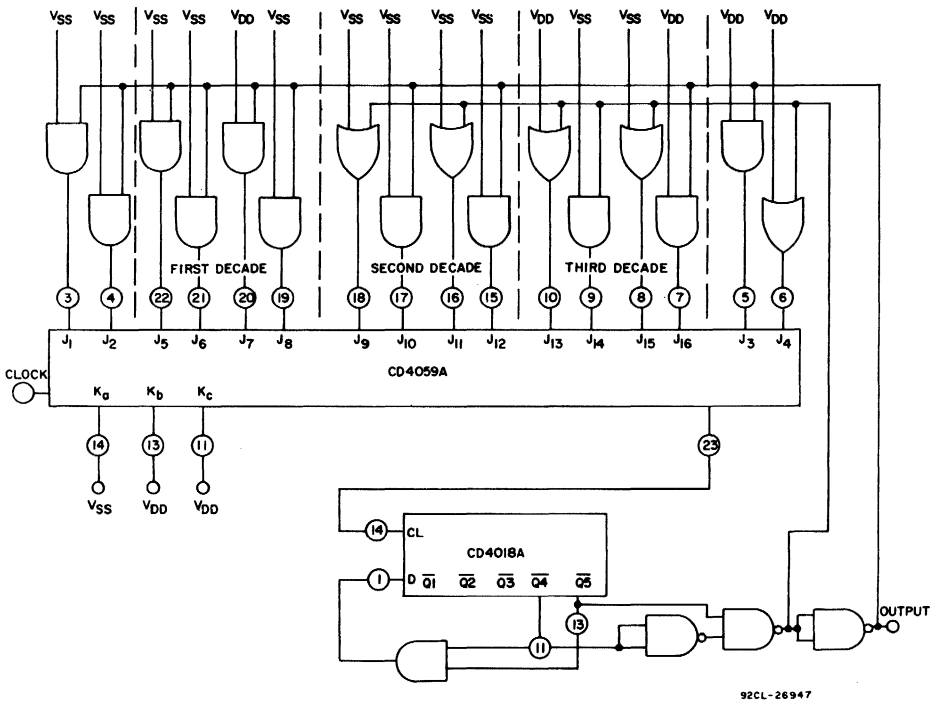


Fig.15 – Dividing by any number from 88,003 to 103,999.

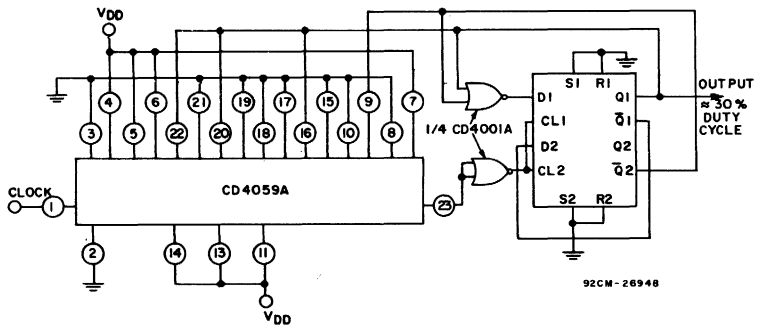


Fig.16 – Division by 47,690 in ÷2 mode.

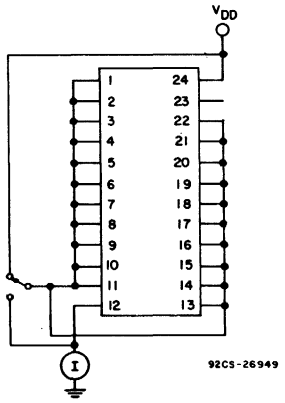


Fig.17 – Quiescent device current test circuit.

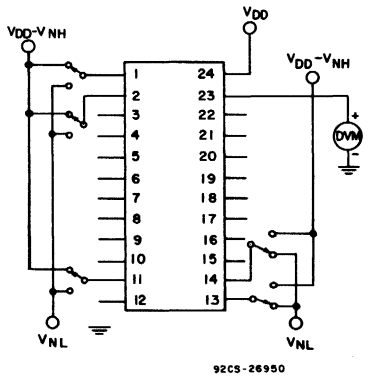


Fig.18 – Noise immunity test circuit.

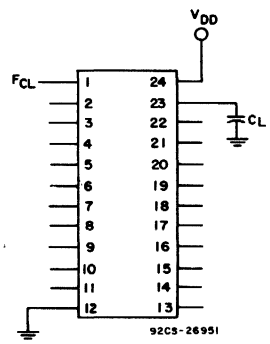


Fig.19 – Power dissipation test circuit (all ÷ modes).

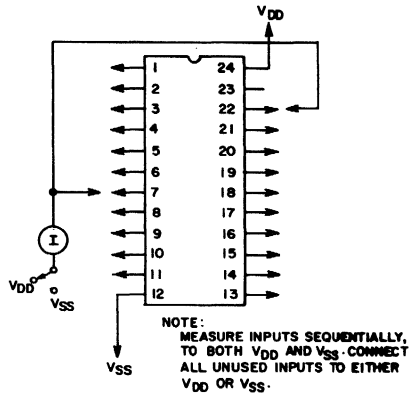


Fig.20 – Input leakage current test circuit.

CD4060A Types
COS/MOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_I(\phi_O)$. All inputs and outputs are fully buffered.

The CD4060A-Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

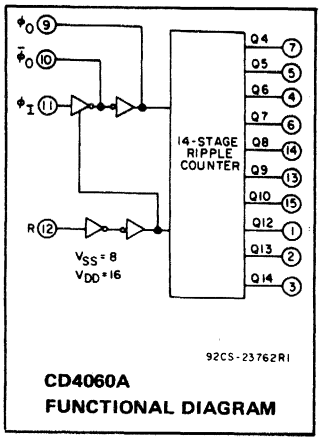
- **4-MHz operating frequency (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Common reset**
- **Fully static operation**
- **10 buffered outputs available**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**

Applications:

- **Timers**
- **Frequency dividers**



CD4060A FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E, Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y). . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E,Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D,F,K,H Packages		*E,Y Packages*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W f = 100 kHz	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	–	15	–	15	μs
	10	–	7.5	–	7.5	
Input-Pulse Frequency, f_ϕ	5	–	1	–	0.9	MHz
	10	–	3	–	2.75	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

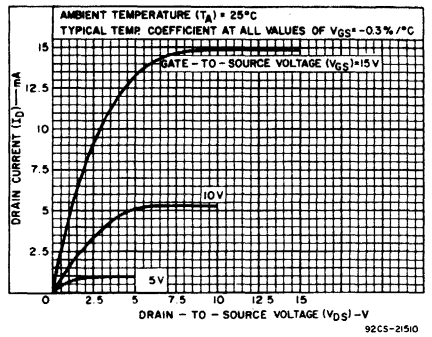


Fig. 1 – Typical n-channel drain characteristics.

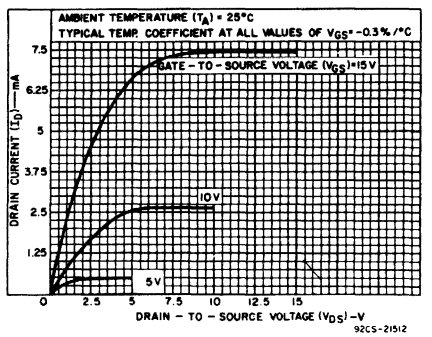


Fig. 2 – Minimum n-channel drain characteristics.

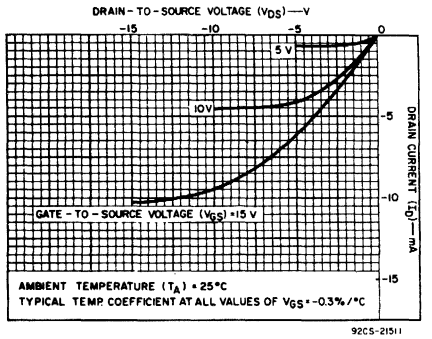


Fig. 3 – Typical p-channel drain characteristics.

CD4060A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,K,F,H Packages				E,Y Packages				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	10	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current:* n-Channel (Sink), I_DN Min.	0.5	–	5	0.22	0.36	0.18	0.125	0.21	0.36	0.18	0.15	mA
	0.5	–	10	0.44	0.75	0.36	0.25	0.42	0.75	0.36	0.3	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.15	-0.25	-0.125	-0.085	-0.145	-0.25	-0.125	-0.1	
	9.5	–	10	-0.3	-0.5	-0.25	-0.175	-0.29	-0.5	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

* Data not applicable to Terminal 9 or 10

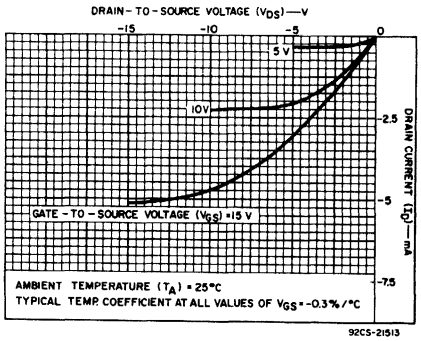


Fig. 4 – Minimum p-channel drain characteristics.

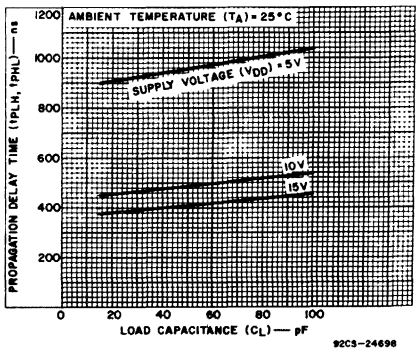


Fig. 5 – Typical propagation delay time vs. load capacitance (ϕ_I to Q4 output).

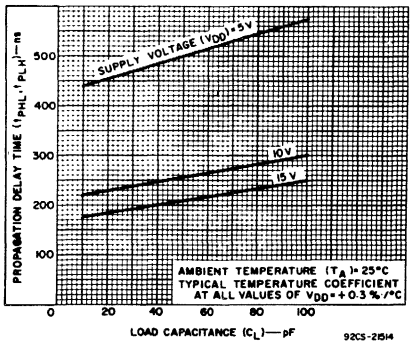


Fig. 6 – Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

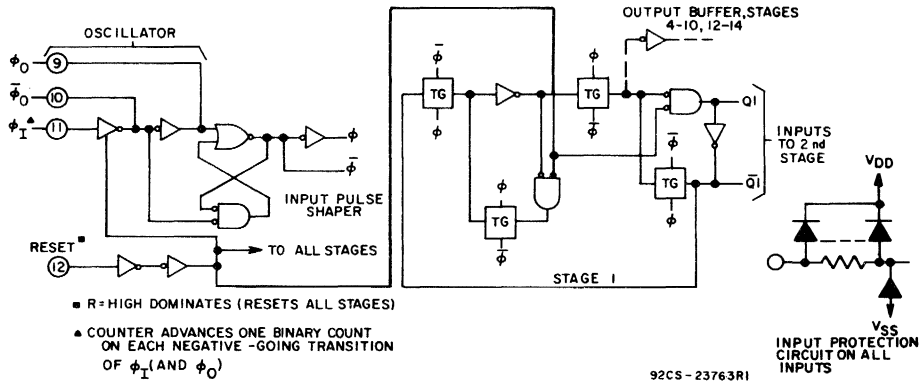


Fig. 7 – Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

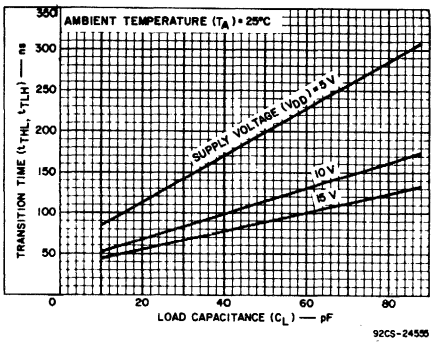


Fig. 8 – Typical output transition time vs. load capacitance.

CD4060A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D,F,K,H Packages			*E,Y Packages*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation									
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	900	1800	–	900	1900	ns
		10	–	450	900	–	450	950	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Min. Input-Pulse Width t_W	f=100 kHz	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Max. Input-Pulse Frequency, f_ϕ		5	1	1.75	–	0.9	1.75	–	MHz
		10	3	4	–	2.75	4	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

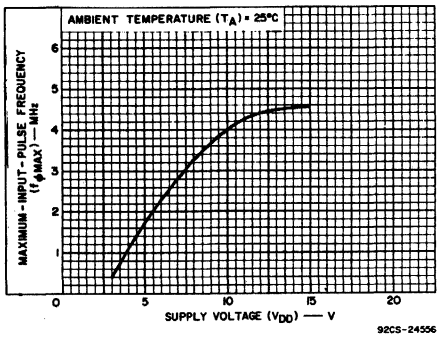


Fig. 9 – Typical maximum-input-pulse frequency vs. supply voltage.

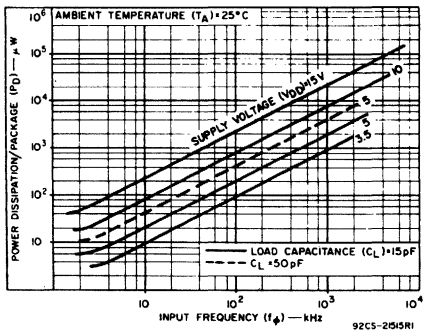


Fig. 10 – Typical dynamic power dissipation characteristics.

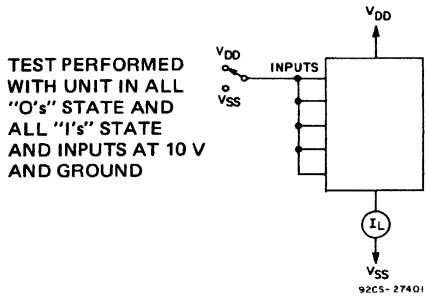


Fig. 11 – Quiescent-device current test circuit.

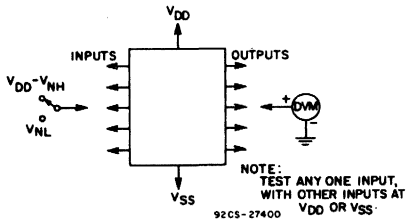


Fig. 12 – Noise-immunity test circuit.

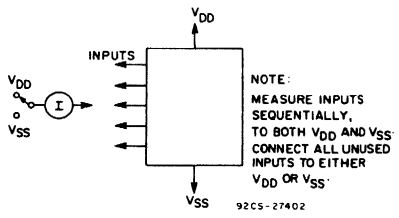


Fig. 13 – Input-leakage-current test circuit.

CD4062A Types
COS/MOS 200-Stage Dynamic Shift Register

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES K, T, H . . . . . -55 to +125° C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -55 to +100° C (PACKAGE TYPES K, T) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES K, T) . . Derate Linearly at 12 mW/° C to 200 mW

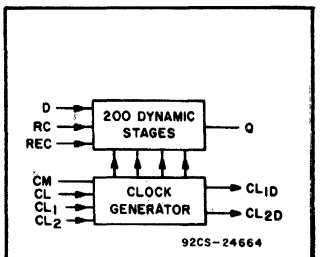
DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265° C



CD4062A
FUNCTIONAL DIAGRAM

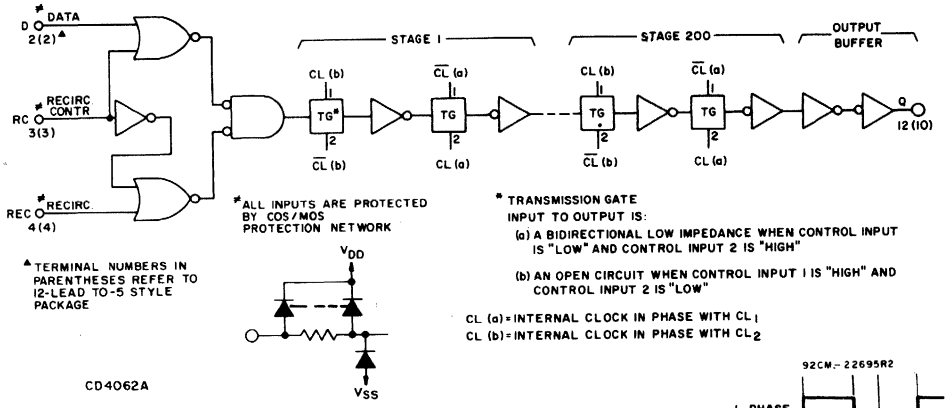


Fig. 1 – CD4062A logic block diagram.

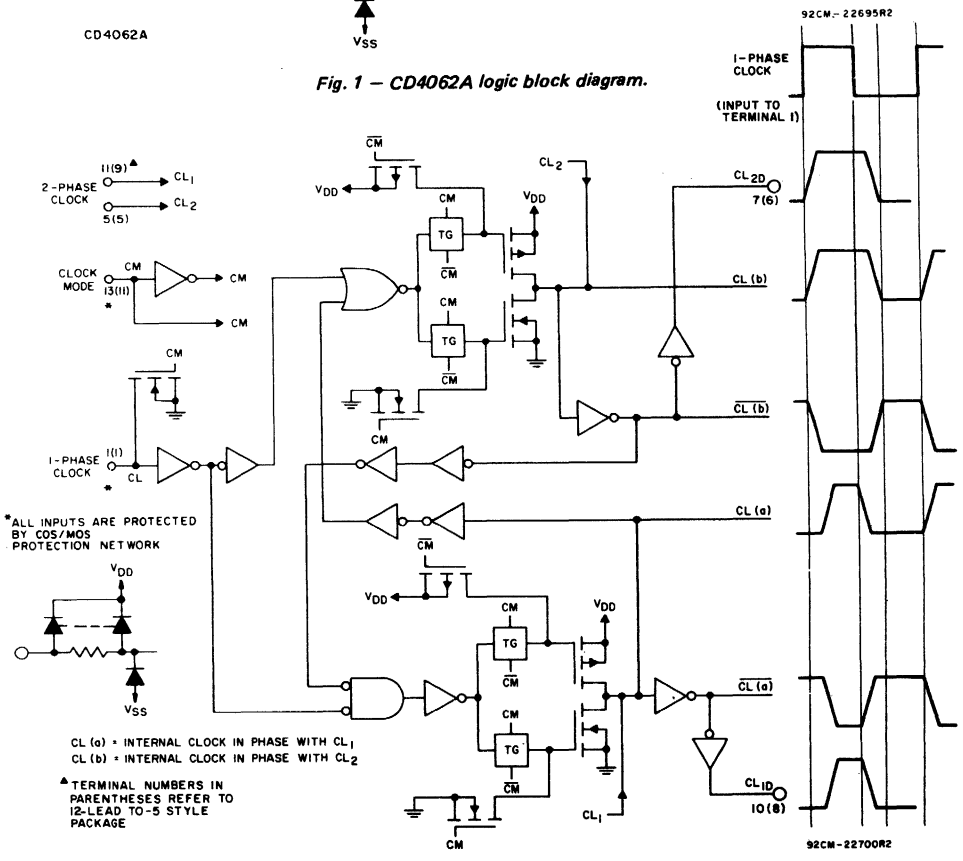


Fig. 2 – Clock circuit logic diagram.

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

The CD4062A-Series types are supplied in 16-lead flat packages (K suffix), 12-lead hermetic TO-5 packages (T suffix), and in chip form (H suffix).

Features:

- **Minimum shift rates over full temperature range–**

  Single-phase clock: $3 V \leq V_{DD} \leq 10 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

  Two-phase clock: $3 V \leq V_{DD} \leq 15 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

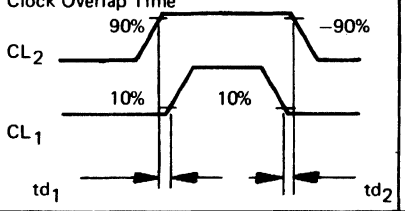
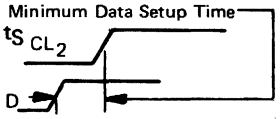
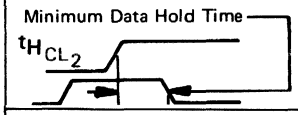
CD4062A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range):				
Single-Phase Clock		3	10	V
Two-Phase Clock		3	12	V
Clock Input Frequency, f_{CL}*	5	0.15	500	kHz
	10	0.15	1000	kHz
Clock Pulse Width, t_W*	5	250	66.7 X 10^6	ns
	10	500	66.7 X 10^6	ns
Clock Rise or Fall Times, t_rCL or t_fCL*	5	–	10	μs
	10	–	1	μs
Data Hold Time, t_H*	5	150	–	ns
	10	50	–	ns

* For single-phase clock, 50% duty cycle

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ≤ V_{DD} ≤ 15 V. See Figure 4.

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	MHz
Minimum Clock Input Frequency, f_{CL}	5	150	10	–	Hz
	10	150	10	–	Hz
Clock Overlap Time 		40	–	–	ns
Average Input Capacitance, C_I CL_1, CL_2		–	50	–	pF
Propagation Delays; t_{PHL}, t_{PLH} CL_1 to Q	5	–	250	500	ns
	10	–	100	200	ns
CL_1 to CL_{1D}	5	–	250	500	ns
CL_2 to CL_{2D}	10	–	100	200	ns
Minimum Data Setup Time 	5	–	150	300	ns
	10	–	50	100	ns
Minimum Data Hold Time 	5	–	–	0	ns
	10	–	–	0	ns
Clock Rise and Fall Times t_rCL_1, CL_2 t_fCL_1, CL_2			No Restrictions If Clock Overlap Requirement Is Met		

Features (Cont'd):

- **Low power dissipation**
  0.3 mW/bit at 1 MHz and 10 V
  0.04 mW/bit at 0.5 MHz and 5V
  (alternating 1-0 data pattern)
- **Data output TTL-DTL compatible**
- **Recirculating capability**
- **Delayed two-phase clock outputs available for cascading registers**
- **Asynchronous ripple-type presettable to all 1's or 0's**
- **Ultra-low-power-dissipation standby operation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time-delay circuits**
- **CRT refresh memory**
- **Long serial memory**

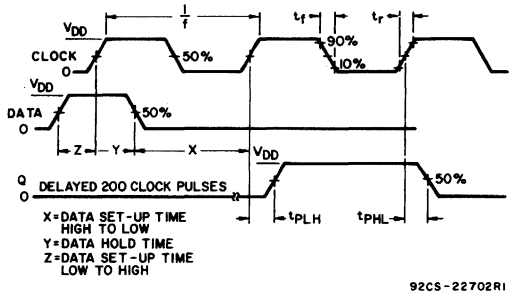


Fig. 3 – Timing diagram–single-phase clock.

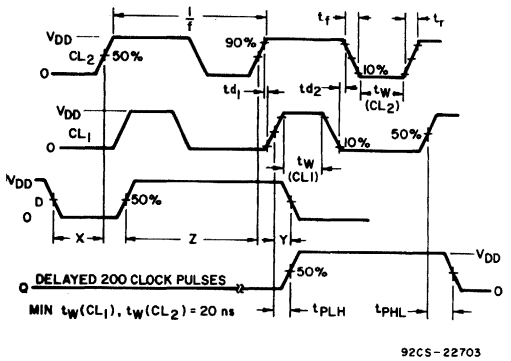


Fig. 4 – Timing diagram–two-phase clock.

CD4062A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)				UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	
Quiescent Device Current, I_L Max.	–	–	5	12	0.5	12	720	μA
	–	–	10	25	1	25	1500	
CM=High, CL_1=High, CL_2=Low	–	–	15	50	1	50	2000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max				V
	–	10	10	0 Typ.; 0.05 Max				
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.				
	–	0	10	9.95 Min.; 10 Typ.				
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.				V
	9	–	10	3 Min.; 4.5 Typ.				
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.				
	1	–	10	3 Min.; 4.5 Typ.				
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.				V
	9	–	10	1 Min.				
Inputs High, V_{NMH}	0.5	–	5	1 Min.				
	1	–	10	1 Min.				
Output Drive Current: N-Channel (Sink), I_DN Min. Q Output	0.4	–	4.5	1.6	2.6	1.3	0.91	mA
	0.5	–	10	5	8*	4	3.2	
CL_{1D}, CL_{2D}	0.5	–	5	0.87	1.4	0.7	0.49	
	0.5	–	10	2.2	3.6	1.8	1.26	
P-Channel (Source): I_DP Min. Q Output	4.5	–	5	-0.31	-0.5	-0.25	-0.17	mA
	2.5	–	5	-0.93	-1.5	-0.75	-0.52	
	9.5	–	10	-0.87	-1.4	-0.7	-0.49	
CL_{1D}, CL_{2D}	4.5	–	5	-0.43	-0.7	-0.35	-0.24	
	9.5	–	10	-1.1	-1.8	-0.9	-0.63	
Input Leakage Current, I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.				μA

* Maximum power dissipation rating ≤ 200 mW.

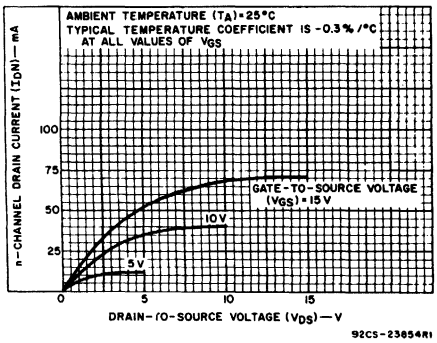


Fig. 5— Typical n-channel drain characterstics for Q output.

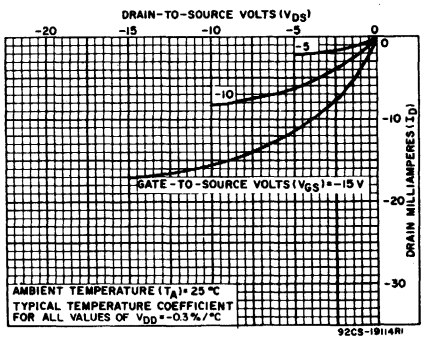


Fig. 6— Typical p-channel drain characteristics for Q output.

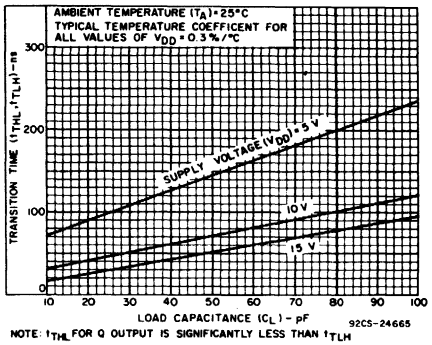


Fig. 7— Typical transition time vs. C_L for data outputs.

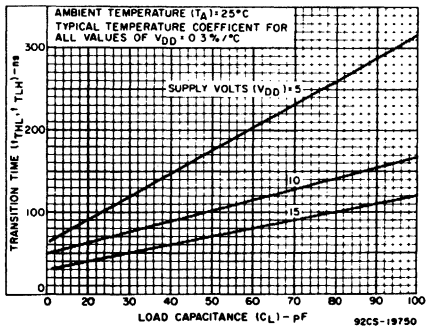
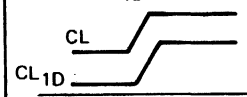
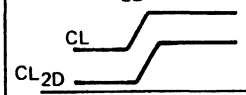
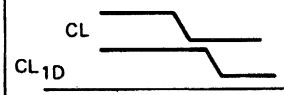
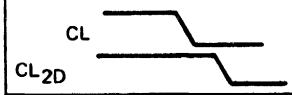
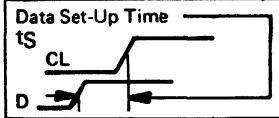
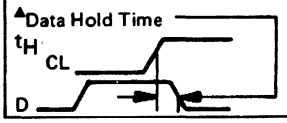


Fig. 8— Typical transition time vs. C_L for delayed clock output.

CD4062A Types

DYNAMIC CHARACTERISTICS AT T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ≤ V_{DD} ≤ 10 V (See Figure 3)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL} (50% Duty Cycle)	t_r, t_f=20 ns	5	0.5	1	–	MHz
		10	1	2	–	
Minimum Clock Input Frequency, f_{CL} (50% Duty Cycle)		5	150	10	–	Hz
		10	150	10	–	
Clock Rise and Fall Times** t_rCL, t_fCL		5	–	–	10	μs
		10	–	–	1	
Average Input Capacitance, C_I	All Inputs Except CL_1 and CL_2		–	5	–	pF
Propagation Delays: CL to Q		5	–	1000	2000	ns
		10	–	400	800	
CL to CL_{1D} (Positive Going) 	(50% Points)	5	–	750	1500	ns
		10	–	300	600	
CL to CL_{2D} (Positive Going) 	(50% Points)	5	–	500	1000	
		10	–	200	400	
CL to CL_{1D} (Negative Going) 	(50% Points)	5	–	450	900	
		10	–	175	350	
CL to CL_{2D} (Negative Going) 	(50% Points)	5	–	750	1500	
		10	–	300	600	
Transition Time: t_{TLH}, t_{THL} Q Output		5	–	100	200	ns
		10	–	50	100	
CL_{1D}, CL_{2D}		5	–	200	400	
		10	–	100	200	
Data Set-Up Time t_S 		5	–	–	0	ns
		10	–	–	0	
▲Data Hold Time t_H 		5	–	–	150	ns
		10	–	–	150	

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).

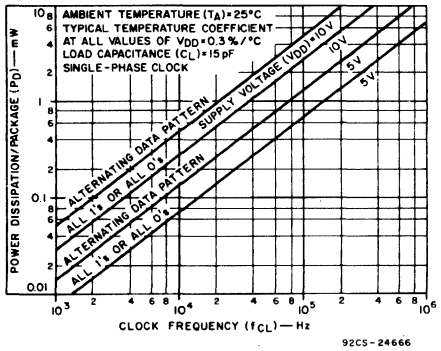


Fig. 9— Typical power dissipation vs. frequency.

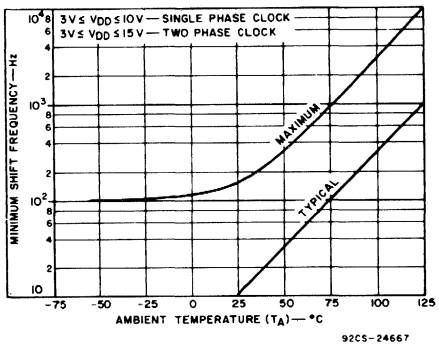


Fig. 10— Minimum shift frequency vs. ambient temperature.

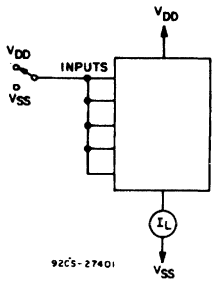


Fig. 11— Quiescent-device-current test circuit.

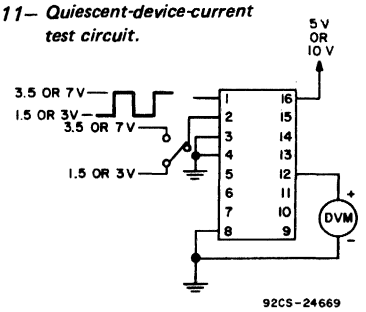


Fig. 12— Noise-immunity test circuit.

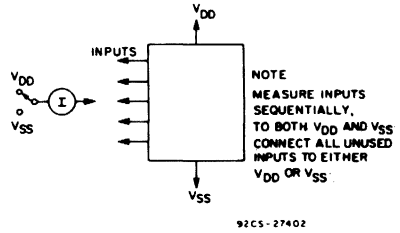


Fig. 13—Input-leakage-current test circuit.

CD4066A Types
COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

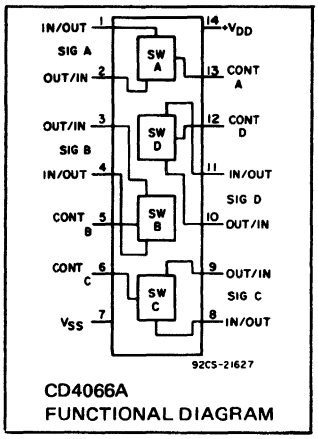
The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

The CD4066A is available in 14-lead ceramic dual-in line packages (D, F, Y suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **80Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 5 Ω over 15-V signal-input range**
- **ON resistance flat over full peak-to-peak signal range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: < 0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15-V**
- **Maximum control input leakage current of 1-μA at 15-V (Full package-temperature range)**



CD4066A
FUNCTIONAL DIAGRAM

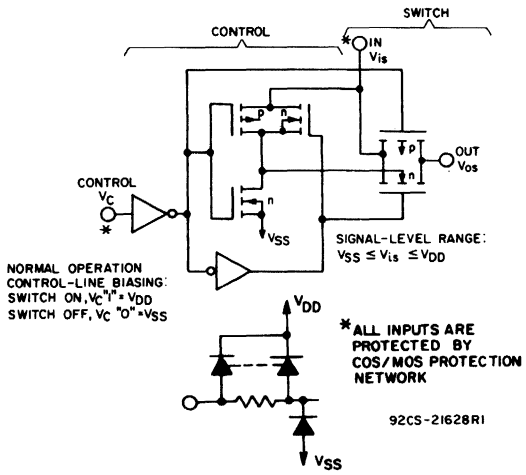


Fig. 1 — Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

SPECIAL CONSIDERATIONS — CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +125°C

OPERATING TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES (E, Y) . . . . . -40 to +85°C

DC SUPPLY VOLTAGE RANGE, V_{DD}

(Voltages referenced to V_{SS}) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE:

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) Derate Linearly at 12 mW/°C . . . . . 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C . . . 200 mW

DEVICE DISSIPATION PER SECTION:

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

ALL SIGNAL AND DIGITAL CONTROL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temperature Range)	—	3	12	V

CD4066A Types

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating** — **Modulator**
  - **Squelch control** — **Demodulator**
  - **Chopper** — **Commutating switch**
- **Digital signal switching/Multiplexing**
- **Transmission-gate logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*			LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages Values at -40°C, +25°C, +85°C Apply to E, Y Packages						UNITS
			V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Quiescent Device Current, I_L max. D, F, K, H Pkgs.			5	0.25	–	–	7.5	0.01	0.25	μA
			10	0.5	–	–	15	0.01	0.5	
			15	2	–	–	40	0.02	2	
E, Y Pkgs.			5	–	2.5	15	–	0.25	2.5	μA
			10	–	5	30	–	0.25	5	
			15	–	50	500	–	0.5	50	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})										
ON Resistance, R_{ON} Max.	$V_C = V_{DD}$	V_{SS}	V_{is}							Ω
	$R_L = 10k\Omega$*									
	+7.5	-7.5	-7.5 to +7.5	220	250	300	320	80	280	
	+15	0	0 to +15							
	+5	-5	-5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	-2.5	-2.5 to +2.5	3000	3500	5200	5500	270	5000	
	-5	0	0 to +5							
Δ_{ON} Resistance Between Any 2 of 4 Switches, ΔR_{ON}	$R_L = 10k\Omega$*									Ω
	+7.5 or +15	-7.5 or 0	+7.5 to -7.5 / +15 to 0	–	–	–	–	5	–	
	+5 or +10	-5 or 0	+5 to -5 / +10 to 0	–	–	–	–	10	–	
Sine Wave Response (Distortion)	+5	-5	5V p-p▲	–	–	–	–	0.4	–	%
	$R_L = 10k\Omega$, $f_{is} = 1kHz$									
Frequency Response Switch ON (Sine-Wave Input)	+5	-5	-5 p-p	–	–	–	–	40	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -3dB$									
Feedthrough-Switch OFF	+5	-5	-5 p-p	–	–	–	–	1.25	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -50dB$									
Input or Output Leakage – Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C = V_{SS}$	±7.5	–	–	–	–	±0.1	±100*	nA
	+7.5	-7.5								
	+5	-5	±5	–	–	–	–	±0.1	±100*	
Crosstalk Between Any 2 of the 4 Switches (f at –50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$		(A) 5V p-p	–	–	–	–	0.9	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)} = -50dB$									

* Limit determined by minimum feasible leakage measurement for automatic testing.

Δ Symmetrical about 0 volts. • For all test conditions.

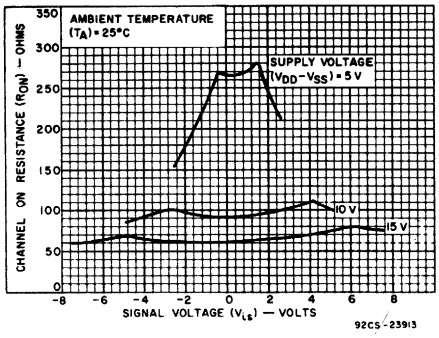


Fig. 2 (a) – Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

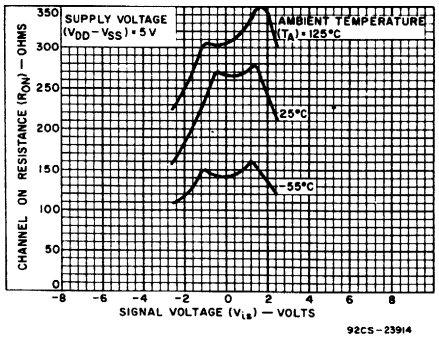


Fig. 2 (b) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

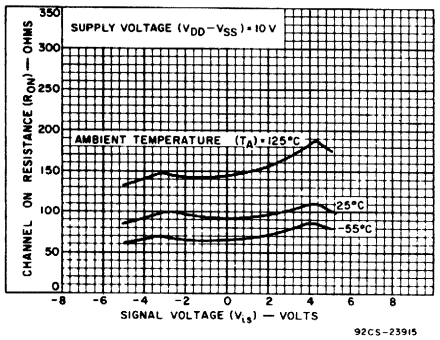


Fig. 2 (c) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

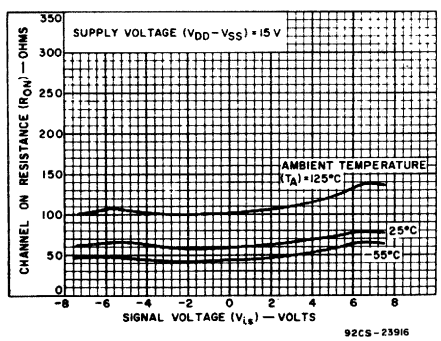


Fig. 2 (d) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

CD4066A Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*		LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages; Values at -40°C, +25°C, +85°C Apply to E, Y Packages						UNITS
		V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$, V_{SS} = GND, C_L = 15pF, V_{is} = sq. wave, t_r, t_f = 20 ns (Input Signal)	V_{DD} = 5	–	–	–	–	20	50	ns
		V_{DD} = 10	–	–	–	–	10	25	
Capacitance: Input, C_{is}	V_{DD} = +5, $V_{CC} = V_{SS}$ = -5		–	–	–	–	8	–	pF
Output, C_{os}			–	–	–	–	8	–	
Feedthrough, C_{ios}			–	–	–	–	0.5	–	
CONTROL (V_C)									
Noise Immunity, V_{NL} Min.	$V_{is} \leqslant V_{DD}$, I_{is} = 10μA, $V_{DD} - V_{SS}$ = 10		2	2	2	2	2 min 4.5	–	V
Input Leakage Current, I_{IL} Max.	$V_{is} \leqslant V_{DD}$, $V_{DD} - V_{SS}$ = 15, $V_C \leqslant V_{DD} - V_{SS}$		±1				$\pm 10^{-6}$	±1	μA
Crosstalk Control Input to Signal Output	$V_{DD} - V_{SS}$ = 10, V_C = 10 (sq. wave), $t_{rc} = t_{fc}$ = 20 ns	R_L = 10kΩ	–	–	–	–	50	–	mV
Propagation Delay, t_{pdC}		R_L=300kΩ, $V_{is} \leqslant 10$, C_L = 15pF	–	–	–	–	35	–	ns
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1kΩ, C_L=15pF, V_C = 10 (sq. wave), t_r, t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

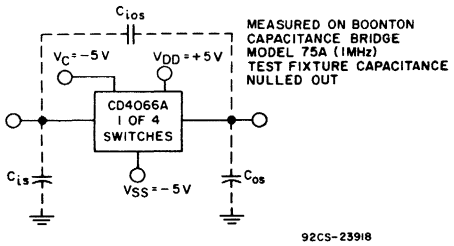


Fig. 6 – Capacitance test circuit.

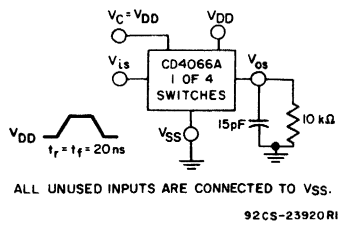


Fig. 8 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

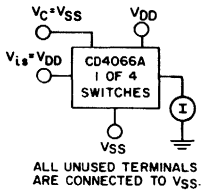


Fig. 7 – OFF switch input or output leakage.

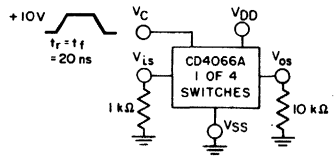


Fig. 9 – Crosstalk-control input to signal output.

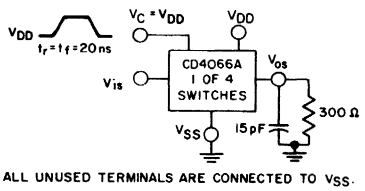


Fig. 11 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

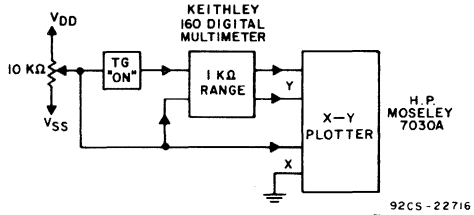


Fig. 3 – Channel ON resistance measurement circuit.

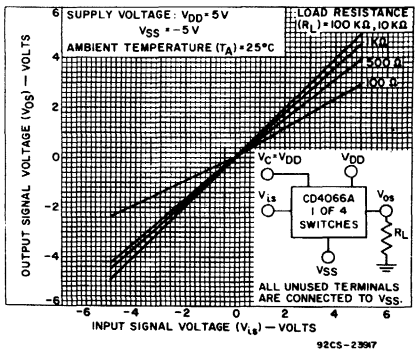


Fig. 4 – Typical ON characteristics for 1 of 4 channels.

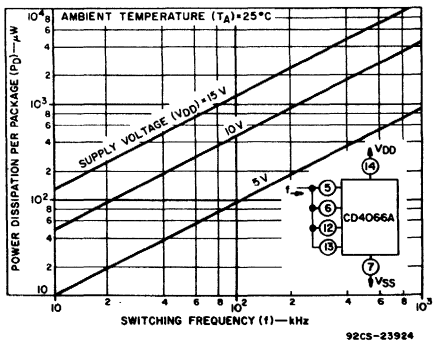


Fig. 5 – Power dissipation per package vs. switching frequency.

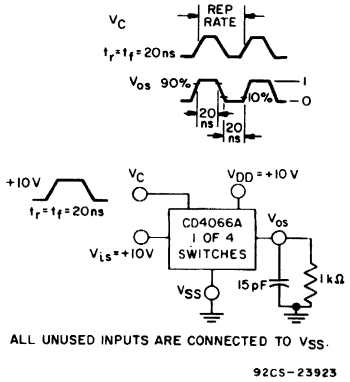


Fig. 10 – Maximum allowable control input repetition rate.

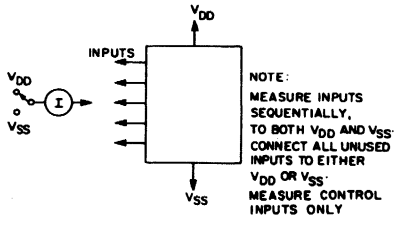


Fig. 12 – Input leakage current test circuit.

CD4000B, CD4001B, CD4002B, CD4025B Types

COS/MOS NOR Gates

High-Voltage Types (3-to-20-Volt Rating)
Dual 3 Input
plus Inverter—CD4000B
Quad 2 Input—CD4001B
Dual 4 Input—CD4002B
Triple 3 Input—CD4025B

Features:

- **Standard "B"-Series symmetrical output drive**
- **Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

The RCA-CD4000B, CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates.

The CD4000B, CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

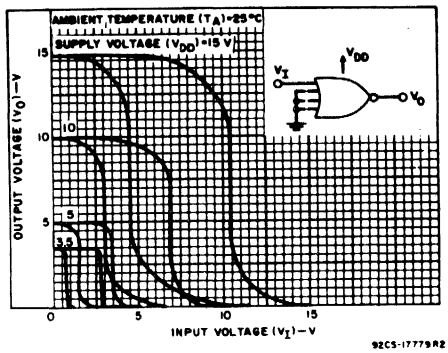


Fig. 1 – Minimum & maximum voltage transfer characteristics.

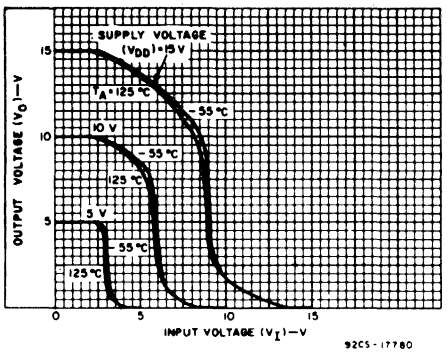
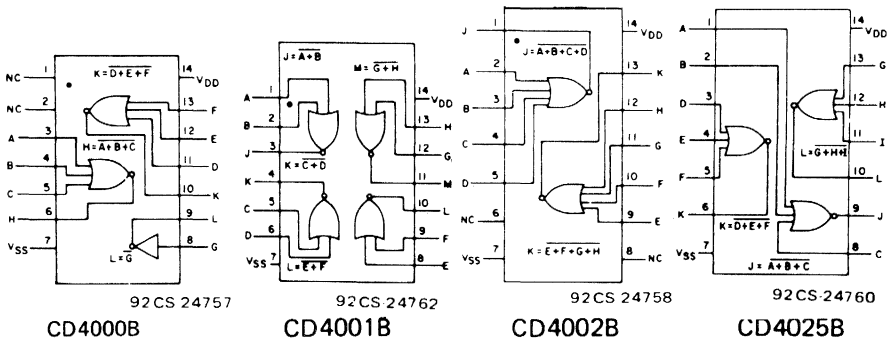


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

FUNCTIONAL DIAGRAMS



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance, C_I	Any Input		5	–	pF

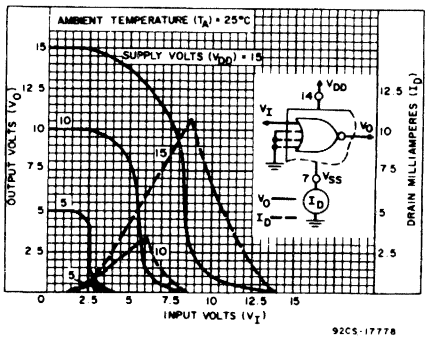


Fig. 3 – Typical current & voltage transfer characteristics.

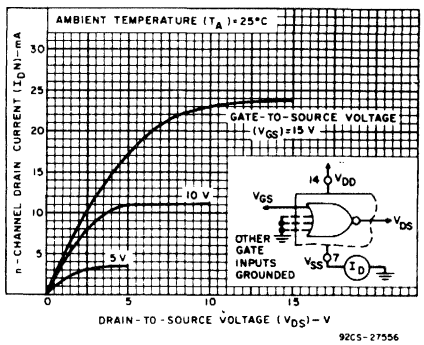


Fig. 4 – Typical output-N-channel drain characteristics.

CD4000B, CD4001B, CD4002B, CD4025B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, K, F, H Packages Values at -40, +25, +85 Apply to E, Y Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High-Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.1	–	5	1				1	2.25	–	V
	8.2	–	10	2				2	4.5	–	
	12.3	–	15	3				3	6.75	–	
Inputs High V_{NH} Min.	0.9	–	5	1				1	2.25	–	
	1.8	–	10	2				2	4.5	–	
	2.7	–	15	3				3	6.75	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA

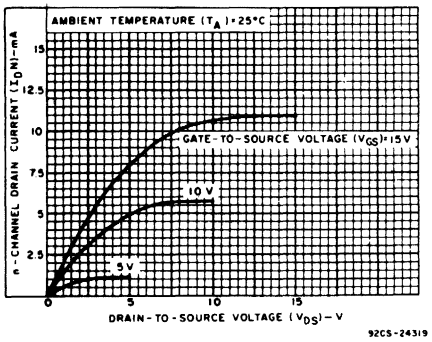


Fig. 5 – Minimum output-N-channel drain characteristics.

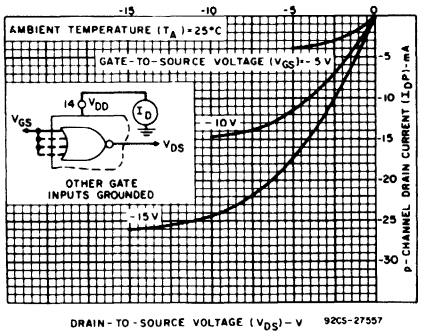


Fig. 6 – Typical output-P-channel drain characteristics.

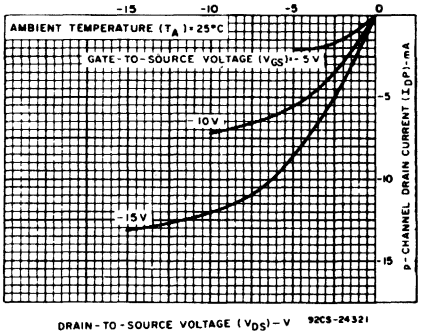


Fig. 7 – Minimum output-P-channel drain characteristics.

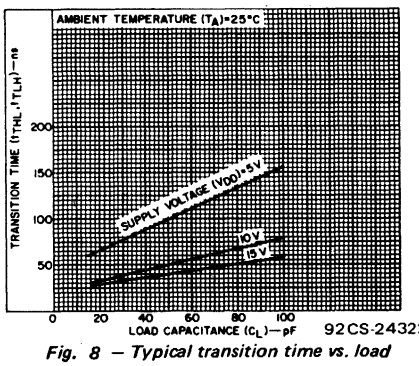


Fig. 8 – Typical transition time vs. load capacitance.

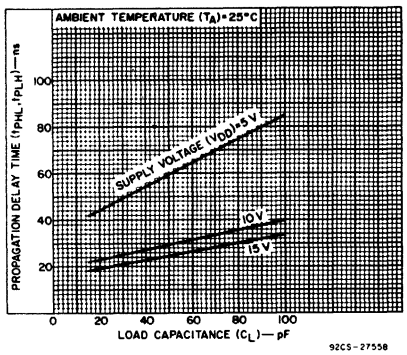


Fig. 9 – Typical propagation delay time vs. load capacitance.

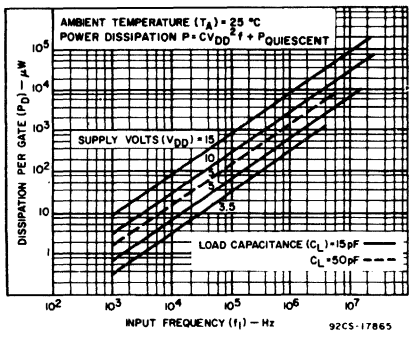


Fig. 10 – Typical dissipation characteristics.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

CD4008B Types
COS/MOS 4-Bit Full Adder

With Parallel Carry Out

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

The RCA-CD4008B types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008B's. CD4008B inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. CD4008B outputs include the four sum bits, S_1 to S_4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

The CD4008B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **4 sum outputs plus parallel look-ahead carry-output**
- **Standard "B"-Series symmetrical output drive**
- **High-speed operation—sum in-to-sum out, 100 ns typ.; carry in-to-carry out, 55 ns typ. at V_{DD} = 10 V, C_L = 50 pF**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 = μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Binary addition/arithmetic units**

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D,K,F,H Packages; Values at -40, +25, +85 Apply to E,Y Packages: -55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	UNITS
Quiescent Device Current, I_L Max	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	200	200	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05					0	0.05	
High-Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA

TRUTH TABLE

A_i	B_i	C_i	C_0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

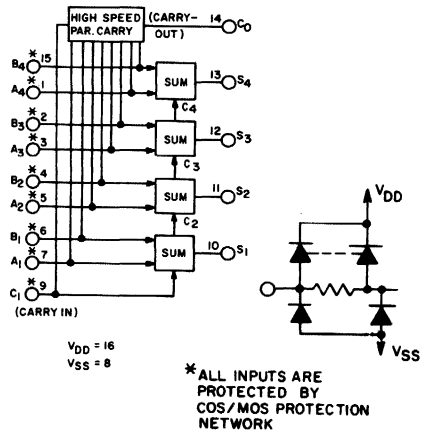


Fig. 1 – CD4008B logic diagram.

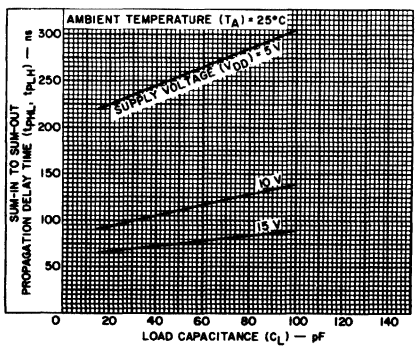


Fig. 2 – Typical sum-in to sum-out propagation delay time vs. load capacitance.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

CD4008B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} Sum In to Sum Out	5	255	510	ns
	10	110	220	
	15	75	150	
Carry In to Sum Out	5	185	270	ns
	10	80	160	
	15	60	120	
Sum In to Carry Out	5	240	480	ns
	10	100	200	
	15	75	150	
Carry In to Carry Out	5	115	230	ns
	10	55	110	
	15	40	80	
Output Transition Time: t_{PHL}, t_{PLH} All Outputs	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_I (Any Input)	—	5	—	pF

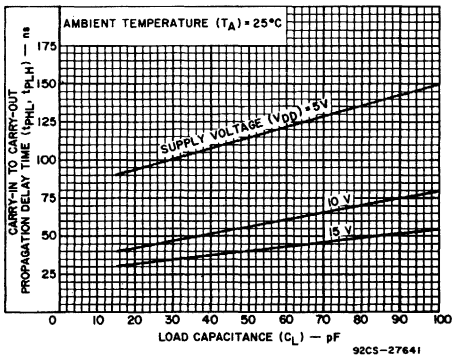


Fig. 3 — Typical carry-in to carry-out propagation delay time vs. load capacitance.

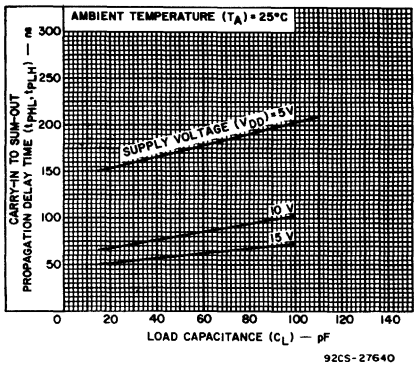


Fig. 4 — Typical carry-in to sum-out propagation delay time vs. load capacitance.

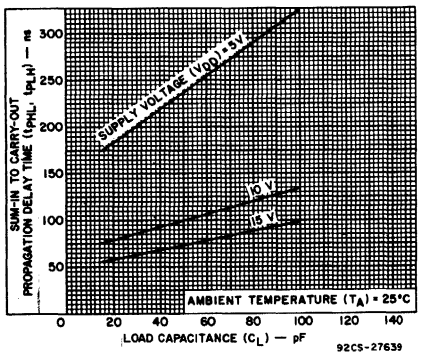


Fig. 5 — Typical sum-in to carry-out propagation delay time vs. load capacitance.

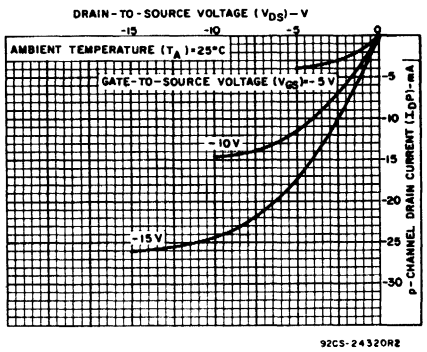


Fig. 6 — Typical output p-channel drain characteristics.

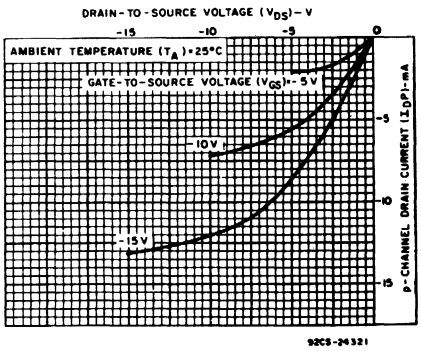


Fig. 7 — Minimum output p-channel drain characteristics.

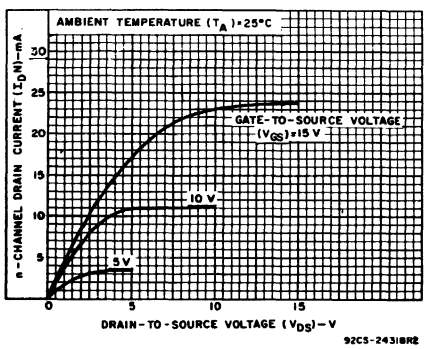


Fig. 8 — Typical output n-channel drain characteristics.

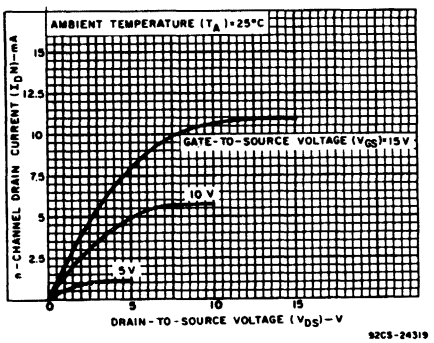


Fig. 9 — Minimum output n-channel drain characteristics.

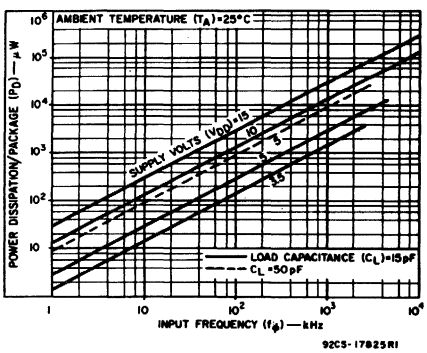


Fig. 10 — Typical dissipation characteristics.

CD4009B, CD4010B Types

COS/MOS Hex Buffers/Converters

High-Voltage Types (3-to-20-Volt Rating)

Inverting Type: CD4009B
Non-Inverting Type: CD4010B

The RCA-CD4009B and CD4010B Hex Buffer/Converters may be used as COS/MOS to TTL or DTL logic-level converters or COS/MOS high-sink-current drivers.

The CD4049B and CD4050B are preferred hex buffer replacements for the CD4009B and CD4010B, respectively, in all applications except multiplexers. For applications not requiring high sink current or voltage conversion, the CD4069B Hex Inverter is recommended.

The CD4009B and CD4010B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packs (K suffix), and in chip form (H suffix).

Applications:

- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter
- Multiplexer – 1 to 6 or 6 to 1

Features:

- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings
- High sink current for driving 2 TTL loads
- High-to-low level logic conversion

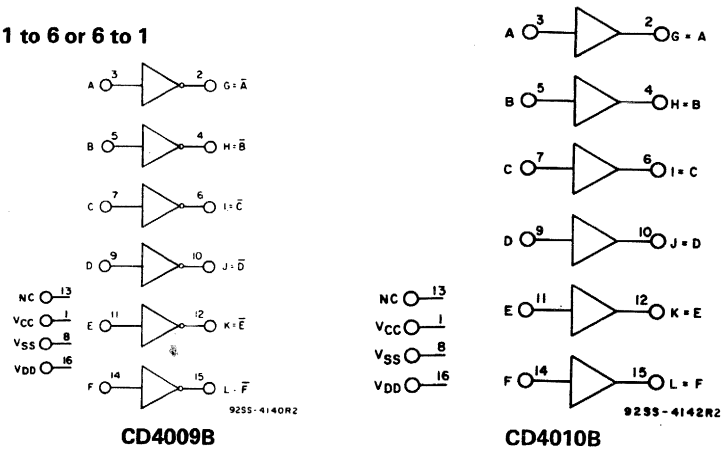


Fig.1 – Logic diagrams.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}, V_{CC})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

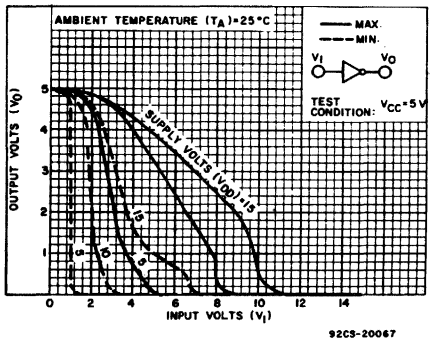


Fig. 2 – Minimum & maximum voltage transfer characteristics – CD4009B.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range: V_{DD}, V_{CC} (For T_A = Full Package Temperature Range)	3	18	V
Input Voltage Range (V_S)	V_{CC}*	18	V

*The CD4009 and CD4010 have high-to-low level voltage conversion capability but not low-to-high level, therefore it is recommended that $V_{DD} \geq V_I \geq V_{CC}$.

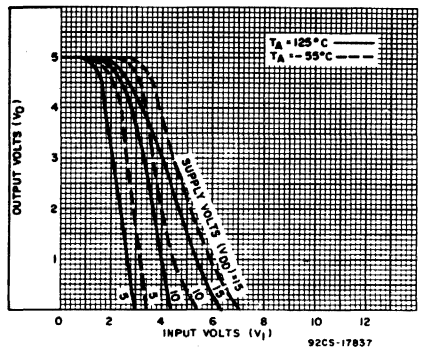


Fig. 3 – Typical voltage transfer characteristics as function of temp. – CD4009B.

CD4009B, CD4010B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) VALUES AT −55,+25,+125 APPLY TO D,K,F,H PACKAGES VALUES AT −40,+25,+85 APPLY TO E,Y PACKAGES							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{CC}* (V)	−55	−40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, I_L Max	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	5	3.75	3.6	2.4	2.1	3	4	–	mA
	0.5	–	10	10	9.6	6.4	5.6	8	10	–	
	1.5	–	15	30	40	19	16	24	36	–	
P-Channel (Source), I_{DP} Min.	4.6	–	5	-0.25	-0.^3	-0.18	-0.15	-0.2	-0.4	–	
	2.5	–	5	-1	-0.9	-0.65	-0.58	-0.8	-1.6	–	
	9.5	–	10	-0.55	-0.5	-0.38	-0.33	-0.45	-0.9	–	
	13.5	–	15	-1.65	-1.6	-1.25	-1.1	-1.5	-3	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min. CD4010B	3.6	–	5	1.5				1.5	2.25	–	V
	7.2	–	10	3				3	4.5	–	
	10.8	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min. All Types	1.4	–	5	1.5				1.5	2.25	–	
	2.8	–	10	3				3	4.5	–	
	4.2	–	15	4.5				4.5	6.75	–	
Inputs Low V_{NL} Min. CD4009B	3.6	–	5	1				1	1.5	–	
	7.2	–	10	2				2	3	–	
	10.8	–	15	2.25				2.25	3.5	–	
Noise Margin: Inputs Low, V_{NML} Min. CD4010B	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min CD4010B	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

*$V_{CC} = V_{DD}$

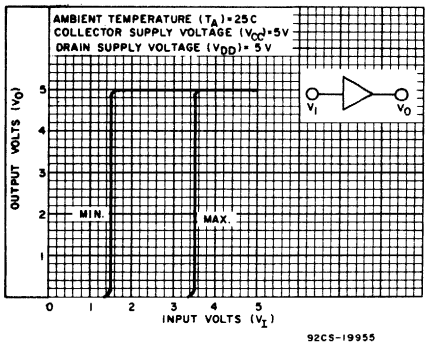


Fig. 4 — Minimum & maximum voltage transfer characteristics (V_{DD} = 5) — CD4010B.

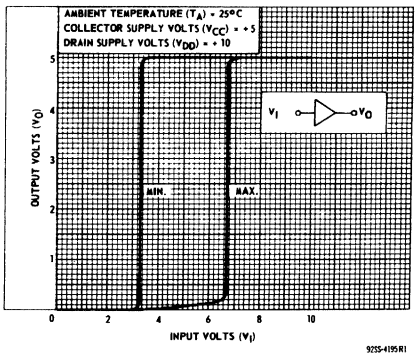


Fig. 5 — Minimum & maximum voltage transfer characteristics (V_{DD} = 10) — CD4010B.

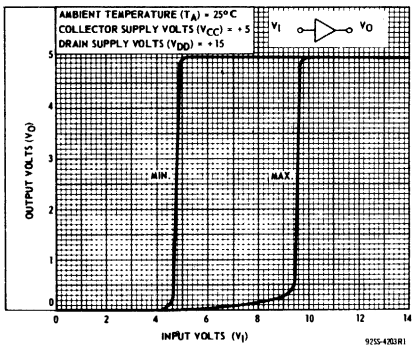


Fig. 6 — Minimum & maximum voltage transfer characteristics (V_{DD} = 15) — CD4010B.

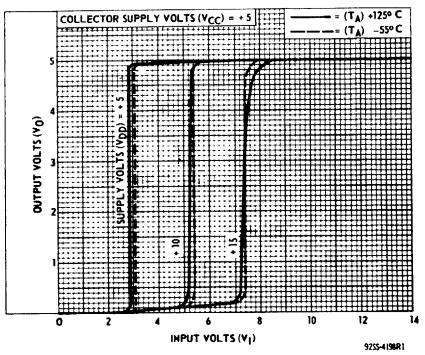


Fig. 7 — Typical voltage transfer characteristics as a function of temperature —CD4010B.

CD4009B, CD4010B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A=25°C; Input t_r, t_f=20 ns, C_L=50 pF, R_L=200 KΩ*

CHARACTERISTIC	CONDITIONS V_{DD} (V)	V_I (V)	V_{CC} (V)	LIMITS ALL PKGS TYP.	MAX.	UNIT
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	5	70	140	
	10	10	10	40	80	
CD4009B	10	10	5	35	70	ns
	15	15	15	30	60	
	15	15	5	30	60	
	5	5	5	100	200	
	10	10	10	50	100	
CD4010B	10	10	5	50	100	ns
	15	15	15	35	70	
	15	15	5	35	70	
High-to-Low, t_{PHL}	5	5	5	30	60	
	10	10	10	20	40	
CD4009B	10	10	5	15	30	ns
	15	15	15	15	30	
	15	15	5	10	20	
	5	5	5	65	130	
	10	10	10	35	70	
CD4010B	10	10	5	30	70	ns
	15	15	15	25	50	
	15	15	5	20	40	
Transition Time: Low-to-High, t_{TLH}	5	5	5	150	350	
	10	10	10	75	150	ns
	15	15	15	55	110	
High-to-Low, t_{THL}	5	5	5	35	70	
	10	10	10	20	40	ns
	15	15	15	15	30	
Input Capacitance, C_I CD4009B	–	–	–	15	–	
CD4010B	–	–	–	5	–	pF

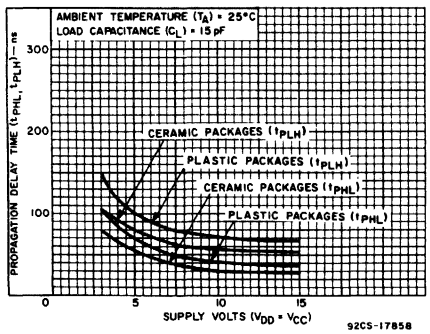


Fig. 8 — Max. propagation delay time vs. V_{DD} — CD4010B.

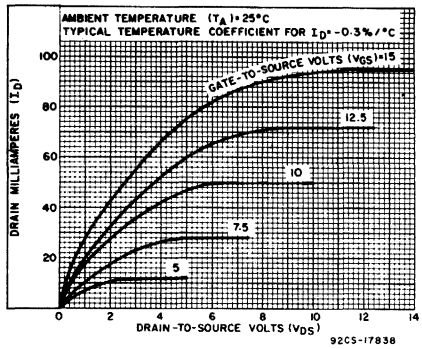


Fig. 9 — Typical n-channel drain characteristics — CD4009B, CD4010B.

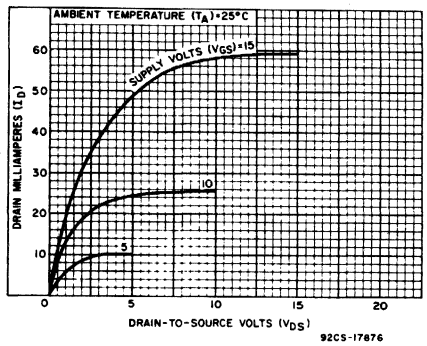


Fig. 10 — Minimum n-channel drain characteristics.

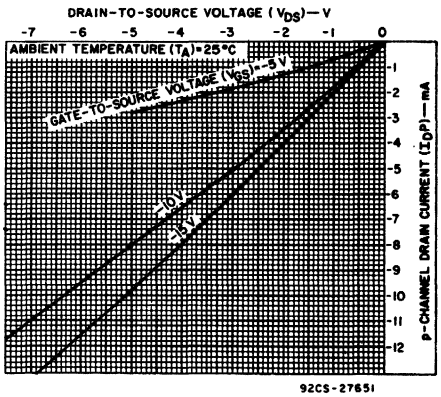


Fig. 11 — Typical output p-channel drain characteristics.

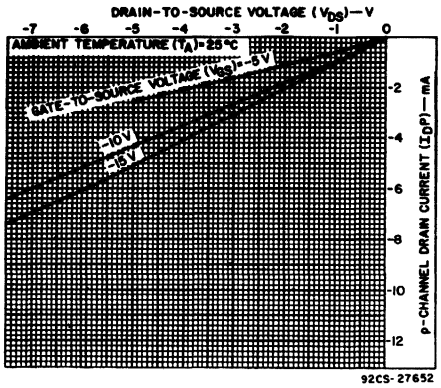


Fig. 12 — Minimum output p-channel drain characteristics.

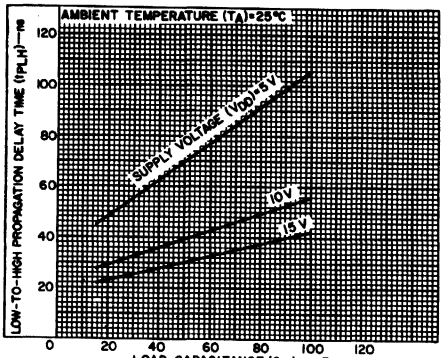


Fig. 13 — Typical low-to-high propagation delay time vs. load capacitance (CD4009B).

CD4009B, CD4010B Types

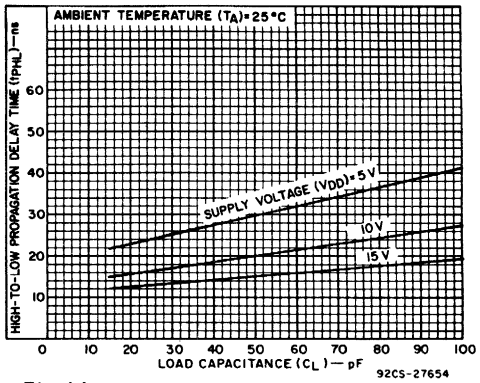


Fig. 14 — Typical high-to-low propagation delay time vs. load capacitance (CD4009B).

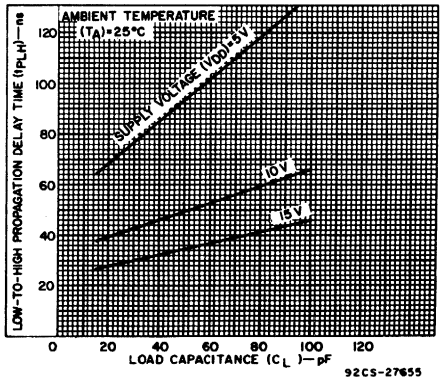


Fig. 15 — Typical low-to-high propagation delay time vs. load capacitance (CD4010B).

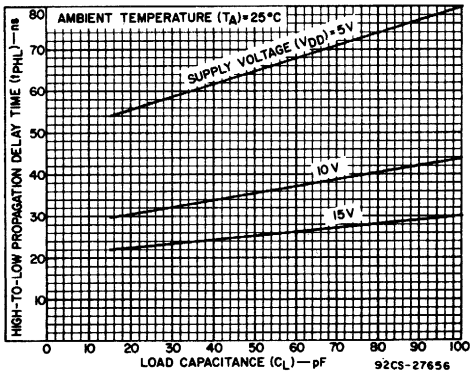


Fig. 16 — Typical high-to-low propagation delay time vs. load capacitance (CD4010B).

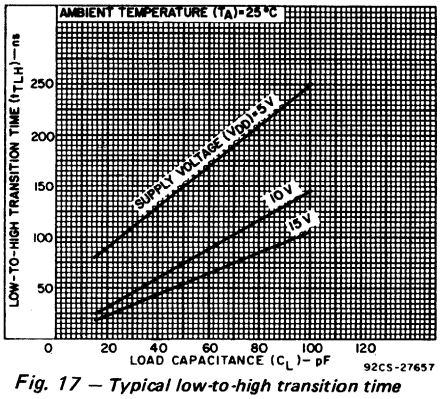


Fig. 17 — Typical low-to-high transition time vs. load capacitance.

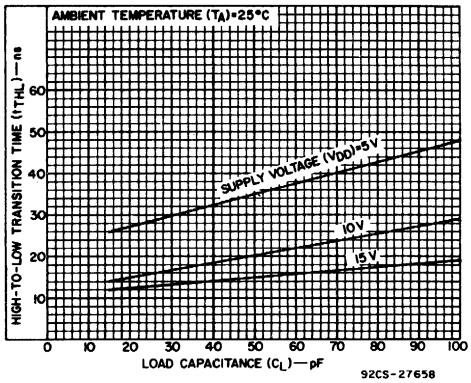


Fig. 18 — Typical high-to-low transition time vs. load capacitance.

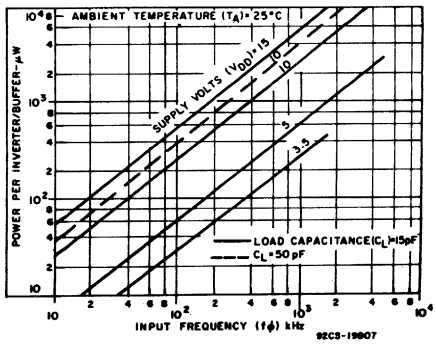


Fig. 19 — Typical dissipation characteristics.

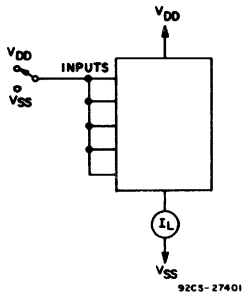


Fig. 20 — Quiescent device current test circuit.

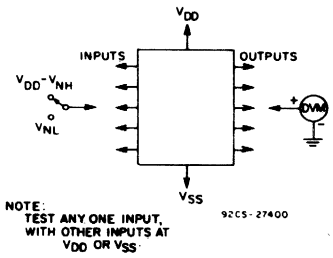


Fig. 21 — Noise immunity test circuit.

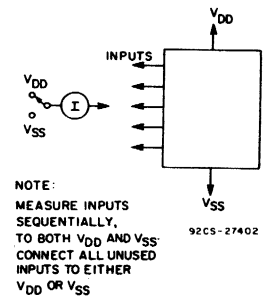


Fig. 22 — Input leakage current test circuit.

CD4011B, CD4012B, CD4023B Types

COS/MOS NAND Gates

Quad 2 Input—CD4011B
Dual 4 Input—CD4012B
Triple 3 Input—CD4023B

The RCA-CD4011B, CD4012B, and CD4023B NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates.

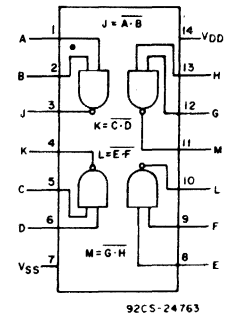
The CD4011B, CD4012B, and CD4023B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

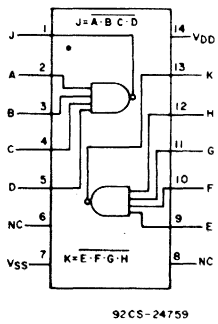
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

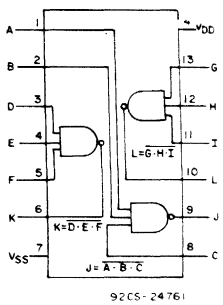
CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range (over full temp. range)	3	18	V



CD4011B



CD4012B



CD4023B

Fig. 1 — Functional diagrams.

Features:

- 5-V, 10-V, and 15-V parametric ratings
- Standard "B" Series symmetrical output drive
- Propagation delay time = 30 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)

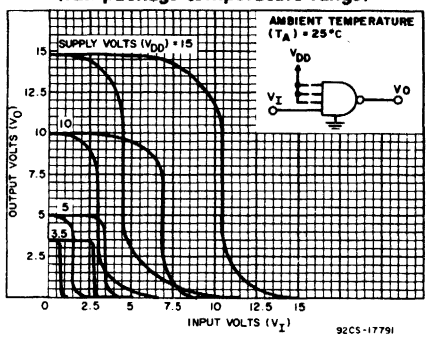


Fig. 2 — Minimum & maximum voltage transfer characteristics.

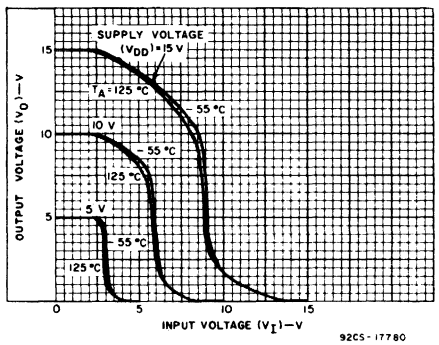


Fig. 3 — Typical voltage transfer characteristics as a function of temperature.

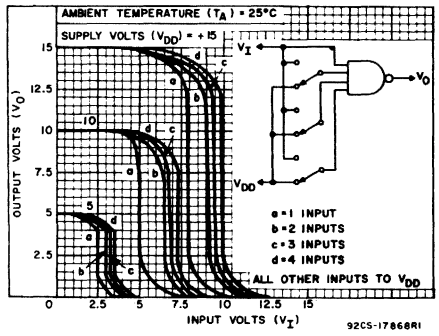


Fig. 4 — Typical multiple input switching transfer characteristics for CD4012B.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, and C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	60	120	ns
		10	30	60	
		15	25	50	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance, C_I	Any Input		5	—	pF

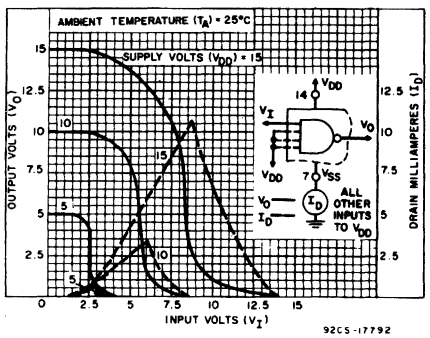


Fig. 5 — Typical current & voltage transfer characteristics.

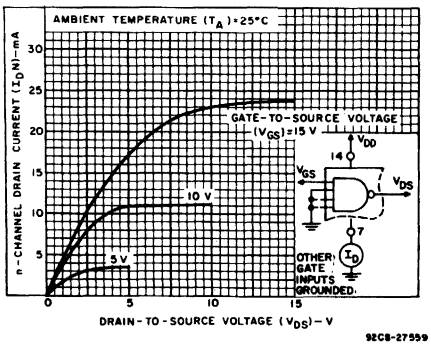


Fig. 6 — Typical output-N-channel drain characteristics.

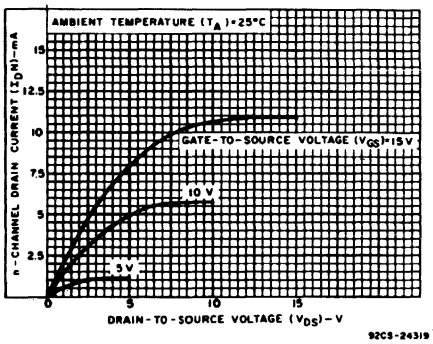


Fig. 7 — Minimum output-N-channel drain characteristics.

CD4011B, CD4012B, CD4023B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55, +25, +125 Apply to D, K, F, H Packages* *Values at -40, +25, +85 Apply to E, Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.1	–	5	1				1	2.25	–	V
	8.2	–	10	2				2	4.5	–	
	12.3	–	15	3				3	6.75	–	
Inputs High, V_{NH} Min.	0.9	–	5	1				1	2.25	–	
	1.8	–	10	2				2	4.5	–	
	2.7	–	15	3				3	6.75	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

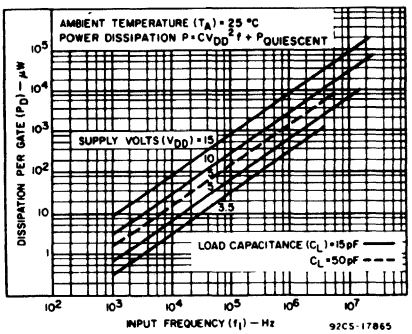


Fig. 11 – Typical dissipation characteristics.

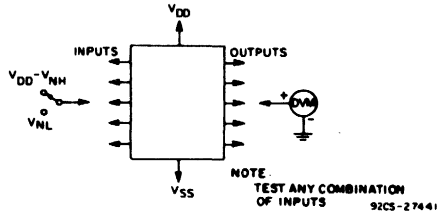


Fig. 13 – Noise immunity test circuit.

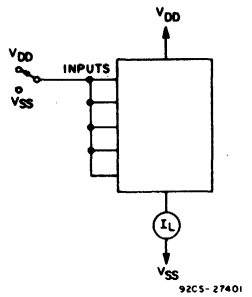


Fig. 12 – Quiescent device current test circuit.

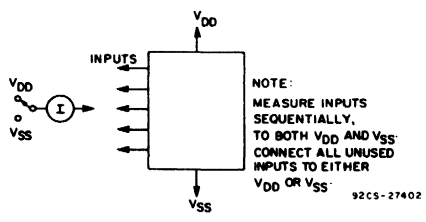


Fig. 14 – Input leakage current test circuit.

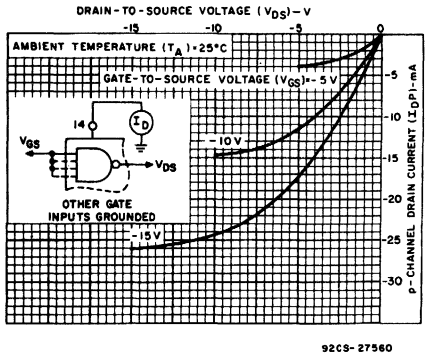


Fig. 8 – Typical output P-channel drain characteristics.

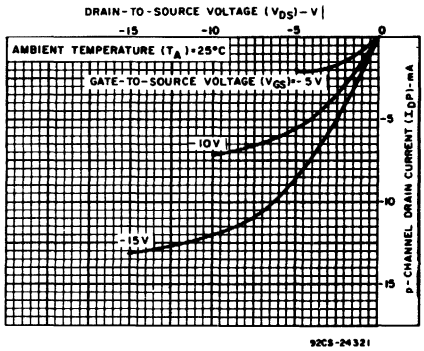


Fig. 9 – Minimum output P-channel drain characteristics.

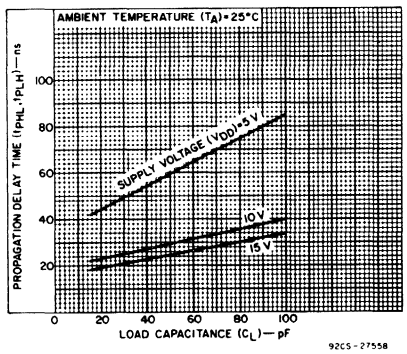


Fig. 10 – Typical propagation delay time vs. load capacitance.

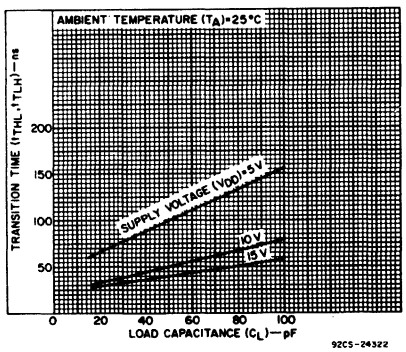


Fig. 15 – Typical transition time vs. load capacitance.

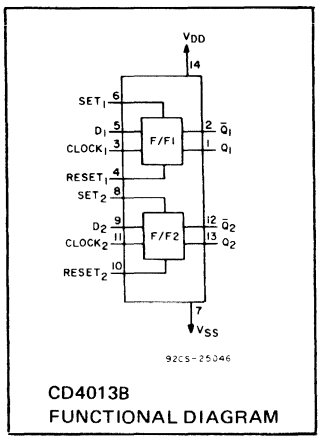
CD4013B Types

Dual 'D'-Type Flip-Flop

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4013B
FUNCTIONAL DIAGRAM

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

Features:

- **Set-Reset capability**
- **Static flip-flop operation – retains state indefinitely with clock level either "high" or "low"**
- **Medium-speed operation – 16 MHz (typ.) clock toggle rate at 10V**
- **Standard symmetrical output drive**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Registers, counters, control circuits**

RECOMMENDED OPERATING CONDITIONS

At T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		ALL PACKAGES		
		MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Data Setup Time t_S	5	40	–	ns
	10	30	–	
	15	25	–	
Clock Pulse Width t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency f_{CL}	5		3.5	MHz
	10	dc	8	
	15		12	
Clock Rise or Fall Time t_rCL,* t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Set or Reset Pulse Width t_W	5	200	–	ns
	10	100	–	
	15	50	–	

*If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

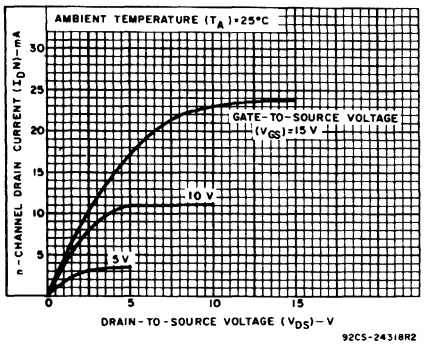


Fig. 1 – Typical output-N-channel drain characteristics.

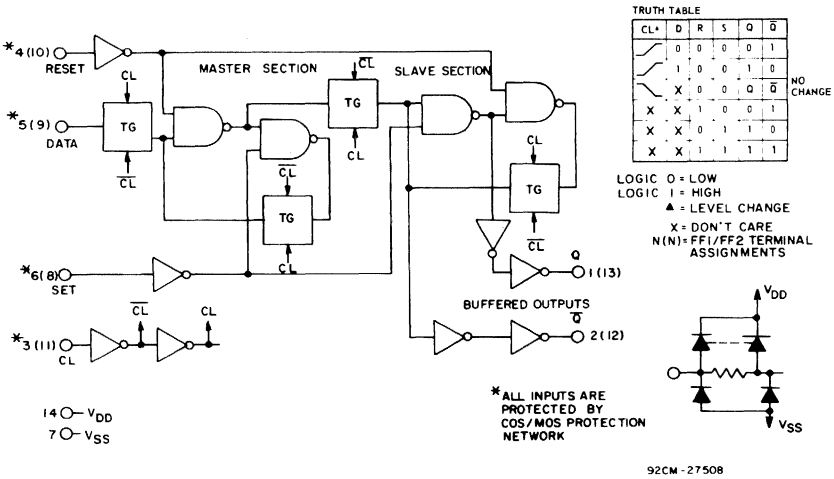


Fig. 2 – Logic diagram and truth table for CD4013B (one of two identical flip-flops).

CD4013B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55,+25,+125 Apply to D,K,F,H Packages* *Values at -40,+25,+85 Apply to E,Y Packages*							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

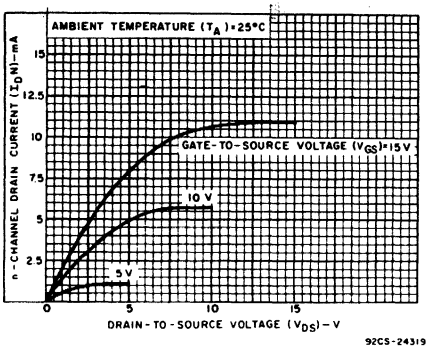


Fig. 3 – Minimum output-N-channel drain characteristics.

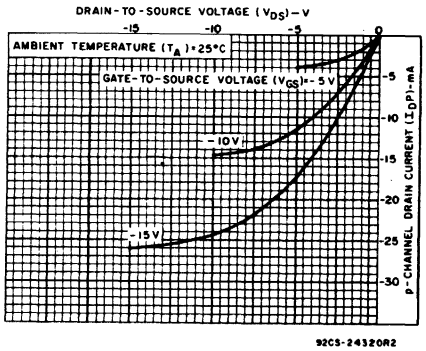


Fig. 4 – Typical output-P-channel drain characteristics.

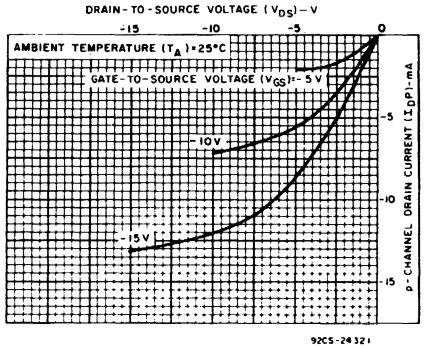


Fig. 5 – Minimum output-P-channel drain characteristics.

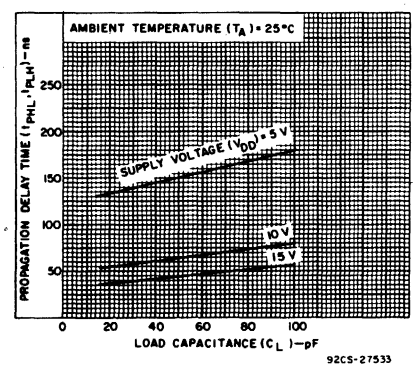


Fig. 6 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$).

CD4013B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES MIN.	TYP.	MAX.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency Frequency # f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	20	40	ns
	10	–	15	30	
	15	–	12	25	
Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	10	
	15	–	–	5	
Average Input Capacitance C_I	Any Input	–	5	–	pF

#Input t_r, t_f = 5 ns.

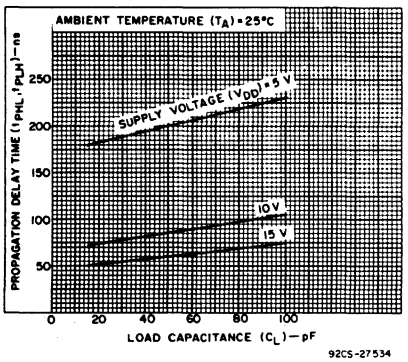


Fig. 7 – Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q.

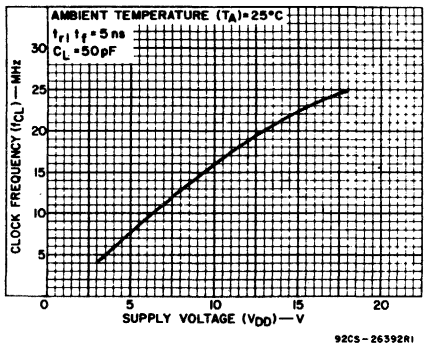


Fig. 8 – Typical maximum clock frequency vs. supply voltage.

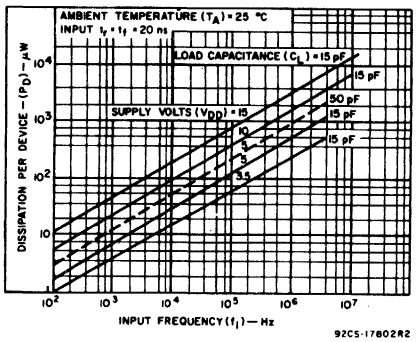


Fig. 9 – Typ. dissipation characteristics.

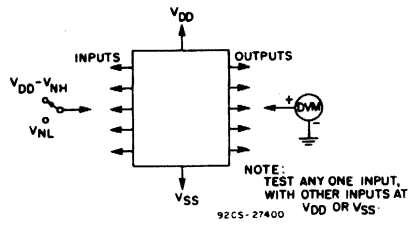


Fig. 10 – Noise immunity test circuit.

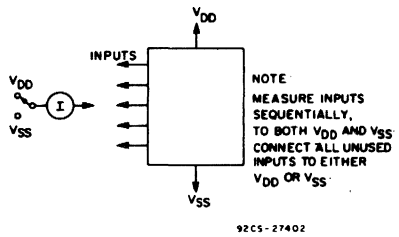


Fig. 11 – Input leakage current test circuit.

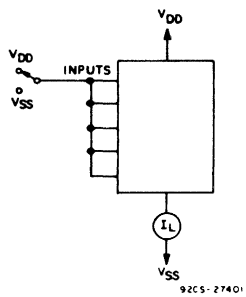


Fig. 12 – Quiescent device current test circuit.

CD4016B Types

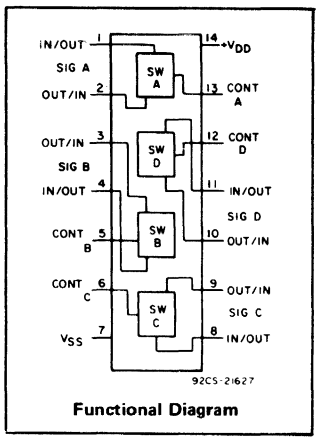
COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4016B Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

The CD4016 "B" Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F,Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TYPICAL "ON" RESISTANCE CHARACTERISTICS

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1kΩ		R_L = 10kΩ		R_L = 100kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON}(max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON}(max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON}(max.)	+ 5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON}(max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+ 5	− 5	260	+ 5	250	+ 5	240	+ 5
			310	− 5	250	− 5	240	− 5
R_{ON}(max.)	+ 5	− 5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	-2.5	520	-2.5	520	−2.5
R_{ON}(max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

* Variation from a perfect switch, R_{ON} = 0Ω.

Features:

- **20-V digital or ± 10-V peak-to-peak switching**
- **280-Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 10 Ω typ. over 15-V signal-input range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit: 10^{12} Ω typ.**
- **Low crosstalk between switches: −50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20 V (full package-temperature range)**

Applications:

- **Analog signal switching/multiplexing**
  - **Signal gating**
  - **Squelch control**
  - **Chopper**
  - **Modulator**
  - **Demodulator**
  - **Commutating switch**
- **Digital signal switching/multiplexing**
- **COS/MOS logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

CD4016B Types

ELECTRICAL CHARACTERISTICS (All inputs. . . . . $V_{SS} \leq V_I \leq V_{DD}$)

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$). .3 to 15 V)

Characteristic	Test Conditions: All Voltage Values are in Volts			Limits: Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E,Y Packages						Unit
			V_{DD} (V)	−55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	
Quiescent Device Current, I_L max (All switches ON or all Switches OFF) D,F,K,H Pkgs.			5	0.25	–	–	10	0.01	0.25	μA
			10	0.5	–	–	20	0.01	0.5	
			15	2	–	–	40	0.01	2	
			20	10	–	–	200	0.02	10	
E,Y Pkgs.			5	–	0.25	5	–	–	0.25	μA
			10	–	0.5	10	–	–	0.5	
			15	–	2	20	–	–	2	
			20	–	10	100	–	–	10	
Signal Inputs (V_{is}) and Outputs (V_{os})										
ON Resistance, R_{ON}	$V_C=V_{DD}$	V_{SS}	V_{is}	Typ/Max	Typ/Max	Typ/Max	Typ/Max			Ω
	R_L = 10 kΩ●									
	+7.5	-7.5	+7.5	120/360	130/370	260/520	300/600	200	400	
			−7.5	120/360	130/370	260/520	300/600	200	400	
			±0.25	130/775	160/790	400/1080	470/1230	280	850	
	+5	−5	+5	130/600	150/610	340/840	400/960	250	660	
			−5	130/600	150/610	340/840	400/960	250	660	
			±0.25	325/1870	370/1900	770/2380	900/2600	580	2000	
	+15	0	+15	120/360	130/370	260/520	300/600	200	400	
			+0.25	120/360	130/370	260/520	300/600	200	400	
			+9.3	150/775	180/790	400/1080	490/1230	300	850	
	+10	0	+10	130/600	150/610	340/840	400/960	250	660	
			+0.25	130/600	150/610	340/840	400/960	250	660	
			+5.6	300/1870	350/1900	750/2380	880/2600	560	2000	
ΔON Resistance Between Any 2 of 4 Switches ΔR_{ON}	R_L = 10 kΩ●									Ω
	+7.5	-7.5	+7.5	–	–	–	–	10	–	
	+5	−5	+5	–	–	–	–	15	–	
Sine Wave Response (Distortion)	+5	−5	5V p-p▲	–	–	–	–	0.4	–	%
	R_L = 10 kΩ, f_{is} = 1 kHz									
Frequency Response Switch ON (Sine-Wave Input)	+5	−5	5 p-p	–	–	–	–	40	–	MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −3 dB									
Feedthrough Switch OFF	V_{DD} = +5, $V_C=V_{SS}$=−5		−5 p-p	–	–	–	–	1.25	–	MHz
	R_L = 1 kΩ, $20 \log_{10} \frac{V_{os}}{V_{is}}$ = −50 dB									
Input or Output Leakage Current Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C=V_{SS}$	±7.5	–	–	–	–	±100	–	pA
	+7.5	-7.5								
	+5	−5	±5	–	–	–	–	$\pm 10 \times 10^{-3}$	±125*	nA

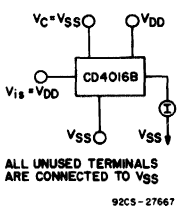


Fig.4 — "OFF" switch input or output leakage current test circuit.

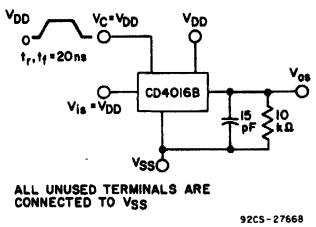


Fig.5 — Test circuit for square-wave response.

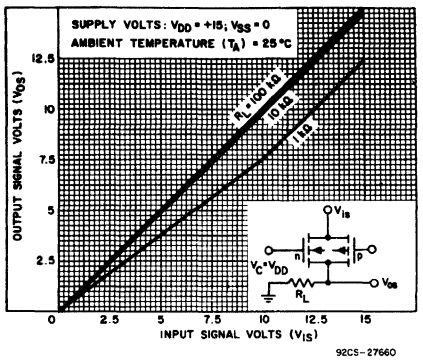


Fig.1 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +15 V, V_{SS} = 0 V.

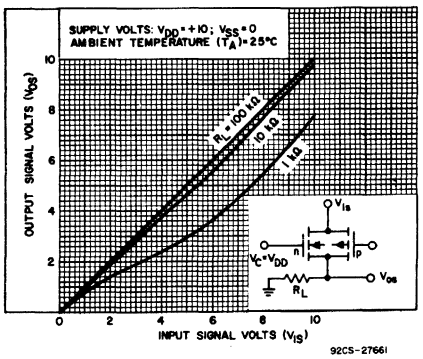


Fig.2 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +10 V, V_{SS} = 0 V.

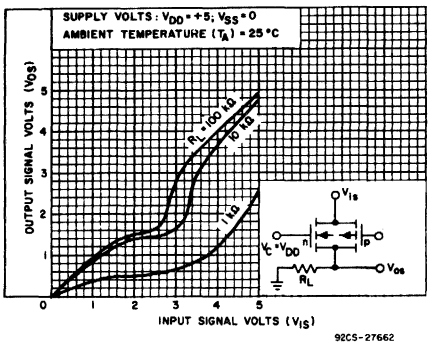


Fig.3 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = 0 V.

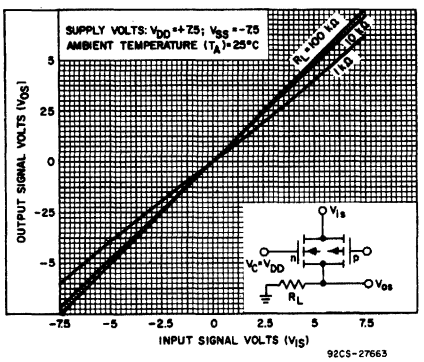


Fig.6 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +7.5 V, V_{SS} = -7.5 V.

CD4016B Types

ELECTRICAL CHARACTERISTICS (Cont'd) $(V_{SS} \leq V_I \leq V_{DD})$

Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . .3 to 15 V)

Characteristic	Test Conditions *All Voltage Values are in Volts*	V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D,F,K,H Packages; Values at −40°C,+25°C,+85°C Apply to E,Y Packages* −55°	−40°	+85°	+125°	+25°C Typ.	+25°C Max.	Unit
Crosstalk Between Any 2 of 4 Switches (f = −50 dB)	$V_C(A)=V_{DD}=+5$; $V_C(B)=V_{SS}=-5$; $V_{is}(A)$ = 5 p-p; R_L=1 kΩ; $20\log_{10}\frac{V_{os}(B)}{V_{is}(A)}$ = −50 dB		–	–	–	–	0.9	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	$V_C = V_{DD}$ = 10; V_{SS} = GND; C_L = 50 pF; V_{is} = 10 Sq. Wave; t_r, t_f = 20 ns	5					40	100	ns
		10	–	–	–	–	20	50	
		15					15	40	
Capacitance: Input, C_{is}	V_{DD}=+5		–	–	–	–	4	–	pF
Output, C_{os}	$V_{CC}=V_{SS}=-5$		–	–	–	–	4	–	
Feedthrough, C_{ios}			–	–	–	–	0.2	–	
Control (V_C)									
Switch Threshold Voltage, V_{TH}	I_{is} = 10μA	5	1 min; 2.25 typ.						V
		10	2 min; 4.5 typ.						
		15	2 min; 6.75 typ.						
Input Leakage Current, I_{IL} max	$V_{is} \leq V_{DD}$	=20	$\pm 10^{-5}$ typ; ±1 max.						μA
Crosstalk (Control Input to Signal Output)	V_C=10 (Sq.Wave); t_r,t_f=20 ns; R_L=10 kΩ	=10	–	–	–	–	50	–	mV
Turn-On Propagation Delay, t_p dc	$V_{DD}-V_{SS}$=10; V_{DD}=10, (See Fig.25); t_r,t_f=20 ns; C_L=50 pF; R_L= 1 kΩ	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Allowable Control Input Repetition Rate	V_{DD}=10, V_{SS}=GND, R_L=1 kΩ, C_L=50pF, V_{CC}=10(Sq.Wave); t_r,t_f = 20 ns		–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I			–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage current measurement for automatic testing.

▲ Symmetrical about 0 volts.

● For all test conditions.

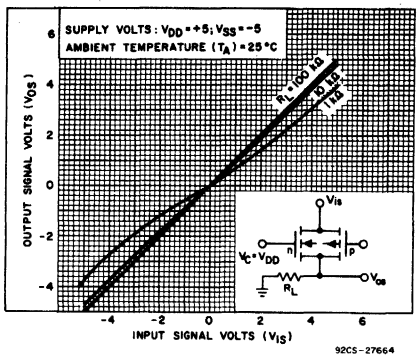


Fig.7 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

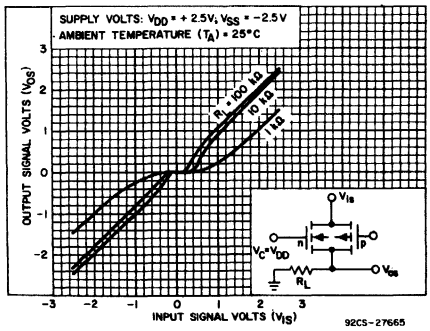


Fig.8 — Typ. "ON" characteristics for 1 of 4 switches with V_{DD} = +2.5 V, V_{SS} = -2.5 V.

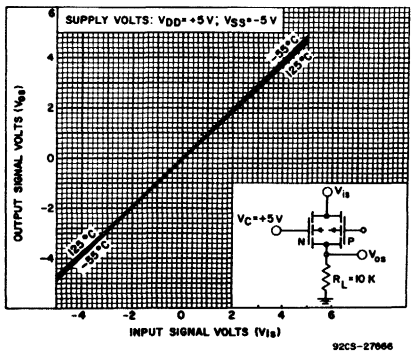


Fig.9 — Typ. "ON" characteristics as a function of temp. for 1 of 4 switches with V_{DD} = +5 V, V_{SS} = -5 V.

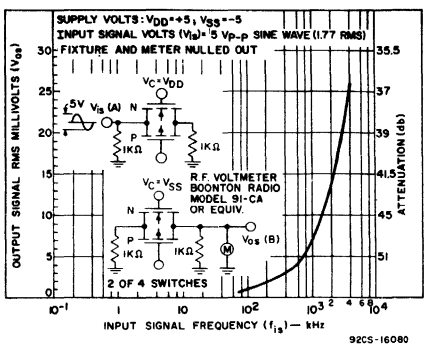


Fig.10 — Typical crosstalk between switch circuits in the same package.

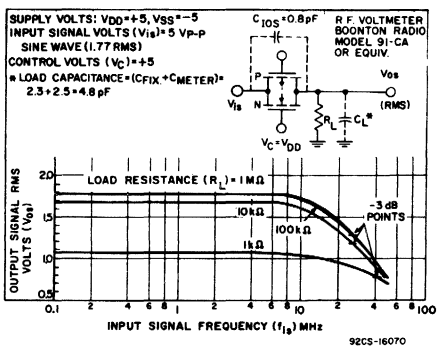


Fig.11 — Typical switch frequency response — switch "ON".

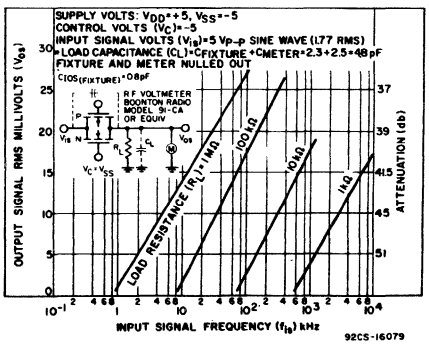


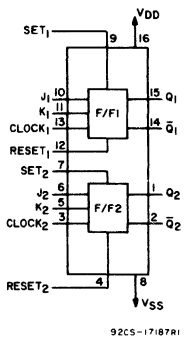
Fig.12 — Typ. feedthru vs. frequency — switch "OFF".

CD4027B Types
COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4027B
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS All Packages Min.	LIMITS All Packages Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		–	3	18	V
Data Setup Time	t_S	5	200	–	ns
		10	75	–	
		15	50	–	
Clock Pulse Width	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Clock Input Frequency (Toggle Mode)	f_{CL}	5	dc	3.5	MHz
		10		8	
		15		12	
Clock Rise or Fall Time	t_rCL*, t_fCL	5	–	15	μs
		10	–	5	
		15	–	5	
Set or Reset Pulse Width	t_W	5	180	–	ns
		10	80	–	
		15	50	–	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

Features:

- **Set-Reset capability**
- **Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"**
- **Medium speed operation — 16 MHz (typ.) clock toggle rate at 10 V**
- **Standard symmetrical output drive**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (Full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Registers, counters, control circuits**

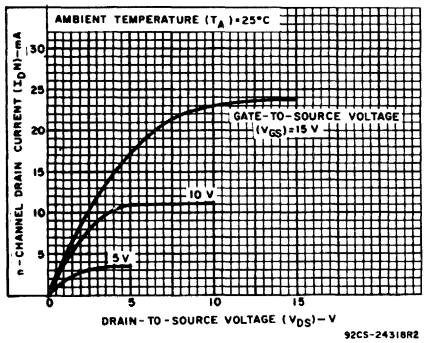


Fig.1 — Typical output N-channel drain characteristics.

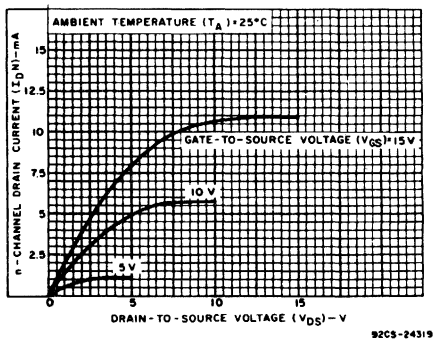


Fig.2 — Minimum output N-channel drain characteristics.

CD4027B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1					$\pm 10^{-5}$	±1	μA

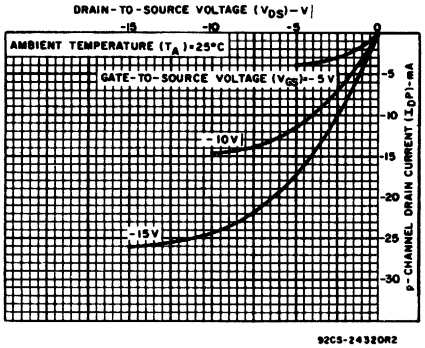


Fig.3 – Typical output P-channel drain characteristics.

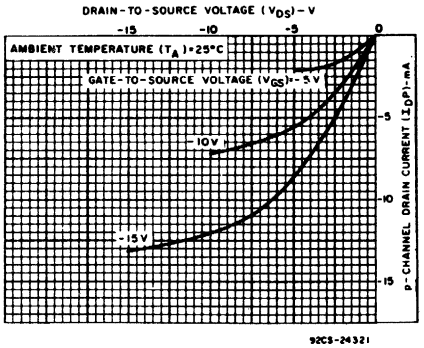


Fig.4 – Minimum output P-channel drain characteristics.

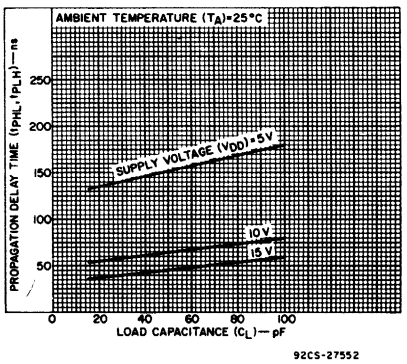
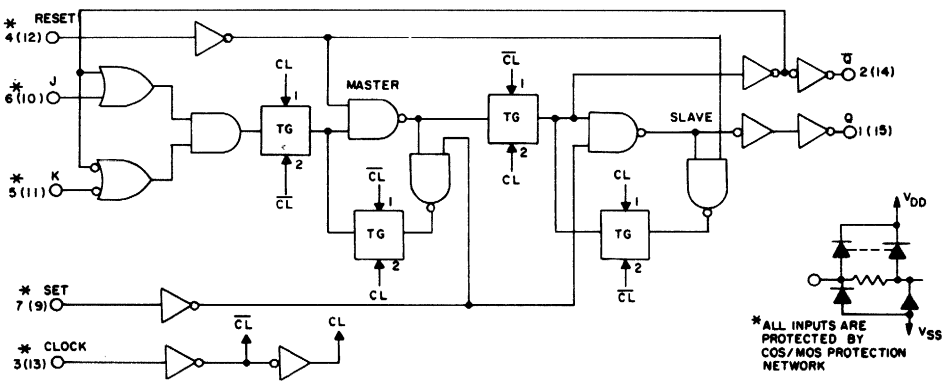


Fig.5 – Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$.



PRESENT STATE INPUTS J	K	S	R	OUTPUT Q	CL*	NEXT STATE OUTPUTS Q	$\overline{Q}$	
↑	X	0	0	Q		1	0	
X	↑	0	0	Q		0	1	
0	X	0	0	1		1	0	
X	0	0	0	0		0	1	
1	1	0	0	Q		Q	$\overline{Q}$	← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
1	1	1	1	X	X	1	1	

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
↑ = LEVEL CHANGE
X = DON'T CARE

92CM-27551

Fig.6 – Logic diagram & truth table for CD4027B (one of two identical J-K flip flops).

CD4027B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to Q or Reset to $\overline{Q}$ t_{PLH}	5	–	150	300	ns
	10	–	65	130	
	15	–	45	90	
Set to $\overline{Q}$ or Reset to Q t_{PHL}	5	–	200	400	ns
	10	–	85	170	
	15	–	60	120	
Transition Time t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Maximum Clock Input Frequency# (Toggle Mode) f_{CL}	5	3.5	7	–	MHz
	10	8	16	–	
	15	12	24	–	
Minimum Clock Pulse Width t_W	5	–	70	140	ns
	10	–	30	60	
	15	–	20	40	
Minimum Set or Reset Pulse Width t_W	5	–	90	180	ns
	10	–	40	80	
	15	–	25	50	
Minimum Data Setup Time t_S	5	–	100	200	ns
	10	–	35	75	
	15	–	25	50	
Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	–	–	15	μs
	10	–	–	10	
	15	–	–	5	
Average Input Capacitance C_I	Any Input	–	5	–	pF

Input t_r, t_f = 5 ns.

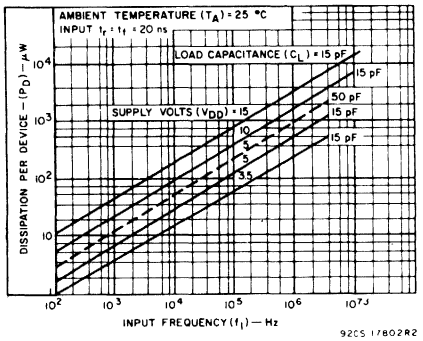


Fig.7 – Typical dissipation characteristics.

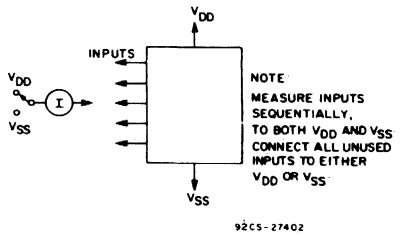


Fig.8 – Input leakage current test circuit.

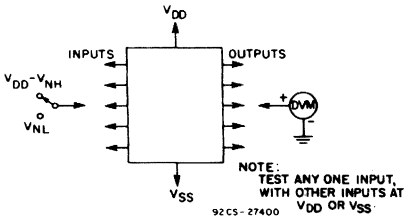


Fig.9 – Noise immunity test circuit.

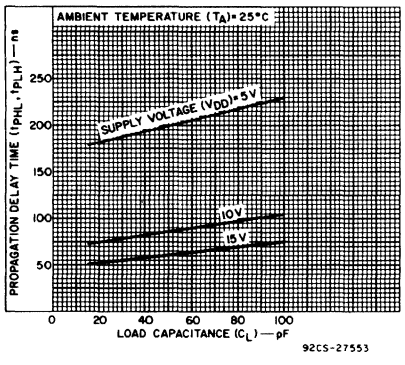


Fig.10 – Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q).

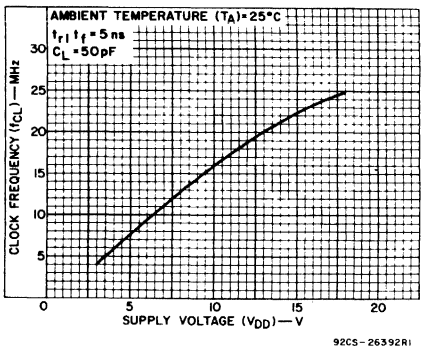


Fig.11 – Typical maximum clock frequency vs. supply voltage (toggle mode).

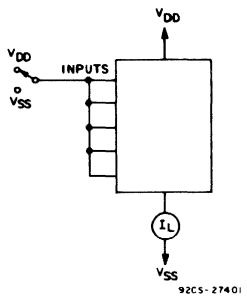
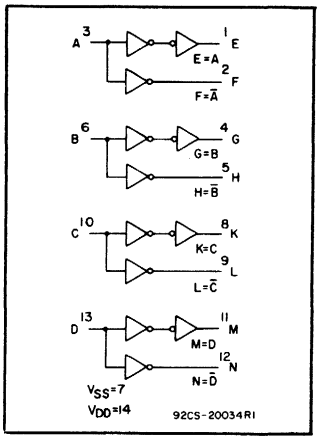


Fig.12 – Quiescent device current test circuit.

CD4041B Types
COS/MOS Quad True/Complement Buffer

High Voltage Types (3 to 20-Volt Rating)



The RCA-CD4041B types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The CD4041 is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

The CD4041B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D,F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Balanced sink and source current; approximately 4 times standard "B" drive**
- **Equalized delay to true and complement outputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **High current source/sink driver**
- **COS/MOS-to-DTL/TTL Converter**
- **Display driver**
- **MOS clock driver**
- **Resistor network driver (Ladder or weighted R)**
- **Buffer**
- **Transmission line driver**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH}	5	60	120	ns
	10	35	70	
	15	25	50	
Transition Time t_{THL}, t_{TLH}	5	40	80	ns
	10	20	40	
	15	15	30	
Average Input Capacitance C_I	Any Input	5	–	pF

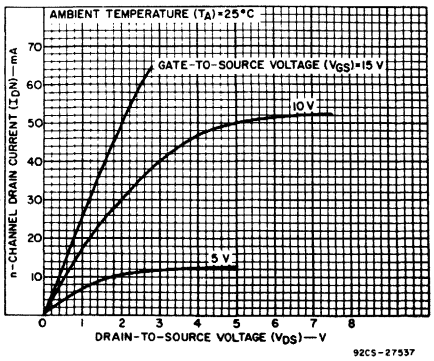


Fig. 1 – Typical output-N-channel drain characteristics.

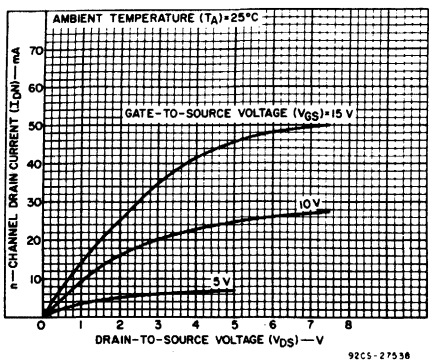


Fig. 2 – Minimum output-N-channel drain characteristics.

CD4041B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current N-Channel (Sink) I_{DN} Min.	0.4	–	5	2.1	1.8	1.44	1.2	1.6	3.2	1.6	mA
	0.5	–	10	6.25	5.6	4.5	3.5	5	10	5	
	1.5	–	15	24	23	17	13	19	38	19	
P-Channel (Source) I_{DP} Min.	4.6	–	5	−2.1	−1.8	−1.44	−1.2	−1.6	−3.2	−1.6	
	2.5	–	5	−8.4	−6.7	−5.4	−4.6	−6.4	−12.8	−6.4	
	9.5	–	10	−6.25	−5.6	−4.5	−3.5	−5	−10	−5	
	13.5	–	15	−24	−23	−17	−13	−19	−38	−19	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	3.6	–	5	1.5				1.5	2.25	–	V
	7.2	–	10	3				3	4.5	–	
	10.8	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	1.4	–	5	1.5				1.5	2.25	–	
	2.8	–	10	3				3	4.5	–	
	4.2	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

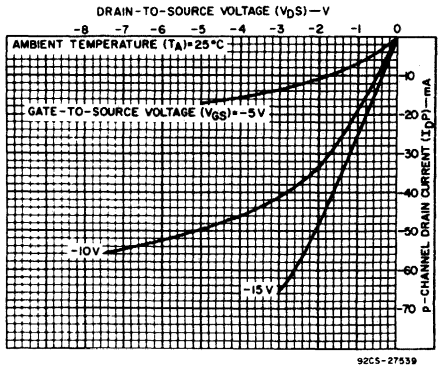


Fig.3 – Typical output-P-channel drain characteristics.

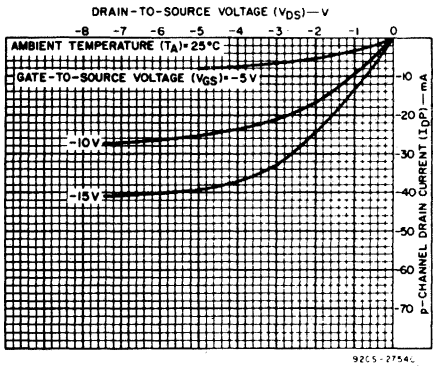


Fig.4 – Minimum output-P-channel drain characteristics.

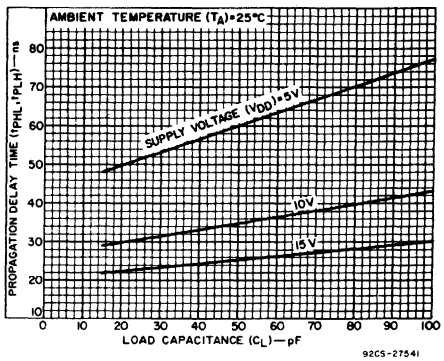


Fig.5 – Typical propagation delay time vs. load capacitance.

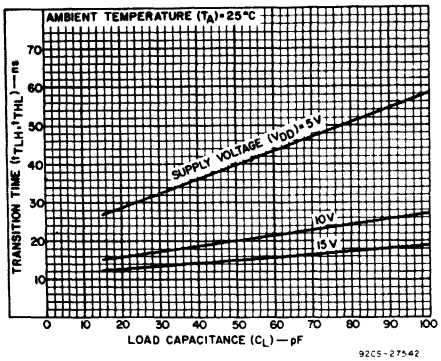


Fig.6 – Typical transition time vs. load capacitance.

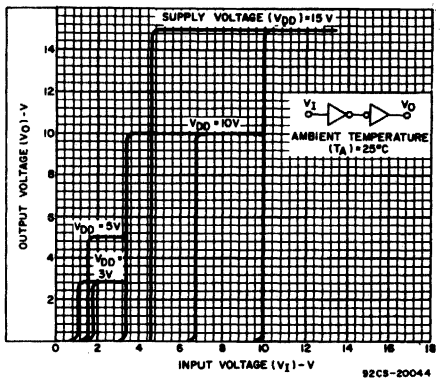


Fig.7 – Minimum and maximum transfer characteristics – true output.

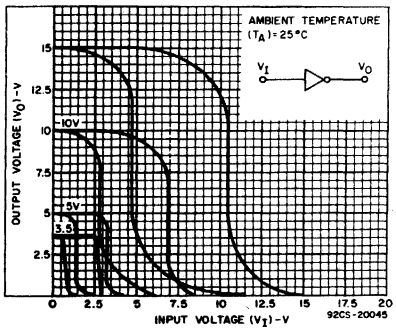


Fig.8 – Minimum and maximum transfer characteristics – complement output.

CD4041B Types

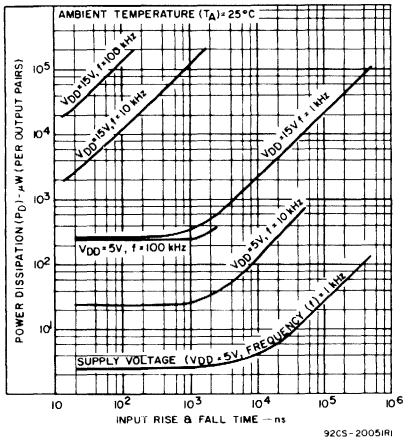


Fig.9 — Typical power dissipation vs. input rise & fall time per output pair.

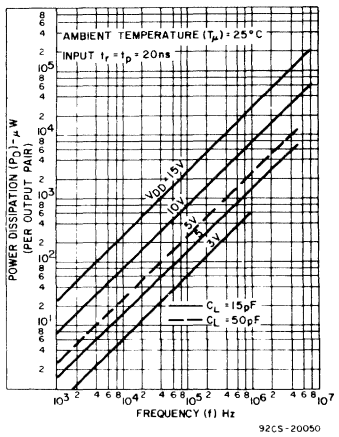


Fig.10 — Typical power dissipation vs frequency per output pair.

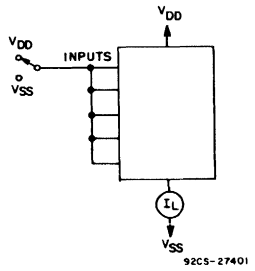


Fig.11 — Quiescent device current test circuit.

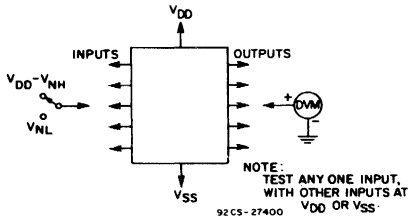


Fig.12 — Noise immunity test circuit.

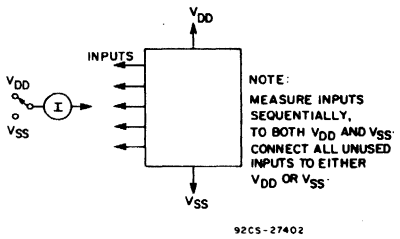


Fig.13 — Input-leakage-current test circuit.

CD4042B Types

COS/MOS Quad Clocked "D" Latch

High-Voltage Types (3-to-20-Volt Rating)

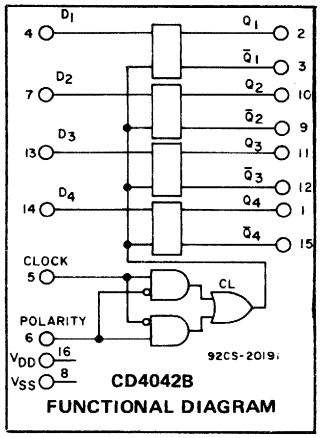
The RCA-CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.

Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

Features:

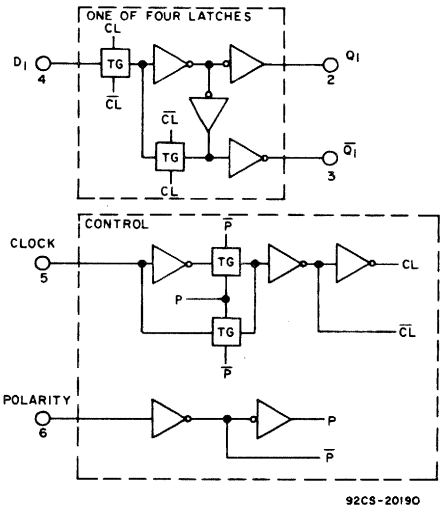
- **Clock polarity control**
- **Q and $\overline{Q}$ outputs**
- **Common clock**
- **Low power TTL compatible**
- **Standard "B"-Series symmetrical output drive**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



Applications:

- **Buffer storage**
- **Holding register**
- **General digital logic**



CLOCK	POLARITY	Q
0	0	D
⌐	0	LATCH
1	1	D
¬	1	LATCH

Fig. 1 – Logic block diagram & truth table.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C

PACKAGE TYPES E,Y . . . . . –40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES Min.	LIMITS ALL TYPES Max.	UNITS
Supply-Voltage Range (For T_A=Full Package Temperature Range)	–	3	18	V
Clock Pulse Width, t_W	5 10 15	150 100 60	– – –	ns
Setup Time, t_S	5 10 15	50 30 25	– – –	ns
Hold Time, t_H	5 10 15	120 60 50	– – –	ns
Clock Rise or Fall Time: t_r , t_f	5,10 15	Not rise or fall time sensitive.		μS

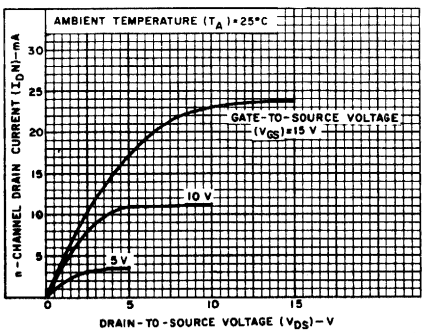


Fig. 2 – Typical output n-channel drain characteristics.

CD4042B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: n-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
p-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	−2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

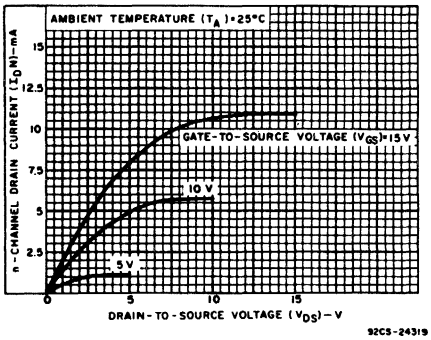


Fig. 3 – Minimum output n-channel drain characteristics.

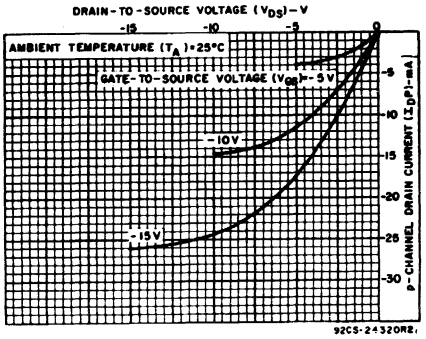


Fig. 4 – Typical output p-channel drain characteristics.

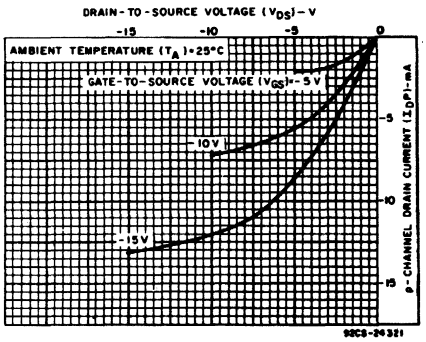


Fig. 5 – Minimum output p-channel drain characteristics.

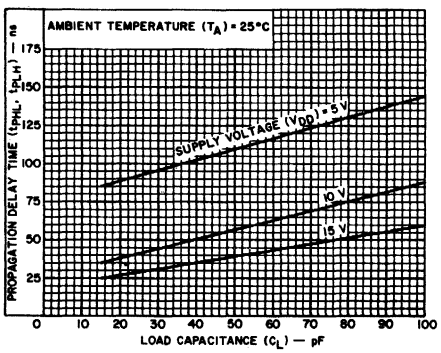
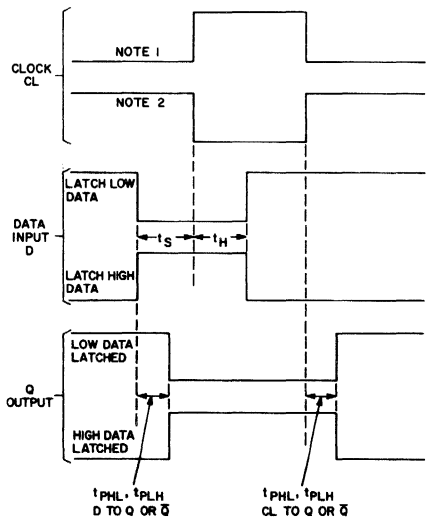


Fig. 6 – Typical propagation delay time vs. load capacitance—data to Q.



NOTES:
1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

92CS-27630

Fig. 7 – Dynamic test paragneters.

CD4042B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES Typ.	LIMITS ALL TYPES Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	110	220	ns
	10	55	110	
	15	40	80	
Data In to $\overline{Q}$	5	150	300	ns
	10	75	150	
	15	50	100	
Clock to Q	5	225	450	ns
	10	100	200	
	15	80	160	
Clock to $\overline{Q}$	5	250	500	ns
	10	115	230	
	15	90	180	
Transition Time : t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum Clock Pulse Width, t_W	5	100	200	ns
	10	50	100	
	15	30	60	
Minimum Hold Time, t_H	5	60	120	ns
	10	30	60	
	15	25	50	
Minimum Setup Time, t_S	5	0	50	ns
	10	0	30	
	15	0	25	
Clock Rise or Fall Time: t_r, t_f	5,10 15	Not rise or fall time sensitive.		μS
Input Capacitance, C_I (Any Input)	—	5	—	pF

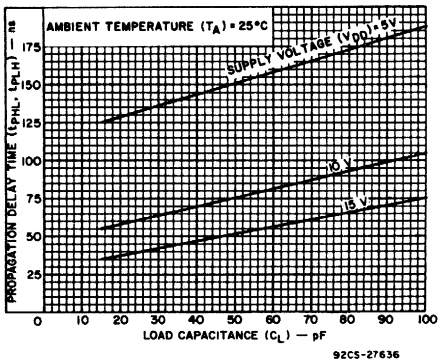


Fig. 8 — Typical propagation delay time vs. load capacitance—data to $\overline{Q}$.

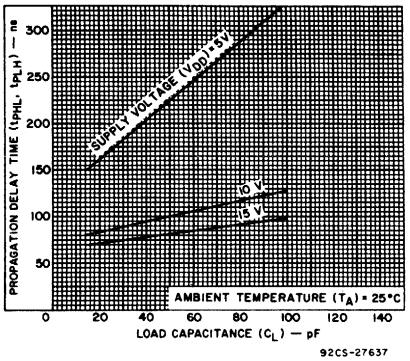


Fig. 9 — Typical propagation delay time vs. load capacitance—clock to Q

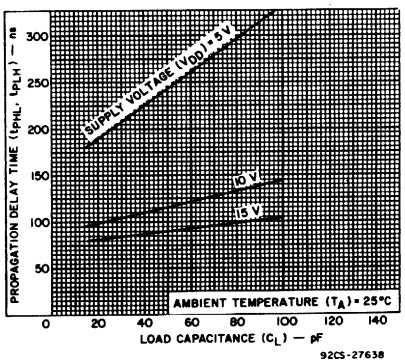


Fig. 10 — Typical propagation delay time vs. load capacitance—clock to $\overline{Q}$.

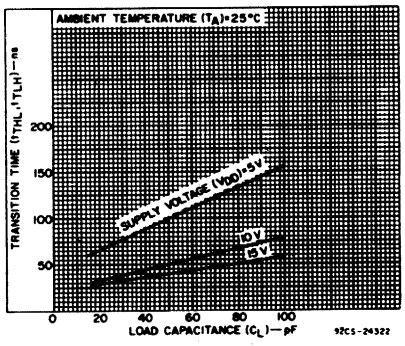


Fig. 11 — Typical transition time vs. load capacitance.

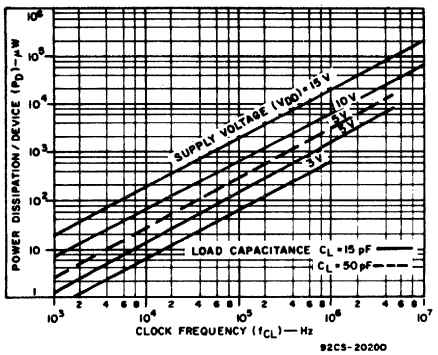


Fig. 12 — Typical dissipation characteristics.

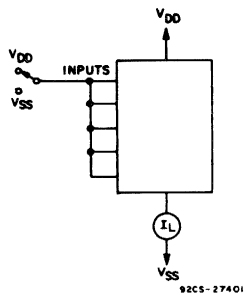


Fig. 13 — Quiescent-device-current test circuit.

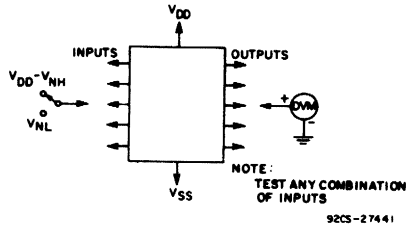


Fig. 14 — Noise-immunity test circuit.

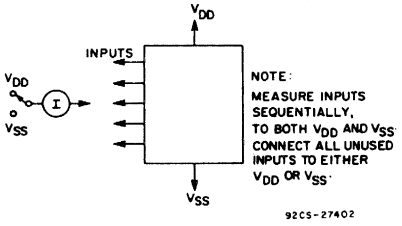


Fig. 15 — Input-leakage-current test circuit.

CD4043B, CD4044B Types

COS/MOS Quad 3-State R/S Latches

High-Voltage Types (3-to-20-Volt Rating)

Quad NOR R/S Latch – CD4043B
Quad NAND R/S Latch – CD4044B

The RCA-CD4043B types are quad cross-coupled 3-state COS/MOS NOR latches and the CD4044B types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

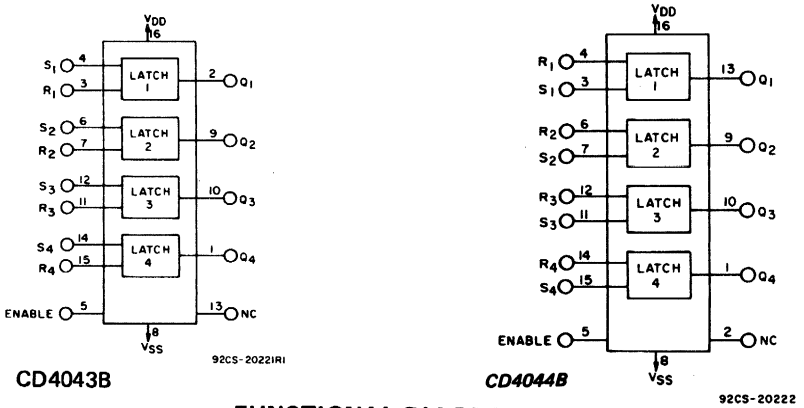
The CD4043B and CD4044B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 16-lead dual in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 3-Level outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- NOR and NAND configurations
- Standard "B"-Series symmetrical output drive
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Holding register in multi-register system
- Four bits of independent storage with output ENABLE
- Strobed register
- General digital logic



CD4043B *CD4044B*

FUNCTIONAL DIAGRAMS

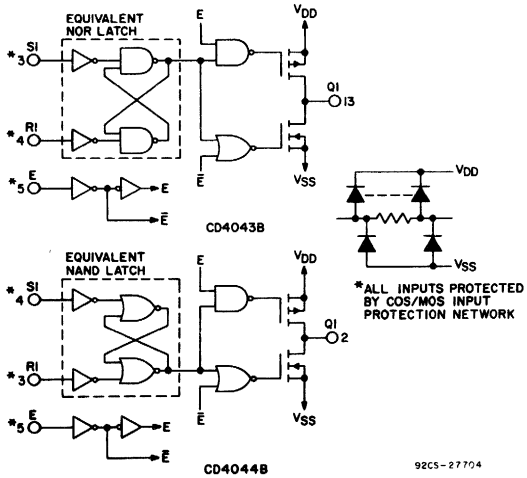


Fig. 1 – Logic diagrams.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25° C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
SET or RESET Pulse Width, t_W	5	160	–	ns
	10	80	–	
	15	40	–	

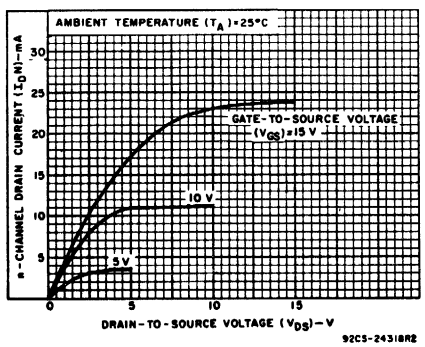


Fig. 2 – Typical output n-channel drain characteristics.

CD4043B, CD4044B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55,+25,+125 Apply to D,K,F,H Packages Values at -40,+25,+85 Apply to E, Y Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High-Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

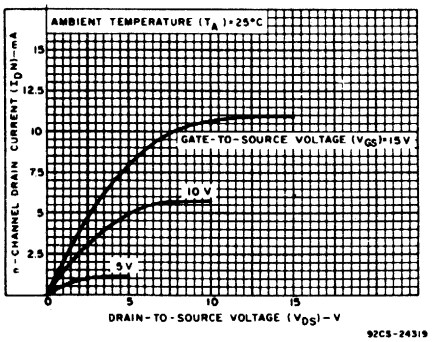


Fig. 3 – Minimum output n-channel drain characteristics.

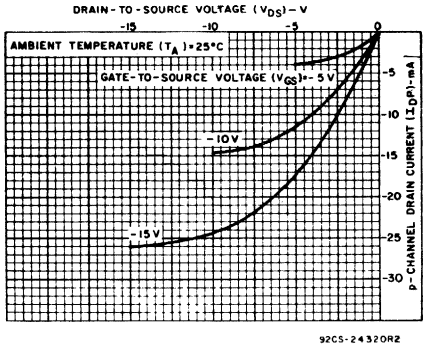


Fig. 4 – Typical output p-channel drain characteristics.

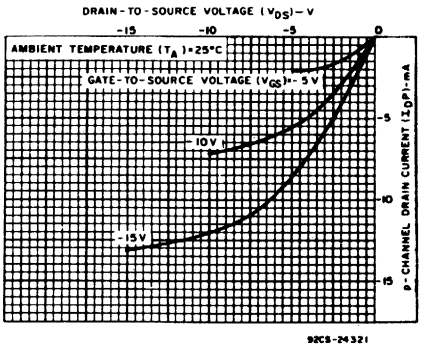


Fig. 5 – Minimum output p-channel drain characteristics.

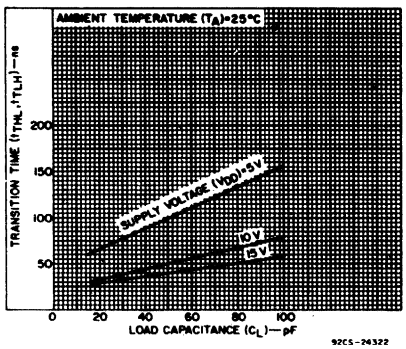


Fig. 6 – Typical transition time vs. load capacitance.

CD4043B, CD4044B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} SET or RESET to Q	5	150	300	ns
	10	70	140	
	15	50	100	
3-State Propagation Delay Time: ENABLE to Q t_{PHZ}, t_{PZH}	5	115	230	ns
	10	55	110	
	15	40	80	
t_{PLZ}, t_{PZL}	5	90	180	ns
	10	50	100	
	15	35	70	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum SET or RESET Pulse Width, t_W	5	80	160	ns
	10	40	80	
	15	20	40	
Average Input Capacitance, (Any Input) C_I	–	5	–	pF

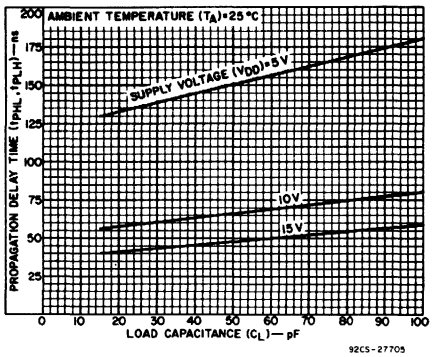


Fig. 7 – Typical propagation delay time vs. load capacitance–SET, RESET to Q, $\overline{Q}$.

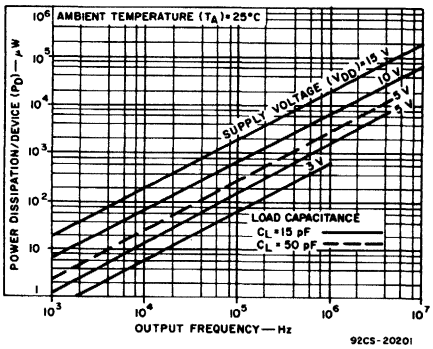


Fig. 8 – Typical power dissipation vs. frequency.

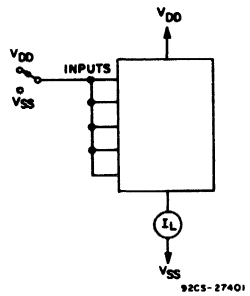


Fig. 9 – Quiescent device current test circuit.

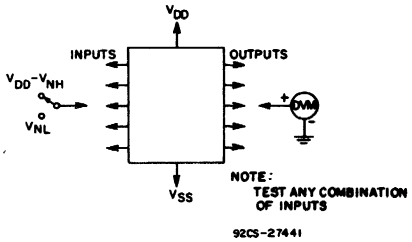


Fig. 10 – Noise immunity test circuit.

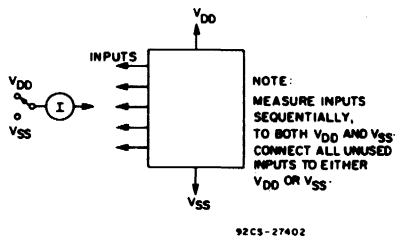


Fig. 11 – Input leakage current test circuit.

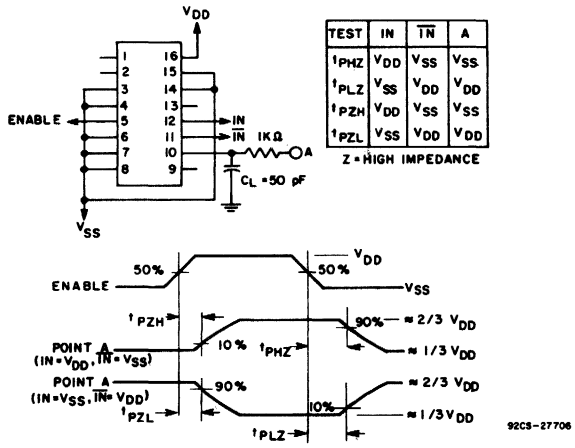


Fig. 12 – ENABLE propagation delay time test circuit and waveforms.

CD4049B, CD4050B Types

COS/MOS Hex Buffer/Converters

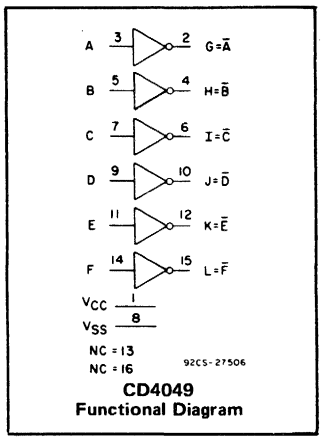
High-Voltage Types (3-to-20-Volt Rating)

CD4049B—Inverting Type
CD4050B—Non-Inverting Type

The RCA-CD4049B and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, V_{OL}≥0.4 V, and I_{DN}≥3.2 mA.)

The CD4049B and CD4050B are designated as replacements for CD4009B and CD4010B, respectively. Because the CD4049B and CD4050B require only one power supply, they are preferred over the CD4009B and CD4010B and should be used in place of the CD4009B and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049B and CD4050B are pin compatible with the CD4009B and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049B or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

The CD4049B and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



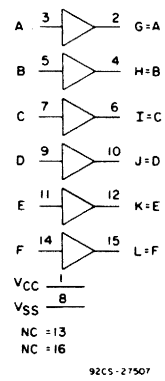
CD4049
Functional Diagram

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**

Applications:

- **COS/MOS to DTL/TTL hex converter**
- **COS/MOS current "sink" or "source" driver**
- **COS/MOS high-to-low logic-level converter**



CD4050
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{CC}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A= −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A= +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A= −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A= +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_I)	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_I \geq V_{CC}$.

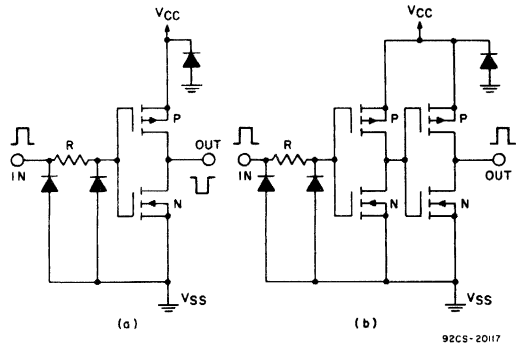


Fig. 1—a) Schematic diagram of CD4049B, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

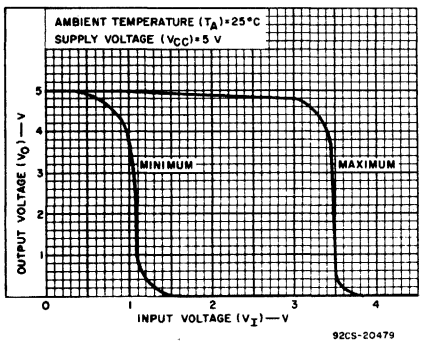


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049B.

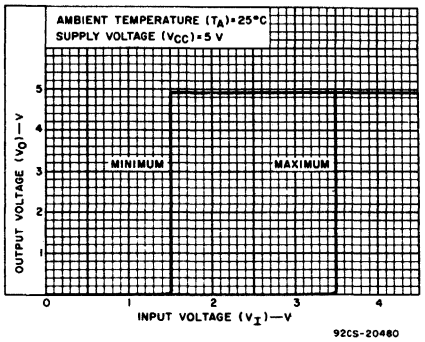


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050B.

CD4049B, CD4050B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) Values at −55,+25,+125 Apply to D,K,F,H Pkgs. Values at −40,+25,+85 Apply to E,Y Pkgs.							Units
	V_O (V)	V_{IN} (V)	V_{CC} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	4.5	3.3	3.1	2.1	1.8	2.6	5.2		mA
	0.4		5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	–	10	10	9.6	6.6	5.6	8	16		
	1.5	–	15	26	25	20	18	24	48	–	
P-Channel (Source), I_DP Min.	4.6	–	5	1	0.9	0.72	0.6	−0.8	−1.6	–	
	2.5		5	4	3.6	−2.6	−2.3	−3.2	−6.4	–	
	9.5		10	−2.2	−2	1.5	1.3	1.8	3.6		
	13.5		15	6.6	6.4	5	4.4	6	12		
Output Voltage: Low-Level, V_{OL} Max.		0.5	5	0.05				–	0	0.05	V
		0, 10	10	0.05					0	0.05	
		0, 15	15	0.05					0	0.05	
High-Level, V_{OH} Min.		0, 5	5	4.95				4.95	5		
		0, 10	10	9.95				9.95	10		
		0, 15	15	14.95				14.95	15		
Noise Immunity: Inputs Low, V_{NL} Min.	3.6		5	1.5				1.5	2.25		V
	7.2		10	3				3	4.5		
CD4050B	10.8		15	4.5				4.5	6.75		
Inputs High, V_{NH} Min.	1.4		5	1.5				1.5	2.25		
	2.8		10	3				3	4.5		
All Types	4.2		15	4.5				4.5	6.75		
Inputs Low, V_{NL} Min.	3.6		5	1				1	1.5		
	7.2		10	2				2	3		
CD4049B	10.8		15	2.5				2.5	4.5		
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1				1			V
	9		10	1				1			
CD4050B	13.5		15	1				1			
Inputs High, V_{NMH} Min.	0.5		5	1				1	–		
	1		10	1				1	–	–	
CD4050B	1.5		15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1					±10⁻⁵	±1	μA

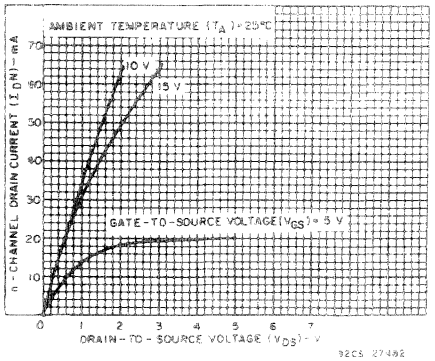


Fig. 4 – Typical output n-channel drain characteristics.

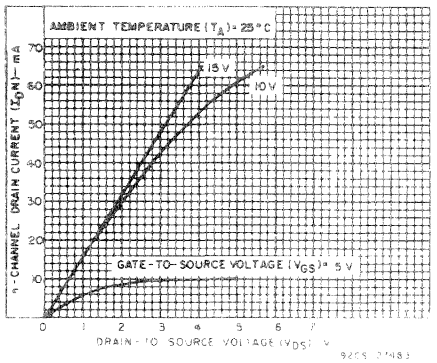


Fig. 5—Minimum output n-channel drain characteristics.

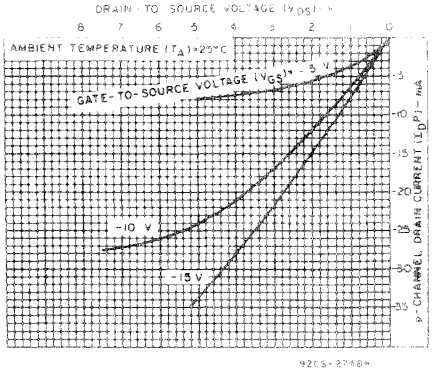


Fig. 6—Typical output p-channel drain characteristics.

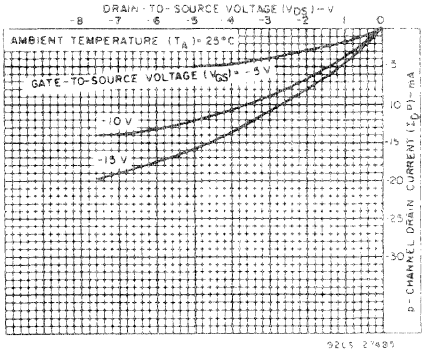


Fig. 7—Minimum output p-channel drain characteristics.

CD4049B, CD4050B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_I	V_{CC}	Typ.	Max.	
Propagation Delay Time:	5	5	60	120	ns
Low-to-High, t_{PLH}	10	10	32	65	
CD4049B	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
	5	5	70	140	
	10	10	40	80	
CD4050B	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL}	5	5	32	65	ns
	10	10	20	40	
CD4049B	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
	5	5	55	110	
	10	10	22	55	
CD4050B	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time:	5	5	80	160	ns
Low-to-High, t_{TLH}	10	10	40	80	
	15	15	30	60	
	5	5	30	60	
High-to-Low, t_{THL}	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_I					
CD4049B	–	–	15	–	pF
CD4050B	–	–	5	–	

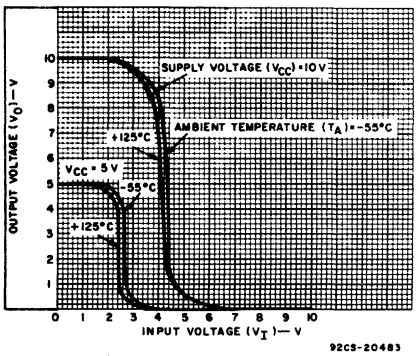


Fig. 8—Typical voltage transfer characteristics as a function of temperature for CD4049B.

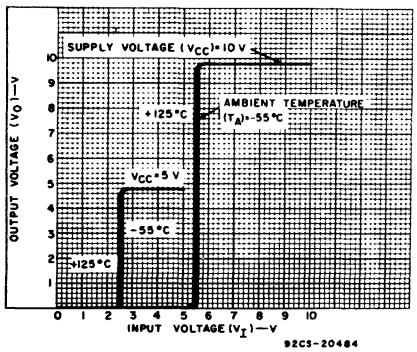


Fig. 9—Typical voltage transfer characteristics as a function of temperature for CD4050B.

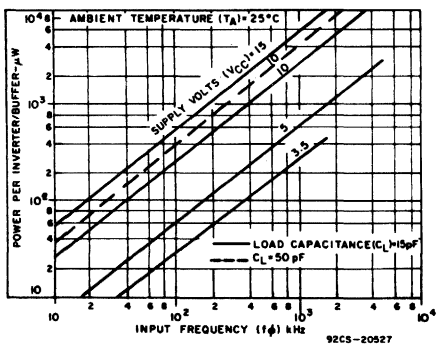


Fig. 10—Typical dissipation characteristics for CD4049B, CD4050B.

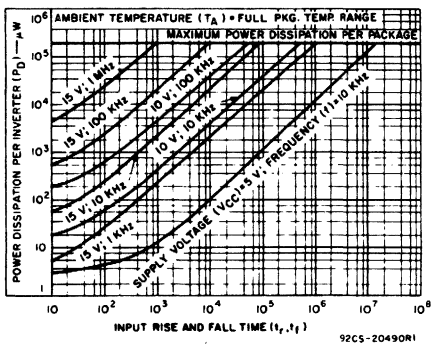


Fig. 11—Typical power dissipation vs. transition time per inverter CD4049B.

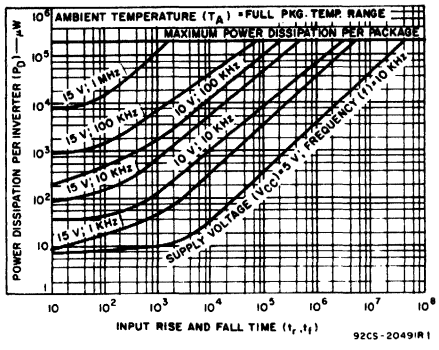


Fig. 12—Typical power dissipation vs. transition time per inverter CD4050B.

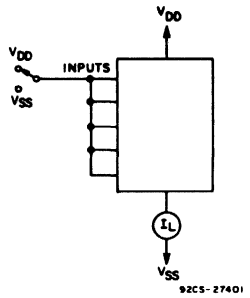


Fig. 13—Quiescent device current test circuit.

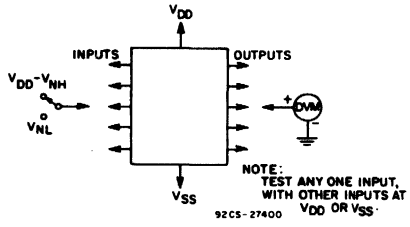


Fig. 14—Noise immunity test circuit.

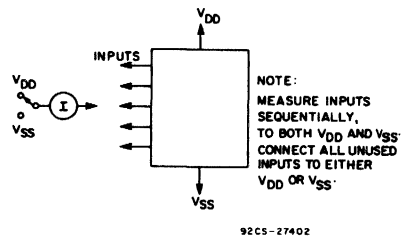


Fig. 15—Input leakage current test circuit.

CD4051B, CD4052B, CD4053B Types
COS/MOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

The RCA-CD4051, CD4052, and CD4053 analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +5 V, V_{SS} = 0, and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 4.5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are OFF.

The CD4051 is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned ON, and connect one of the 8 inputs to the output.

The CD4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051, CD4052, and CD4053 are supplied in 16-lead ceramic dual-in-line packages (D, F, Y suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

High-Voltage Types (3-to-20-Volt Rating)

CD4051B — Single 8-Channel Multiplexer/Demultiplexer
CD4052B — Differential 4-Channel Multiplexer/Demultiplexer
CD4053B — Triple 2-Channel Multiplexer/Demultiplexer

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{STG})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
Package Types D, F, K, H	−55 to +125°C
Package Types E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, V_{DD}:	
(Voltages referenced to V_{SS} or V_{EE}, whichever is more negative)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE:	
For T_A = −40 to +60°C (Package Types E, Y)	500 mW
For T_A = +60 to +85°C (Package Types E, Y)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (Package Types D, F, K)	500 mW
For T_A = +100 to +125°C (Package Types D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER CHANNEL:	
For T_A = Full Package-Temperature Range (All Package Types)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS AT T_A =25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	–	3	18	V
Multiplexer Switch Input Current Capability*	–	–	25	mA
Output Load Resistance	–	100	–	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4,14, and 15 on the CD4053.

Applications:

- **Analog and digital multiplexing and demultiplexing**
- **A/D and D/A conversion**
- **Signal gating**

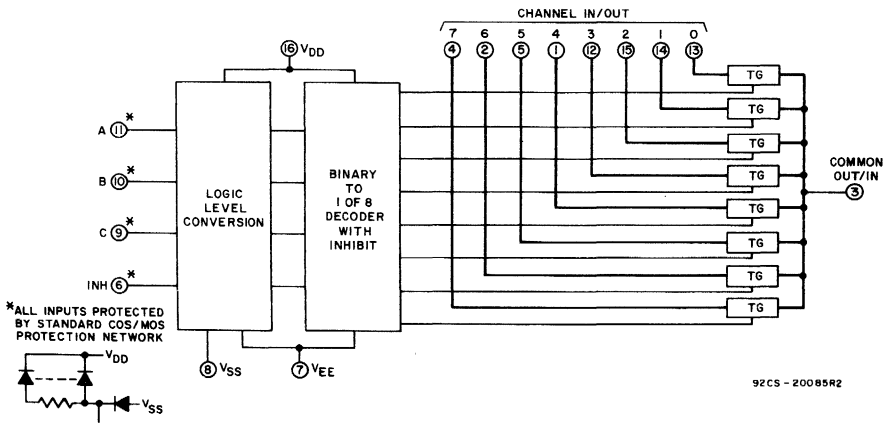


Fig.1 — Functional diagram of CD4051.

Features:

- **Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}**
- **Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for V_{DD}-V_{EE} = 15 V**
- **High OFF resistance: channel leakage of ± 10 pA (typ.) @ V_{DD}-V_{EE} = 10 V**
- **Logic-level conversion for digital addressing signals of 3 to 20 V (V_{DD}-V_{SS} = 3 to 20 V) to switch analog signals to 20 V p-p (V_{DD}-V_{EE} = 20 V); see introductory text**
- **Matched switch characteristics: R_{ON} = 5 Ω (typ.) for V_{DD}-V_{EE} = 15 V**
- **Very low quiescent power dissipation under under all digital-control input and supply conditions: 0.2 μW (typ.) @ V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10 V**
- **Binary address decoding on chip**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-, 10-, and 15-V parametric ratings**

CD4051B, CD4052B, CD4053B,Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125, apply to D,F,K,H pkg Values at −40,+25,+85, apply to E,Y pkgs −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_L Max.				5	5	5	50	100	–	0.02	5	μA
				10	10	10	100	200	–	0.02	10	
				15	20	20	200	400	–	0.02	20	
				20	100	100	1000	2000	–	0.04	100	
ON Resistance $0 \leqslant V_{is} \leqslant V_{DD}$ R_{ON} Max.		0	0	5	2000	2100	3200	3500	–	470	2500	Ω
		0	0	10	310	330	520	580	–	180	400	
		0	0	15	220	230	360	400	–	125	280	
Δ ON Resistance (Between Any Two Channels) ΔR_{ON}		0	0	5	–	–	–	–	–	10	–	Ω
		0	0	10	–	–	–	–	–	10	–	
		0	0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max.		0	0	10	±200*				–	±0.1	±200*	nA
		0	0	15	±500*				–	±0.1	±200*	
		0	0	20	±1000*				–	±0.1	±200*	
All Channels OFF (Common OUT/IN) Max.		0	0	10	±200*				–	±0.1	±200*	
		0	0	15	±500*				–	±0.1	±200*	
		0	0	20	±1000*				–	±0.1	±200*	
Capacitance: Input, C_{is}					–	–	–	–	–	5	–	pF
Output, C_{os} CD4051					–	–	–	–	–	30	–	
CD4052		−5	−5	5	–	–	–	–	–	18	–	
CD4053					–	–	–	–	–	9	–	
Feedthrough, C_{ios}					–	–	–	–	–	0.2	–	
Propagation Delay Time (Signal Input to Output	10V	R_L = 10 kΩ		5	–	–	–	–	–	30	–	ns
		C_L = 50 pF		10	–	–	–	–	–	15	–	
		t_r, t_f = 20 ns		15	–	–	–	–	–	11	–	

* Determined by minimum feasible leakage measurement for automatic testing.

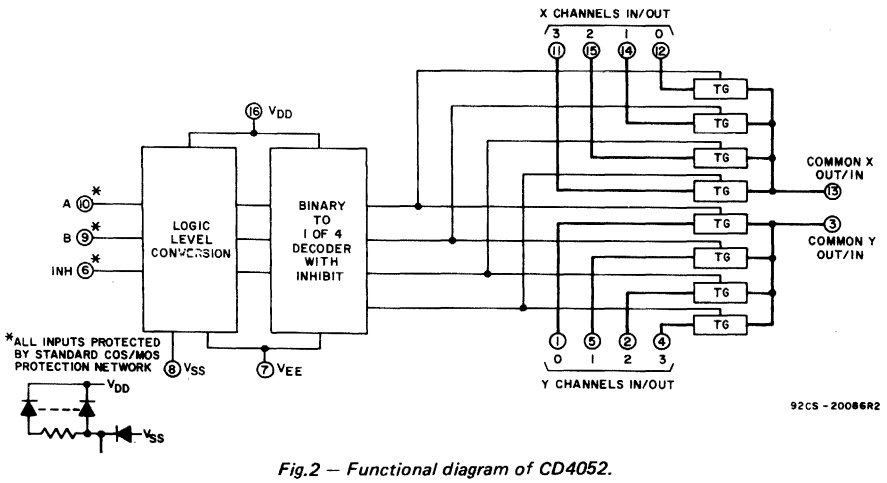


Fig.2 – Functional diagram of CD4052.

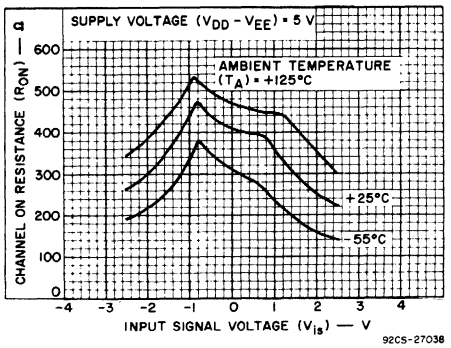


Fig.3 – Typical channel ON resistance vs input signal voltage (all types).

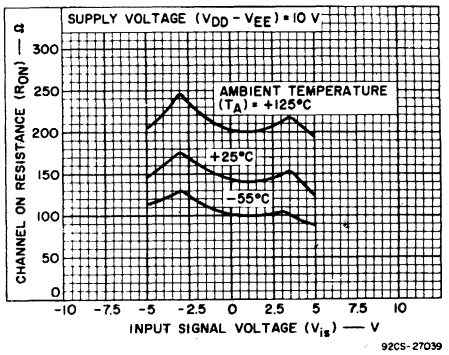


Fig.4 – Typical channel ON resistance vs. input signal voltage (all types).

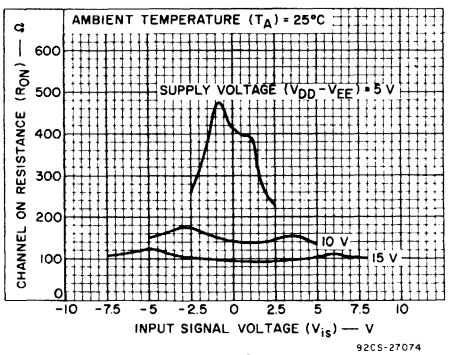


Fig.5 – Typical channel ON resistance vs. input signal voltage (all types).

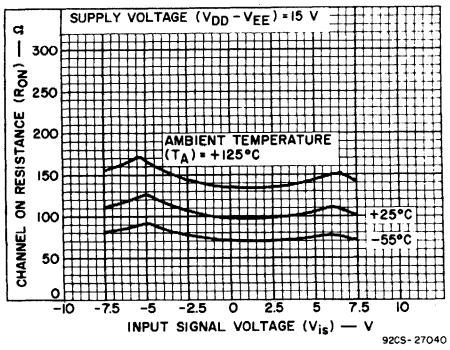


Fig. 6 – Typical channel ON resistance vs. input signal voltage (all types).

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS V_{is} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperature (°C) Values at −55,+25,+125, apply to D,F,K,H pkg Values at −40,+25,+85, apply to E,Y pkgs −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
CONTROL (ADDRESS or INHIBIT) V_C												
Noise Immunity: Min.												
Inputs Low, V_{NL}	=V_{DD} thru 1 kΩ	$V_{EE}=V_{SS}$ R_L=1 kΩ to V_{SS} I_{IS}< 2 μA on all OFF Channels	5		1.5				1.5	2.25	–	V
			10		3				3	4.5	–	
			15		4.5				4.5	6.75	–	
Inputs High, V_{NH}			5		1.5				1.5	2.25	–	
			10		3				3	4.5	–	
			15		4.5				4.5	6.75	–	
Input Leakage Current; I_{IL}, I_{IH} Max.		("A" Series)	15		±1				–	±10−5	±1	μA
		("B" Series)	20		±1				–	±10−5	±1	
Propagation Delay Time:	t_r,t_f = 20 ns, C_L = 50 pF											
Address-to-Signal OUT (Channels ON or OFF) See Figs.14,15,18		0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	
		0	0	15	–	–	–	–	–	120	240	
		−5	0	5	–	–	–	–	–	225	450	
	R_L=10 kΩ, C_L=50 pF t_r, t_f = 20 ns											
Inhibit-to-Signal OUT (Channel turning ON)		0	0	5	–	–	–	–	–	360	720	ns
		0	0	10	–	–	–	–	–	160	320	
		0	0	15	–	–	–	–	–	120	240	
		−10	0	5	–	–	–	–	–	200	400	
	R_L=300Ω, C_L=50 pF t_r,t_f = 20 ns											
Inhibit-to-Signal OUT (Channel turning OFF)		0	0	5	–	–	–	–	–	200	450	ns
		0	0	10	–	–	–	–	–	90	210	
		0	0	15	–	–	–	–	–	70	160	
		−10	0	5	–	–	–	–	–	130	300	
Average Input Capacitance, C_I (Any Address or Inhibit Input)					–	–	–	–	–	5	–	pF

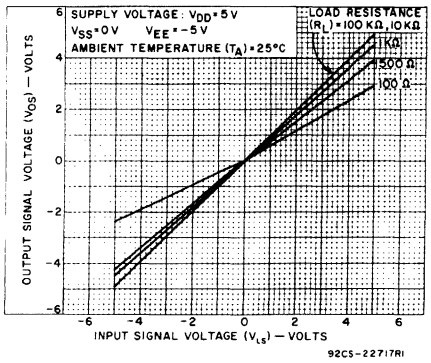


Fig.8 – Typical ON characteristics for 1 of 8 channels (CD4051).

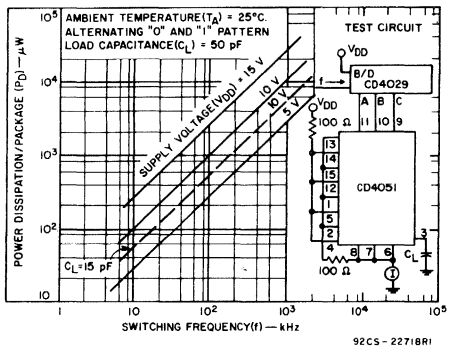


Fig.9 – Typical dynamic power dissipation vs. switching frequency (CD4051).

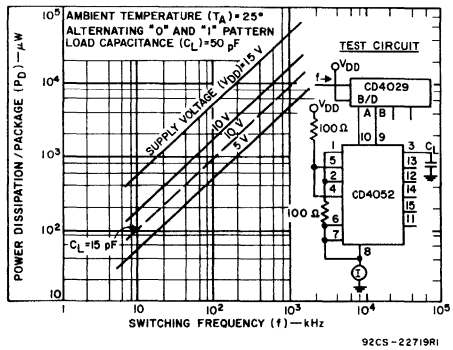


Fig.10 – Typical dynamic power dissipation vs. switching frequency (CD4052).

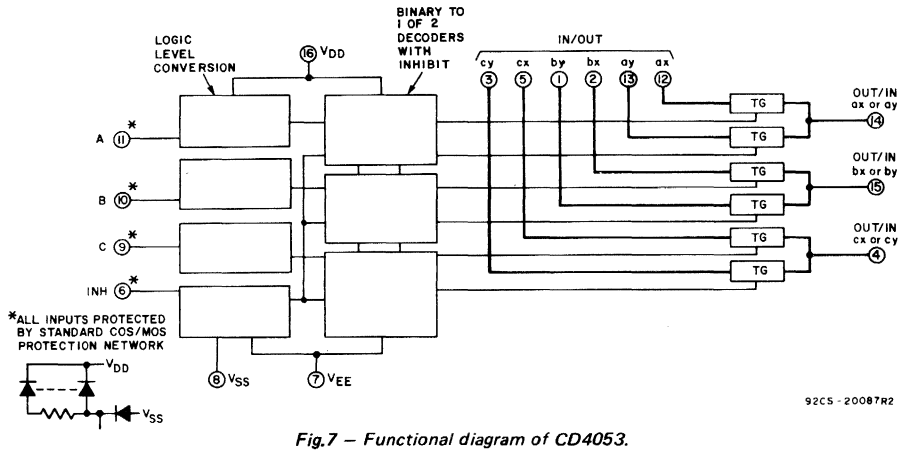


Fig.7 – Functional diagram of CD4053.

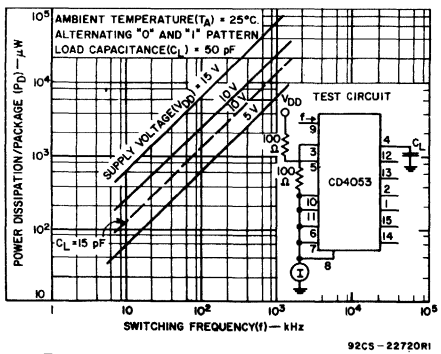


Fig.11 – Typical dynamic power dissipation vs. switching frequency (CD4053).

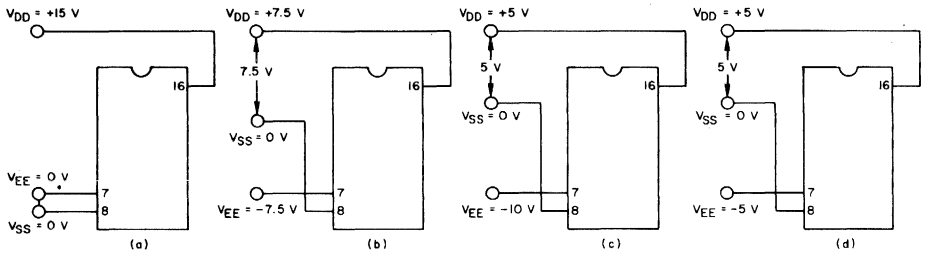
CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{is} (V)	V_{DD} (V)	R_L (kΩ)	TYPICAL LIMITS AT INDICATED CONDITIONS		VALUE	UNITS
Frequency Response Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4053	30	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4052	25	
					CD4051	20	
				V_{os} at Any Channel		60	
Sine Wave Response (Distortion)	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	$V_{EE} = V_{SS}$, f_{is} = 1 kHz						
Feedthrough (All Channels OFF)	5●	10	1	V_{os} at Common OUT/IN	CD4053	8	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -40$dB				CD4052	10	
					CD4051	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels		3	MHz
	$V_{EE} = V_{SS}$, $20 \log \frac{V_{os}}{V_{is}} = -40$dB			Between Sections CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any 2 Sections CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to Signal Crosstalk	–	10	10#			65	mV (Peak)
	V_{EE}=0, V_{SS}=0, t_r, t_f =20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

Both ends of channel



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

92CS-20088R1

Fig. 12 – Typical bias voltages.

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051				
0	0	0	0	0
0	0	0	0	1
0	0	1	1	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052				
INHIBIT		**B**	**A**	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	NONE
CD4053				
INHIBIT		**A or B or C**		
0		0		ax or bx or cx
0		1		ay or by or cy
1		X		NONE

X = Don't care

Fig. 13 – Truth tables.

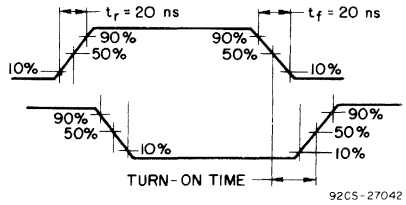


Fig. 14 – Waveforms, channel being turned ON (R_L = 10 kΩ).

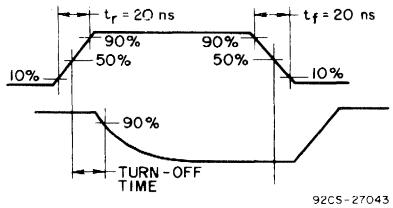


Fig. 15 – Waveforms, channel being turned OFF (R_L = 300 Ω).

CD4051B, CD4052B, CD4053B Types

TEST CIRCUITS

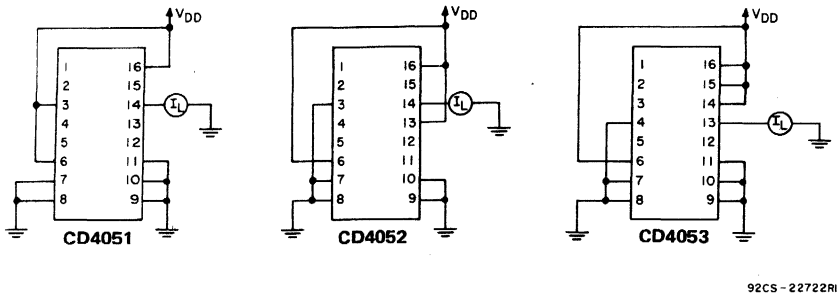


Fig.16 – OFF channel leakage current – any channel OFF.

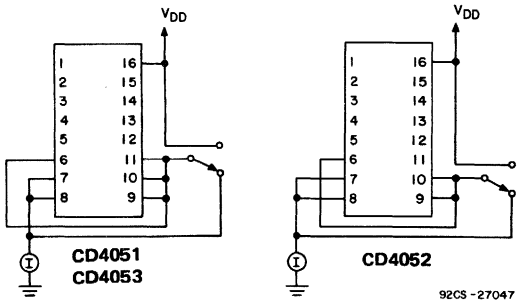


Fig.21 – Quiescent device current.

TEST CIRCUITS (Cont'd)

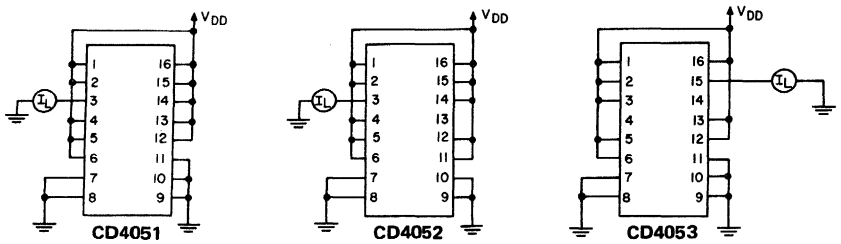


Fig.17 – OFF channel leakage current – all channels OFF.

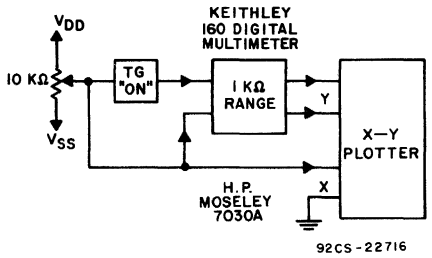


Fig.22 – Channel ON resistance measurement circuit.

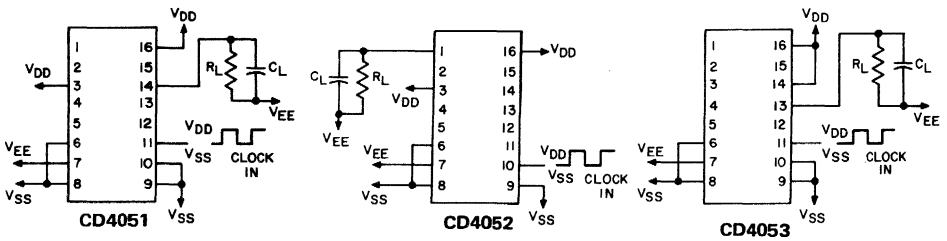


Fig.18 – Propagation delay – address input to signal output.

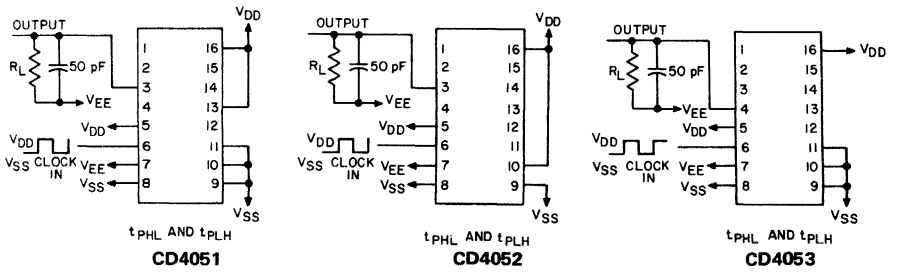


Fig.19 – Propagation delay – inhibit input to signal output.

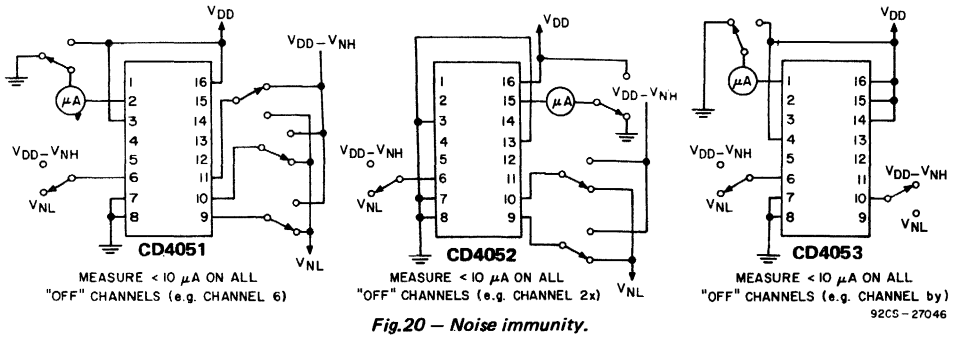


Fig.20 – Noise immunity.

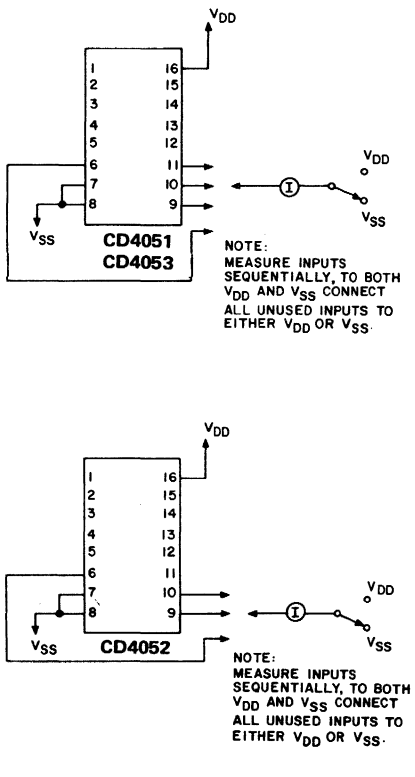


Fig.23 – Input leakage current.

CD4051B, CD4052B, CD4053B Types

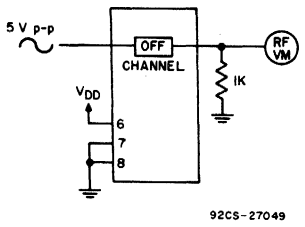


Fig.24 – Feedthrough (all types).

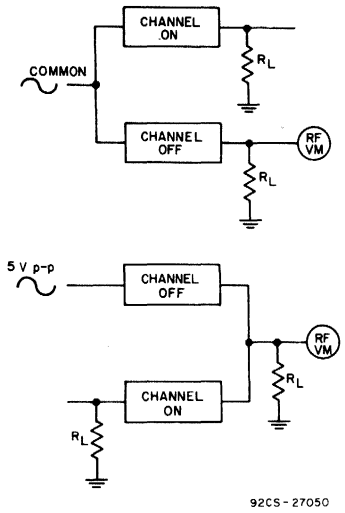


Fig.25 – Crosstalk between any two channels (all types).

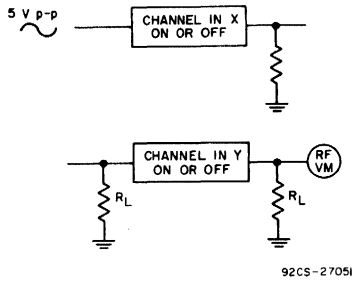


Fig.26 – Crosstalk between duals or triplets (CD4052, CD4053).

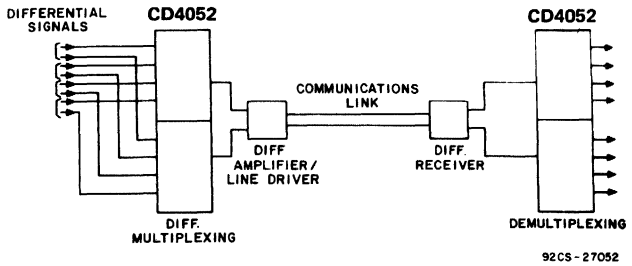


Fig.27 – Typical time-division application of the CD4052.

SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051, CD4052, or CD4053.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to V_{EE}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning ON a channel will similarly dump some charge to V_{EE}.

The amount of charge dumped is mostly a function of the signal level above V_{EE}. Typically, at V_{DD}-V_{EE} = 10 V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4 % of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel OFF, there is no charge dumping to V_{EE}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

CD4054B, CD4055B, CD4056B Types

COS/MOS Liquid-Crystal Display Drivers

High-Voltage Types (3-to-20-Volt Rating)

CD4054B – 4-Segment Display Driver
CD4055B – BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output
CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

The RCA-CD4055 and CD4056 types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as low as 0 to −3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to −15 V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4 V.

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. The DF input square wave is required to provide equivalent ac drive to liquid-crystal displays such as RCA Dev. Nos. TA8054T, TA8055T, TA8074T and R, TA8092T and R, TA8093T and R, TA8094T and R. DF square-wave repetition rates for liquid-crystal displays usually range from 30Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055 provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056 provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055 and CD4056 provides displays of 0 to 9 as well as L, P, H, A,–, and a blank position.

The CD4054 provides level shifting similar to the CD4055 and CD4056, independently strobed latches, and common DF control on 4 signal lines. The CD4054 is intended to provide drive-signal compatibility with the CD4055 and CD4056 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054 output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The CD4054 may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-

(Cont'd on next page)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{STG}) . . . . . −65 to +150°C
OPERATING TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPES E, Y . . . . . −40 to +85°C
DC SUPPLY VOLTAGE RANGE, V_{DD}
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +20 V
POWER DISSIPATION PER PACKAGE:
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K, K) Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = Full Package-Temperature Range (All Package Types) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)				3	18	V
Setup Time (t_s)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	
Strobe Pulse Width (t_W)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	

● For CD4054 and CD4056 only.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS ALL PACKAGE TYPES CD4054 Typ.	CD4054 Max.	CD4055,CD4056 Typ.	CD4055,CD4056 Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} (Any Input to Any Output)	−5	0	5	400	800	650	1300	ns
	0	0	10	340	680	575	1150	
	0	0	15	250	500	375	750	
Transition Time, t_{THL}, t_{TLH} (Any Output)	−5	0	5	100	200	100	200	ns
	0	0	10	100	200	100	200	
	0	0	15	75	150	75	150	
Minimum Data Setup Time, t_S*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
			15	35	70	35	70	
Minimum Strobe Pulse Width, t_W*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
	0	0	15	35	70	35	70	
Average Input Capacitance, C_I (Any Input)	–	–	–	5	–	5	–	pF

* CD4054 and CD4056 only.

CD4054B, CD4055B, CD4056B Types

STATIC ELECTRICAL CHARACTERISTICS:

Characteristic	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS *Values at −55°,+25°,+125°C Apply to D,F,K,H Packages; Values at −40°,+25°,+85°C Apply to E,Y Packages* −55°	−40°	+85°	+125°	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Quiescent Device Current, I_L MAX.	−5	0			5	10		100	200	–	0.02	10	μA
	0	0			10	10		100	200	–	0.02	10	
	0	0			15	20		200	400	–	0.02	20	
	0	0			20	100		1000	2000	–	0.04	100	
Output Voltage: Low Level, V_{OL} MAX.	0	0		0,5	5	0.05				–	0	0.05	V
	0	0		0,10	10	0.05				–	0	0.05	
	0	0		0,15	15	0.05				–	0	0.05	
High Level, V_{OH} MIN.	0	0		0,5	5	4.95				4.95	5	–	
	0	0		0,10	10	9.95				9.95	10	–	
	0	0		0,15	15	14.95				14.95	15	--	
Noise Immunity: Inputs Low, V_{NL} MIN.	−5	0	−4		5	1				1	2.25	–	V
	0	0	1		10	2				2	4.5	–	
	0	0	1.5		15	3				3	6.75	–	
Inputs High, V_{NH} MIN.	−5	0	4		5	1				1	2.25	–	
	0	0	9		10	2				2	4.5	–	
	0	0	13.5		15	3				3	6.75	–	
Noise Margin: Inputs Low, V_{NML} MIN.	0	0	1		5	1				1	–	–	V
	0	0	1		10	1				1	–	–	
	0	0	1.5		15	1				1	–	–	
Inputs High, V_{NMH} MIN.	0	0	4		5	1				1	–	–	
	0	0	9		10	1				1	–	–	
	0	0	13.5		15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_{DN} MIN.	−5	0	−4.5		5	1.1	1	0.75	0.6	0.9	1.8	–	mA
	0	0	0.5		10	1.1	1	0.75	0.6	0.9	1.8	–	
	0	0	1.5		15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_{DP} MIN.	−5	0	4.5		5	−6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	9.5		10	−0.6	−0.55	−0.35	−0.3	−0.45	−0.9	–	
	0	0	13.5		15	−1.9	−1.8	−1.2	−1.1	−1.5	−3	–	
Input Leakage Current (Any Input): I_{IL}, I_{IH} MAX.	0	0	"B" Series		20	±1				–	$\pm 10^{-5}$	±1	μA

signal swings (V_{DD} to V_{EE}) of +5 to −5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus the input and output swings can be selected independently of each other over a 3-to-18-V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the CD4054 and CD4056, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055 can be used by itself to drive a liquid-crystal display. The CD4056, however, must be used together with a CD4054 to provide the common DF output. The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig. 22. Fig. 21 is common to all three types.

The CD4054-, CD4055-, and CD4056-Series types are available in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications

- **General-purpose displays**
- **Calculators and meters**
- **Wall and table clocks**
- **Industrial control panels**
- **Portable lab instruments**
- **Panel meters**
- **Auto dashboard displays**
- **Appliance control panels**

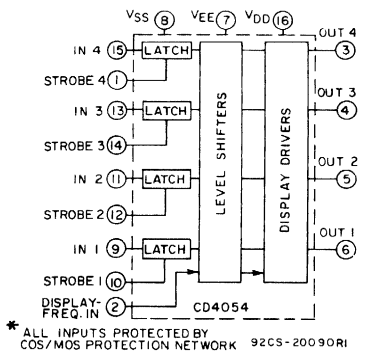


Fig. 1 – CD4054 functional diagram.

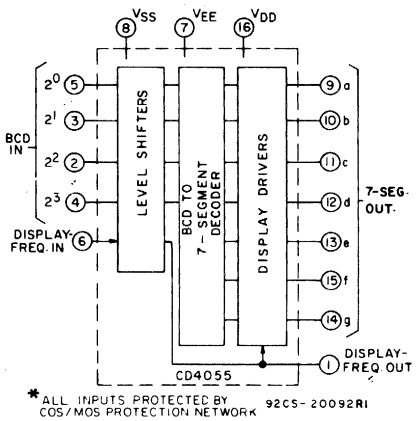
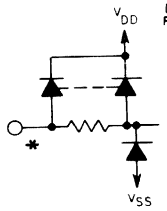


Fig. 2 – CD4055 functional diagram.



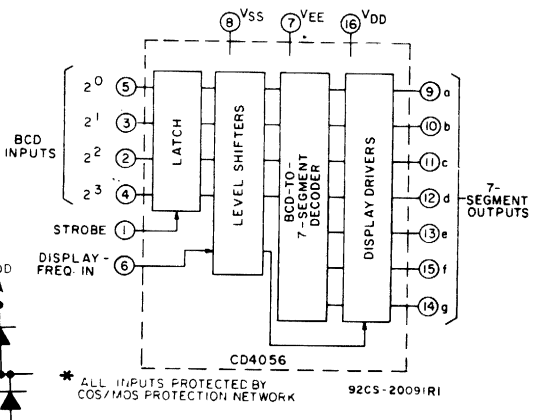


Fig. 3 – CD4056 functional diagram.

CD4054B, CD4055B, CD4056B Types

Features:

- Operation of liquid crystals with COS/MOS circuits provides ultra-low-power displays
- Equivalent ac output drive for liquid-crystal displays — no external capacitor required
- Voltage doubling across display, e.g. $V_{DD} - V_{EE}$ = 18 V results in effective 36 V p-p drive across selected display segments
- Low- or high-output level dc drive for other types of displays
- On-chip logic-level conversion for different input- and output-level swings
- Full decoding of all input combinations: 0-9, L, H, P, A,–, and blank positions
- Strobed-latch function — CD4054 Series and CD4056 Series
- DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal— CD4055 Series (CD4054 Series also; see introductory text)
- Quiescent current specified to 20-V
- Maximum input leakage of 1-μA at 20-V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

TRUTH TABLE

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	1	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	1	0	1	1	
1	0	1	0	0	0	0	1	1	1	0	
1	0	1	1	0	1	1	0	1	1	1	
1	1	0	0	1	1	0	0	1	1	1	
1	1	0	1	1	1	1	0	1	1	1	
1	1	1	0	0	0	0	0	0	0	1	—
1	1	1	1	0	0	0	0	0	0	0	BLANK

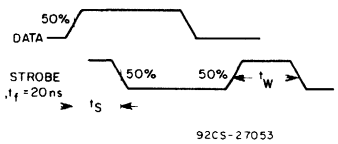


Fig.4 — Data setup time and strobe pulse duration.

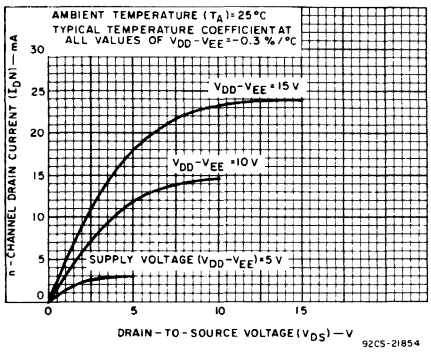


Fig.5 — Typical n-channel drain characteristics.

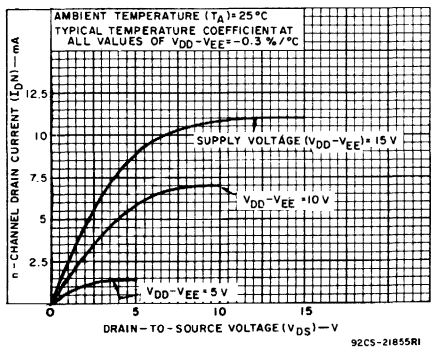


Fig.6 — Minimum n-channel drain characteristics.

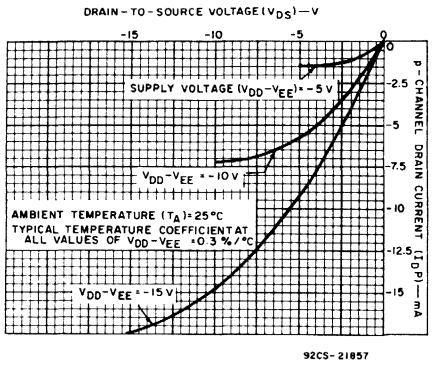


Fig.7 — Typical p-channel drain characteristics.

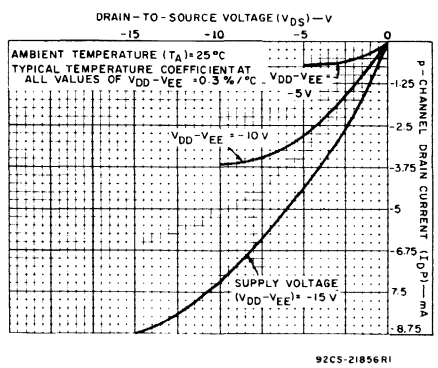


Fig.8 — Minimum p-channel drain characteristics.

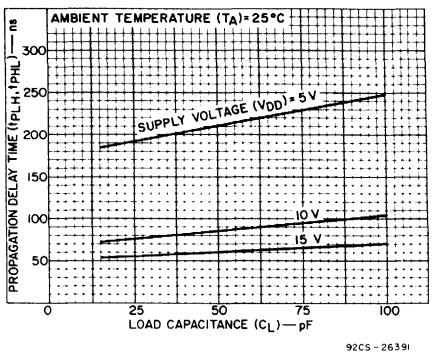


Fig.9 — Typical propagation delay time vs. load capacitance.

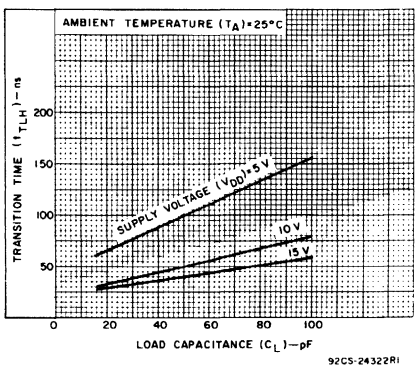


Fig.10 — Typical transition time vs. load capacitance.

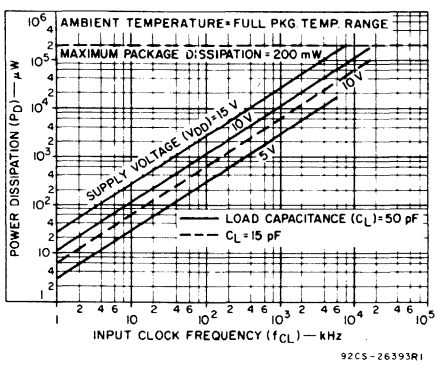


Fig.11 — Typical input clock frequency vs. power dissipation.

CD4054B, CD4055B, CD4056B Types

TEST CIRCUITS

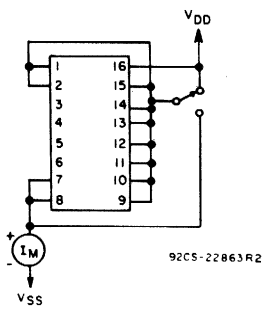


Fig.12 – Quiescent-device-current (CD4054).

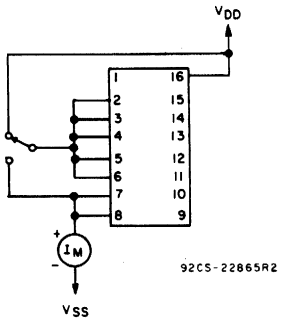


Fig.13 – Quiescent-device-current (CD4055).

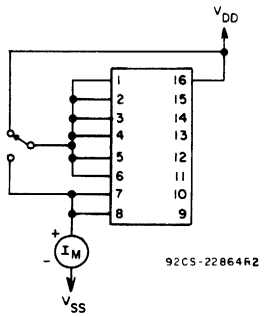


Fig.14 – Quiescent-device-current (CD4056).

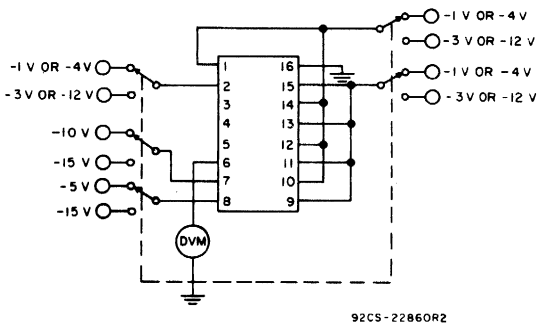


Fig.15 – Noise immunity (CD4054).

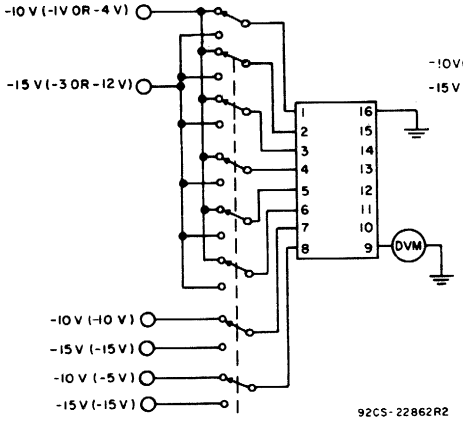


Fig. 16 – Noise immunity (CD4056).

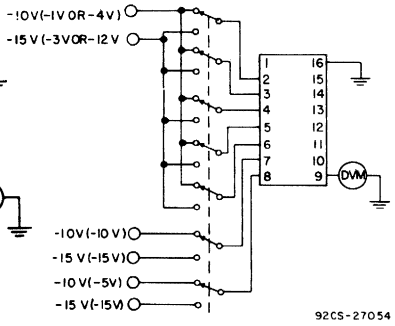


Fig. 17 – Noise immunity (CD4055)

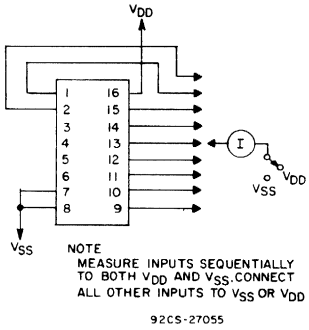


Fig.18 – Input leakage current (CD4054).

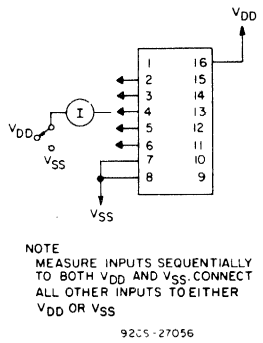


Fig.19 – Input leakage current (CD4055).

APPLICATIONS

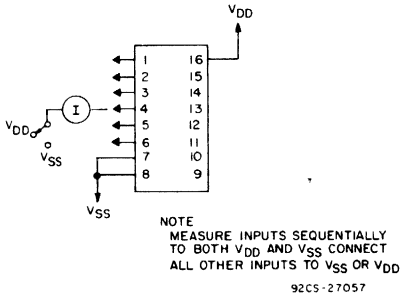
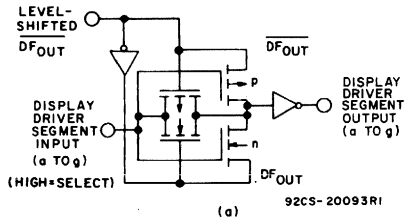


Fig.20 – Input leakage current (CD4056).



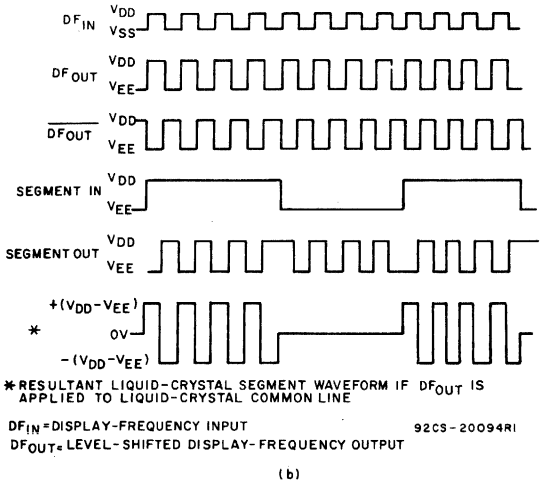


Fig.21 – Display-driver circuit for one segment line and waveforms.

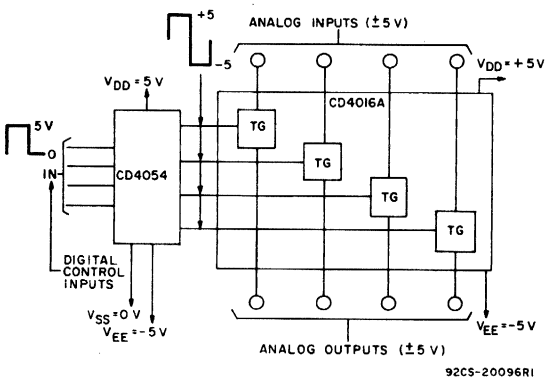


Fig.22 – Digital (0 to +5 V) to bidirectional analog control (+5 to –5 V) level shifter.

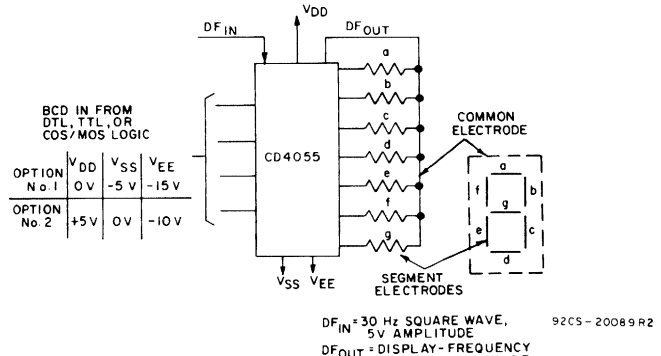


Fig. 23 – Single-digit liquid-crystal display.

CD4063B Types

COS/MOS 4-Bit Magnitude Comparator

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4063 is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

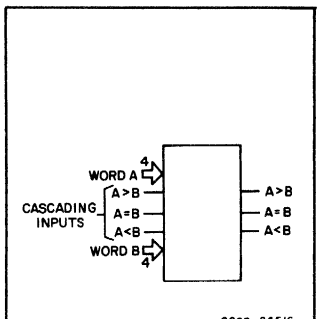
The CD4063 has eight comparing inputs (A3, B3, through A0, B0), three outputs ($A < B$, $A = B$, $A > B$) and three cascading inputs ($A < B$, $A = B$, $A > B$) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063 is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = low.

For words longer than 4 bits, CD4063 devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ($A < B$, $A = B$, and $A > B$) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Expansion to 8, 12, 16 . . . 4N bits by cascading units**
- **Medium-speed operation: compares two 4-bit words in 250 ns (typ.) at 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**



CD4063 Functional Diagram

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

Applications:

- **Servo motor controls**
- **Process controllers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPES E, Y . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A= −40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A= +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A= −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A= +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}	5	625	1250	ns
	10	250	500	
	15	175	350	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}	5	500	1000	ns
	10	200	400	
	15	140	280	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Average Input Capacitance, C_I	Any Input	5	–	pF

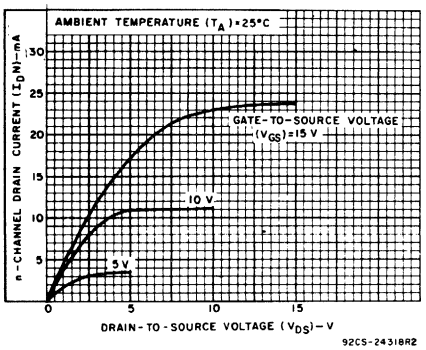


Fig. 1 – Typical output-N-channel drain characteristics.

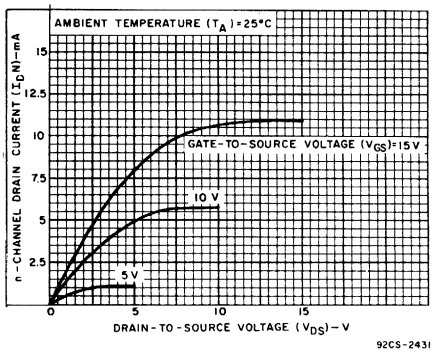


Fig. 2 – Minimum output-N-channel drain characteristics.

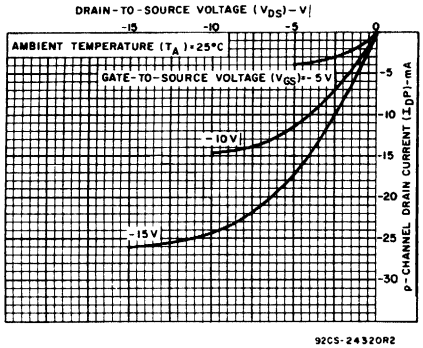


Fig. 3 – Typical output-P-channel drain characteristics.

CD4063B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

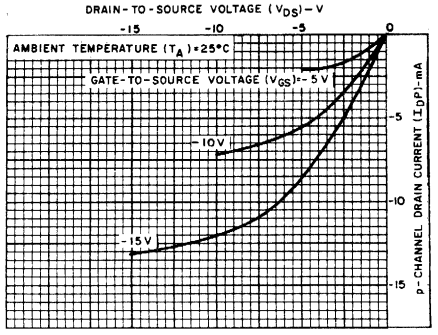


Fig. 4—Minimum output-P-channel drain characteristics.

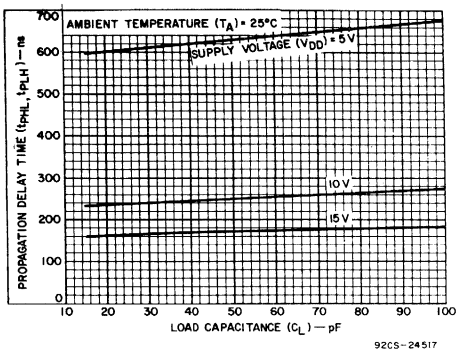


Fig. 5—Typical propagation delay time vs. load capacitance.

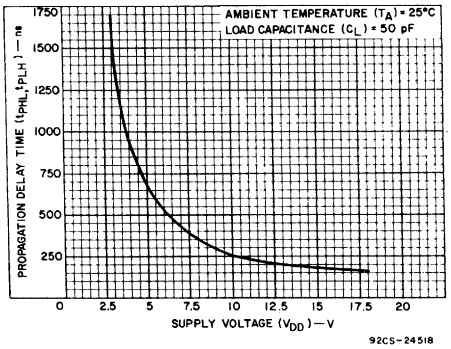


Fig. 6—Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

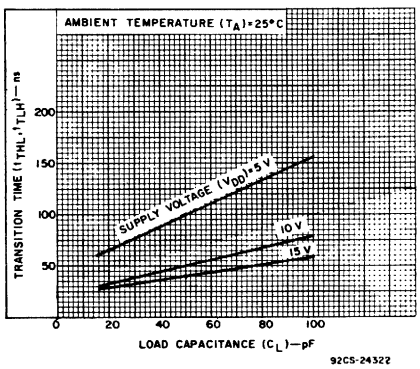


Fig. 7—Typical transition time vs. load capacitance.

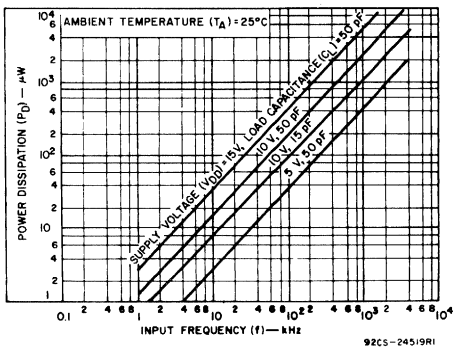


Fig. 8—Typical dynamic power dissipation characteristics (see Fig. — dynamic power dissipation test circuit).

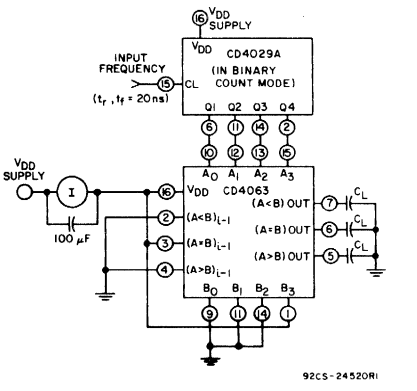


Fig. 9—Dynamic power dissipation test circuit.

CD4063B Types

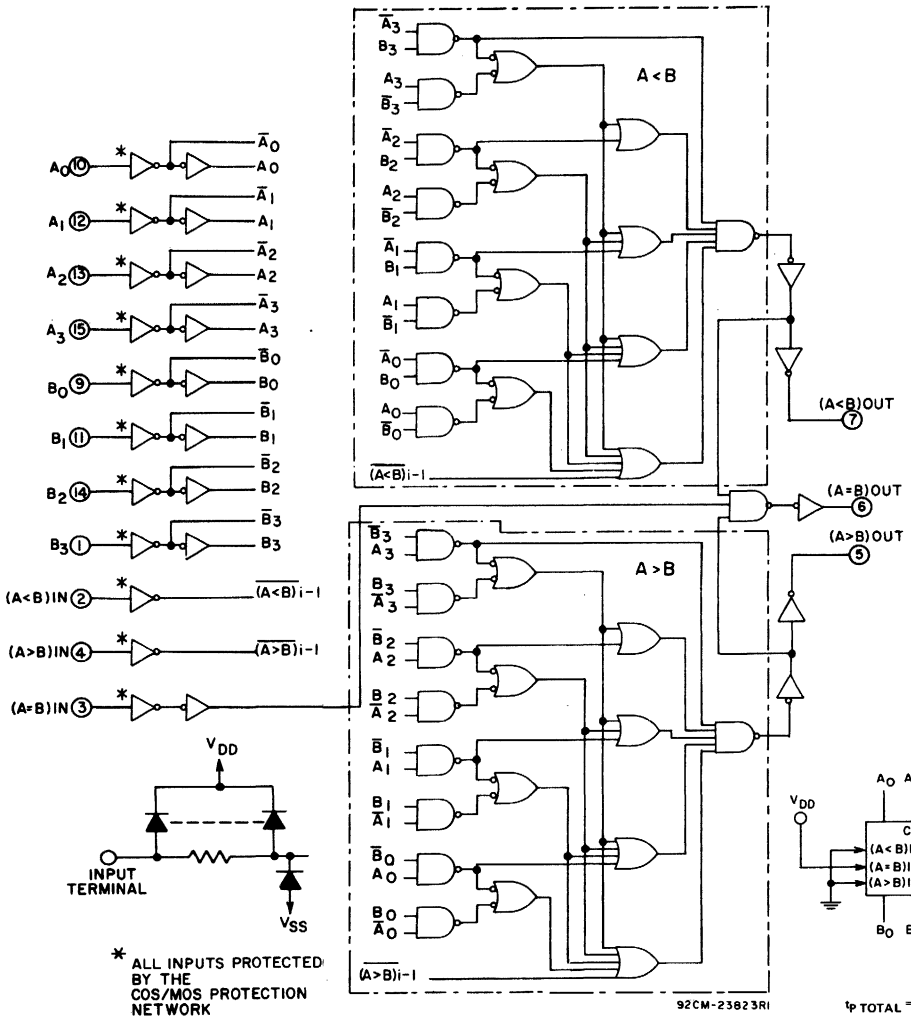


Fig. 10 — Logic diagram for CD4063B.

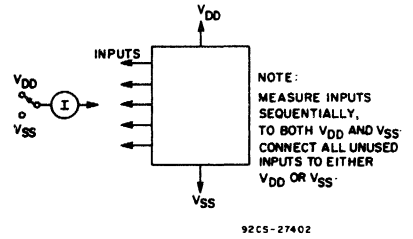


Fig. 11—Input leakage current test circuit.

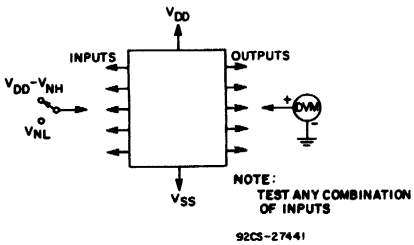
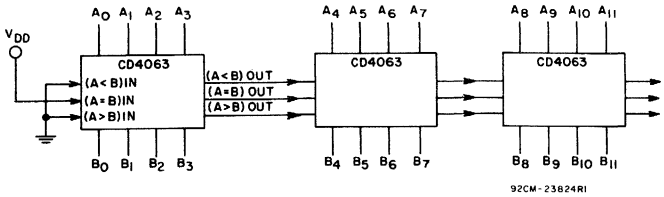


Fig. 12—Noise immunity test circuit.



t_P TOTAL = t_P (COMPARE INPUTS) + 2 x t_P (CASCADE INPUTS), AT V_{DD} = 10V
(3 STAGES)
= 250 + (2 x 200) = 650 ns (TYP.)

Fig. 13—Typical speed characteristics of a 12-bit comparator.

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	X	0	0	1
A3=B3	A2>B2	X	X	X	X	X	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care Logic 1 ≡ High Level Logic 0 ≡ Low Level

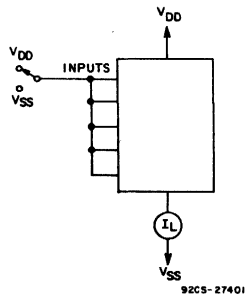


Fig. 14—Quiescent device current test circuit.

CD4067B, CD4097B Types

COS/MOS Analog Multiplexers/Demultiplexers

High-Voltage Types (3- to 20-Volt Rating)
CD4067B – Single 16-Channel Multiplexer/Demultiplexer
CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

The RCA-CD4067 and CD4097 COS/MOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067 is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097 is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067 and CD4097 are supplied in 24-lead dual-in-line white ceramic packages (D suffix), 24-lead ceramic flat-packs (K suffix), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

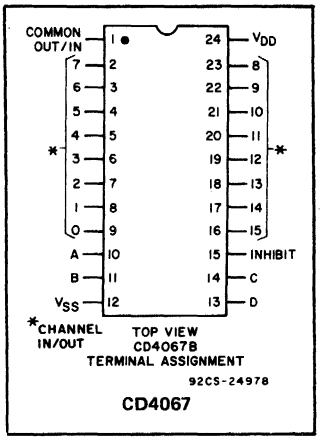
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

Features:

- **Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS}=15$ V**
- **High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}=10$ V**
- **Matched switch characteristics: $R_{ON}=5$ Ω (typ.) for $V_{DD}-V_{SS}=15$ V**
- **Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}=10$ V**
- **Binary address decoding on chip**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20 V (full package-temperature range)**
- **1 V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Analog and digital multiplexing and demultiplexing**
- **A/D and D/A conversion**
- **Signal gating**



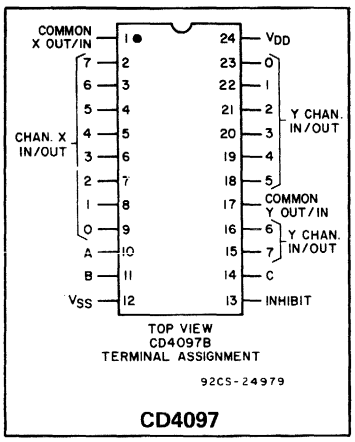


Fig. 2 – Terminal assignment.

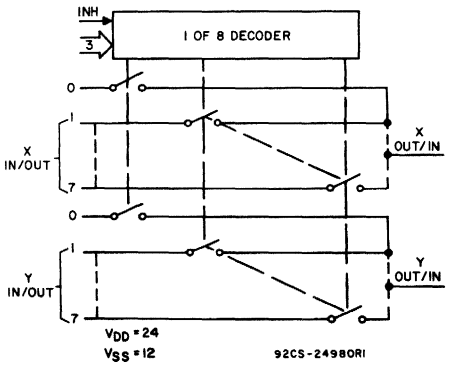


Fig. 1 – CD4097 functional diagram.

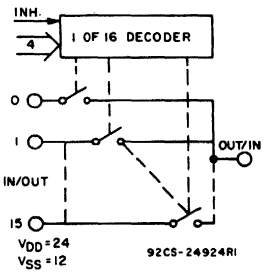


Fig. 3 – CD4067 functional diagram.

Recommended Operating Conditions at $T_A = 25^oC$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:
In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{STG}) ..... –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
Package Types D, K, H ..... –55 to +125°C
Package Type E ..... –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, V_{DD}:
(Voltages referenced to V_{SS}) ..... –0.5 to +20 V
POWER DISSIPATION PER PACKAGE:
For T_A = –40 to +60°C (Package Type E) ..... 500 mW
For T_A = +60 to +85°C (Package Type E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (Package Types D, K) ..... 500 mW
For T_A = +100 to +125°C (Package Types D, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER CHANNEL:
For T_A = Full Package-Temperature Range (All Package Types) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,K,H pkg Values at −40,+25,+85,apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_L Max.			5	5	5	30	100	–	0.02	5	μA
			10	10	10	100	200	–	0.02	10	
			15	20	20	200	400	–	0.02	20	
			20	100	100	1000	2000	–	0.04	100	
ON Resistance $V_{SS} \leqslant V_{is} \leqslant V_{DD}$ R_{ON} Max.		0	5	2000	2100	3200	3500	–	470	2500	Ω
		0	10	310	330	520	580	–	180	400	
		0	15	220	230	360	400	–	125	280	
ΔON Resistance (Between Any Two Channels) ΔR_{ON}		0	5	–	–	–	–	–	10	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current: Any Channel OFF Max.		0	10	±200*				–	±0.1	±200*	nA
		0	15	±500*				–	±0.1	±200*	
		0	20	±1000*				–	±0.1	±200*	
All Channels OFF (Common OUT/IN) Max.		0	10	±200*				–	±0.1	±200*	
		0	15	±500*				–	±0.1	±200*	
		0	20	±1000*				–	±0.1	±200*	
Capacitance: Input, C_{is}				–	–	–	–	–	5	–	pF
Output, C_{os} CD4067		−5	5	–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feedthrough, C_{ios}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output	10 V	R_L=10 KΩ, C_L=50 pF, t_r, t_f=20 ns	5	–	–	–	–	–	30	–	ns
			10	–	–	–	–	–	15	–	
			15	–	–	–	–	–	11	–	

* Determined by minimum feasible leakage measurement for automatic testing.

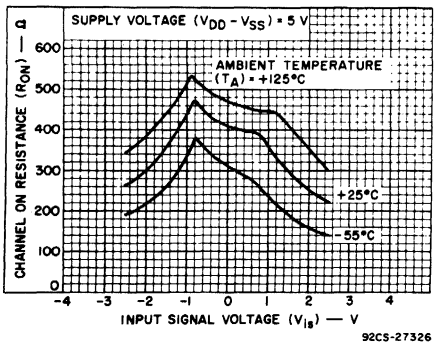


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

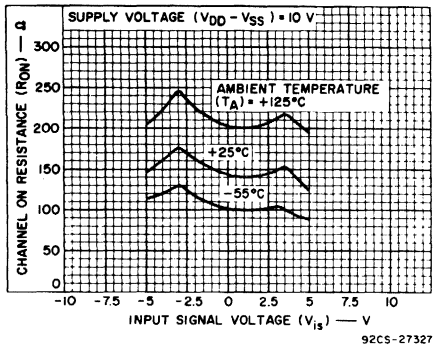


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

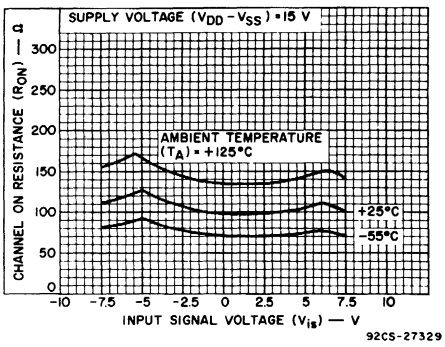


Fig. 6 — Typical ON resistance vs. input signal voltage (all types).

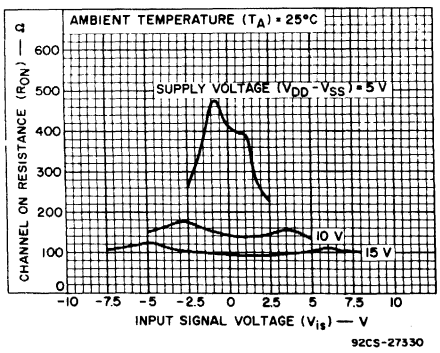
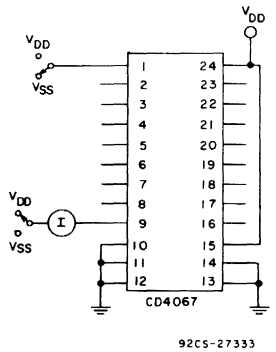


Fig. 7 —Typical ON resistance vs. input signal voltage (all types).

TEST CIRCUITS



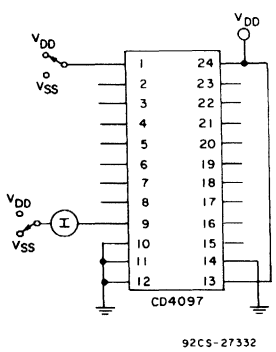


Fig. 8 —OFF channel leakage current—any channel OFF.

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,K,H pkg Values at −40,+25,+85,apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CONTROL (ADDRESS or INHIBIT) V_C											
Noise Immunity Min.: Inputs Low, V_{NL}	$=V_{DD}$ thru 1 KΩ	R_L=1 KΩ to V_{SS} I_{IS}<2 μA on all OFF Channels	5		1.5			1.5	2.25	–	V
			10		3			3	4.5	–	
			15		4.5			4.5	6.75	–	
Inputs High, V_{NH}			5		1.5			1.5	2.25		
			10		3			3	4.5		
			15		3			3	6.75	–	
Input Leakage Current; I_{IL},I_{IH} Max.	("A" Series)		15		±1			–	$\pm10^{-5}$	±1	μA
	("B" Series)		20		±1			–	$\pm10^{-5}$	±1	
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L=10 KΩ,C_L= 50 pF, t_r,t_f=20 ns	0	5	–	–	–	–	–	325	650	ns
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R_L=300 Ω,C_L= 50 pF, t_r,t_f=20 ns	0	5	–	–	–	–	–	220	440	ns
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Average Input Capacitance, C_I	Any Address or Inhibit Input			–	–	–	–	–	5	–	pF

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

TEST CIRCUITS (Cont'd)

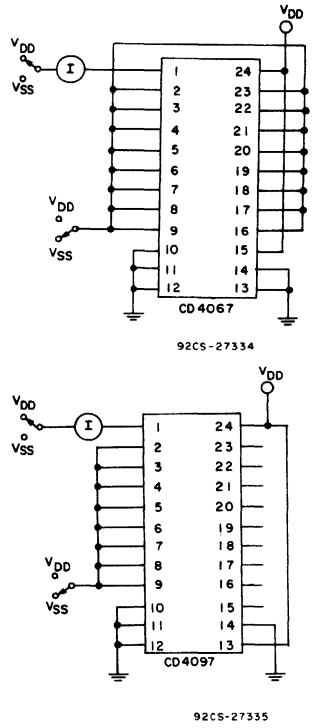


Fig. 9 —OFF channel leakage current—all channels OFF.

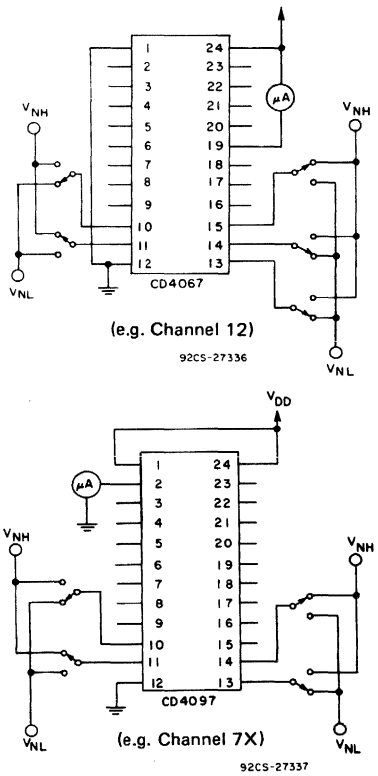


Fig. 10 —Noise immunity—measure < 2 μA on all OFF channels (e.g. channel 12).

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{is} (V)	V_{DD} (V)	R_L (KΩ)	TYPICAL LIMITS AT INDICATED CONDITIONS		TYPICAL VALUES	UNITS
Frequency Response Channel ON (Sine Wave Input)	5●	10	1	V_{os} at Common OUT/IN	CD4067	14	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB				CD4097	20	
				V_{os} at Any Channel		60	
Sine Wave Response (Distortion)	2●	5	10			0.3	%
	3●	10				0.2	
	5●	15				0.12	
	f_{is} = 1 kHz						
Feedthrough (All Channels OFF)	5●	10	1	V_{os} at Common OUT/IN	CD4067	20	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB				CD4097	12	
				V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	Between Any 2 Channels▲		1	MHz
	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB			Between Sections CD4097 Only	Measured on Common	10	
					Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	–	10	10*			75	mV (Peak)
	V_{SS}=0, t_r,t_f=20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)						

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

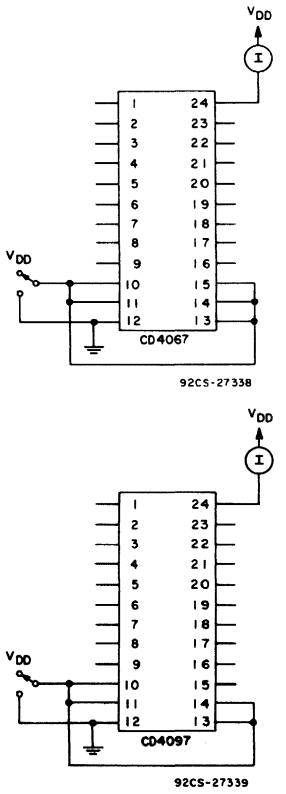


Fig. 11 – Quiescent device current.

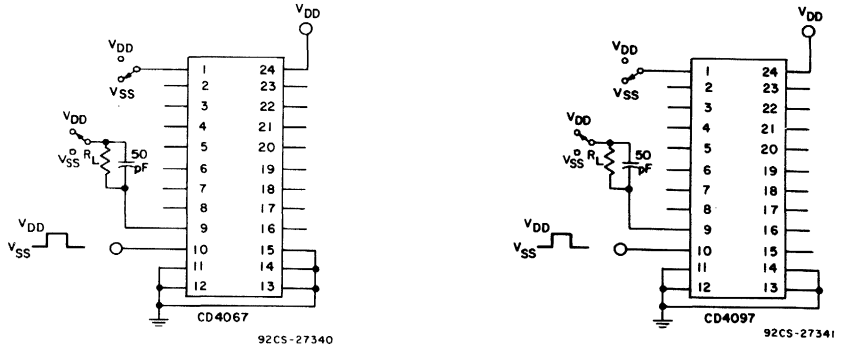


Fig. 12 – Turn-on and turn-off propagation delay–address select input to signal output (e.g. measured on channel 0).

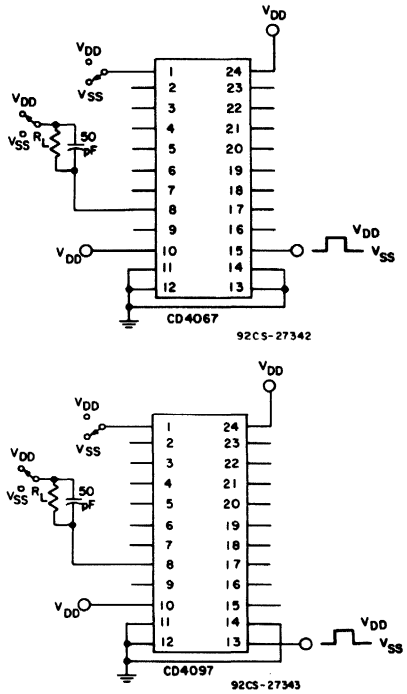


Fig. 13 – Turn-on and turn-off propagation delay–inhibit input to signal output (e.g. measured on channel 1).

CD4067B, CD4097B Types

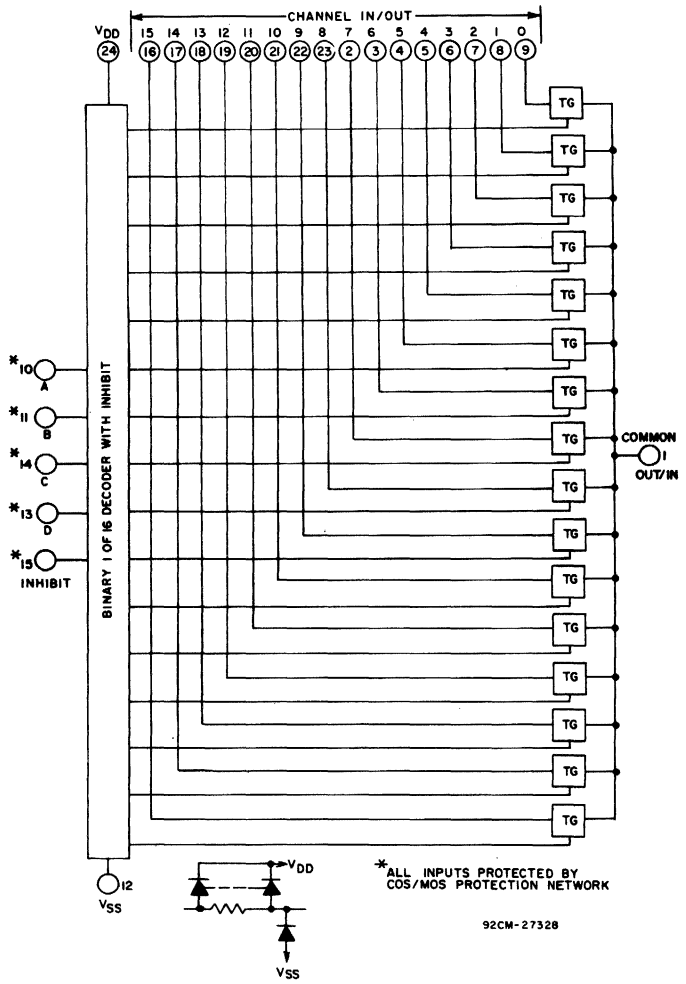


Fig. 14 —CD4067 logic diagram.

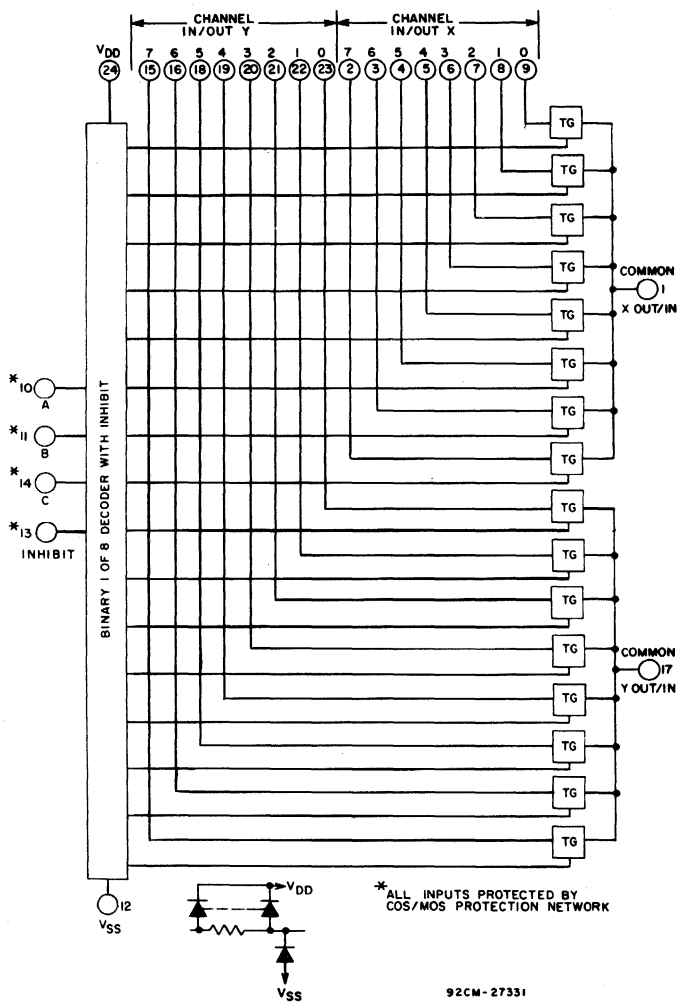


Fig. 15 —CD4097 logic diagram.

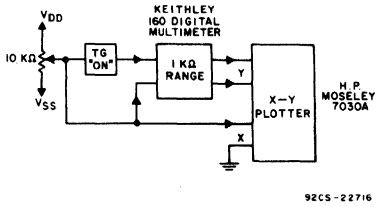


Fig. 16—Channel ON resistance measurement circuit.

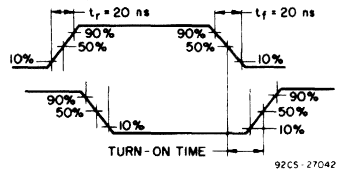


Fig. 17—Propagation delay waveform channel being turned ON (R_L=10 KΩ, C_L= 50 pF).

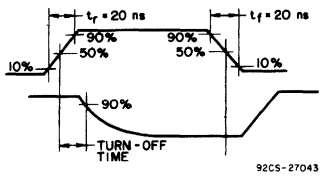


Fig. 18—Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L=effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067 or CD4097.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning ON a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at $V_{DD}-V_{SS}$=10 V, a 100-pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel OFF, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

CD4068B Types

COS/MOS 8-Input NAND Gate

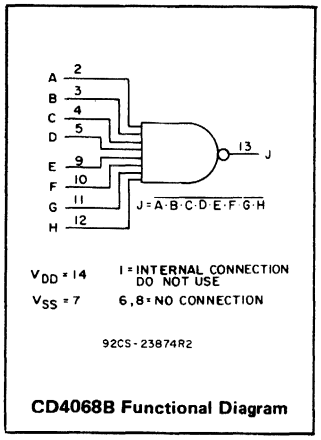
High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4068B NAND gate provides the system designer with direct implementation of the positive-logic 8-input NAND function and supplements the existing family of COS/MOS gates.

The CD4068B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-Speed Operation — t_{PHL} = 130 ns, t_{PLH} = 100 ns (typ.) at 10 V**
- **Buffered Output**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**



CD4068B Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPES E,Y . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = –55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Propagation Delay Time: High-to-Low Level, t_{PHL}	5	325	650	ns
	10	130	260	
	15	100	200	
Low-to-High Level, t_{PLH}	5	250	500	ns
	10	100	200	
	15	75	150	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Average Input Capacitance, C_I	Any Input	5	–	pF

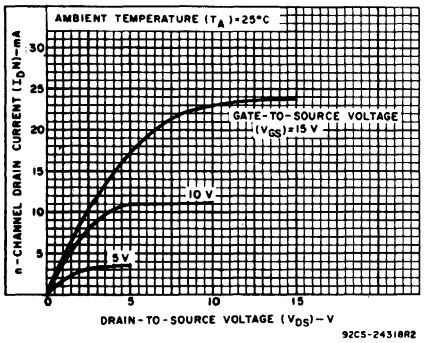


Fig. 1 — Typical output-n-channel drain characteristics.

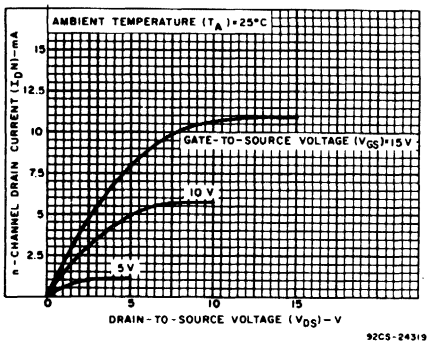


Fig. 2 — Minimum output-n-channel drain characteristics.

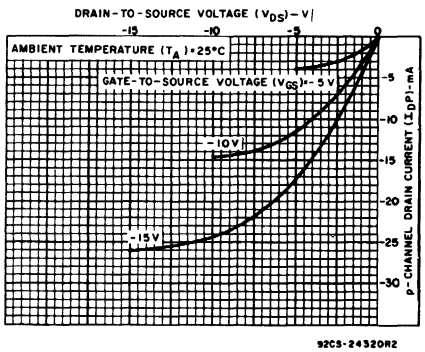


Fig. 3 — Typical output-p-channel drain characteristics.

CD4068B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E, Y Packages*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current; I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: n-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
p-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	−2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL},I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

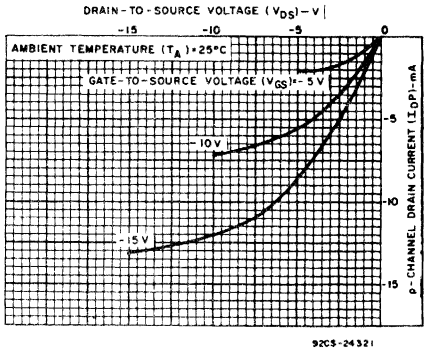


Fig. 4 – Minimum output-p-channel drain characteristics.

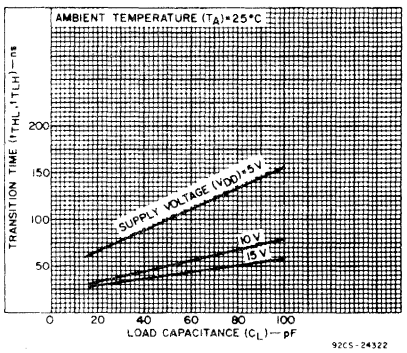


Fig. 5 – Typical transition time vs. load capacitance.

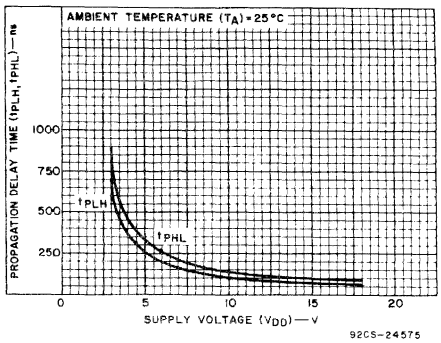


Fig. 6 – Typical propagation delay time vs. supply voltage.

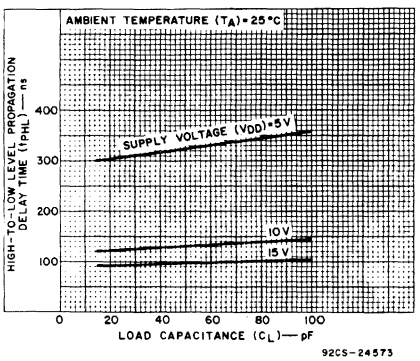


Fig. 7 – Typical high-to-low level propagation delay time vs. load capacitance.

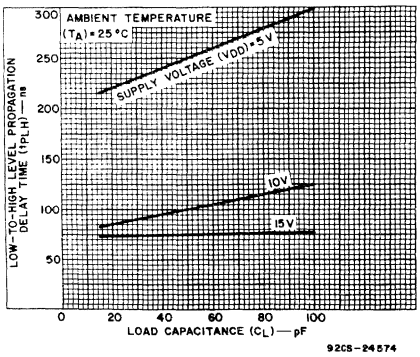


Fig. 8 – Typical low-to-high level propagation delay time vs. load capacitance.

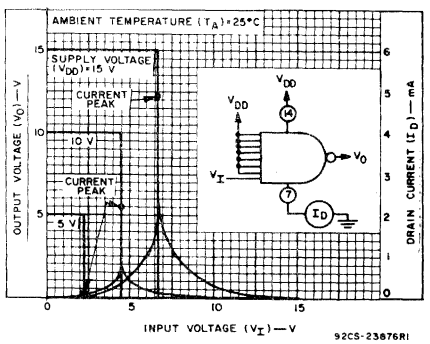


Fig. 9 – Typical voltage and current transfer characteristics.

CD4068B Types

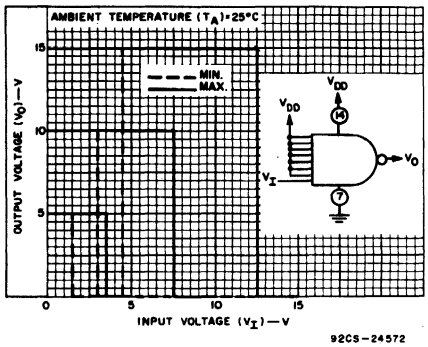


Fig. 10 – Minimum and maximum voltage transfer characteristics.

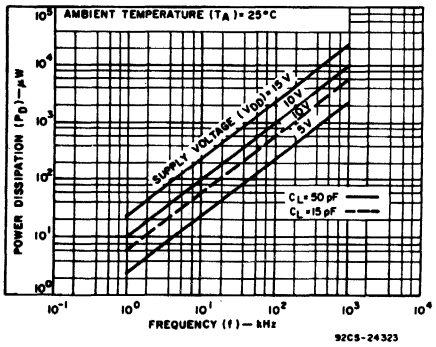


Fig. 11 – Typical power dissipation vs. frequency.

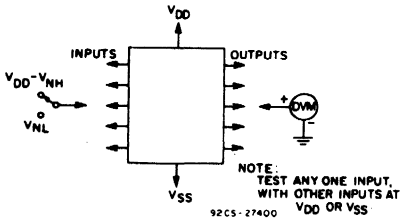


Fig. 12 – Noise immunity test circuit.

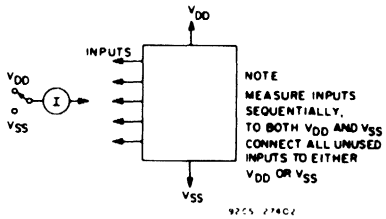


Fig. 13 – Input leakage current test circuit.

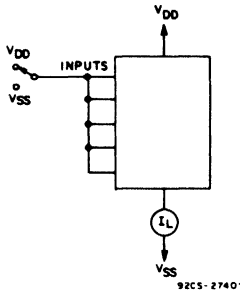


Fig. 14 – Quiescent device current test circuit.

CD4069B Types
COS/MOS Hex Inverter

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4069B consists of six COS/MOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter/Buffers are not required.

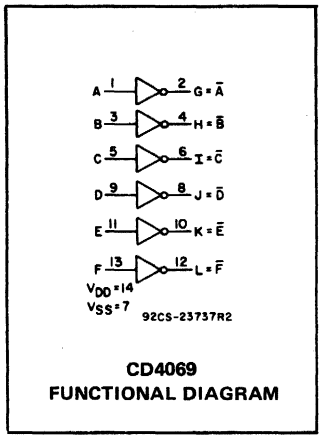
The CD4069B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium Speed Operation – t_{PHL}, t_{PLH} = 40 ns (typ.) at 10 V
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



CD4069
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance;	C_I	Any Input	5	–	pF

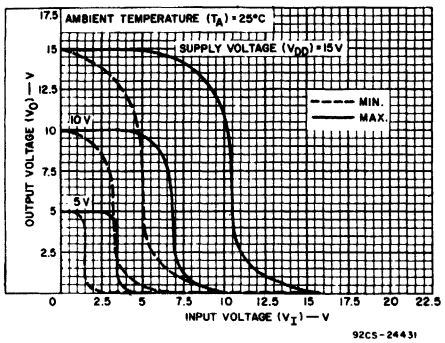


Fig. 1 – Minimum and maximum voltage transfer characteristics.

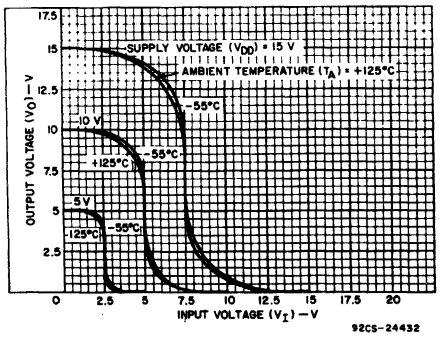


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

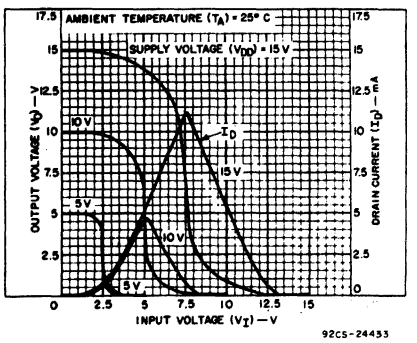


Fig. 3 – Typical current and voltage transfer characteristics.

CD4069B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_{DP} Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	3.6	–	5	1.5				1.5	2.25	–	V
	7.2	–	10	3				3	4.5	–	
	10.8	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	1.4	–	5	1.5				1.5	2.25	–	
	2.8	–	10	3				3	4.5	–	
	4.2	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA

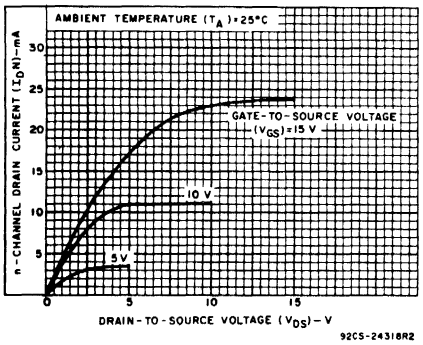


Fig. 4 — Typical output-N-channel drain characteristics.

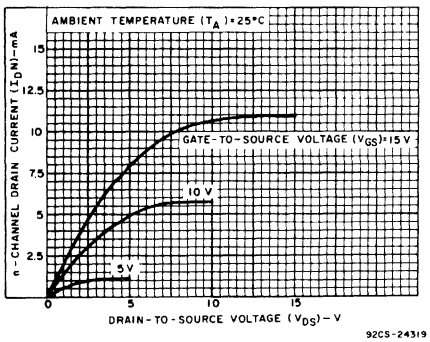


Fig. 5 — Minimum output-N-channel drain characteristics.

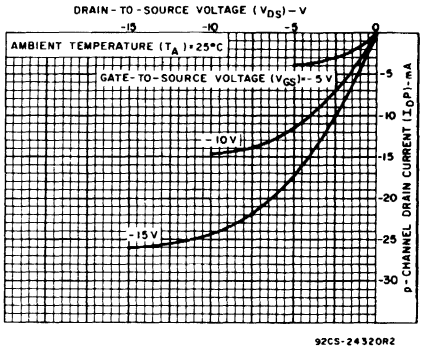


Fig. 6 — Typical output-P-channel drain characteristics.

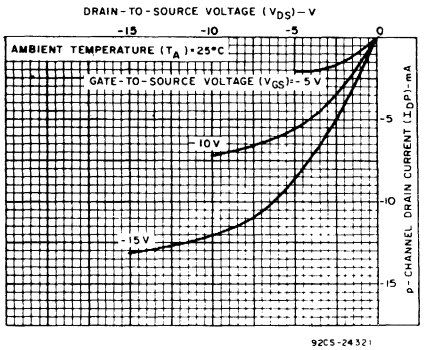


Fig. 7 — Minimum output-P-channel drain characteristics.

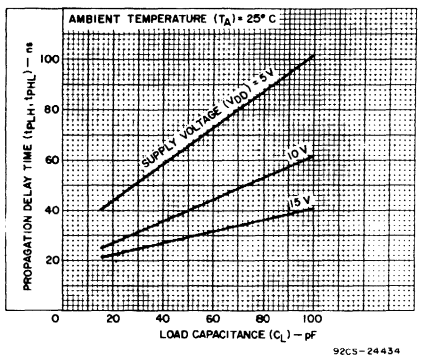


Fig. 8 — Typical propagation delay time vs. load capacitance.

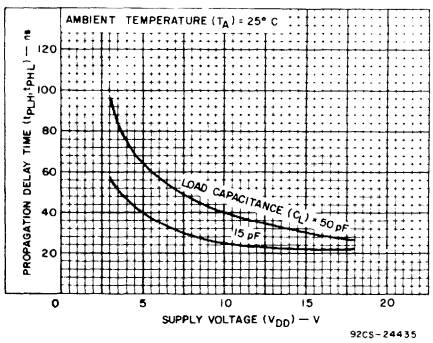


Fig. 9 — Typical propagation delay time vs. supply voltage.

CD4069B Types

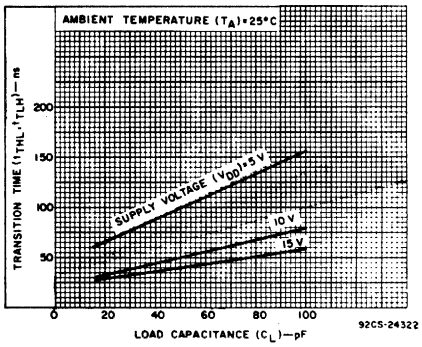


Fig. 10 – Typical transition time vs. load capacitance.

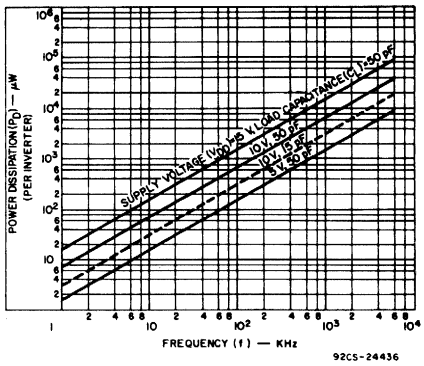


Fig. 11 – Typical dynamic power dissipation.

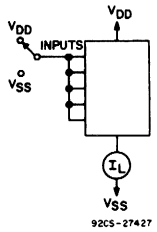


Fig. 12 – Quiescent device current test circuit.

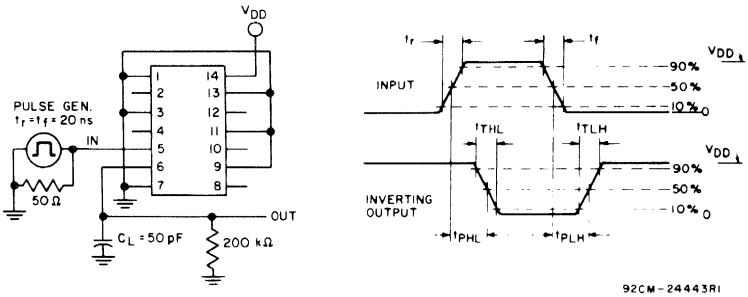


Fig. 13 – Dynamic electrical characteristics test circuit and waveforms.

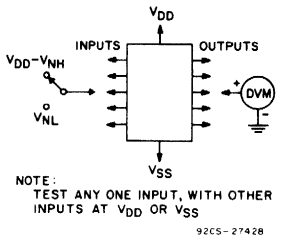


Fig. 14 – Noise immunity test circuit.

APPLICATIONS

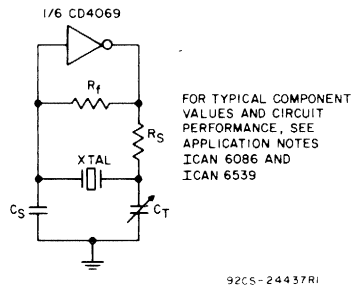


Fig. 15 – Typical crystal oscillator circuit.

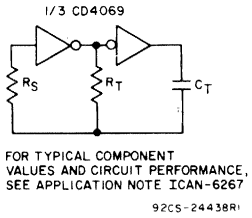


Fig. 16 – Typical RC oscillator circuit.

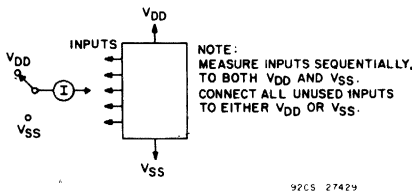


Fig. 17 – Input leakage current test circuit.

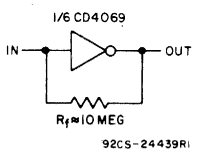


Fig. 18 – High-input impedance amplifier.

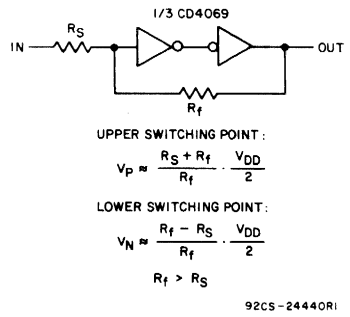


Fig. 19 – Input pulse shaping circuit (Schmitt trigger).

CD4070B, CD4077B Types

COS/MOS Quad Exclusive-OR and Exclusive-NOR Gates

High-Voltage Types (3-to-20-Volt Rating)

CD4070 —— Quad Exclusive-OR Gate

CD4077 —— Quad Exclusive-NOR Gate

The RCA-CD4070B contains four independent Exclusive-OR gates. The RCA-CD4077B contains four independent Exclusive-NOR gates.

The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively. The CD4070 is similar to the RCA-CD4030, but has greater output sourcing capability and higher input impedance.

The CD4070B- and CD4077B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation —— $t_{PHL} = t_{PLH}$ = 70 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Logical comparators**
- **Adders/subtractors**
- **Parity generators and checkers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

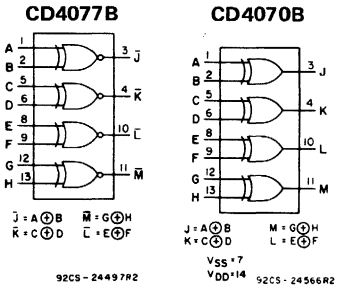


Fig. 1 — Functional diagrams.

TRUTH TABLE CD4070
1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High Level
" 0 = Low Level
$J = A \oplus B$

TRUTH TABLE CD4077
1 of 4 Gates

A	B	$\bar{J}$
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High Level
" 0 = Low Level
$\bar{J} = \overline{A \oplus B}$

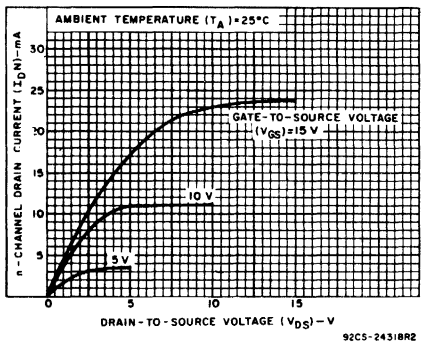


Fig. 2 — Typical output N-channel drain characteristics.

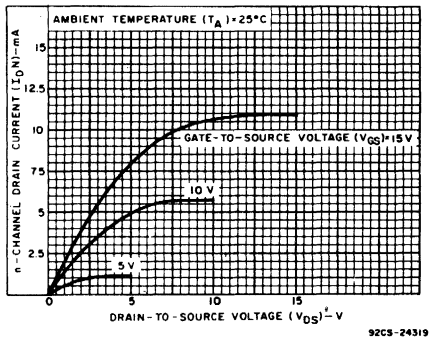


Fig. 3 — Minimum output N-channel drain characteristics.

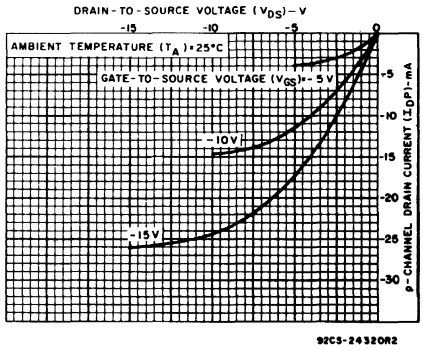


Fig. 4 — Typical output P-channel drain characteristics.

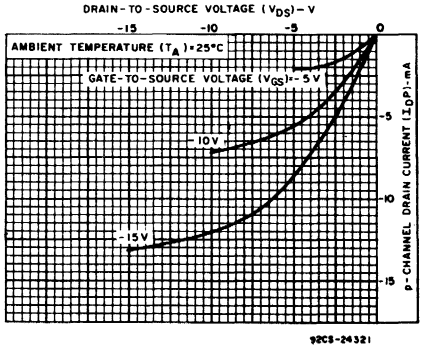


Fig. 5 — Minimum output P-channel drain characteristics.

CD4070B, CD4077B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_{DP} Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

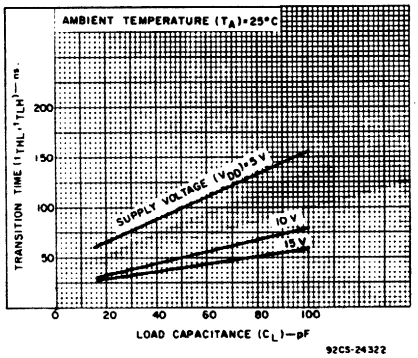


Fig. 6 – Typical transition time vs. load capacitance.

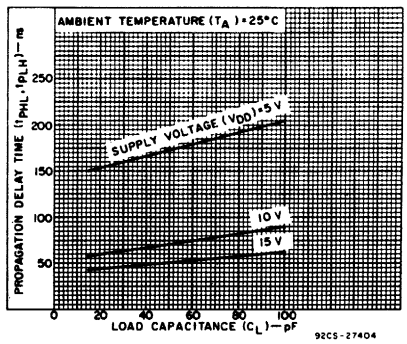


Fig. 7 – Typical propagation delay time vs. load capacitance.

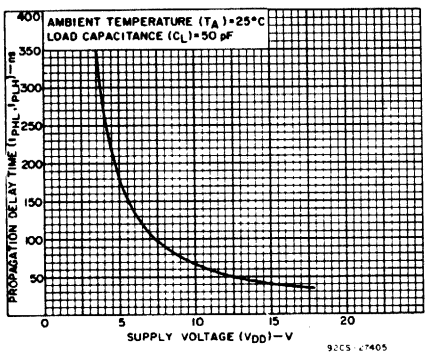


Fig. 8 – Typical propagation delay time vs. supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time;	t_{PLH}, t_{PHL}	5	175	350	ns
		10	70	140	
		15	50	100	
Transition Time;	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance;	C_I	Any Input	5	–	pF

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

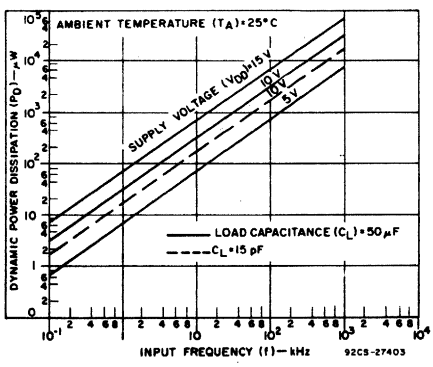


Fig. 9 – Typical dynamic power dissipation vs. input frequency.

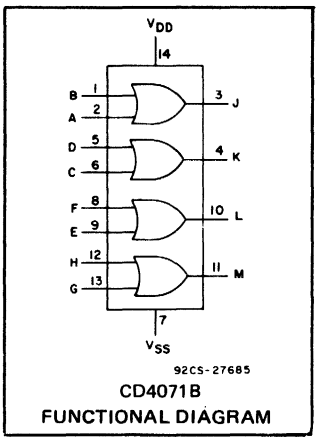
CD4071B, CD4072B, CD4075B Types

COS/MOS OR Gates

High-Voltage Types (3-to-20-Volt Rating)

CD4071B Quad 2-Input OR Gate
CD4072B Dual 4-Input OR Gate
CD4075B Triple 3-Input OR Gate

The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates.



CD4071B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C
PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . .Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . .Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . .-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

The CD4071, CD4072 and CD4075 types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-Speed Operation t_{PLH} = 70 ns (typ.); t_{PHL} = 100 ns (typ.) at 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

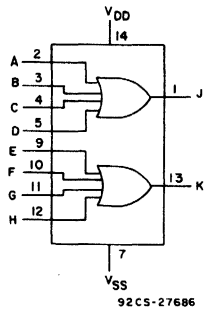


Fig. 1 -- Functional diagram for CD4072B.

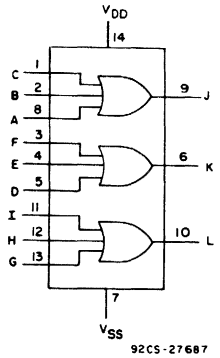


Fig. 2 – Functional diagram for CD4075B.

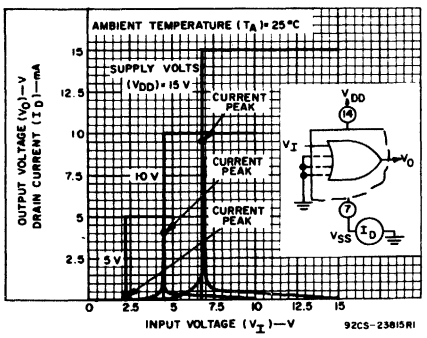


Fig. 3 – Typical voltage and current transfer characteristics.

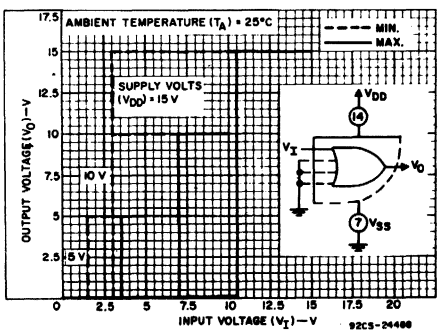


Fig. 4 – Minimum and maximum voltage transfer characteristics.

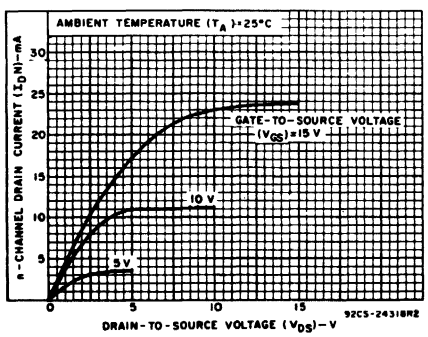


Fig. 5 – Typical output-N-channel drain characteristics.

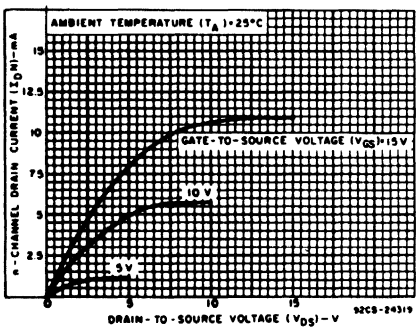


Fig. 6 – Minimum output-N-channel drain characteristics.

CD4071B, CD4072B, CD4075B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55, +25, +125 Apply to D, K, F, H Packages* *Values at -40, +25, +85 Apply to E, Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	3.75				3.75	5.6	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5		
	1.5	–	15	3.75				3.75	5.6	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
			V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	250	500	ns
			10	100	200	
			15	80	150	
Low-to-High Level	t_{PLH}		5	175	350	ns
			10	70	140	
			15	55	110	
Transition Time	t_{THL} t_{TLH}		5	100	200	ns
			10	50	100	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	–	pF

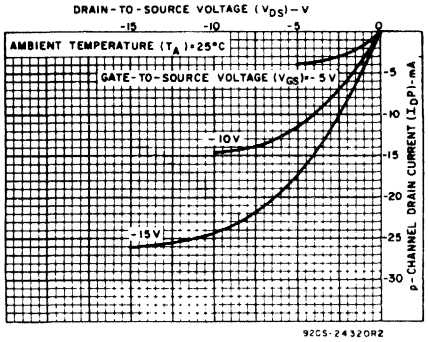


Fig. 7 – Typical output-P-channel drain characteristics.

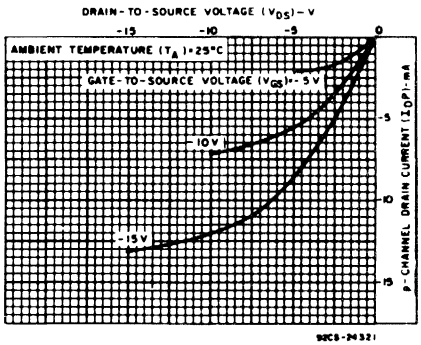


Fig. 8 – Minimum output-P-channel drain characteristics.

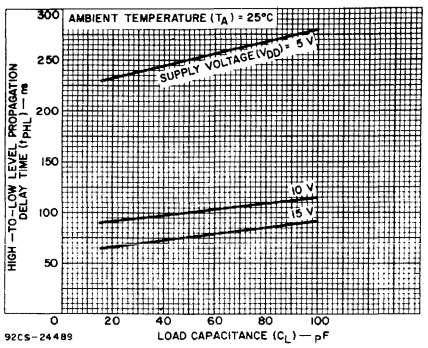


Fig. 9 – Typical high-to-low level propagation delay time vs. load capacitance.

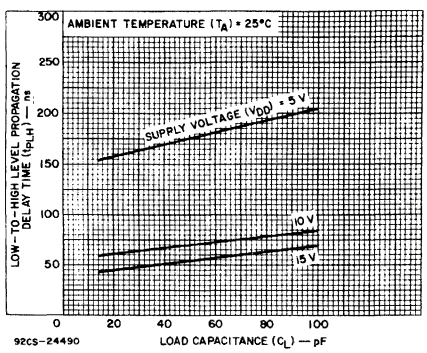


Fig. 10 – Typical low-to-high level propagation delay time vs. load capacitance.

CD4071B, CD4072B, CD4075B Types

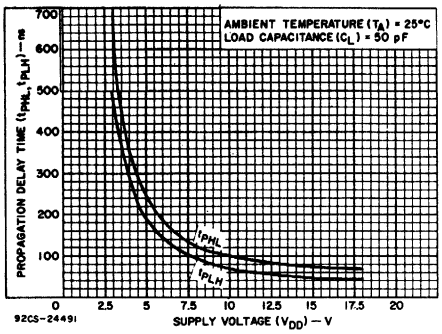


Fig. 11 – Typical propagation delays vs. supply voltage.

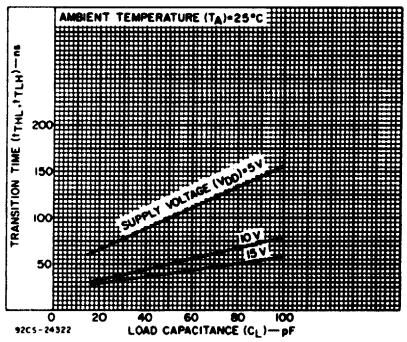


Fig. 12 – Typical transition time vs. load capacitance.

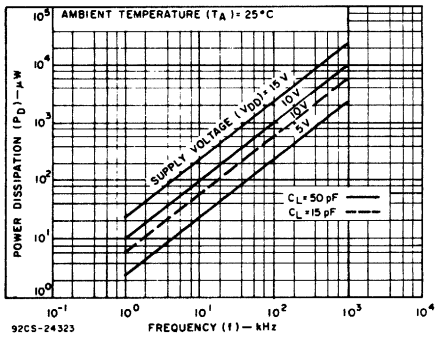


Fig. 13 – Typical dynamic power dissipation vs. frequency.

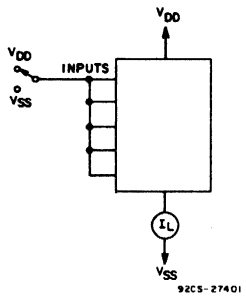


Fig. 14 – Quiescent device current test circuit.

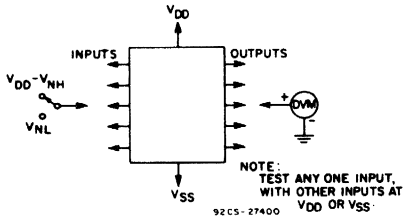


Fig. 15 – Noise immunity test circuit.

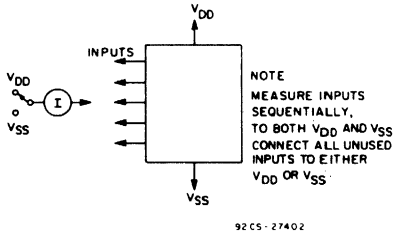


Fig. 16 – Input leakage current test circuit.

CD4073B, CD4081B, CD4082B Types
COS/MOS AND Gates

High-Voltage Types (3-to-20-Volt Rating)

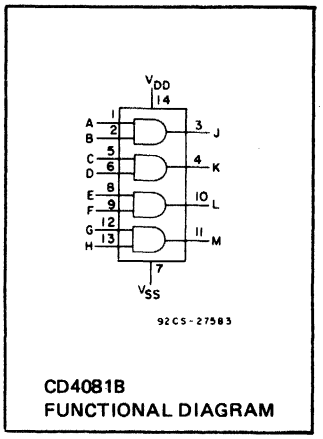
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate
CD4073B Triple 3-Input AND Gate

Features:

- **Medium-Speed Operation — t_{PLH} = 85 ns (typ.); t_{PHL} = 65 ns (typ.) at 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

The RCA-CD4081B, CD4082B, and CD4073B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

The CD4081B, CD4082B, and CD4073B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4081B
FUNCTIONAL DIAGRAM

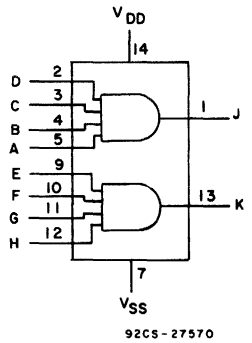


Fig. 1 — Functional diagram for CD4082B

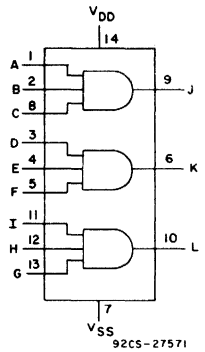


Fig. 2 — Functional diagram for CD4073B

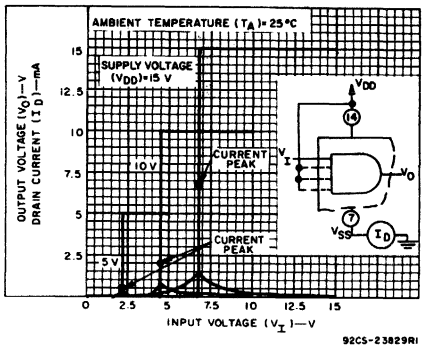


Fig. 3 — Typical voltage and current transfer characteristics.

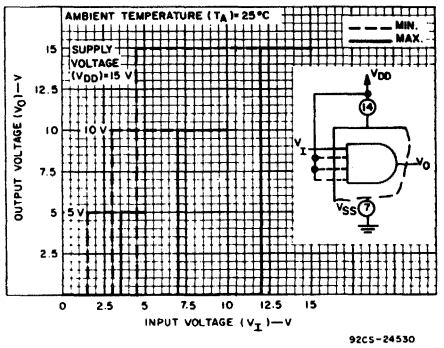


Fig. 4 — Minimum and maximum voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C,*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C
  PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°

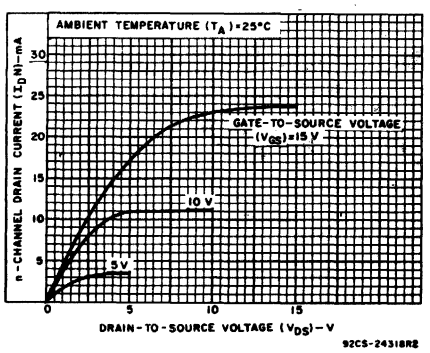


Fig. 5 — Typical output-N-channel drain characteristics.

CD4073B, CD4081B, CD4082B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55,+25,+125 Apply to D,K,F,H Packages* *Values at -40,+25,+85 Apply to E,Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	—	—	5	0.5	0.5	5	10	—	0.01	0.5	μA
	—	—	10	1	1	10	20	—	0.01	1	
	—	—	15	2	2	20	40	—	0.01	2	
	—	—	20	10	10	100	200	—	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	—	5	0.5	0.45	0.36	0.3	0.4	0.8	—	mA
	0.5	—	10	1.1	1	0.75	0.65	0.9	1.8	—	
	1.5	—	15	3.3	3.2	2.5	2.2	3	6	—	
P-Channel (Source), I_DP Min.	4.6	—	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	—	
	2.5	—	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	—	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	—	
	13.5	—	15	-3.3	-3.2	-2.5	-2.2	-3	-6	—	
Output Voltage: Low-level, V_{OL} Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
High Level, V_{OH} Min.	—	0, 5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	—	5	1.5				1.5	2.25	—	V
	9	—	10	3				3	4.5	—	
	13.5	—	15	4.5				4.5	6.75	—	
Inputs High, V_{NH} Min.	0.8	—	5	1.5				1.5	2.25	—	
	1	—	10	3				3	4.5	—	
	1.5	—	15	4.5				4.5	6.75	—	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	—	5	1				1	—	—	V
	9	—	10	1				1	—	—	
	13.5	—	15	1				1	—	—	
Inputs High, V_{NMH} Min.	0.5	—	5	1				1	—	—	
	1	—	10	1				1	—	—	
	1.5	—	15	1				1	—	—	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				—	$\pm 10^{-5}$	±1	μA

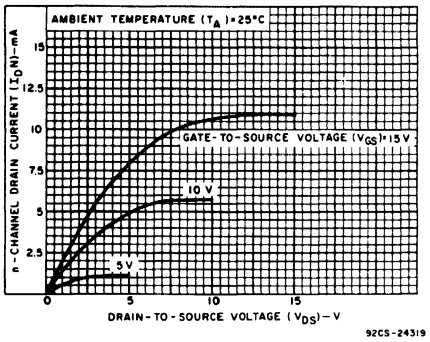


Fig. 6 — Minimum output-N-channel drain characteristics.

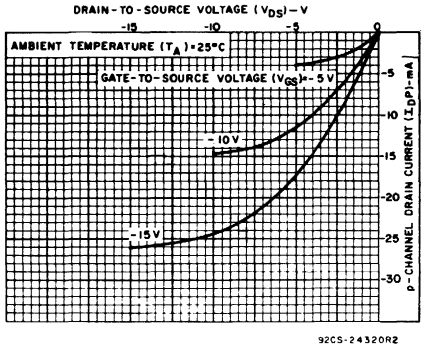


Fig. 7 — Typical output-P-channel drain characteristics.

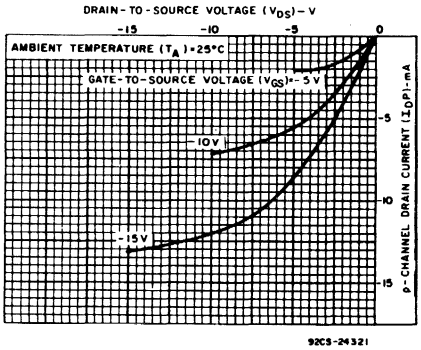


Fig. 8 — Minimum output-P-channel drain characteristics.

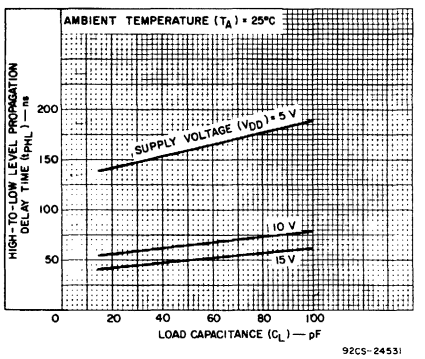


Fig. 9 — Typical high-to-low level propagation delay vs. load capacitance.

CD4073B, CD4081B, CD4082B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
			V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time: High-to-Low Level	t_{PHL}		5	160	320	ns
			10	65	130	
			15	50	100	
Low-to-High Level	t_{PLH}		5	210	420	ns
			10	85	170	
			15	65	130	
Transition Time	t_{THL} t_{TLH}		5	100	200	ns
			10	50	100	
			15	40	80	
Average Input Capacitance	C_I	Any Input		5	—	pF

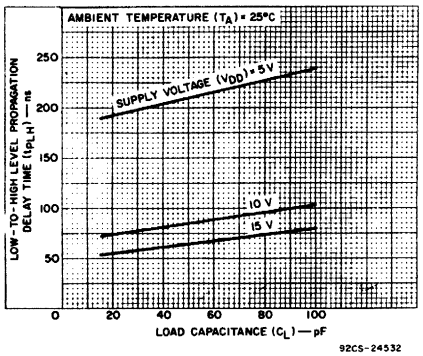


Fig. 10 – Typical low-to-high level propagation delay vs. load capacitance.

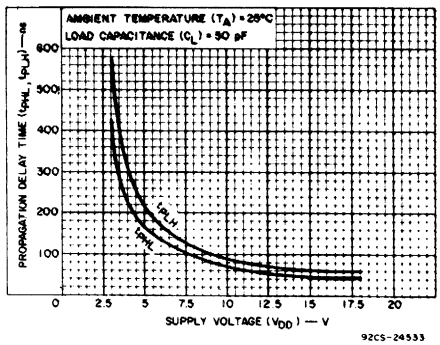


Fig. 11 – Typical propagation delay vs. supply voltage.

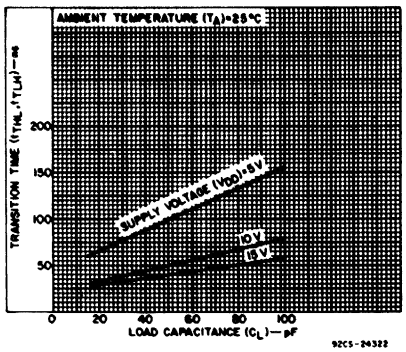


Fig. 12 – Typical transition time vs. load capacitance.

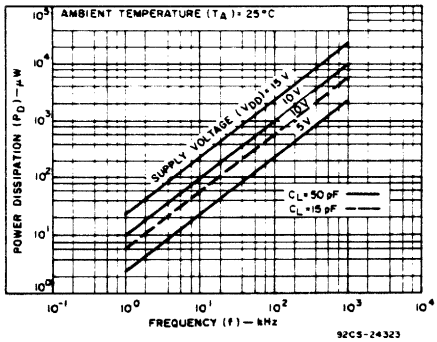


Fig. 13 – Typical dynamic power dissipation vs. frequency.

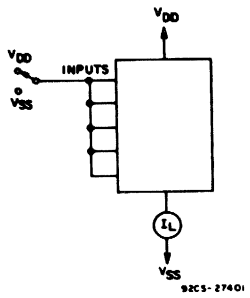


Fig. 14 – Quiescent device current test circuit.

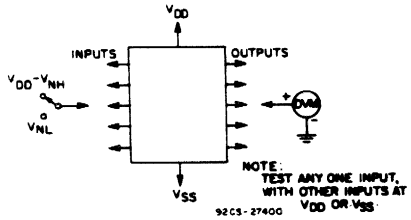


Fig. 15 – Noise immunity test circuit.

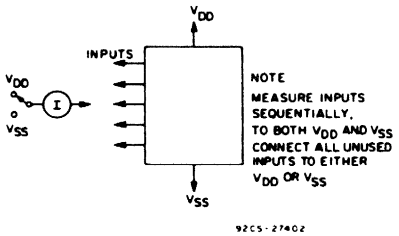


Fig. 16 – Input leakage current test circuit.

CD4076B Types

COS/MOS 4-Bit D-Type Registers

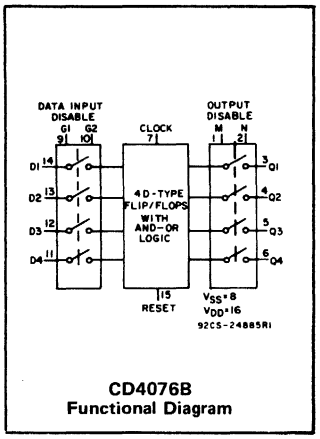
High-Voltage Types (3-to-20-Volt Rating)

The CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Three-state outputs**
- **Input disabled without gating the clock**
- **Gated output control lines for enabling or disabling the outputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**



CD4076B Functional Diagram

- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Truth Table

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⎍	1	X	X	Q	NC
0	⎍	X	1	X	Q	NC
0	⎍	0	0	1	1	
0	⎍	0	0	0	0	
0	1	X	X	X	Q	NC
0	⎎	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level
0 ≡ Low Level
X = Don't Care
NC = No Change

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	200	–	ns
	10	80	–	
	15	60	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	80	–	
Clock Input Frequency, f_{CL}	5	dc	3	MHz
	10		6	
	15		8	
Clock Rise or Fall Time, t_rCL, t_fCL:	3 - 20	–	15	μs
Reset Pulse Width, t_W	5	120	–	ns
	10	50	–	
	15	40	–	
Data Input Disable Setup Time, t_S	5	180	–	ns
	10	100	–	
	15	70	–	

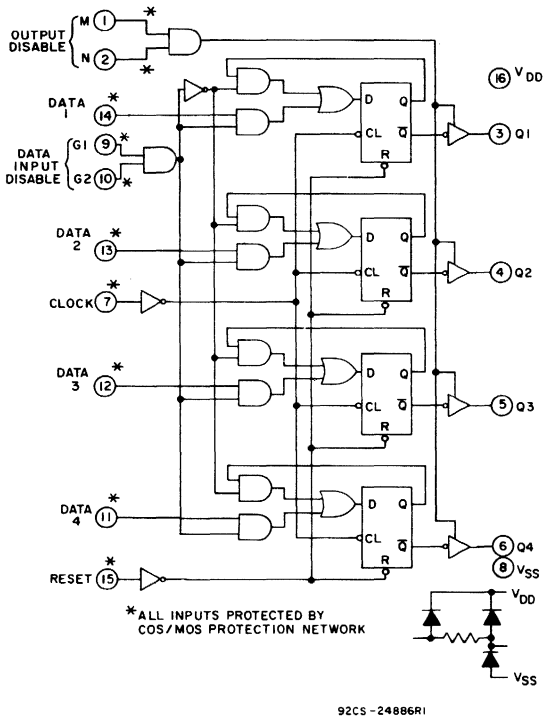


Fig. 1 – CD4076B logic diagram.

CD4076B Types

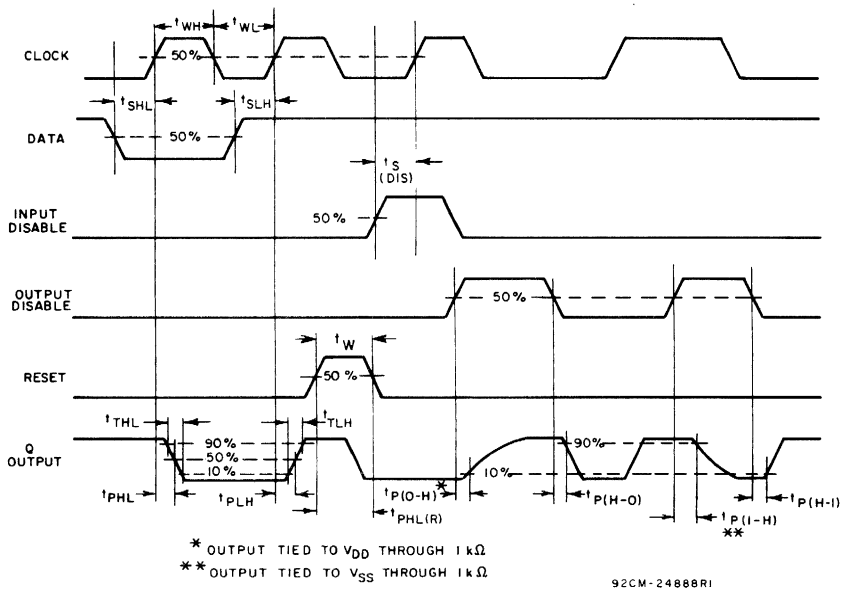


Fig. 2 – Functional waveforms for CD4076B.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF,R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q Output, t_{PHL}, t_{PLH}		5	–	300	600	ns
		10	–	125	250	
		15	–	90	180	
Reset, $t_{PHL}(R)$		5	–	230	460	
		10	–	100	200	
		15	–	75	150	
3-State Output 1 or 0 to High Impedance, $t_P(1\text{-}H)$, $t_P(0\text{-}H)$		5	–	150	300	
		10	–	75	150	
		15	–	60	120	
3-State High Impedance to 1 or 0 Output, $t_P(H\text{-}1)$, $t_P(H\text{-}0)$		5	–	150	300	
		10	–	75	150	
		15	–	60	120	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, (f_{CL})		5	3	6	–	MHz
		10	6	12	–	
		15	8	16	–	
Minimum Clock Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Reset Pulse With, t_W		5	–	60	120	ns
		10	–	25	50	
		15	–	20	40	
Minimum Data Setup Time, t_S		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Minimum Data Input Disable Setup Time, t_S		5	–	90	180	ns
		10	–	50	100	
		15	–	35	70	
Average Input Capacitance, C_I	Any Input	–	–	5	–	pF

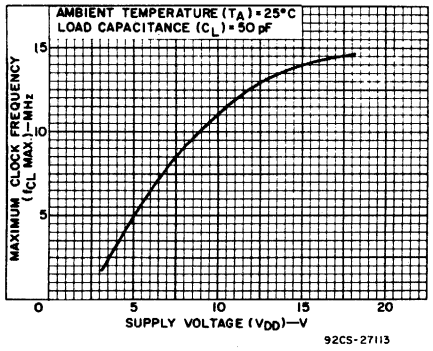


Fig. 3—Typical maximum clock input frequency vs. supply voltage.

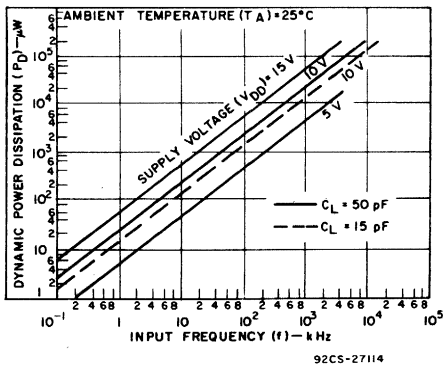


Fig. 4—Typical dynamic power dissipation vs. frequency.

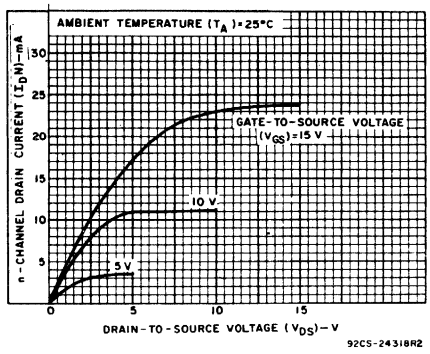


Fig. 5—Typical output-N-channel drain characteristics.

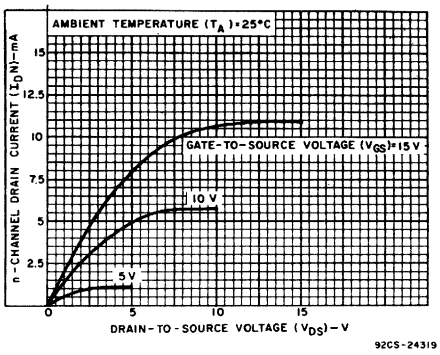


Fig. 6—Minimum output-N-channel drain characteristics.

CD4076B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA
3-State Output Leakage Current I_{OL}, I_{OH} Max.	Forced (Output Disabled) 0, 20	–	20	±2				–	$\pm 10^{-4}$	±2	μA

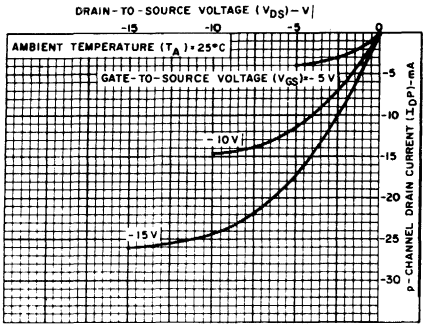


Fig. 7—Typical output-P-channel drain characteristics.

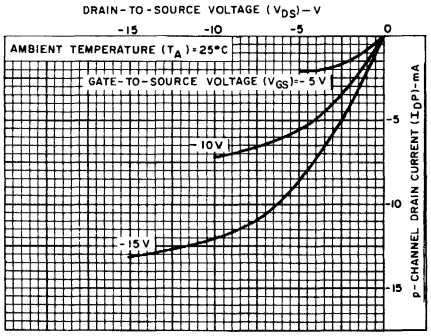


Fig. 8—Minimum output-P-channel drain characteristics.

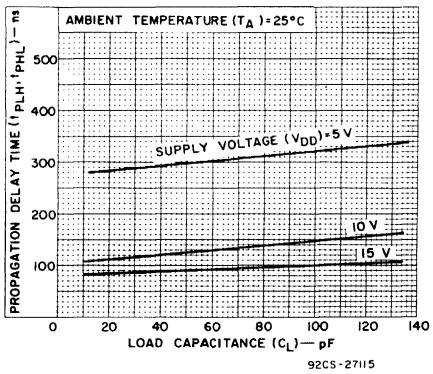


Fig. 9—Typical propagation delay time vs. load capacitance.

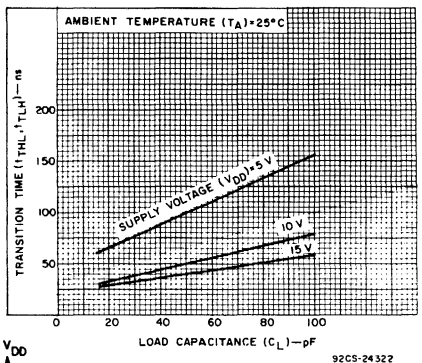


Fig. 10—Typical transition time vs. load capacitance.

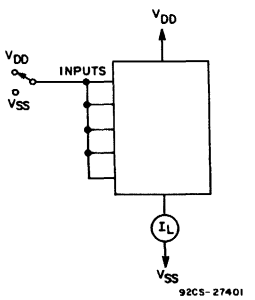


Fig. 11—Quiescent device current test circuit.

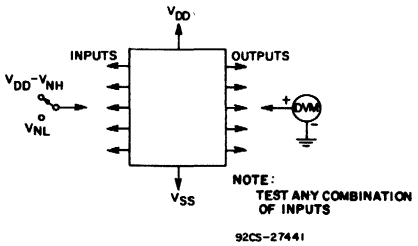


Fig. 12—Noise immunity test circuit.

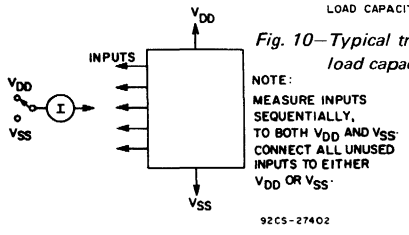


Fig. 13—Input leakage current test circuit.

CD4078B Types

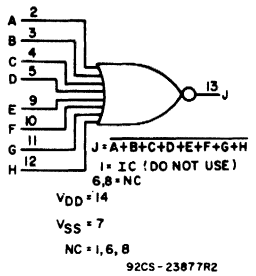
COS/MOS 8-Input NOR Gate

High-Voltage Types (3-to-20 Volt Rating)

The RCA-CD4078B NOR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR function and supplements the existing family of COS/MOS gates.

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.



CD4078
FUNCTIONAL DIAGRAM

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200kΩ

CHARACTERISTIC	TEST CONDITIONS		ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time: High-to-Low Level, t_{PHL}		5	200	400	ns
		10	80	160	
		15	60	120	
Low-to-High Level, t_{PLH}		5	425	850	ns
		10	170	340	
		15	120	240	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance, C_I	Any Input		5	–	pF

Features:

- **Medium-speed operation – t_{PHL} = 80 ns, t_{PLH} = 170 ns (typ.) at 10 V**
- **Buffered Output**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1μA at 20 V (full-package-temperature range)**

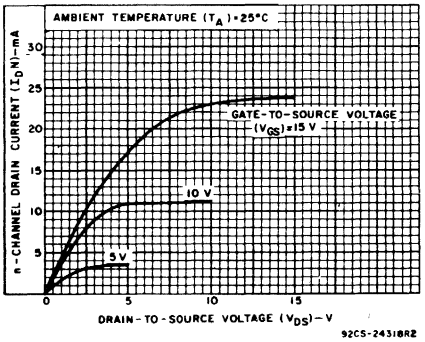


Fig. 1 – Typical output-N-channel drain characteristics.

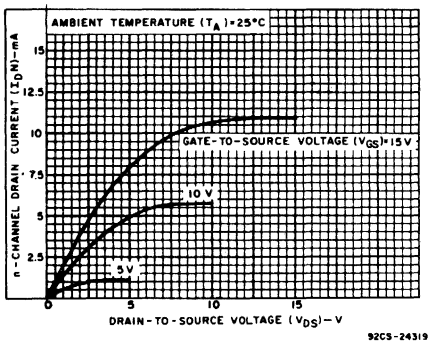


Fig. 2 – Minimum output-N-channel drain characteristics.

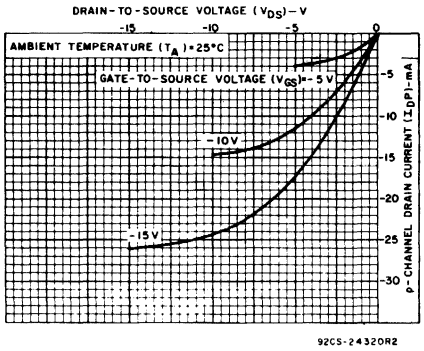


Fig. 3 – Typical output-P-channel drain characteristics.

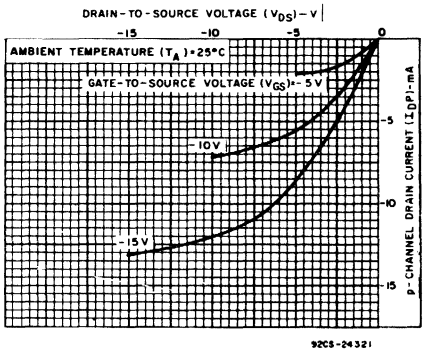


Fig. 4 – Minimum output-P-channel drain characteristics.

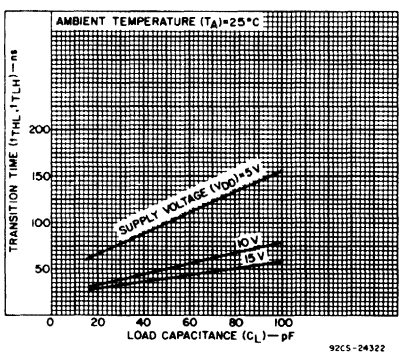


Fig. 5 – Typical transition time vs. load capacitance.

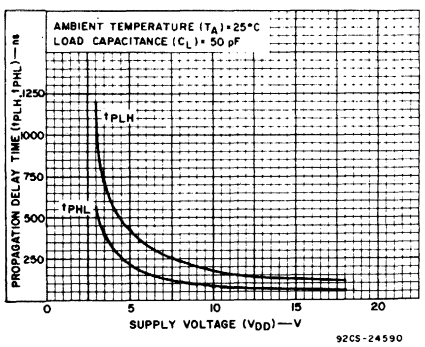


Fig. 6 – Typical propagation delay time vs. supply voltage.

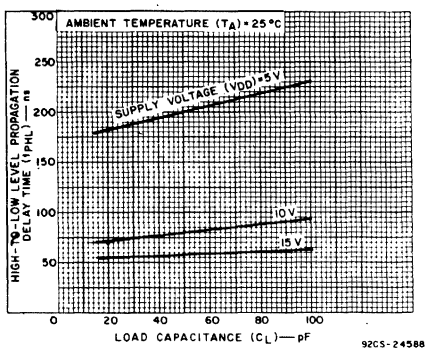


Fig. 7 – Typical high-to-low level propagation delay time vs. load capacitance.

CD4078B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55,+25,+125 Apply to D,K,F,H Packages* *Values at -40,+25,+85 Apply to E,Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	3.75				3.75	5.6	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	3.75				3.75	5.6	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input			±1				–	$\pm 10^{-5}$	±1	μA

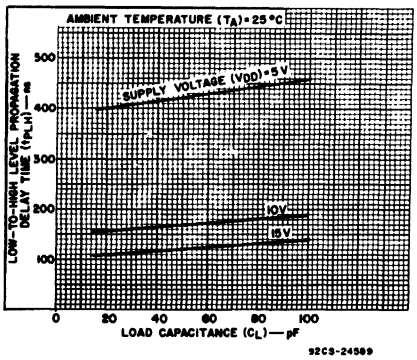


Fig. 8 – Typical low-to-high level propagation delay time vs. load capacitance.

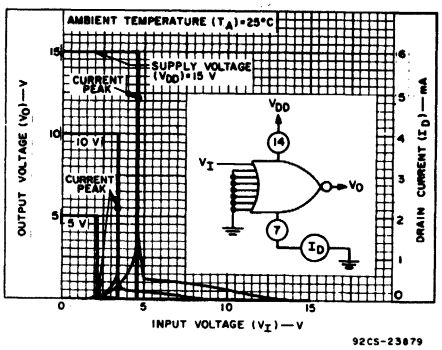


Fig. 9 – Typical voltage and current transfer characteristics.

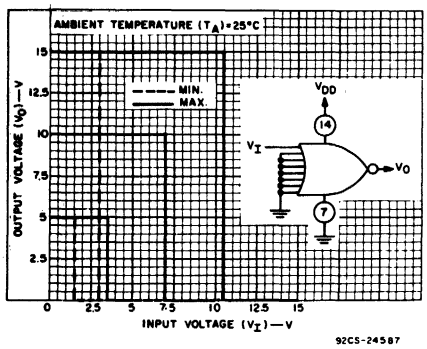


Fig. 10 – Minimum and maximum voltage transfer characteristics.

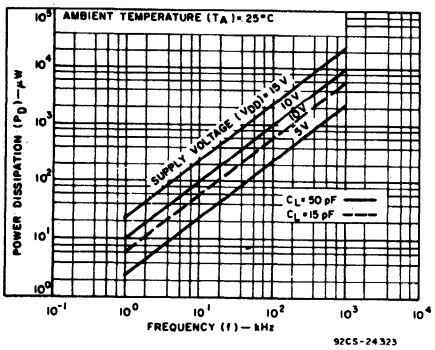


Fig. 11 – Typical power dissipation vs. frequency.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

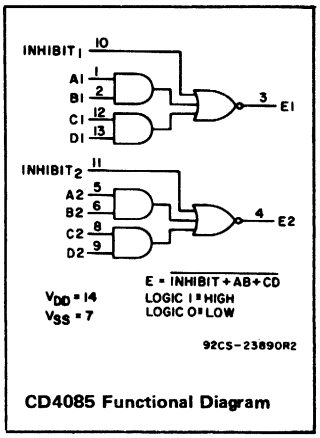
CD4085B Types

COS/MOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input OR gate followed by an inverter. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead dual-in-line ceramic packages (D, F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (K suffix), and in chip form (H suffix).



CD4085 Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time (Data): High-to-Low Level,	t_{PHL}	5	225	450	ns
		10	90	180	
		15	65	130	
Low-to-High Level,	t_{PLH}	5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level,	$t_{PHL(INH)}$	5	150	300	ns
		10	60	120	
		15	40	80	
Low-to-High Level,	$t_{PLH(INH)}$	5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time,	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance,	C_I	Any Input	5	–	pF

Features.

- Medium-speed operation – t_{PHL} = 90 ns; t_{PLH} = 125 ns (typ.) at 10 V
- Individual inhibit controls
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

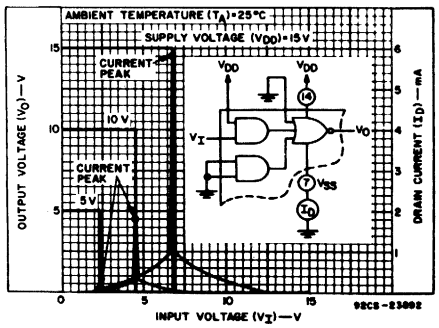


Fig. 1 - Typical voltage and current transfer characteristics.

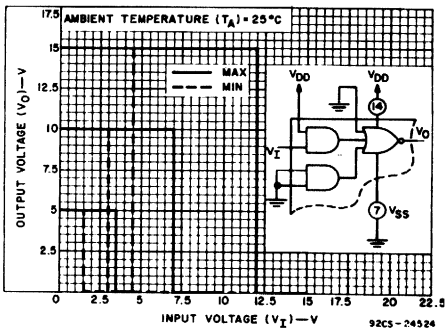


Fig. 2 - Min. and max. voltage transfer characteristics.

CD4085B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

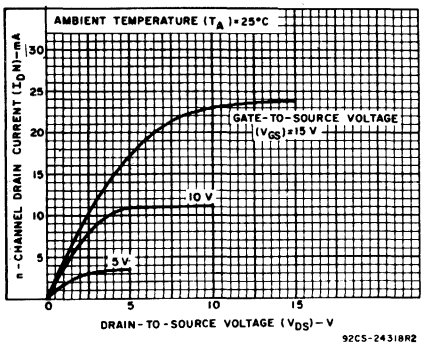


Fig.3 – Typical output n-channel drain characteristics.

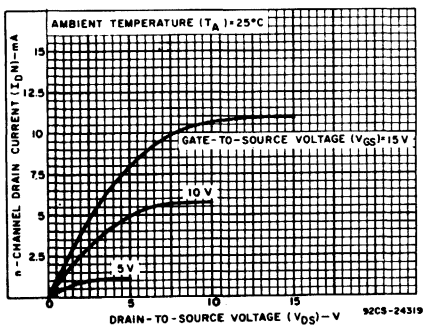


Fig.4 – Minimum output n-channel drain characteristics.

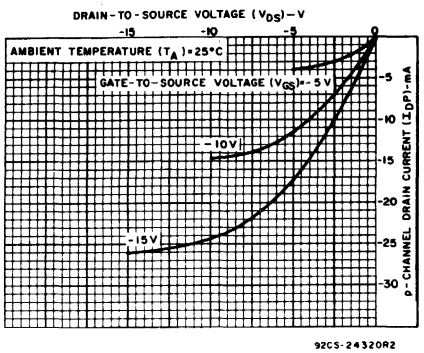


Fig.5 – Typical output p-channel drain characteristics.

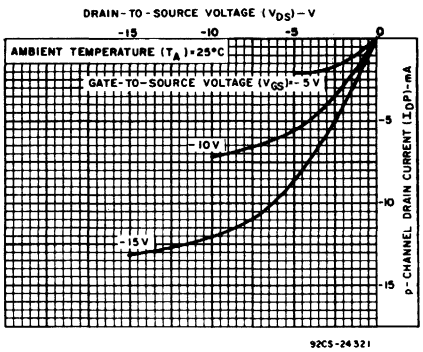


Fig.6 – Minimum output p-channel drain characteristics.

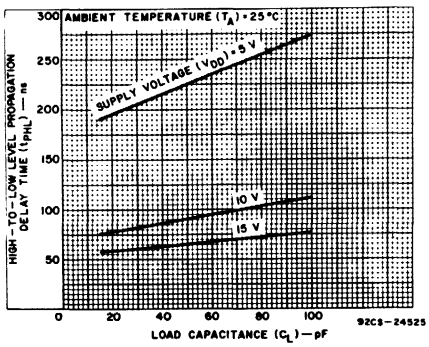


Fig.7 – Typical data high-to-low level propagation delay time vs. load capacitance.

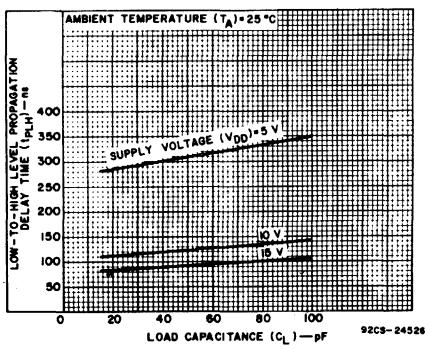


Fig.8 – Typical data low-to-high level propagation delay time vs. load capacitance.

CD4085B Types

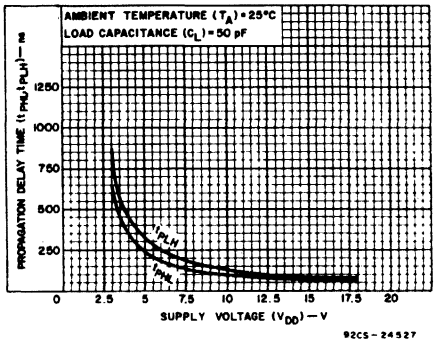


Fig.9 – Typical data propagation delay time vs. supply voltage.

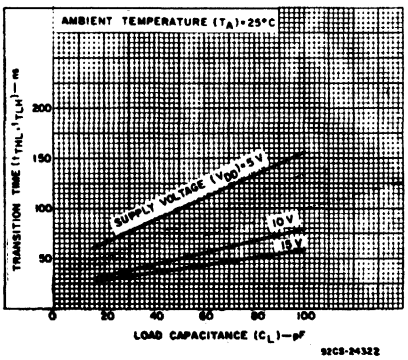


Fig.10 – Typical transition time vs. load capacitance.

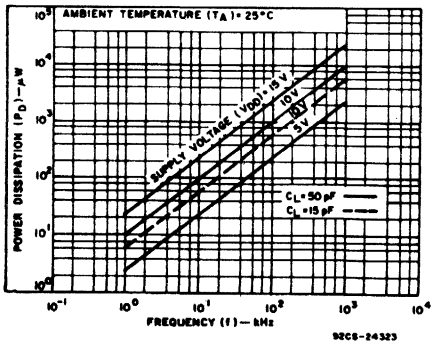


Fig.11 · Typical power dissipation vs. frequency.

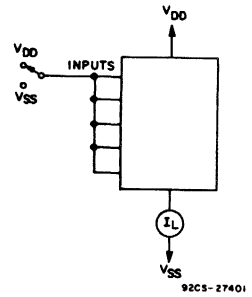


Fig.12 – Quiescent device current test circuit.

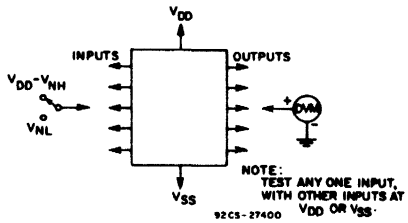


Fig.13 - Noise immunity test circuit.

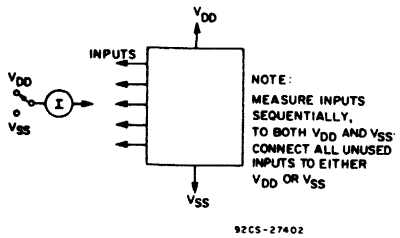


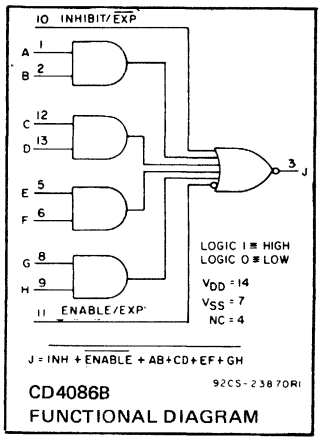
Fig.14 – Input leakage current test circuit.

CD4086B Types
COS/MOS Expandable 4-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4086B contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}. See Fig. 2 and its associated explanation for applications where a capability greater than 4-wide is required.

The CD4086B is supplied in 14-lead dual-in-line ceramic packages (D, F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packs (K suffix), and in chip form (H suffix).



CD4086B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y). . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Features:

- **Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 140 ns (typ.) at 10 V**
- **INHIBIT and ENABLE inputs**
- **Buffered outputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	TYP.	MAX.	
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}	5	225	450	ns
	10	90	180	
	15	60	120	
Low-to-High Level, t_{PLH}	5	350	700	ns
	10	140	280	
	15	100	200	
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{PHL(INH)}$	5	150	300	ns
	10	60	120	
	15	40	80	
Low-to-High Level, $t_{PLH(INH)}$	5	250	500	ns
	10	100	200	
	15	70	140	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Average Input Capacitance; C_I	Any Input	5	–	pF

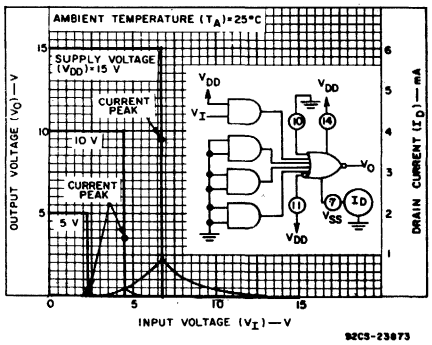


Fig. 1 — Typical voltage and current transfer characteristics.

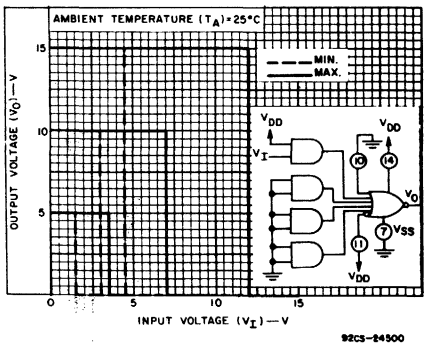


Fig. 2 — Minimum and maximum voltage transfer characteristics.

CD4086B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55,+25,+125 Apply to D,K,F,H Packages* *Values at -40,+25,+85 Apply to E,Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	0.5	0.5	5	10	–	0.01	0.5	μA
	–	–	10	1	1	10	20	–	0.01	1	
	–	–	15	2	2	20	40	–	0.01	2	
	–	–	20	10	10	100	200	–	0.02	10	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

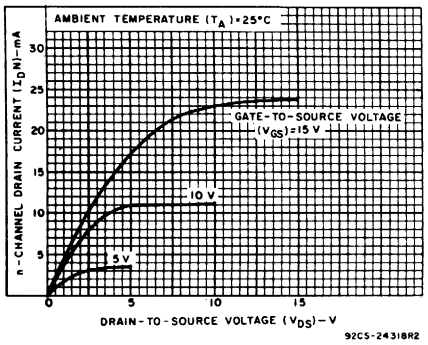


Fig. 3 – Typical output n-channel drain characteristics.

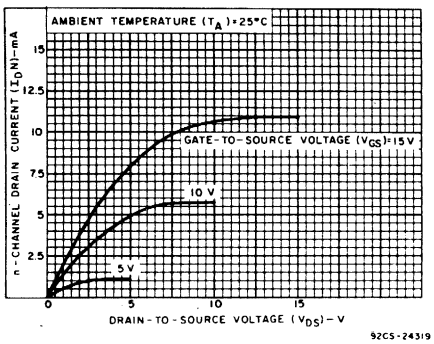


Fig. 4 – Minimum output n-channel drain characteristics.

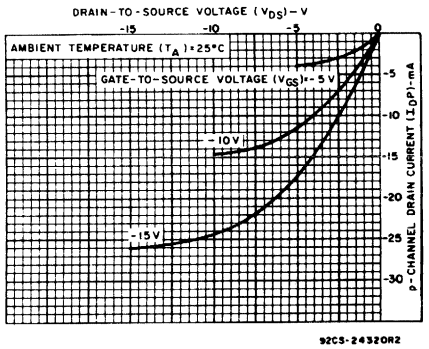


Fig. 5 – Typical output p-channel drain characteristics.

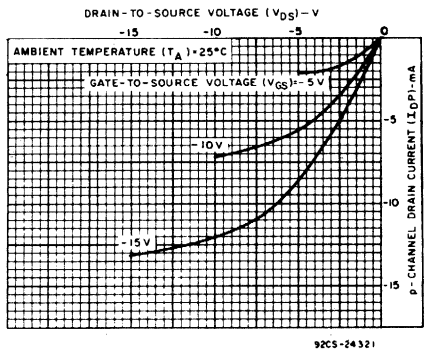


Fig. 6 – Minimum output p-channel drain characteristics.

CD4086B Types

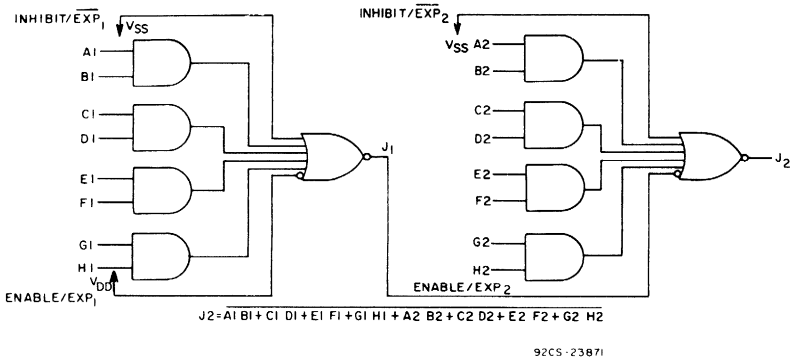


Fig. 7 – Two CD4086B's connected as an 8-wide 2-input A-O-I gate.

Fig. 7 above shows two CD4086's utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one CD4086 is fed directly to the ENABLE/EXP2 line of the second CD4086. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{\text{EXP}}$ input with the same result.

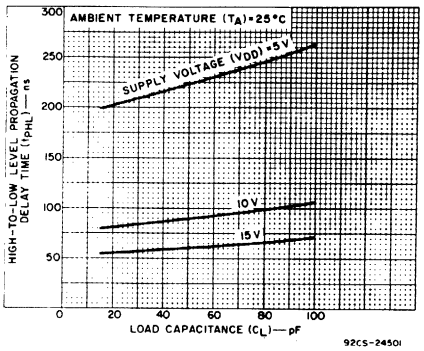


Fig. 8 – Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance.

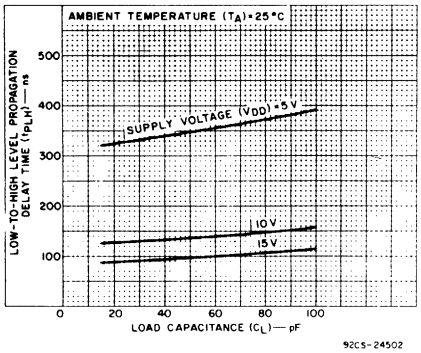


Fig. 9 – Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance.

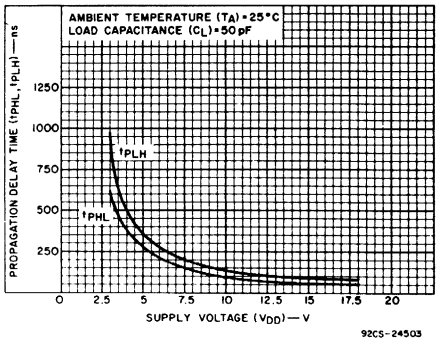


Fig. 10 – Typical DATA or ENABLE propagation delay time vs. supply voltage.

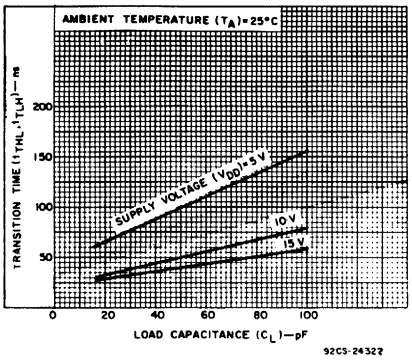


Fig. 11 – Typical transition time vs. load capacitance.

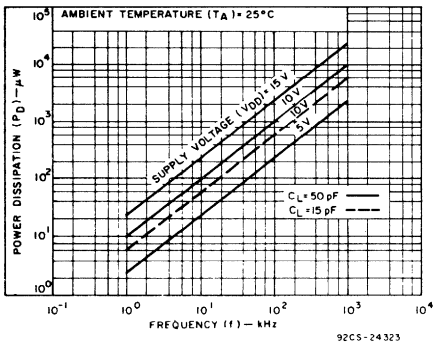


Fig. 12 – Typical power dissipation vs. frequency.

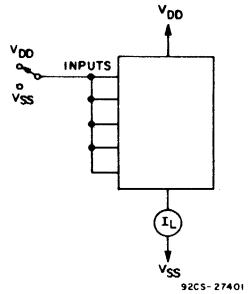


Fig. 13 – Quiescent-device-current test circuit.

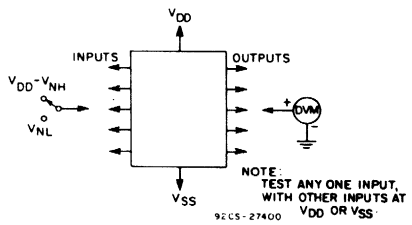


Fig. 14 – Noise-immunity test circuit.

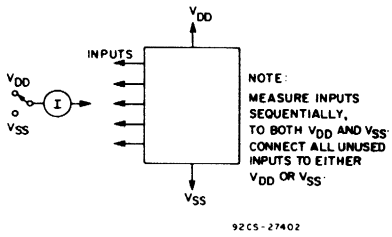


Fig. 15 – Input leakage-current test circuit.

Preliminary CD4089B Types
COS/MOS
Binary Rate Multiplier

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4089 is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089 devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs. 4 and 5). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16}+\frac{13}{256}=\frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16}\times\frac{13}{16}=\frac{143}{256}$$

The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 2.

If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains.

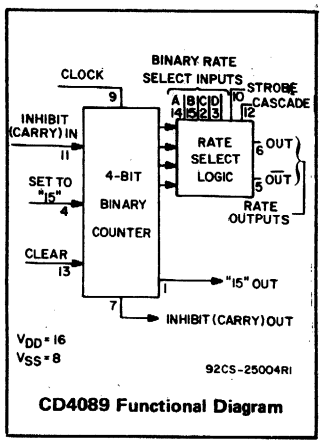
The CD4089B types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Cascadable in multiples of 4-bits
- Set to "15" input and "15" detect output
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis
- For further application information, see ICAN-6739 "COS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions".



CD4089 Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL-PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

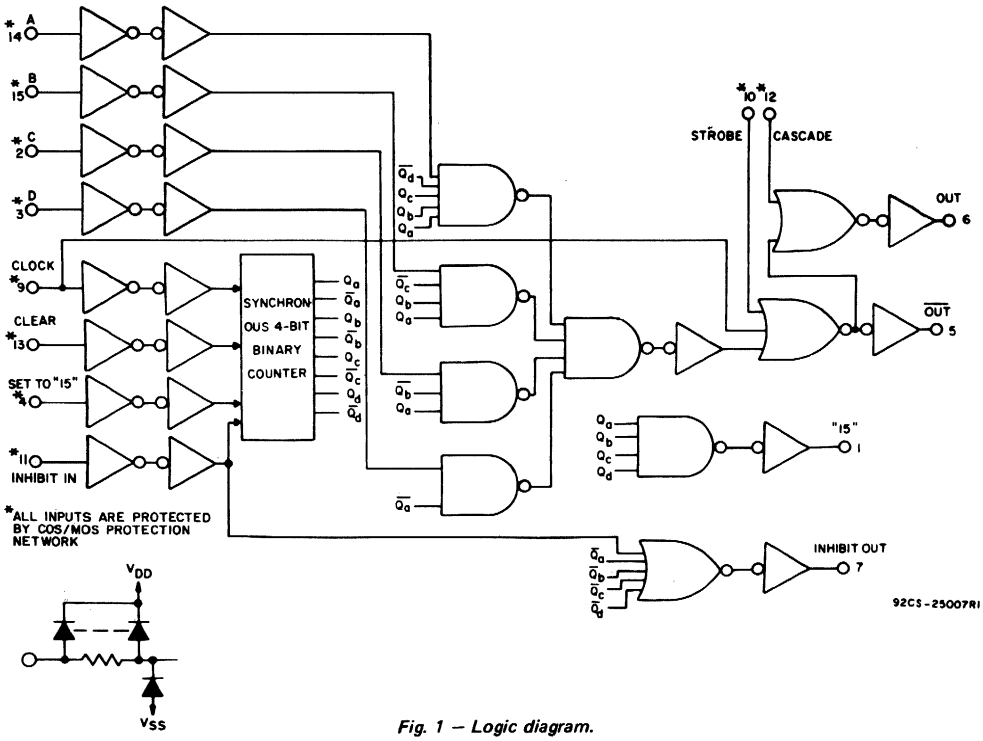
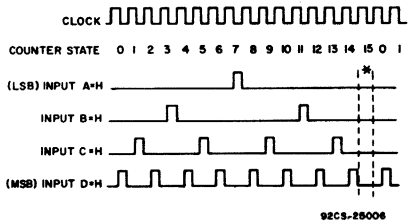


Fig. 1 — Logic diagram.

Preliminary CD4089B Types

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic		Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	TYP. VALUES	Units
Quiescent Device Current,	I_L	–	–	5	0.02	μA
		–	–	10	0.02	
		–	–	15	0.02	
		–	–	20	0.04	
Output Voltage: Low-Level,	V_{OL}	–	0,5	5	0	V
		–	0,10	10	0	
		–	0,15	15	0	
High-Level,	V_{OH}	–	0,5	5	5	
		–	0,10	10	10	
		–	0,15	15	15	
Noise Immunity: Inputs Low,	V_{NL}	4.2	–	5	2.25	V
		9	–	10	4.5	
		13.5	–	15	6.75	
Inputs High,	V_{NH}	0.8	–	5	2.25	
		1	–	10	4.5	
		1.5	–	15	6.75	
Noise Margin: Inputs Low,	V_{NML}	4.5	–	5	1 Min.	V
		9	–	10	1 Min.	
		13.5	–	15	1 Min.	
Inputs High,	V_{NMH}	0.5	–	5	1 Min.	
		1	–	10	1 Min.	
		1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink),	I_DN	0.4	–	5	0.8	mA
		0.5	–	10	1.8	
		1.5	–	15	6	
P-Channel (Source),	I_DP	4.6	–	5	–0.8	
		2.5	–	5	–3.2	
		9.5	–	10	–1.8	
		13.5	–	15	–6	
Input Leakage Current,	I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA



* An output bit may be filled in this counter state by a less significant CD4089 cascaded in the Add mode.

Fig. 2 – Timing diagram.

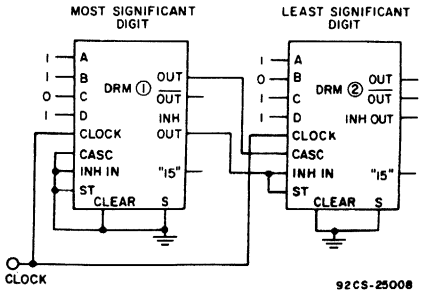


Fig. 3 – Two CD4089's cascaded in the "Add" mode with a preset number of 189.

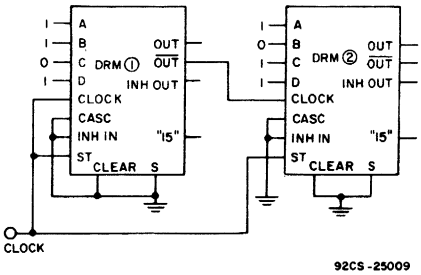


Fig. 4 – Two CD4089's cascaded in the "Multiply" mode with a preset number of 143.

RECOMMENDED OPERATING CONDITIONS AT $T_A = 25°C$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range)		3	18	V
Clock Rise or Fall Time, t_rC_L or t_fCL:	5,10,15	–	15	μs

Preliminary CD4089B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Clock to "Out", t_{PHL}, t_{PLH}	5	180	ns
	10	90	
	15	65	
Clock to "Inhibit Out" t_{PHL}, t_{PLH}	5	260	
	10	130	
	15	100	
Transition Time t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Maximum Clock Input Frequency, $f_{CL(Max.)}$	5	2	MHz
	10	4.5	
	15	5.5	

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

CD4093B Types

COS/MOS Quad 2-Input NAND Schmitt Triggers

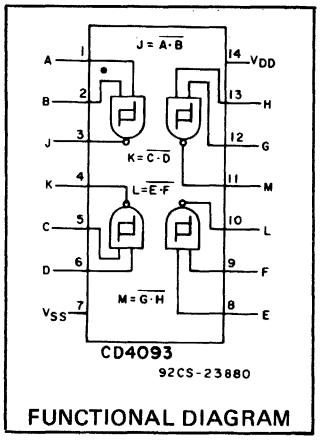
High-Voltage Types (3-to-20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 3).

The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.6 V at V_{DD} = 5 V and 2 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall times
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20V (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings



FUNCTIONAL DIAGRAM

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

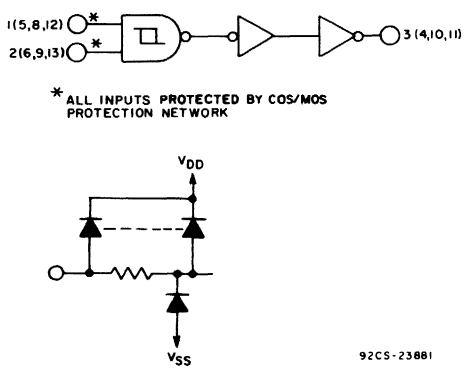


Fig. 1 – Functional diagram—1 of 4 Schmitt triggers.

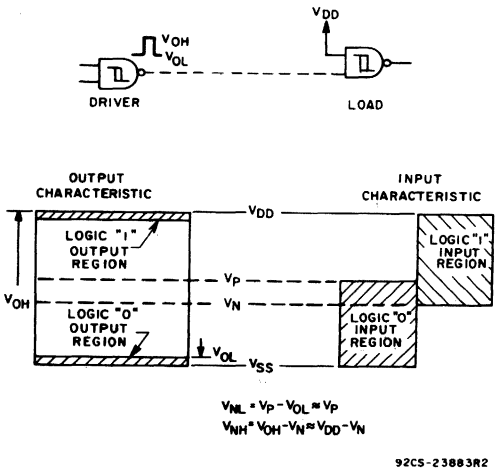


Fig. 2 – Input and output characteristics.

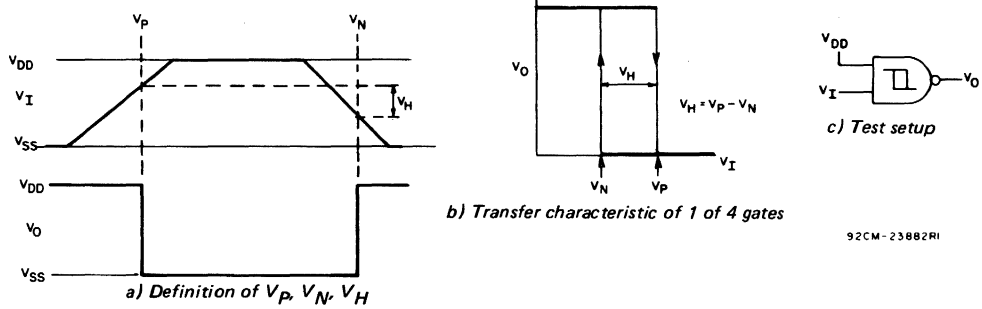


Fig. 3 – Hysteresis definition, characteristic, and test setup.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V

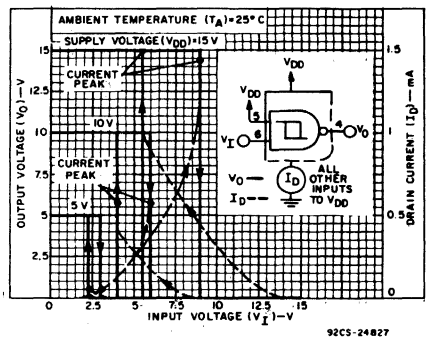


Fig. 4 – Typical current and voltage transfer characteristics.

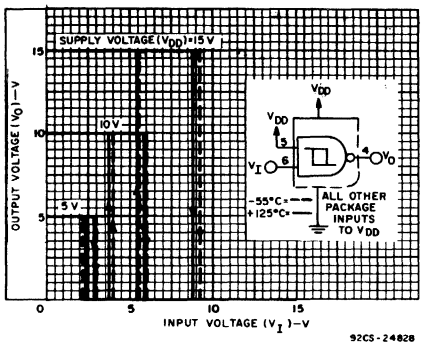


Fig. 5 – Typical voltage transfer characteristics as a function of temperature.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPES E, Y	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
Voltages referenced to V_{SS} Terminal):	-0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

CD4093B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, K, F, H Packages Values at -40, +25, +85 Apply to E, Y Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Positive Trigger Threshold Voltage V_P Typ.	–	–	5	3	3	2.85	2.8	2	2.9	–	V
	–	–	10	6.1	6.05	5.8	5.7	4.5	5.9	–	
	–	–	15	9.4	9.3	8.6	8.5	6.7	8.9	–	
Negative Trigger Threshold Voltage V_N Typ.	–	–	5	2.1	2.1	1.95	1.9	–	2	2.7	
	–	–	10	4.1	4.05	3.8	3.7	–	3.9	5.5	
	–	–	15	5.9	5.8	5.1	4.9	–	5.4	7.5	
Hysteresis Voltage V_H	–	–	5	–	–	–	–	–	0.9	–	V
	–	–	10	–	–	–	–	–	2	–	
	–	–	15	–	–	–	–	–	3.5	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8		
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6		
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High-Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

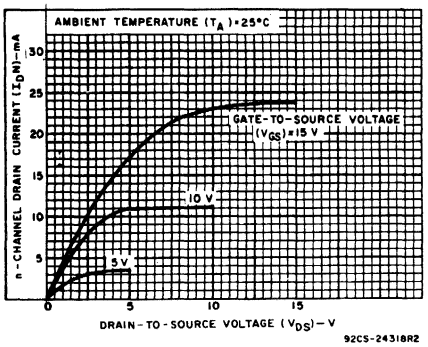


Fig. 6 – Typical output-N-channel drain characteristics.

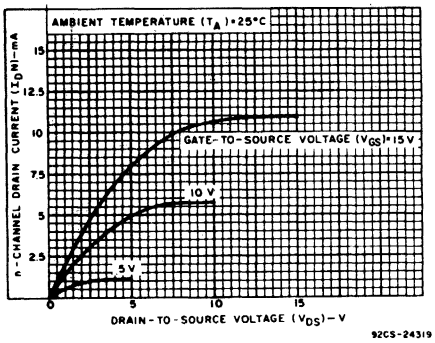


Fig. 7 – Minimum output-N-channel drain characteristics.

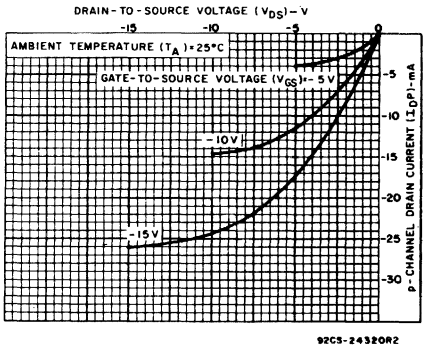


Fig. 8 – Typical output-P-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time t_{PHL}, t_{PLH}	5	300	600	ns
	10	150	300	
	15	120	240	
Transition Time t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Average Input Capacitance, C_I	Any Input	5	–	pF

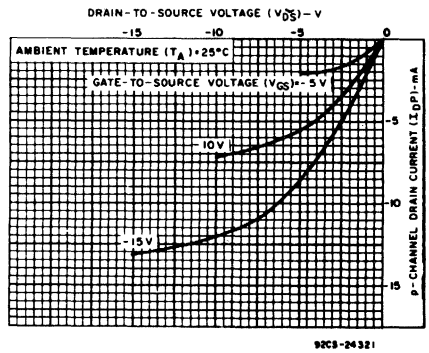


Fig. 9 – Minimum output-P-channel drain characteristics.

CD4093B Types

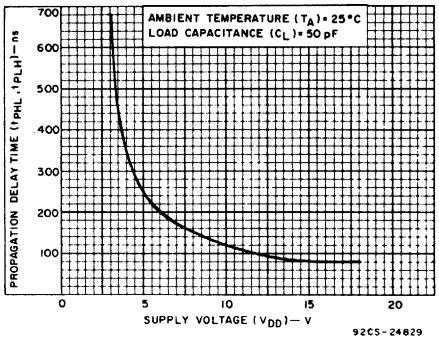


Fig. 10 — Typical propagation delay time vs. supply voltage.

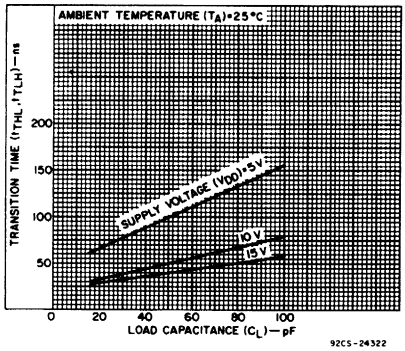


Fig. 11 — Typical transition time vs. load capacitance.

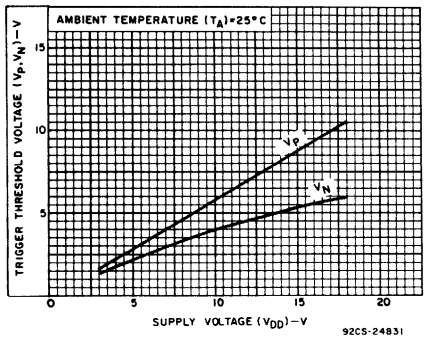


Fig. 12 — Typical trigger threshold voltage vs. V_{DD}.

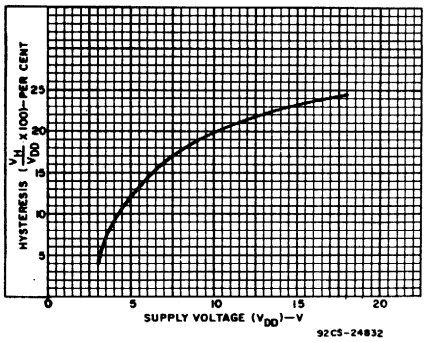


Fig. 13 — Typical per cent hysteresis vs. supply voltage.

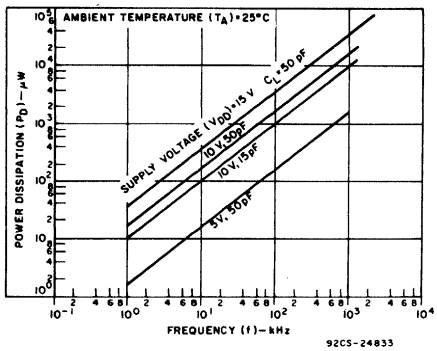


Fig. 14 — Typical dissipation characteristics.

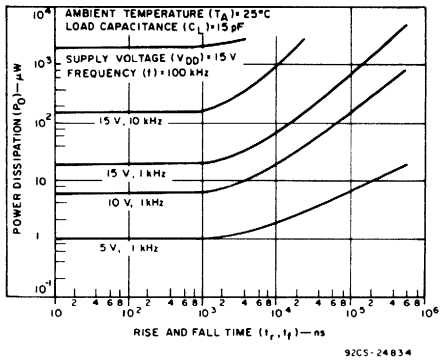


Fig. 15 — Power dissipation vs. rise and fall times.

APPLICATIONS

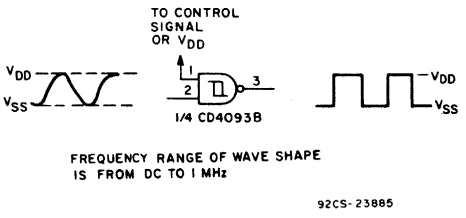


Fig. 16 — Wave shaper.

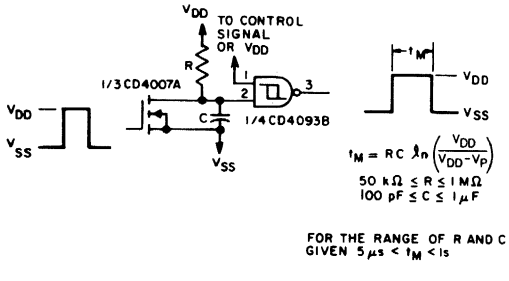


Fig. 17 — Monostable multivibrator

TEST CIRCUITS

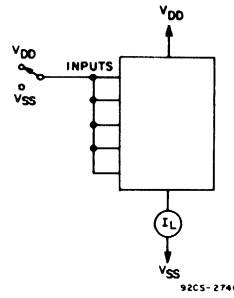


Fig. 18 — Quiescent device current test circuit.

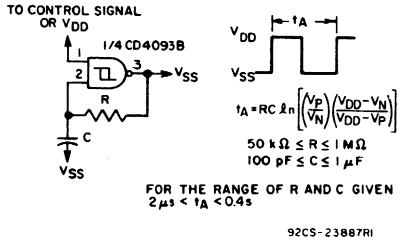


Fig. 19 — Astable multivibrator.

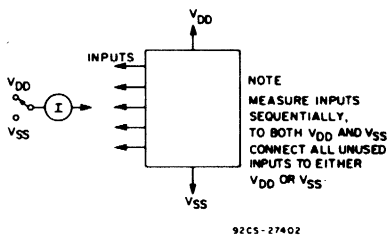


Fig. 20 — Input leakage current test circuit.

CD4094B Types
COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **3-state parallel outputs for connection to common bus**
- **Separate serial outputs synchronous to both positive and negative clock edges for cascading**
- **Medium speed operation – 5 MHz at 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

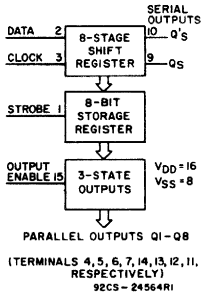
Applications:

- **Serial-to-parallel data conversion**
- **Remote control holding register**
- **Dual-rank shift, hold, and bus applications**

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	125 55 35	– – –	ns
Clock Pulse Width, t_W	5 10 15	200 100 83	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MHz
Clock Rise & Fall Time, t_rCL, t_fCL:*	5, 10, 15	–	15	μs
Strobe Pulse Width, t_W	5 10 15	200 80 70	– – –	ns

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.



CD4094B Functional Diagram

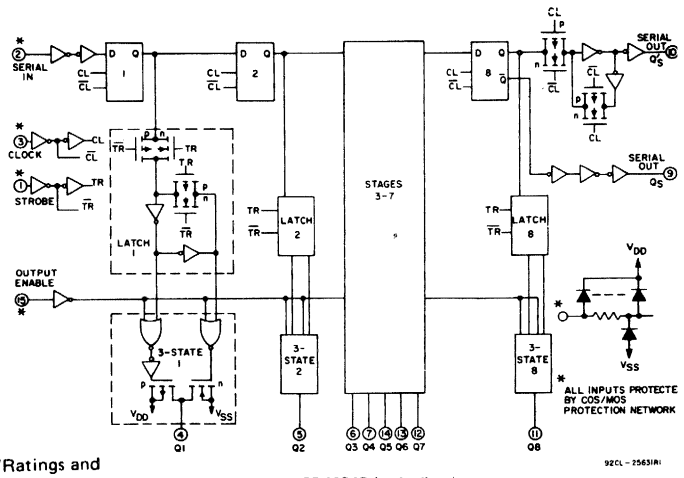


Fig. 2 – CD4094B Logic diagram.

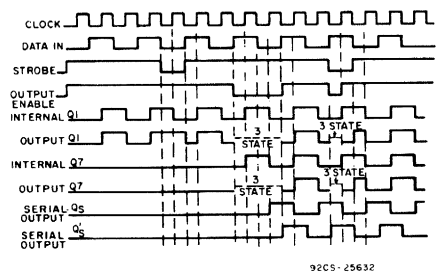


Fig. 1 – Timing diagram.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌙	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌙	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

CD4094B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A=25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL PACKAGES MIN.	TYP.	MAX.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} Clock to Serial Output (Q's)	5	–	300	600	ns
	10	–	125	250	
	15	–	95	190	
Clock to Serial Output (Q's)	5	–	230	460	ns
	10	–	110	220	
	15	–	75	150	
Clock to Parallel Output	5	–	420	840	ns
	10	–	195	390	
	15	–	135	270	
Strobe to Parallel Output	5	–	290	580	ns
	10	–	145	290	
	15	–	100	200	
Output Enable to Parallel Output; t_{PHL}	5	–	140	280	ns
	10	–	75	150	
	15	–	55	110	
t_{PLH}	5	–	225	450	ns
	10	–	95	190	
	15	–	70	140	
Minimum Strobe Pulse Width, t_W	5	–	100	200	ns
	10	–	40	80	
	15	–	35	70	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	50	100	
	15	–	40	83	
Minimum Data Setup Time, t_S	5	–	60	125	ns
	10	–	30	55	
	15	–	20	35	
Transition Time; t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Clock Rise and Fall Time; t_r, t_f	5,10,15	–	–	15	μs
Max. Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	
	15	3	6	–	
Average Input Capacitance, C_I (Any Input)	–	–	5	–	pF

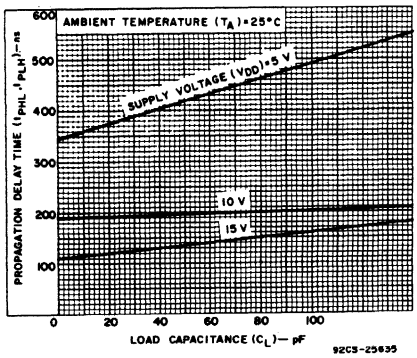


Fig. 3 — Clock-to-parallel output propagation delay vs C_L.

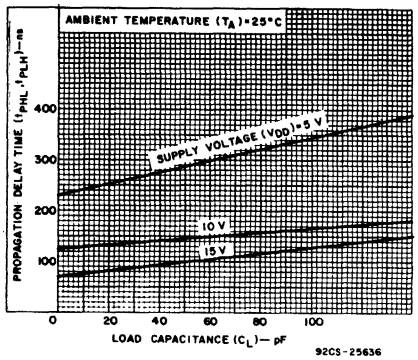


Fig. 4 — Strobe-to-parallel output propagation delay vs C_L.

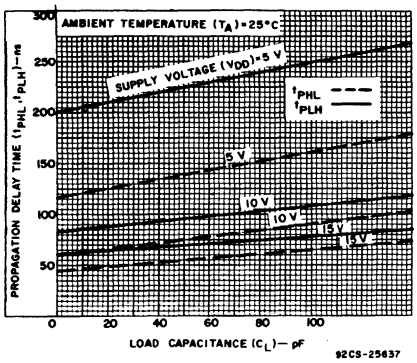


Fig. 5 — Output enable-to-parallel output propagation delay vs C_L.

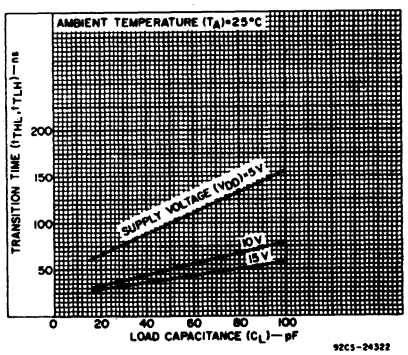


Fig. 6 — Typical transition time vs. load capacitance.

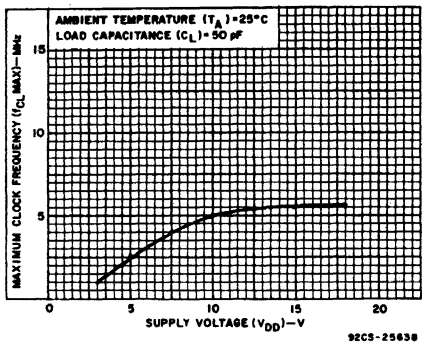


Fig. 7 — Typical maximum-clock-frequency vs. supply voltage.

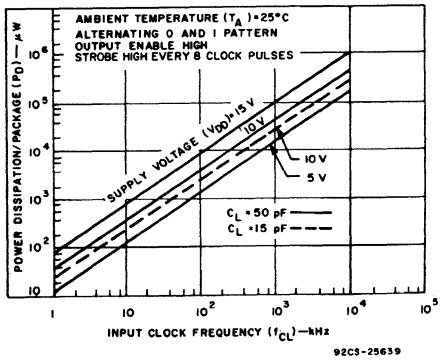


Fig. 8 — Dynamic power dissipation vs. capacitance.

CD4094B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) VALUES AT −55,+25,+125 APPLY TO D,K,F,H PACKAGES VALUES AT −40,+25,+85 APPLY TO E,Y PACKAGES							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_{DP} Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Output Voltage: Low-Level V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA
3-State Output Leakage Current I_{OL}, I_{OH} Max.	Forced (Output Disabled)										
	0, 20	–	20	±2				–	$±10^{-4}$	±2	μA

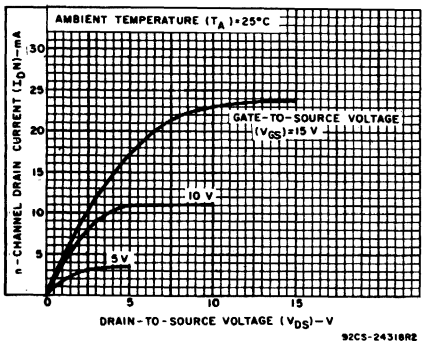


Fig. 9 — Typical output-N-channel drain characteristics.

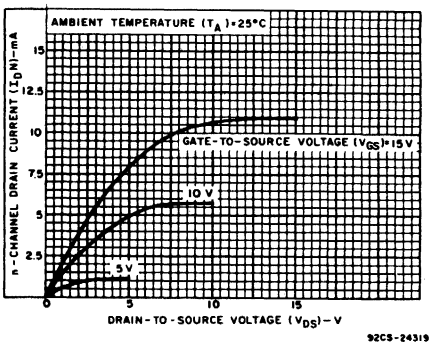


Fig. 10 — Minimum output-N-channel drain characteristics.

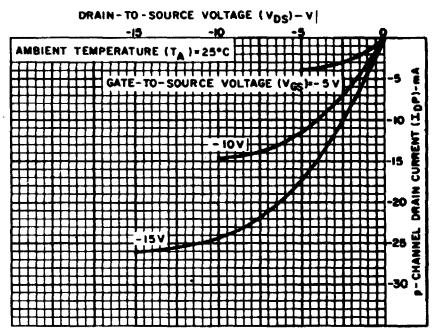


Fig. 11 — Typical output-P-channel drain characteristics.

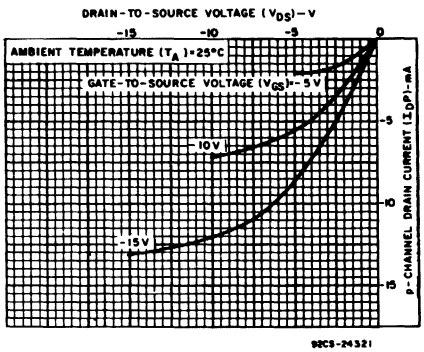


Fig. 12 — Minimum output-P-channel drain characteristics.

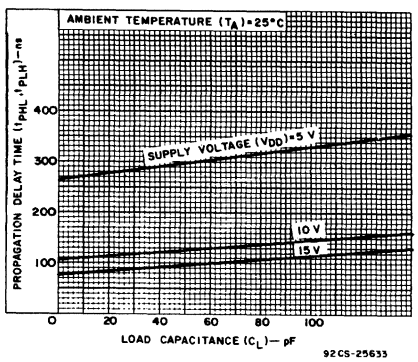


Fig. 13 — Clock-to-serial output Qs propagation delay vs C_L.

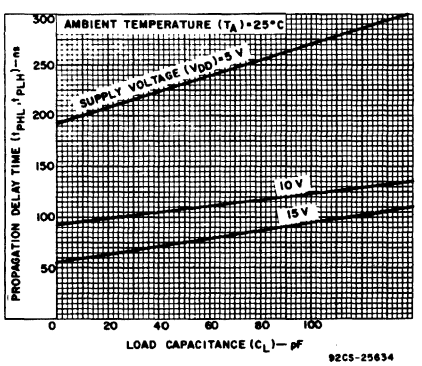


Fig. 14 — Clock-to-serial output Q's propagation delay vs C_L.

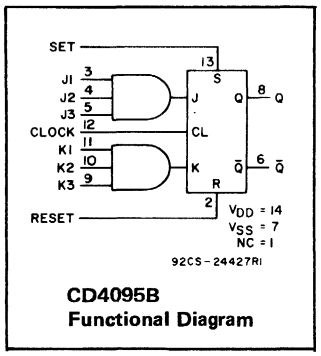
CD4095B, CD4096B Types

COS/MOS Gated J-K Master-Slave Flip-Flops

With Set-Reset Capability

High-Voltage Types (3-to-20-Volt Rating)

CD4095B Non-Inverting J and K Inputs
CD4096B Inverting and Non-Inverting J and K Inputs



CD4095B
Functional Diagram

The RCA-CD4095B and CD4096B are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

The CD4095B and CD4096B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Applications:

- **Registers**
- **Counters**
- **Control circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . -55 to +125° C

PACKAGE TYPES E, Y . . . . . -40 to +85° C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60° C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85° C (PACKAGE TYPES E, Y) . . Derate Linearly at 12 mW/° C to 200 mW

FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES D, F, K)Derate Linearly at 12 mW/° C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW

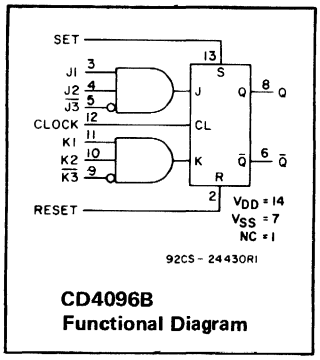
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265° C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	400	–	ns
	10	160	–	
	15	100	–	
Clock Pulse Width, t_W	5	140	–	ns
	10	60	–	
	15	40	–	
Clock Input Frequency, f_{CL}	5	dc	3.5	MHz
	10		8	
	15		12	
Clock Rise and Fall Time, t_rCL, t_fCL:	5, 10	–	15	μs
	15	–	5	
Set or Reset Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	50	–	



CD4096B
Functional Diagram

Features:

- **16 MHz toggle rate (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Gated inputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

TRUTH TABLES

SYNCHRONOUS OPERATION (S=0 R=0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J*	K*	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For CD4095B: J = J1 · J2 · J3; K = K1 · K2 · K3

For CD4096B: J = J1 · J2 · $\overline{J3}$; K = K1 · K2 · $\overline{K3}$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

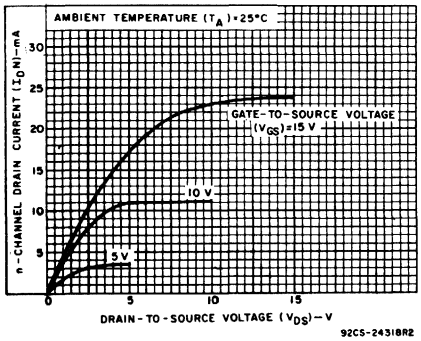


Fig. 1 — Typical output n-channel drain characteristics.

CD4095B, CD4096B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) *Values at -55,+25,+125 Apply to D,K,F,H Packages* *Values at -40,+25,+85 Apply to E,Y Packages*							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA

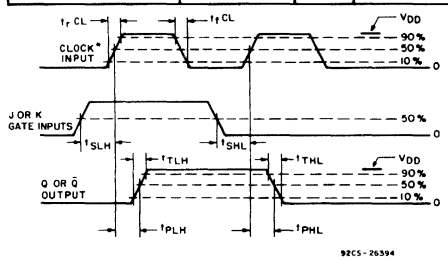


Fig. 5 – Propagation delay, transition, and setup-time waveforms.

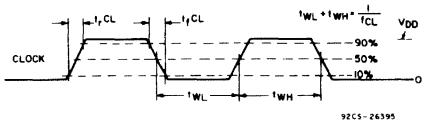


Fig.6 – Clock pulse rise and fall time waveforms.

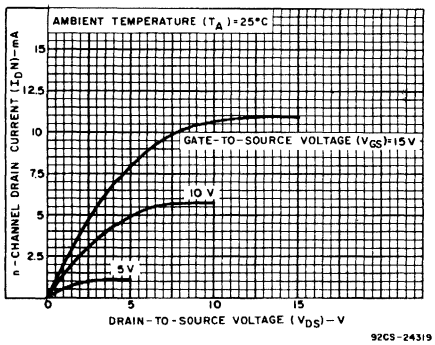


Fig.2 – Minimum output-N-channel drain characteristics.

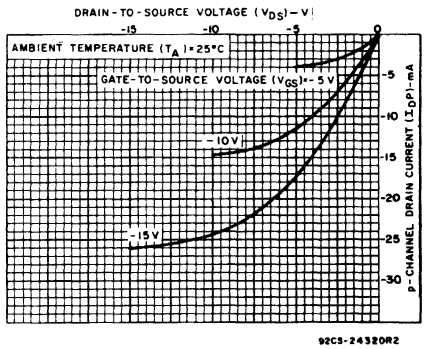


Fig. 3 – Typical output-P-channel drain characteristics.

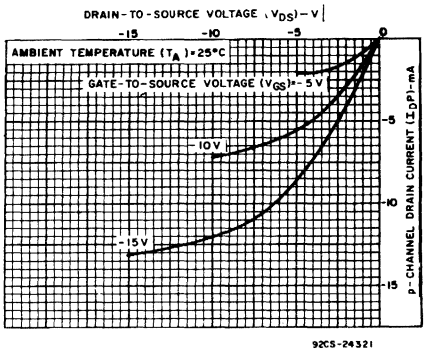


Fig. 4 – Minimum output-P-channel drain characteristics.

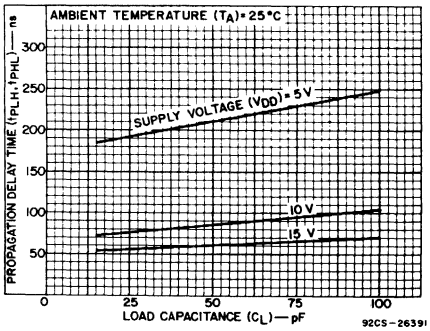


Fig.7 – Typical propagation delay time vs. load capacitance.

CD4095B, CD4096B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH}		5	–	250	500	ns
		10	–	100	200	
		15	–	75	150	
Set or Reset		5	–	150	300	
		10	–	75	150	
		15	–	50	100	
Clock Rise and Fall Time: t_r, t_f		5, 10	–	–	15	ns
		15	–	–	5	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, (f_{CL})		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Minimum Clock Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Minimum Set or Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	25	50	
Minimum Data Setup Time, t_S		5	–	200	400	ns
		10	–	80	160	
		15	–	50	100	
Average Input Capacitance, C_I	Any Input	–	–	5	–	pF

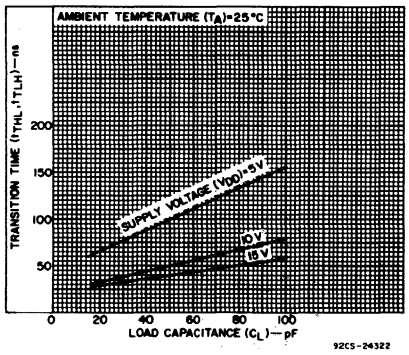


Fig.8 – Typical transition time vs. load capacitance.

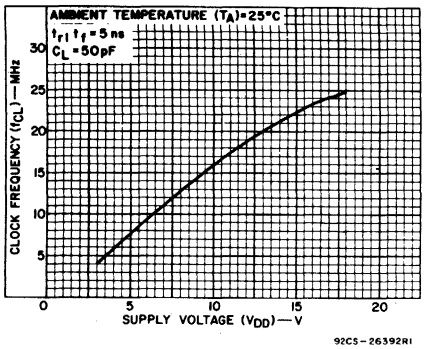


Fig. 9 – Typical clock frequency vs. supply voltage (toggle mode).

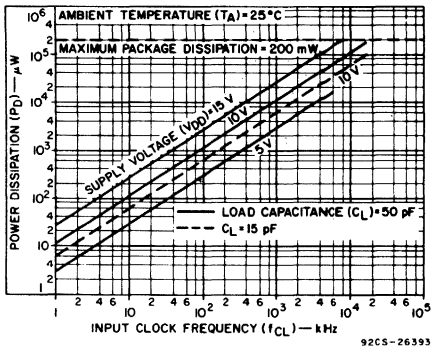


Fig. 10 – Typical input clock frequency vs. power dissipation.

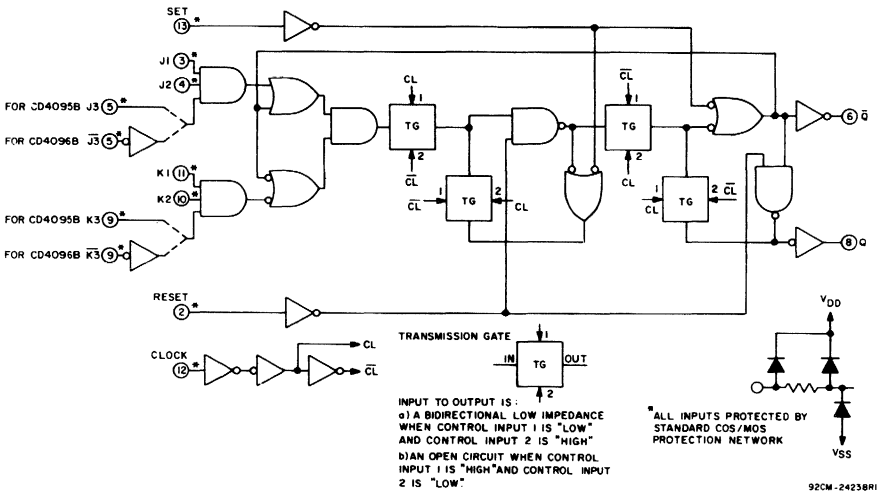


Fig. 11 – CD4095B and CD4096B logic diagram.

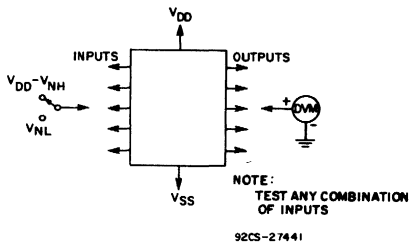


Fig. 12 – Noise immunity test circuit.

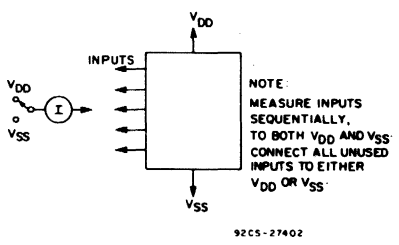


Fig. 13 – Input leakage current test circuit.

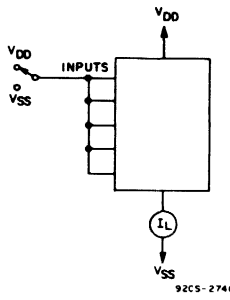


Fig. 14 – Quiescent device current test circuit.

Preliminary CD4098B Types
COS/MOS Dual Monostable Multivibrator

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

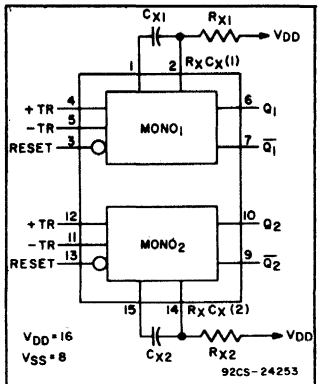
Leading-edge-triggering ($+T_R$) and trailing-edge-triggering ($-T_R$) inputs are provided for triggering from either edge of an input pulse. An unused $+T_R$ input should be tied to V_{SS}. An unused $-T_R$ input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098 is not used, its RESET should be tied to V_{SS}. See table I.

In normal operation, the circuit retriggers on the application of each new pulse. To prevent retriggering when leading-edge triggering is used, $\overline{Q}$ must be connected to $-T_R$. To prevent retriggering when trailing-edge triggering is used, Q must be connected to $+T_R$.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01$ uF. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 2. Note that the exact values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

The CD4098B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4098 is similar to type MC14528.



CD4098
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A)

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal). . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to 85°C (PACKAGE TYPES E, Y) . . . . . .Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . .Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TABLE I

CD4098 FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE LAST INPUT PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE FIRST INPUT PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE) — T_X

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE) — T_X

Features:

- **Retriggerable/resettable capability**
- **Trigger and reset propagation delays independent of R_X, C_X**
- **Triggering from leading or trailing edge**
- **Q and $\overline{Q}$ buffered outputs available**
- **Separate resets**
- **Wide range of output-pulse widths**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Pulse delay and timing**
- **Pulse shaping**
- **Astable Multivibrator**

Preliminary CD4098B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

CHARACTERISTIC	TEST CONDITIONS			TYPICAL VALUES	UNITS
	R_X(kΩ)	C_X(pF)	V_{DD}(V)		
Trigger Propagation Delay Time +TR, −TR to Q, $\bar{Q}$ t_{PLH}, t_{PHL}	5 to 10,000	≥15	5 10 15	300 125 100	ns
Minimum Trigger Pulse Width t_{WL}, t_{WH}	5 to 10,000	≥15	5 10 15	75 30 25	ns
Transition Time t_{TLH}, t_{THL}	5 to 10,000	≤10,000	5 10 15	100 50 40	ns
Reset Propagation Delay Time t_{TLH}, t_{PHL}	5 to 10,000	≥15	5 10 15	250 100 75	ns
Minimum Reset Pulse Width t_W	5	15	5 10 15	125 75 50	ns
	10	1000	5 10 15	500 275 200	
Average Input Capacitance C_I	Any Input			5	pF

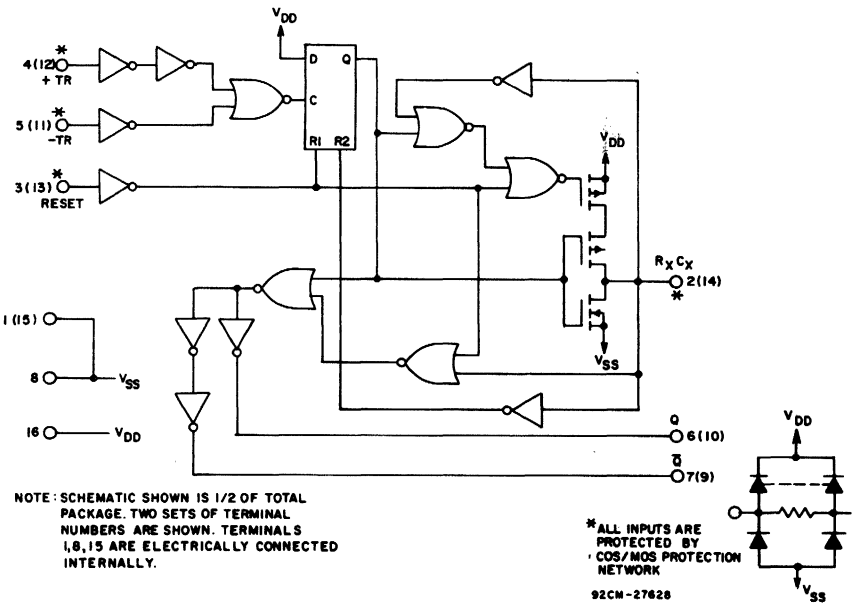


Fig. 1 – CD4098 logic diagram.

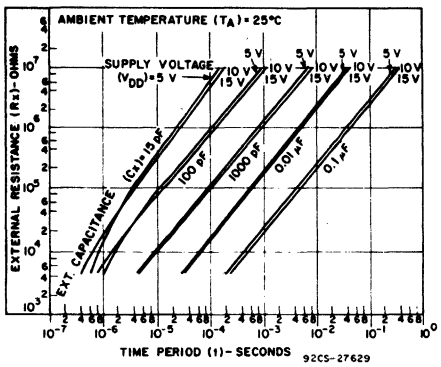


Fig. 2 – Typical external resistance vs. time period for various values of supply voltage and external capacitance.

APPLICATIONS

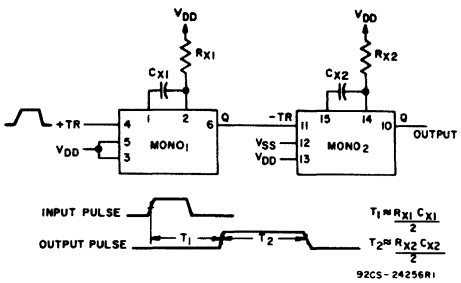


Fig. 3 – Pulse delay.

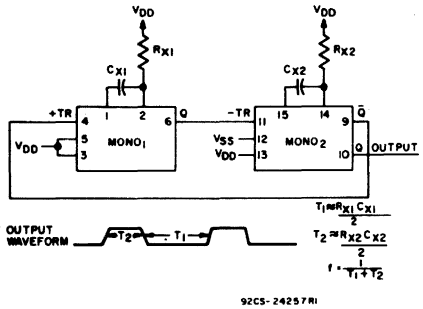


Fig. 4 – Astable multivibrator.

Preliminary CD4098B Types

STATIC ELECTRICAL CHARACTERISTICS *at* $T_A = 25^\circ C$

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 min.	V
	9	–	10	1 min.	
	13.5	–	15	1 min.	
Inputs High, V_{NMH}	0.5	–	5	1 min.	
	1	–	10	1 min.	
	1.5	–	15	1 min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

CD4099B Types

COS/MOS 8-Bit Addressable Latch

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

The RCA-CD4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4099B types are supplied in 16-lead hermetic ceramic dual-in-line packages (D, F, Y suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Serial data input**
- **Active parallel output**
- **Storage register capability**
- **Master clear**
- **Can function as demultiplexer**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Multi-line decoders**
- **A/D converters**

RECOMMENDED OPERATING CONDITIONS *at T_A = 25° C (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 2*	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Minimum Pulse Width, t_W Data	(4)	5	200	–	ns
		10	100	–	
		15	80		
Address	(8)	5	400	–	
		10	200	–	
		15	125	–	
Reset	(5)	5	150	–	
		10	75	–	
		15	50	–	
Setup Time, t_S Data to WRITE DISABLE	(6)	5	100	–	ns
		10	50	–	
		15	35	–	
Hold Time, t_H Data to WRITE DISABLE	(7)	5	150	–	ns
		10	75	–	
		15	50	–	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed (see Fig.1).

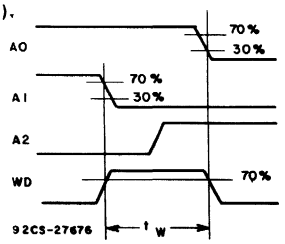


Fig. 1 – Definition of WRITE DISABLE ON time.

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the COS/MOS section.

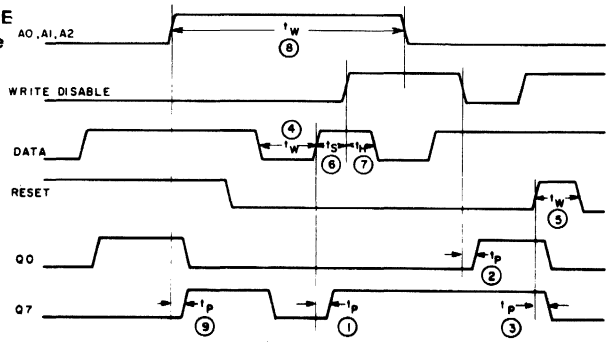
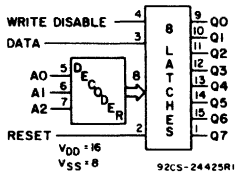


Fig. 2 – Master timing diagram.



FUNCTIONAL DIAGRAM

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE
R = RESET

CD4099B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 KΩ*

CHARACTERISTIC	CONDITIONS SEE FIG. 2*	V_{DD} (V)	LIMITS ALL PACKAGE TYPES TYP.	MAX.	UNITS
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH}, t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL}, (Any Output) t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Average Input Capacitance, C_I	Any Input		5	–	pF

*Circled numbers refer to times indicated on master timing diagram.

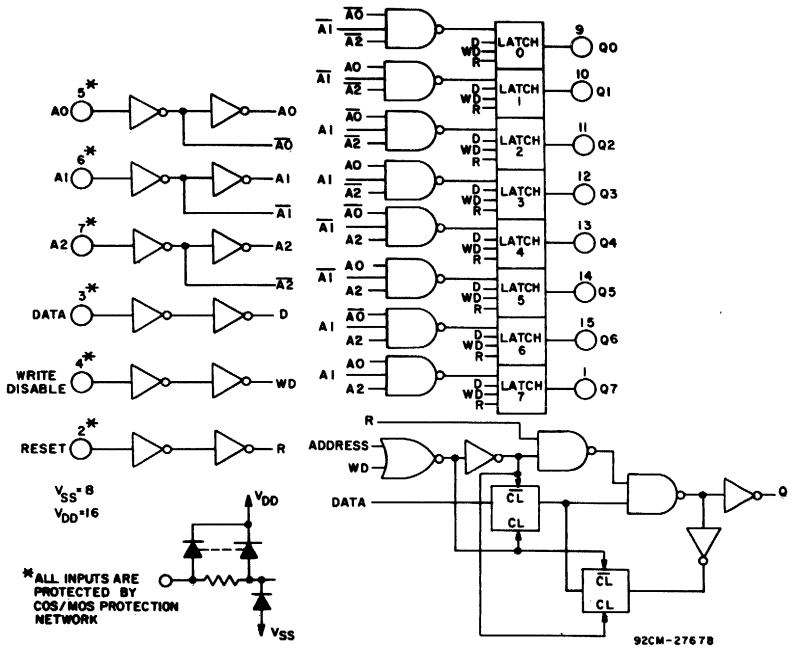


Fig. 3 – Logic diagram and schematic of 1 of 8 latches.

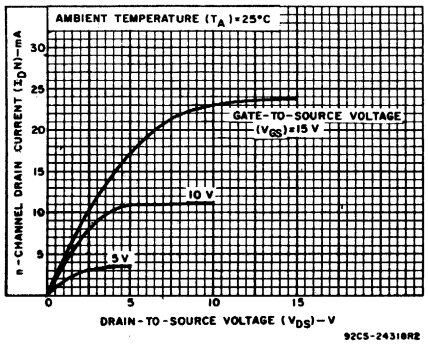


Fig. 4 – Typical output-N-channel drain characteristics.

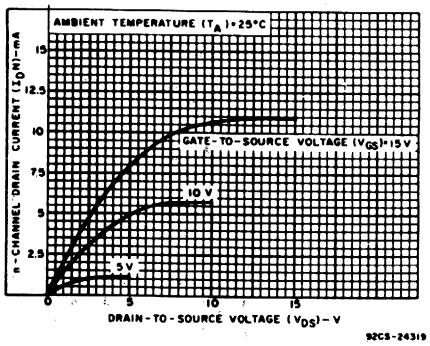


Fig. 5 – Minimum output-N-channel drain characteristics.

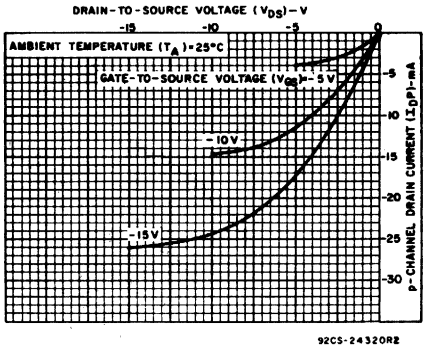


Fig. 6 – Typical output-P-channel drain characteristics.

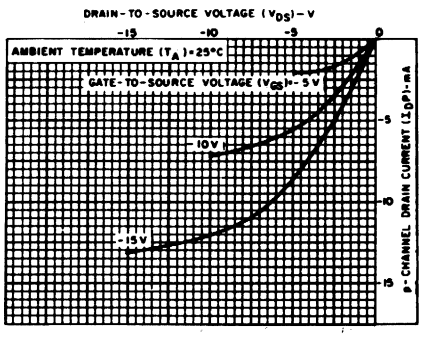


Fig. 7 – Minimum output-P-channel drain characteristics.

CD4099B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (° C) Values at -55, +25, +125 Apply to D, K, F, H Packages Values at -40, +25, +85 Apply to E, Y Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High-Level V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$±10^{-5}$	±1	μA
3-State Output Leakage Current I_{OL}, I_{OH} Max.	Forced (Output Disabled) 0, 20	–	20	±2				–	$±10^{-4}$	±2	μA

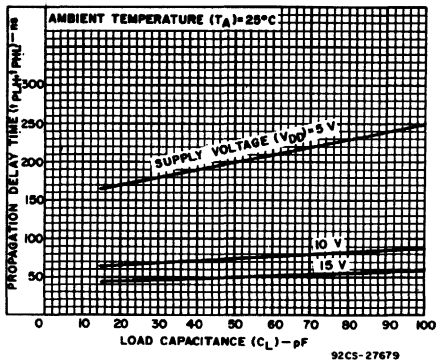


Fig. 8 – Typical propagation delay time (data to Qn) vs. load capacitance.

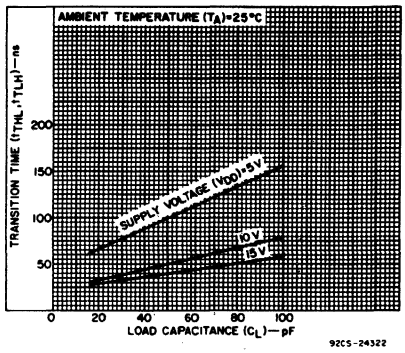


Fig. 9 – Typical transition time vs. load capacitance.

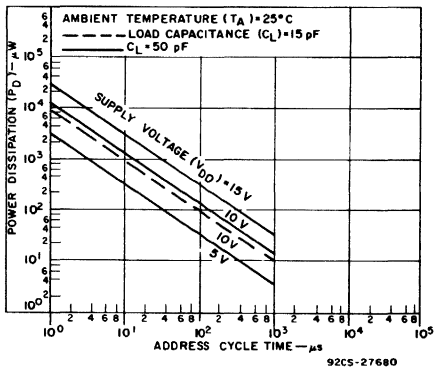


Fig. 10 – Typical dynamic power dissipation vs. address cycle time.

Preliminary CD4502B Types

COS/MOS Strobed Hex Inverter/Buffer

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4502 consists of 6 inverter/buffers with 3-state outputs. When the DISABLE input is at logical "1" all six outputs become high impedance (> 10 MΩ). This feature simplifies design by allowing common busing of the outputs. The INHIBIT input switches all six outputs to logical "0" when INHIBIT is at logical "1".

The CD4502B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

This device is similar to the MC14502.

TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	Z

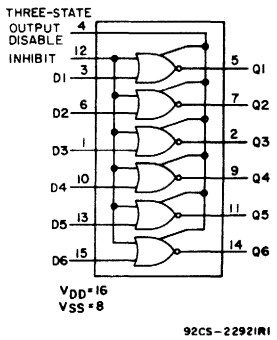
X = Don't Care
Logic 1 = High
Logic 0 = Low
Z = High Impedance

Features:

- 2-TTL-Load Output-Drive Capability
- 3-State Outputs
- Common Output-Disable Control
- Inhibit Control
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- 3-State Hex Inverter for Interfacing IC's with Data Buses
- COS/MOS-to-TTL Hex Buffer



CD4502
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,K,H ..... −55 to +125°C
PACKAGE TYPES E,Y ..... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A=−40 to +60°C (PACKAGE TYPES E,Y) ..... 500 mW
FOR T_A=+60 to +85°C (PACKAGE TYPES E,Y) ..... Derate Linearly at 12 mW/°C to 200 mW
FOR T_A=−55 to +100°C (PACKAGE TYPES D,F,K) ..... 500 mW
FOR T_A=+100 to +125°C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

TEST CONDITIONS		
TEST	PIN 15	POINT A
t_{PHZ}	V_{SS}	V_{SS}
t_{PLZ}	V_{DD}	V_{DD}
t_{PZL}	V_{DD}	V_{DD}
t_{PZH}	V_{SS}	V_{SS}

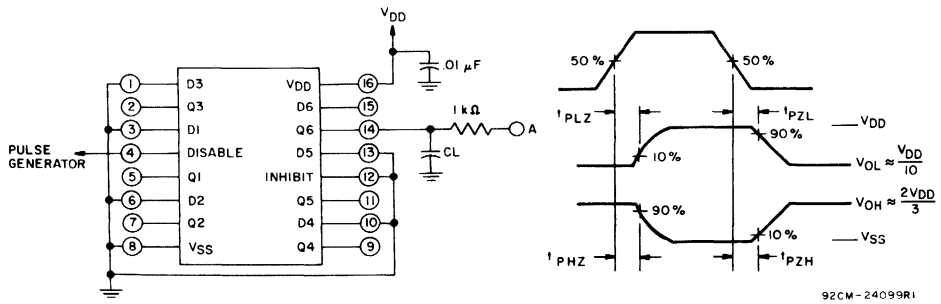


Fig. 1 — Disable delay times test circuit and waveforms.

Preliminary CD4502B Types

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L	–	–	5	0.01	μA
	–	–	10	0.01	
	–	–	15	0.01	
	–	–	20	0.02	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	5.7	mA
	0.5	–	10	12.5	
	1.5	–	15	49	
P-Channel (Source), I_DP	4.6	–	5	−0.8	
	2.5	–	5	−3.2	
	9.5	–	10	−1.8	
	13.5	–	15	−6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current, I_{OL}, I_{OH}	Forced (Output Disabled)				
	0, 20	–	20	$\pm 10^{-4}$	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUES	UNITS
Data or Inhibit Delay Times: High to Low, t_{PHL}		5	135	ns
		10	60	
		15	40	
Low to High, t_{PLH}		5	200	
		10	90	
		15	65	
Disable Delay Times: Output High to High Impedance, t_{PHZ}	See Fig.3	5	60	ns
		10	40	
		15	20	
High Impedance to Output High, t_{PZH}		5	110	
		10	50	
		15	40	
Output Low to High Impedance, t_{PLZ}		5	125	
		10	65	
		15	55	
High Impedance to Output Low, t_{PZL}		5	125	
		10	55	
		15	40	
Transition Times: Low to High, t_{TLH}		5	100	ns
		10	50	
		15	40	
High to Low, t_{THL}		5	60	
		10	30	
		15	20	
Average Input Capacitance, C_I	Any Input		5	pF

Preliminary CD4508B Types

COS/MOS Dual 4-Bit Latch

High-Voltage Types (3-to-20-Volt Rating)

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	V_{DD}	TYPICAL VALUES	UNITS
Transition Time, t_{THL}, t_{TLH}		5 10 15	100 50 40	ns
Minimum Reset Pulse Width, t_W		5 10 15	100 50 40	ns
Minimum Strobe Pulse Width, t_W		5 10 15	70 35 20	ns
Minimum Setup Time, t_S		5 10 15	25 10 5	ns
Minimum Hold Time, t_H		5 10 15	0 0 0	ns
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe to Data Out		5 10 15	120 60 45	ns
3-State Propagation Delay Times: Output High to High Impedance, t_{PHZ}	R_L = 1 kΩ to V_{SS}	5 10 15	95 70 60	ns
High Impedance to Output High, t_{PZH}	R_L = 1 kΩ to V_{SS}	5 10 15	85 50 40	ns
Output Low to High Impedance, t_{PLZ}	R_L = 1 kΩ to V_{DD}	5 10 15	95 70 60	ns
High Impedance to Output Low, t_{PZL}	R_L = 1 kΩ to V_{DD}	5 10 15	85 50 40	ns
Input Capacitance, C_I	Any Input	—	5	pF

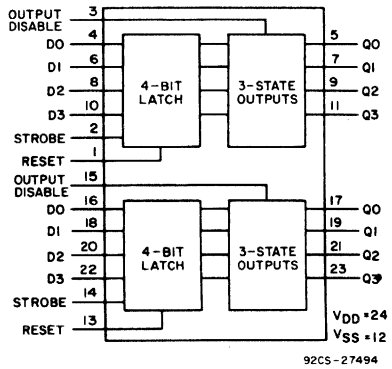


Fig.1 — Functional diagram.

Features:

- **Two independent 4-bit latches**
- **Individual master reset for each 4-bit latch**
- **3-state outputs with high-impedance state for bus line applications**
- **Medium-speed operation: t_{PHL} = t_{PLH} = 60 ns (typ.) at V_{DD} = 10 V and C_L = 50 pF**

Applications:

- **Buffer storage**
- **Holding registers**
- **Data storage and multiplexing**

The RCA-CD4508B dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508B types are supplied in the 24-lead dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4508 is similar to industry type MC14508.

Preliminary CD4508B Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C:

CHARACTERISTIC	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0	V
	–	0,10	10	0	
	–	0,15	15	0	
High-Level, V_{OH}	–	0,5	5	5	
	–	0,10	10	10	
	–	0,15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1,5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.	V
	9	–	10	1 Min.	
	13.5	–	15	1 Min.	
Inputs High, V_{NMH}	0.5	–	5	1 Min.	
	1	–	10	1 Min.	
	1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink) I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	–0.8	
	2.5	–	5	–3.2	
	9.5	–	10	–1.8	
	13.5	–	15	–6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current, I_{OL}, I_{OH}	Forced (Output Disabled)				μA
	0,20	–	20	$\pm 10^{-4}$	

TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
Z = HIGH IMPEDANCE

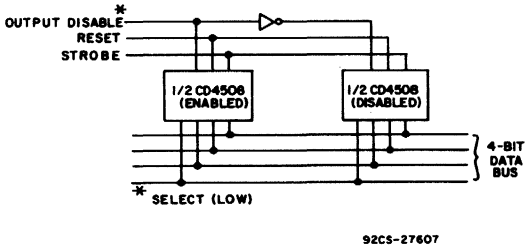


Fig.3 – Typical application.

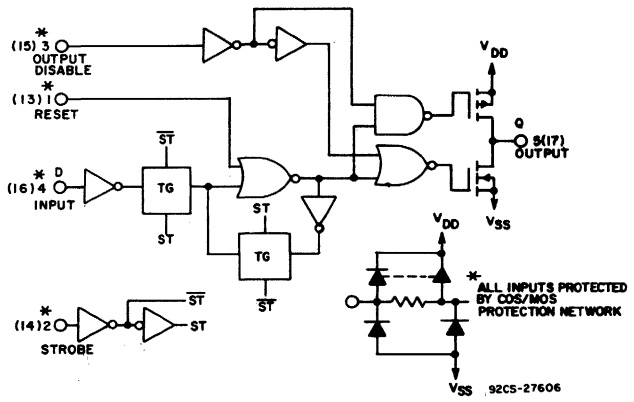


Fig.2 – Logic diagram, 1 of 4 identical latches.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C,
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range	3	18	V

CD4510B, CD4516B Types

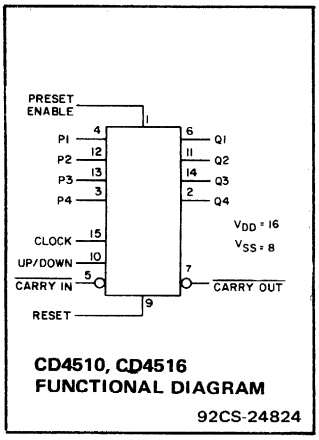
COS/MOS Presettable Up/Down Counters

CD4510B — — — BCD Type CD4516B — — — Binary Type

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4510 Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.



CD4510, CD4516 FUNCTIONAL DIAGRAM

92CS-24824

The CD4510 and CD4516 can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

These devices are similar to types MC14510 and MC14516.

The CD4510B and CD4516B Series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE		−65 to +150°C
OPERATING TEMPERATURE RANGE:		
PACKAGE TYPES D, F, K, H		−55 to +125°C
PACKAGE TYPES E, Y		−40 to +85°C
DC SUPPLY VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} Terminal)		−0.5 to +20 V
POWER DISSIPATION PER PACKAGE:		
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)		500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly to	200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)		500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly to	200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR T_A = Full Package-Temperature Range (All Package Types)		100 mW
INPUT VOLTAGE RANGE, ALL INPUTS		−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max.		+265°C

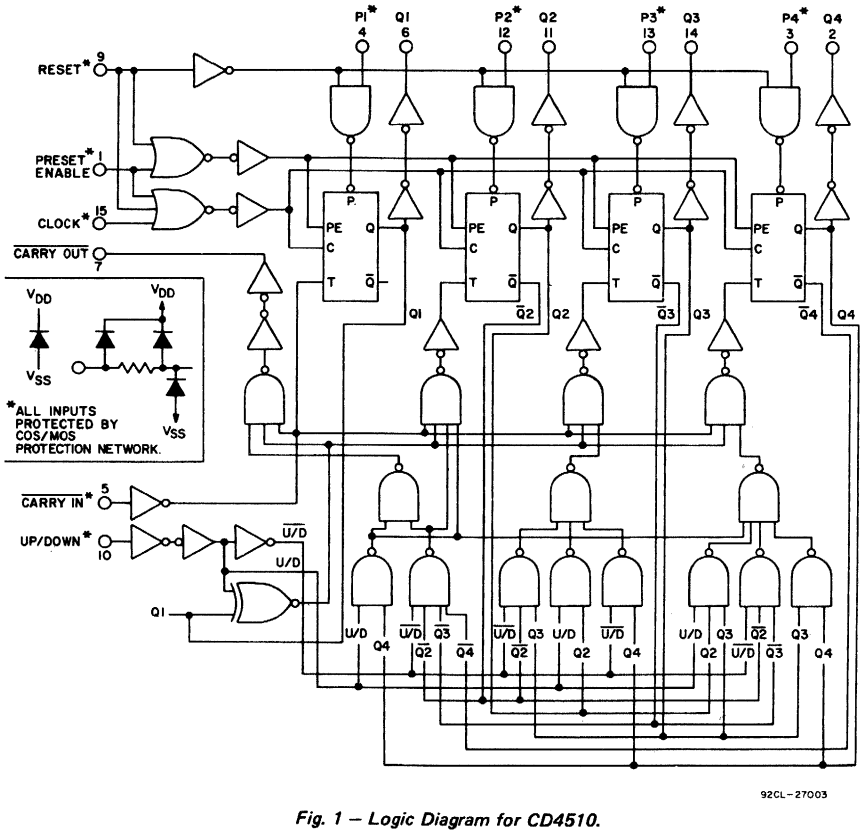


Fig. 1 – Logic Diagram for CD4510.

Features:

- **Medium-speed operation — f_{CL} = 8 MHz typ. at 10 V**
- **Synchronous internal carry propagation**
- **Reset and Preset capability**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1μA at 20 V (full-package-temperature range)**
- **1 V noise margin (full package-temperature range)**
- **Standard symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Up/Down difference counting**
- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**

TRUTH TABLE

CL	$\overline{CI}$	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⌐	0	1	0	0	COUNT UP
⌐	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

CD4510B, CD4516B Types

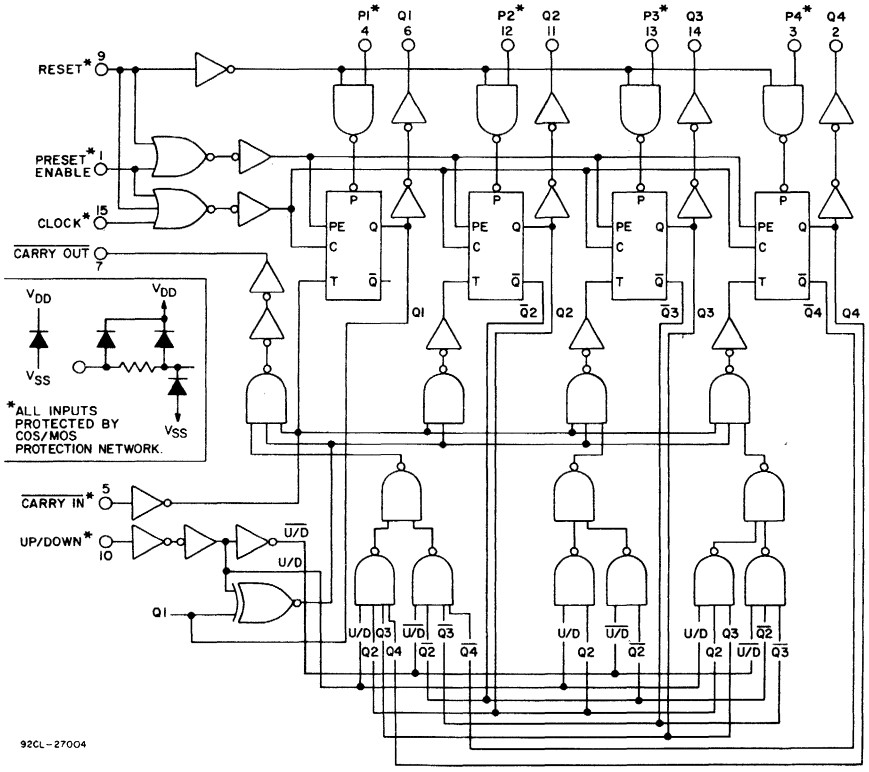


Fig. 2 – Logic Diagram for CD4516.

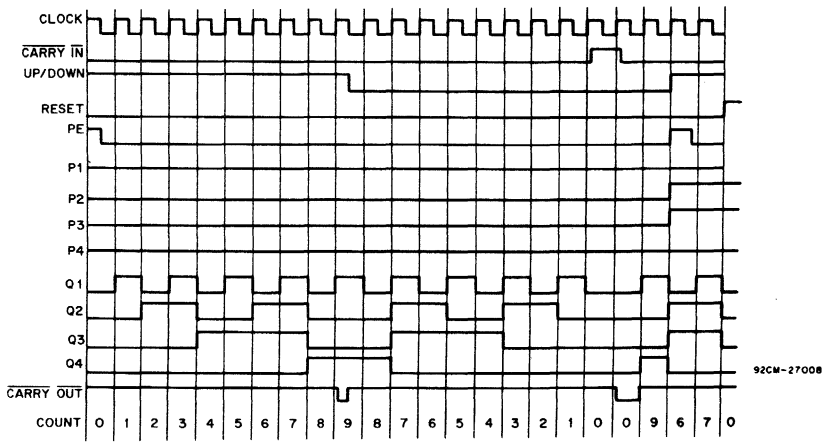


Fig. 3 – Timing diagram for CD4510.

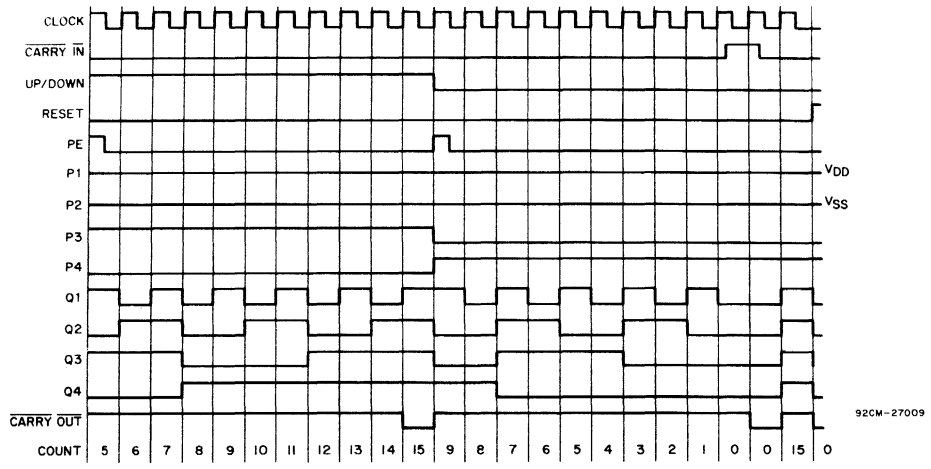


Fig. 4 – Timing diagram for CD4516.

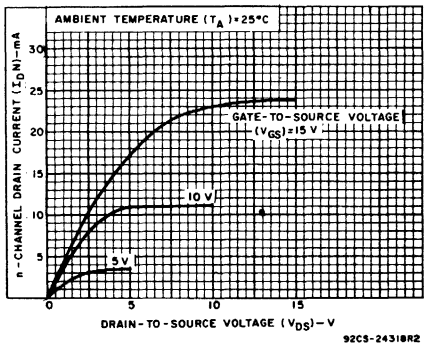


Fig. 5 – Typical output-N-channel drain characteristics.

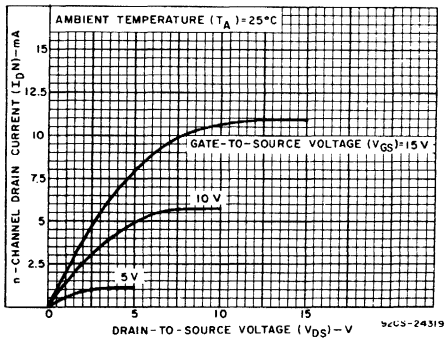


Fig. 6 – Minimum output-N-channel drain characteristics.

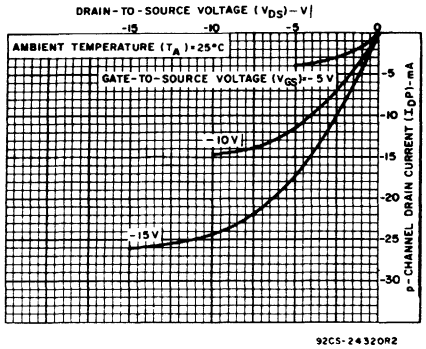


Fig. 7 – Typical output-P-channel drain characteristics.

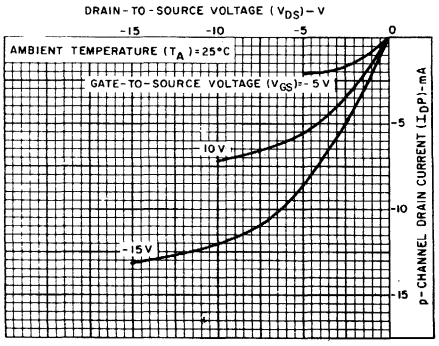


Fig. 8 – Minimum output-P-channel drain characteristics.

CD4510B, CD4516B Types

OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At T_A = Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_W	5	150	–	ns
	10	75	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	4	
	15	–	5.5	
Preset Enable or Reset Removal Time●	5	150	–	ns
	10	80	–	
	15	60	–	
Clock Rise and Fall Time, t_rCL, t_fCL *	3-20	–	15	16
Carry-In Setup Time, t_S	5	130	–	ns
	10	60	–	
	15	45	–	
Up-Down Setup Time, t_S	5	360	–	ns
	10	160	–	
	15	110	–	
Preset Enable or Reset Pulse Width, t_W	5	220	–	ns
	10	100	–	
	15	75	–	

●Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns, R_L = 200 kΩ

Characteristic	Conditions V_{DD} (V)	Limits All Packages Min.	Typ.	Max.	Units
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Q Output (See Fig. 10)	5	–	200	400	ns
	10	–	100	200	
	15	–	75	150	
Preset or Reset-to-Q Output	5	–	210	420	ns
	10	–	105	210	
	15	–	80	160	
Clock-to-Carry Out	5	–	240	480	ns
	10	–	120	240	
	15	–	90	180	
Carry-In-to-Carry Out	5	–	125	250	ns
	10	–	60	120	
	15	–	50	100	
Preset or Reset-to-Carry Out	5	–	320	640	ns
	10	–	160	320	
	15	–	125	250	
Transition Time (t_{THL}, t_{TLH}) (See Fig. 9)	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Average Input Capacitance (C_I) (Any Input)		–	5	–	pF

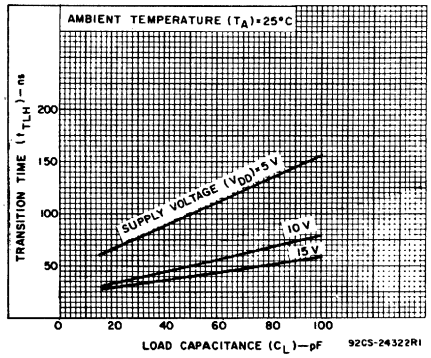


Fig. 9 – Typical transition time vs. load capacitance.

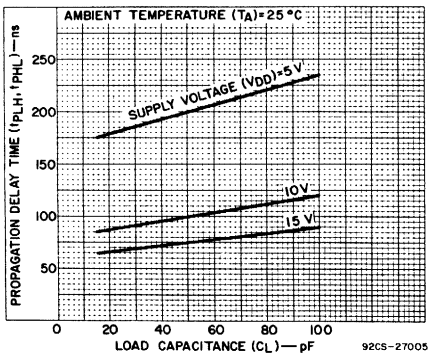


Fig. 10 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

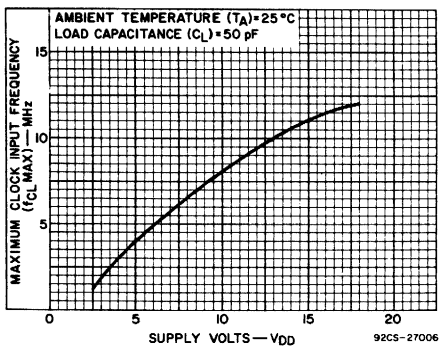


Fig. 11 – Typical maximum clock input frequency vs. supply voltage.

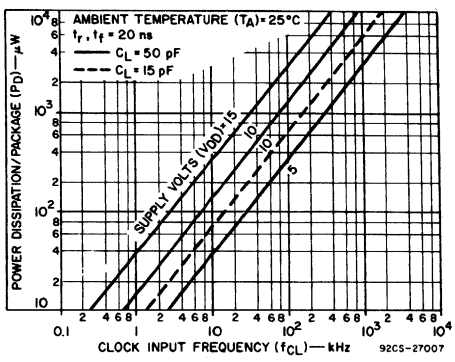


Fig. 12 – Typical dynamic power dissipation characteristics.

CD4510B, CD4516B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits *Values at −55°C, +25°C, +125°C Apply to D,K,H Packages* *Values at −40°C, +25°C, +85°C Apply to E Packages*							Units
									+25°		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°	−40°	+85°	+125°	Min.	Typ.	Max.	
Quiescent Device Current, I_L MAX	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage: Low-Level, V_{OL} MAX	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High-Level, V_{OH} MIN	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	
		0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} MIN	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} MIN	0.8	–	5	1.5				1.5	2.25	–	V
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Input Low, V_{NML} MIN	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} MIN	0.5	–	5	1				1	–	–	V
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_{DN} MIN (See Figs.5,6)	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP MIN (See Figs.7,8)	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	mA
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−11	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current (Any Input) I_{IL}, I_{IH} MAX			20	±1				–	$\pm 10^{-5}$	±1	μA

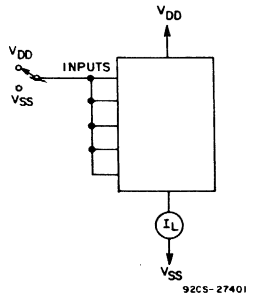


Fig. 13 – Quiescent device current test circuit.

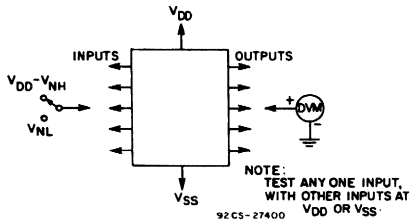
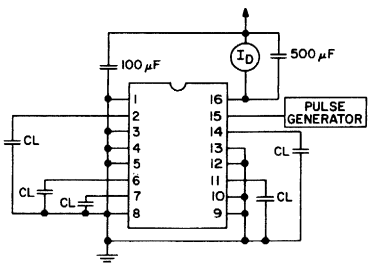


Fig. 14 – Noise immunity test circuit.



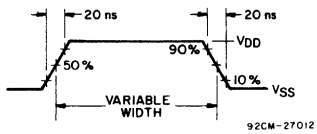


Fig. 15 – Power dissipation test circuit and input waveform.

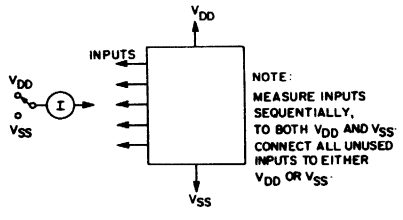


Fig. 16 – Input leakage current.

CD4511B Types

COS/MOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

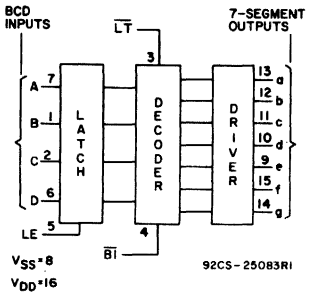
The CD4511B types are BCD-to-7-segment latch decoder drivers constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.

Lamp Test (LT), Blanking (BI), and Latch Enable (LE) inputs are provided to test the display, shut off or intensify-modulate it, and store a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used. The CD4511B is supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix). For ordering information, see dimensional outline page 12.

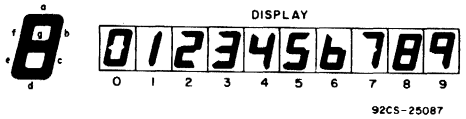
These devices are similar to the type MC14511.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C)							Units
					Values at −55, +25, +125 for D, F, K, H Packages Values at −40, +25, +85 for E, Y Packages				+25			
	I_{OH} (mA)	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current: I_L MAX	–	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	–	10	10	10	100	200	–	0.02	10	
	–	–	–	15	20	20	200	400	–	0.02	20	
	–	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage:												
	–	–	0,5	5	0.05				–	0	0.05	
Low-Level V_{OL} MAX	–	–	0,10	10	0.05				–	0	0.05	V
	–	–	0,15	15	0.05				–	0	0.05	
	–	–	0,5	5	4	4	4.2	4.2	4.1	4.55	–	
High-Level V_{OH} MIN	–	–	0,10	10	9	9	9.2	9.2	9.1	9.55	–	V
	–	–	0.15	15	14	14	14.2	14.2	14.1	14.55	–	
Noise Immunity:												
	–	3.3	–	5	1.5				1.5	2.25	–	
Inputs Low V_{NL} MIN	–	8.1	–	10	3				3	4.5	–	V
	–	12.6	–	15	4.5				4.5	6.75	–	
	–	0.8	–	5	1.5				1.5	2.25	–	
Inputs High V_{NH} MIN	–	1	–	10	3				3	4.5	–	V
	–	1.5	–	15	4.5				4.5	6.75	–	
Output Drive Voltage: High Level V_{OH} MIN	0	–	–	5	4.0	4.0	4.20	4.20	4.10	4.55	–	V
	5	–	–		–	–	–	–	–	4.25	–	
	10	–	–		3.80	3.80	3.90	3.90	3.90	4.10	–	
	15	–	–		–	–	3.50	3.50	–	3.95	–	
	20	–	–		3.55	3.55	–	–	3.40	3.75	–	
	25	–	–		3.40	3.40	–	–	3.10	3.55	–	
	0	–	–	10	9.0	9.0	9.20	9.20	9.10	9.55	–	V
	5	–	–		–	–	–	–	–	9.25	–	
	10	–	–		8.85	8.85	9.00	9.00	9.00	9.15	–	
	15	–	–		–	–	–	–	–	9.05	–	
	20	–	–		8.70	8.70	8.40	8.40	8.60	8.90	–	
	25	–	–		8.60	8.60	–	–	8.30	8.75	–	
	0	–	–	15	14.0	14.0	14.20	14.20	14.10	14.55	–	V
	5	–	–		–	–	–	–	–	14.30	–	
	10	–	–		13.90	13.90	14.0	14.0	14.0	14.20	–	
	15	–	–		–	–	–	–	–	14.10	–	
	20	–	–		13.75	13.75	13.50	13.50	13.70	13.95	–	
	25	–	–		13.65	13.65	13.10	13.10	13.50	13.80	–	
Output Drive Current: N-Channel (Sink) I_{DN} MIN	–	0.4	–	5	0.63	0.56	0.45	0.38	0.5	1.0	–	mA
	–	0.5	–	10	1.4	1.3	0.19	0.81	1.1	2.2	–	
	–	1.5	–	15	4.1	4.0	3.1	2.8	3.7	7.4	–	
Input Leakage Current: I_{IL}, I_{IH} MAX	Any Input			20	±1					$±10^{-5}$	±1	μA



CD4511 Functional Diagram



Features:

- **High-output-sourcing capability..... up to 25 mA**
- **Input latches for BCD Code storage**
- **Lamp Test and Blanking capability**
- **7-segment outputs blanked for BCD input codes > 1001**
- **Quiescent current specified to 20 V**
- **Max. input leakage of 1 μA at 20 V, full package-temperature range**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Driving common-cathode LED displays**
- **Multiplexing with common-cathode LED displays**
- **Driving incandescent displays**
- **Driving low-voltage fluorescent displays**

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	Test Conditions	LIMITS All Packages			UNITS
	V_{DD} Volts	Min.	Typ.	Max.	
Propagation Delay Time: (Data) High-to-Low Level, t_{PHL}	5	–	520	1040	ns
	10	–	210	420	
	15	–	150	300	
Low-to-High Level, t_{PLH}	5	–	660	1320	ns
	10	–	260	520	
	15	–	180	360	
Propagation Delay Time: ($\overline{BL}$) High-to-Low Level, t_{PHL}	5	–	350	700	ns
	10	–	175	350	
	15	–	125	250	
Low-to-High Level, t_{PLH}	5	–	400	800	ns
	10	–	175	350	
	15	–	150	300	
Propagation Delay Time: ($\overline{LT}$) High-to-Low Level, t_{PHL}	5	–	250	500	ns
	10	–	125	250	
	15	–	85	170	
Low-to-High Level, t_{PLH}	5	–	150	300	ns
	10	–	75	150	
	15	–	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	–	40	100	ns
	10	–	30	75	
	15	–	25	65	
High-to-Low Level, t_{THL}	5	–	125	310	ns
	10	–	75	185	
	15	–	65	160	
Minimum Set-Up Time, t_S	5	150	75	–	ns
	10	70	35	–	
	15	40	20	–	
Minimum Hold Time, t_H	5	0	–75	–	ns
	10	0	–35	–	
	15	0	–20	–	
Latch Enable Pulse Width, t_W	5	400	200	–	ns
	10	160	80	–	
	15	100	50		
Average Input Capacitance (Any Input), C_I		–	5	–	pF

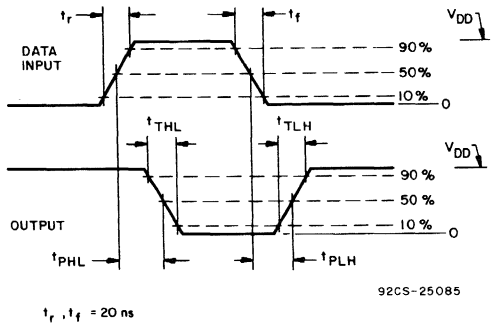
TRUTH TABLE

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X ≡ Don't Care

*Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).



OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A): (Full Package-Temperature Range)	–	3	18	V
Set-Up Time (t_S)	5	150	–	ns
	10	70	–	ns
	15	40	–	ns
Hold Time (t_H)	5	0	–	ns
	10	0	–	ns
	15	0	–	ns
Latch Enable Pulse Width (t_W)	5	400	–	ns
	10	160	–	ns
	15	100	–	ns

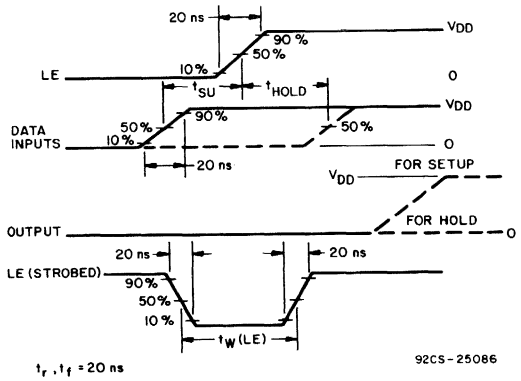


Fig. 1 – Dynamic waveforms.

CD4511B Types

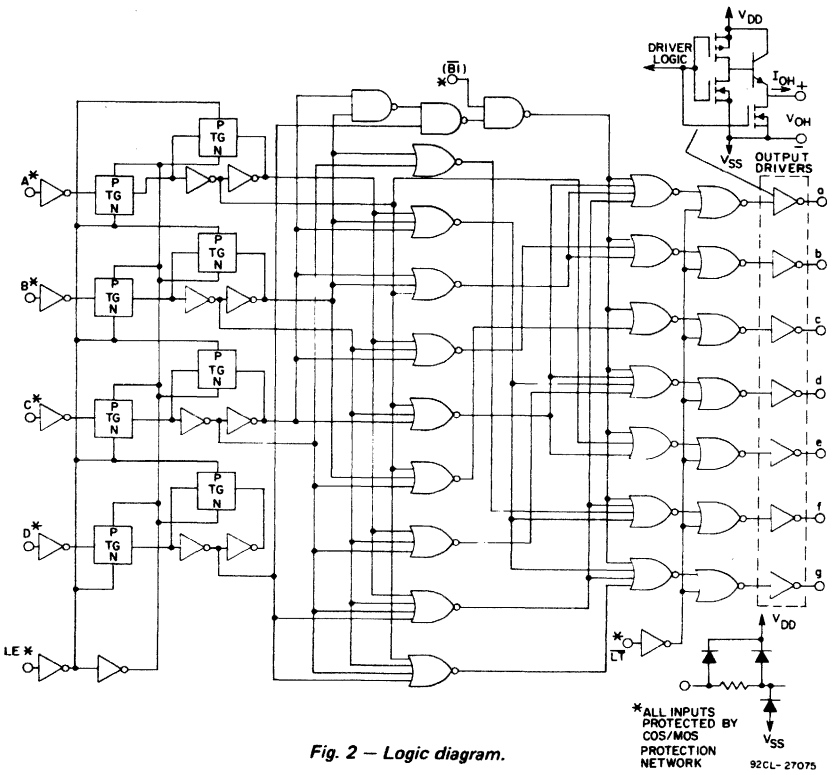


Fig. 2 – Logic diagram.

TYPICAL CHARACTERISTICS CURVES

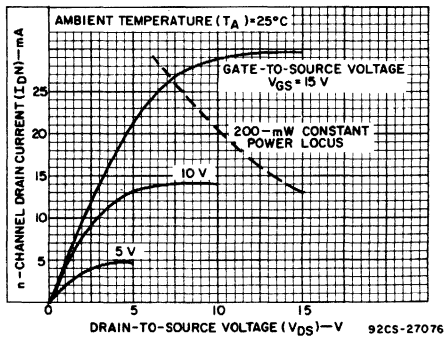


Fig. 3 – Typical output N-channel drain characteristics.

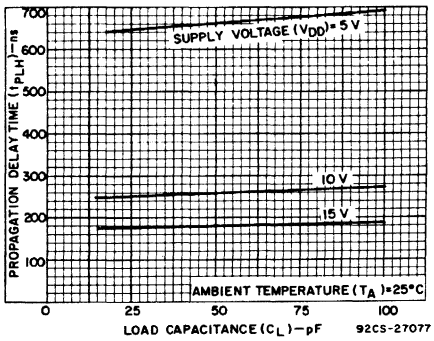


Fig. 4 – Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

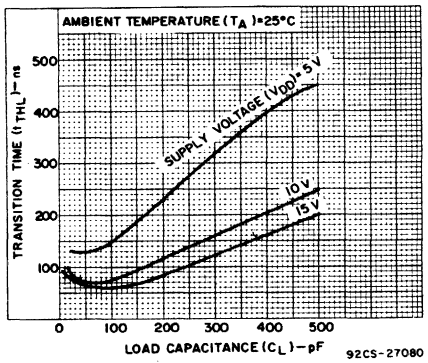


Fig. 7 – Typical high-to-low transition time as a function of load capacitance.

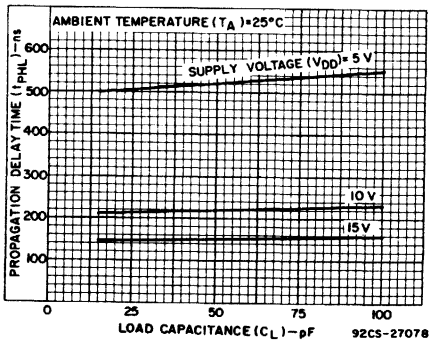


Fig. 5 – Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

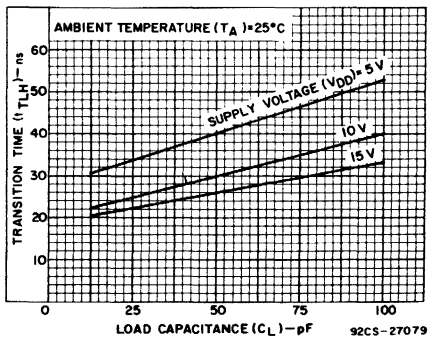


Fig. 6 – Typical low-to-high-level transition time as a function of load capacitance.

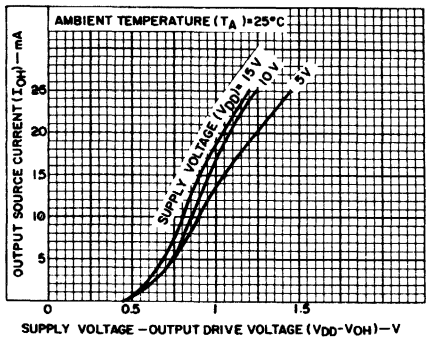
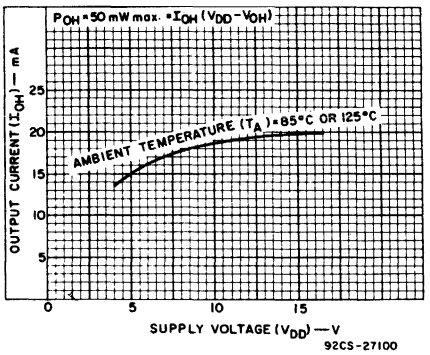


Fig. 8 – Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.



Maximum continuous derated output current I_{OH} applies to a single output with all other outputs sourcing an equal amount of current at the supply voltages shown. Operation above the derating curve is not recommended.

Fig. 9 –Derated static output current per output at T_A = 125°C (package types D, F, K) and at T_A = 85°C (package types E, Y).

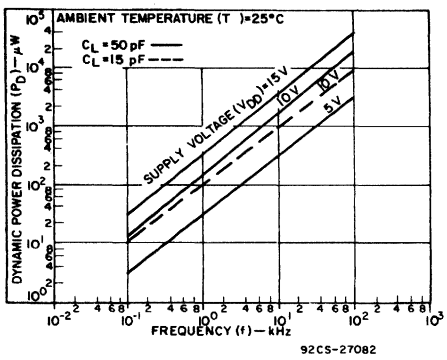
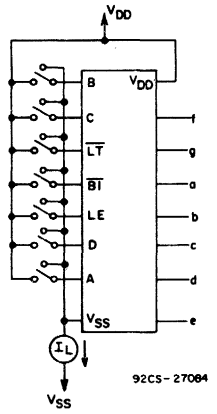


Fig. 10 – Typical dynamic power dissipation characteristics.

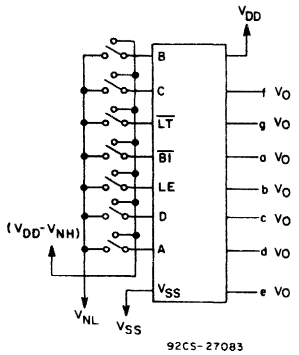
CD4511B Types

TEST CIRCUITS



Quiescent Device Current (I_L) is measured in all states shown in Truth Table, Fig. 2.

Fig. 11 – Quiescent Device Current.



Inputs, B, C, $\overline{LT}$, $\overline{BI}$, LE, D, A are switched as shown in Truth Table, Fig. 2. Outputs a-f are tested for V_O. Inputs are switched between V_{NL} and $(V_{DD}-V_{NH})$.

Fig. 12 – Noise Immunity

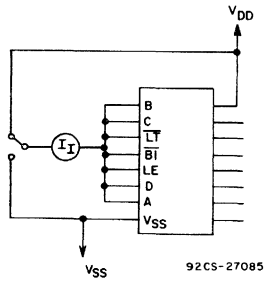


Fig. 13 – Input Leakage current.

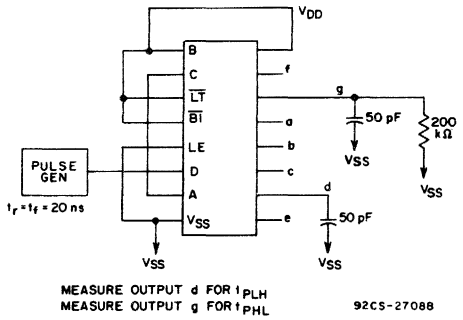


Fig. 14 – Data propagation delay.

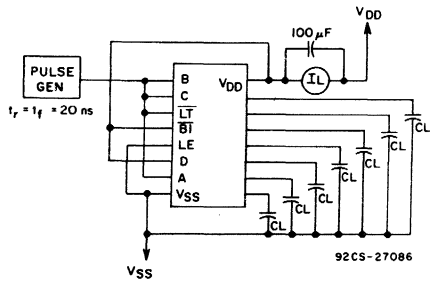


Fig. 15 – Dynamic power dissipation.

CD4514B, CD4515B Types

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (3-to-20-Volt Rating)

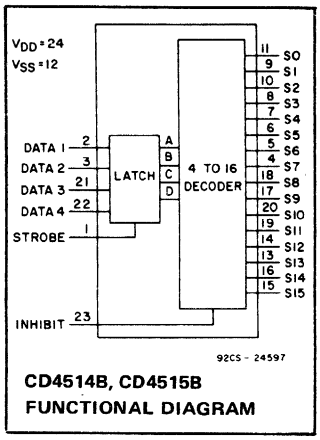
CD4514B Output "High" on Select
CD4515B Output "Low" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4514B, CD4515B
FUNCTIONAL DIAGRAM

Features:

- Strobed input latch
- Inhibit control
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding
- Program-counter decoding
- Control decoder

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D,K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	250	—	ns
	10	100	—	
	15	75	—	
Strobe Pulse Width, t_W	5	350	—	ns
	10	100	—	
	15	75	—	

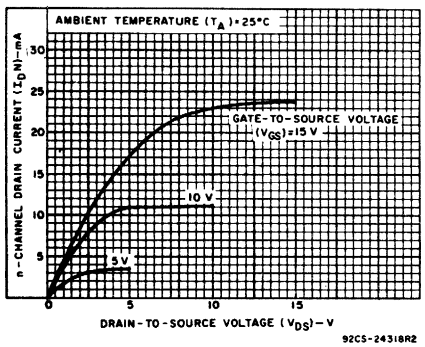


Fig. 2 — Typical output-n-channel drain characteristics.

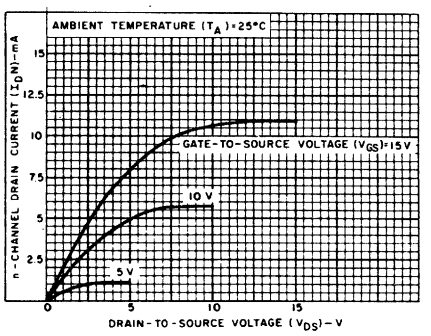


Fig. 3 — Minimum output-n-channel drain characteristics.

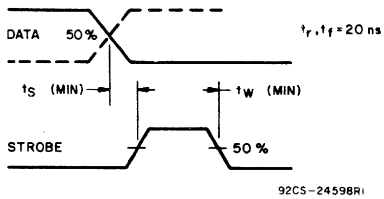


Fig. 1 — Waveforms for setup time and strobe pulse width.

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low

CD4514B, CD4515B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,H Packages* *Values at −40,+25,+85 Apply to E Package*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: n-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
p-Channel (Source), I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

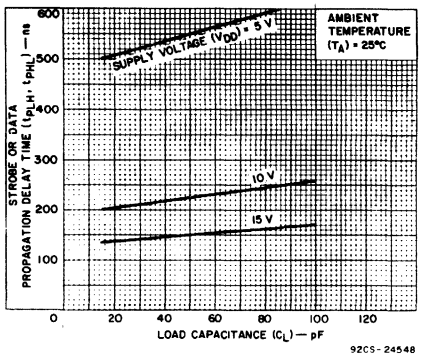


Fig. 4 – Typical strobe or data propagation delay time vs. load capacitance.

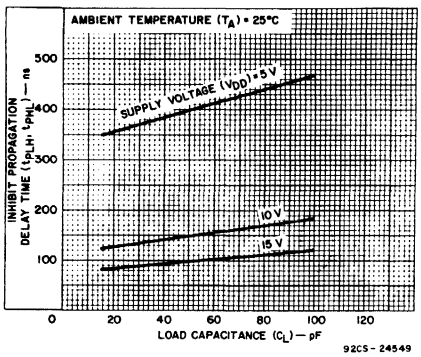


Fig. 5 – Typical inhibit propagation delay time vs. load capacitance.

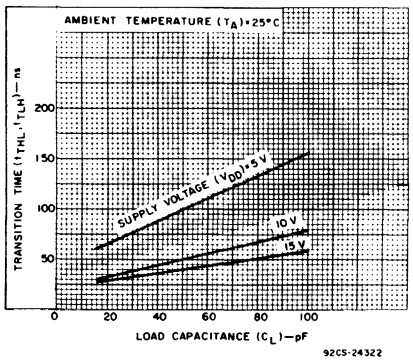


Fig. 6 – Typical low-to-high transition time vs. load capacitance.

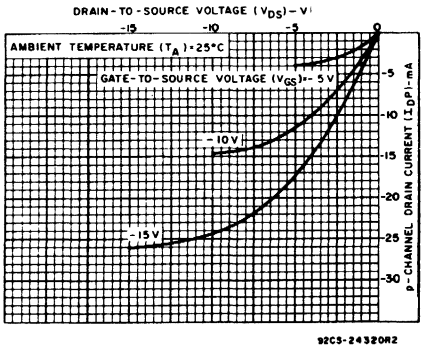


Fig. 7 – Typical output-p-channel drain characteristics.

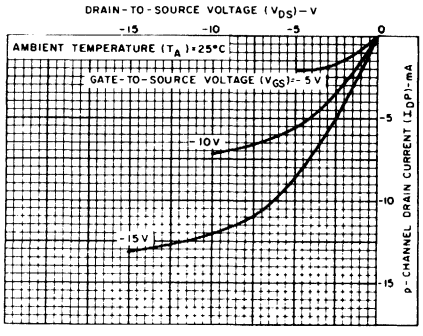


Fig. 8 – Minimum output-p-channel drain characteristics.

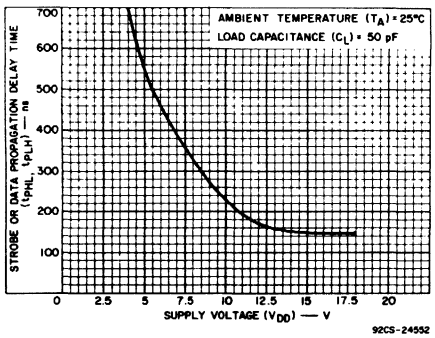


Fig. 9 – Typical strobe or data propagation delay time vs. supply voltage.

CD4514B, CD4515B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} V	Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Strobe or Data	5	550	1100	ns
	10	225	450	
	15	165	330	
Inhibit	5	400	800	
	10	150	300	
	15	125	250	
Transition Time, t_{TLH}, t_{THL}	5	100	200	
	10	50	100	
	15	40	80	
Minimum Strobe Pulse Width, t_W	5	175	350	ns
	10	50	100	
	15	40	75	
Minimum Data Setup Time, t_S	5	125	250	ns
	10	50	100	
	15	40	75	
Average Input Capacitance, C_I	Any Input	–	5	–	pF

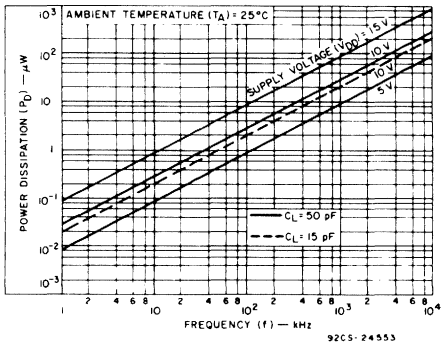


Fig. 10 – Typical power dissipation vs. frequency.

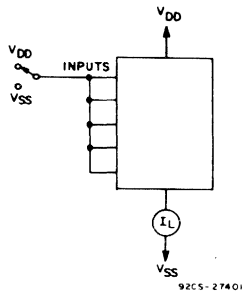


Fig. 11 – Quiescent device current test circuit.

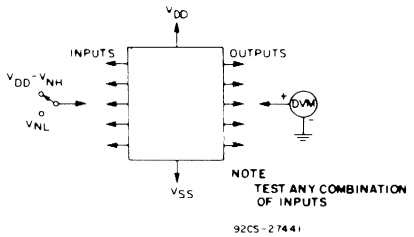


Fig. 12 – Noise immunity test circuit.

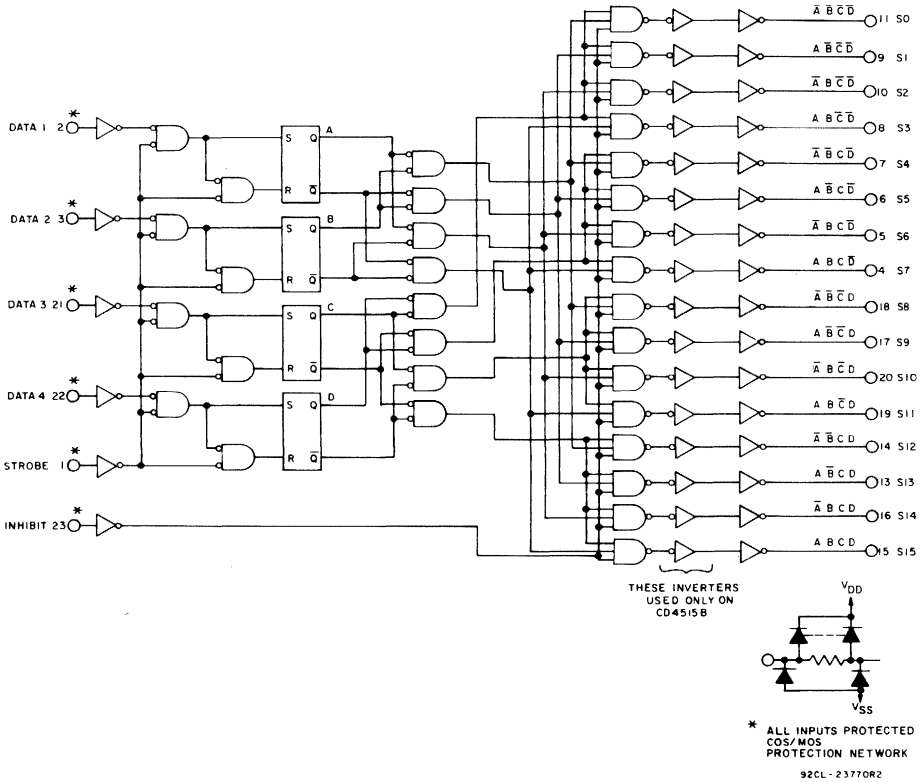


Fig. 13 – Logic diagram for CD4514B and CD4515B.

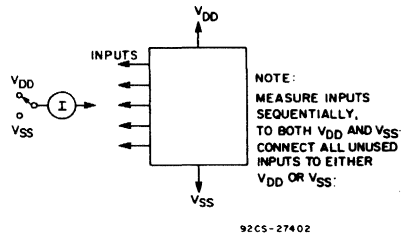


Fig. 14 – Input leakage current test circuit.

CD4518B, CD4520B Types

COS/MOS Dual Up-Counters

High-Voltage Types (3-to-20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

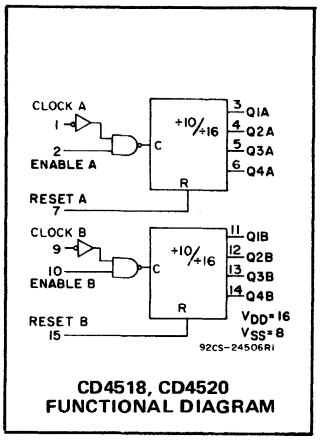
The RCA-CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐¬	1	0	Increment Counter
0	¬⌐	0	Increment Counter
¬⌐	X	0	No Change
X	⌐¬	0	No Change
⌐¬	0	0	No Change
1	¬⌐	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State



CD4518, CD4520
FUNCTIONAL DIAGRAM

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Medium-speed operation — 6-MHz typical clock frequency at 10 V**
- **Positive- or negative-edge triggering**
- **Synchronous internal carry propagation**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Multistage synchronous counting**
- **Multistage ripple counting**
- **Frequency dividers**

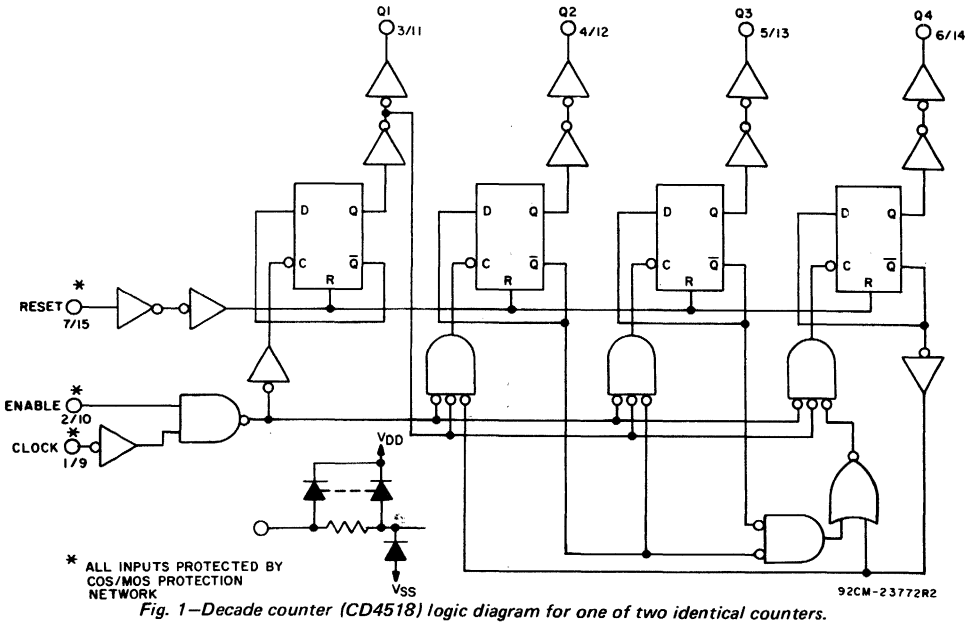


Fig. 1—Decade counter (CD4518) logic diagram for one of two identical counters.

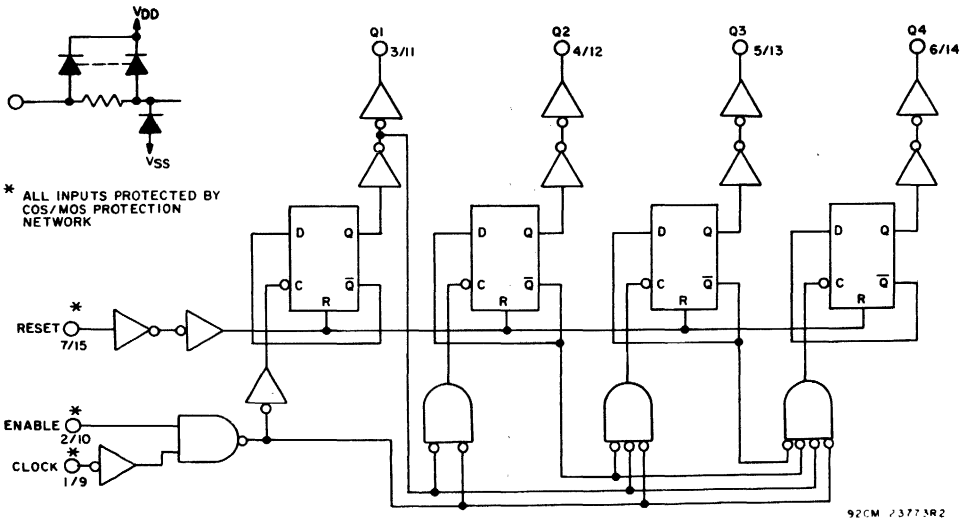


Fig. 2—Binary counter (CD4520) logic diagram for one of two identical counters.

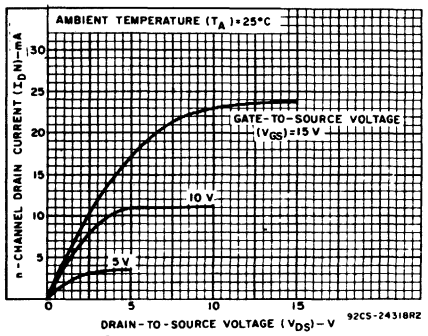


Fig. 3—Typical output-N-channel drain characteristics.

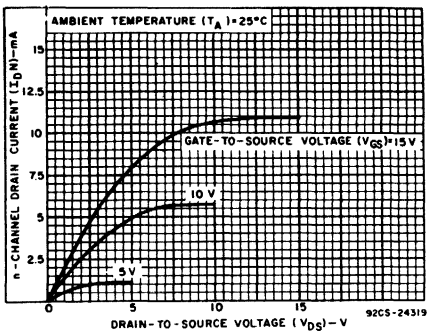


Fig. 4—Minimum output-N-channel drain characteristics.

CD4518B, CD4520B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High. V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

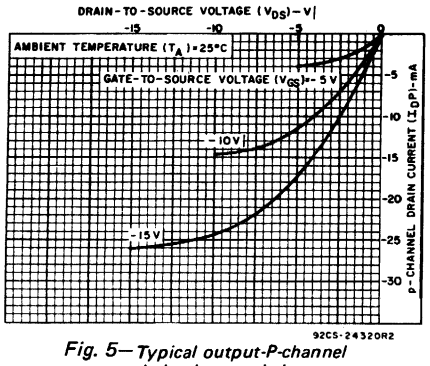


Fig. 5—Typical output-P-channel drain characteristics.

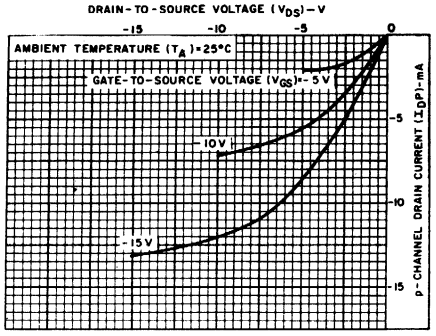


Fig. 6—Minimum output-P-channel drain characteristics.

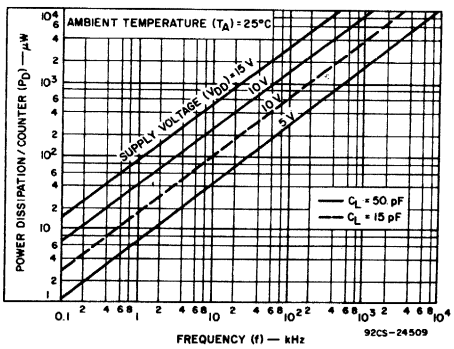


Fig. 7—Typical power dissipation characteristics.

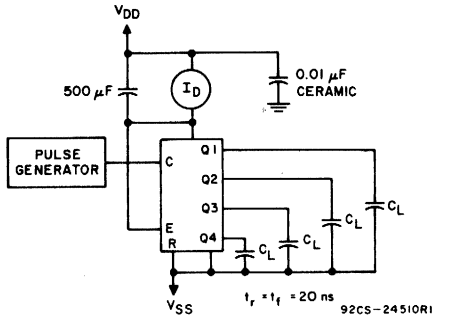


Fig. 8—Dynamic power-dissipation test circuit.

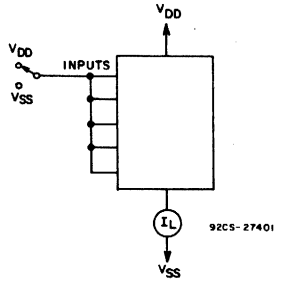


Fig. 9—Quiescent-device-current test circuit.

CD4518B, CD4520B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}: Reset to Output		5	–	280	560	ns
		10	–	115	230	
		15	–	80	160	
Clock or Enable to Output		5	–	330	650	
		10	–	130	225	
		15	–	90	170	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	–	MHz
		10	3	6	–	
		15	4	8	–	
Minimum Clock Pulse Width, t_W		5	–	100	200	ns
		10	–	50	100	
		15	–	35	70	
Clock Rise or Fall Time, t_r or t_f:		5,10	–	–	15	μs
		15	–	–	5	
Minimum Reset Pulse Width, t_W		5	–	125	250	ns
		10	–	55	110	
		15	–	40	80	
Minimum Enable Pulse Width, t_W		5	–	200	400	ns
		10	–	100	200	
		15	–	70	140	
Average Input Capacitance, C_I	Any Input	–	–	5	–	pF

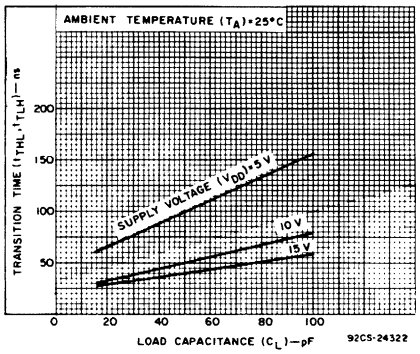


Fig. 10—Typical transition time vs. load capacitance.

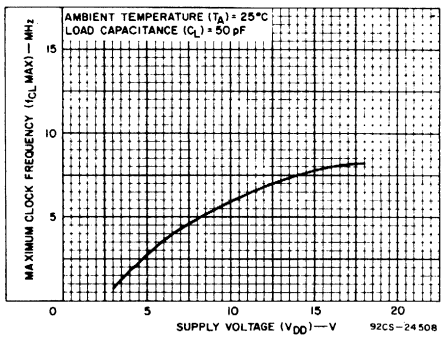


Fig. 11—Typical maximum-clock-frequency vs. supply voltage.

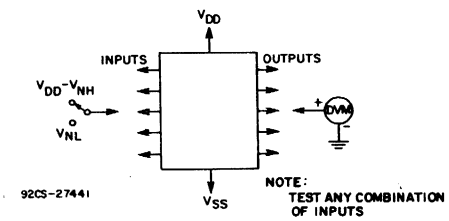


Fig. 12 – Noise-immunity test circuit.

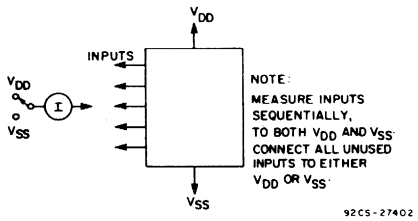


Fig. 13 – Input-leakage-current circuit.

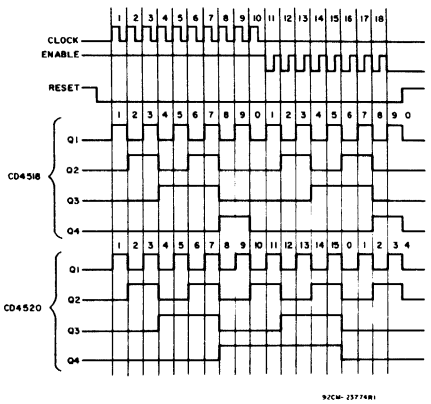


Fig. 14—Timing diagrams for CD4518 and CD4520

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Enable Pulse Width, t_W	5	400	–	ns
	10	200	–	
	15	140	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	70	–	
Clock Input Frequency, f_{CL}	5	dc	1.5	MHz
	10		3	
	15		4	
Clock Rise or Fall Time, t_rCL or t_fCL:	5,10	–	15	μs
	15	–	5	
Reset Pulse Width, t_W	5	250	–	ns
	10	110	–	
	15	80	–	

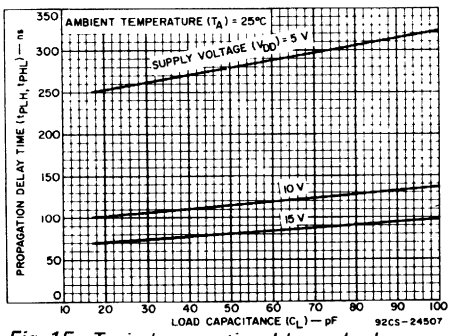


Fig. 15—Typical propagation delay vs. load capacitance (clock or enable to output).

Preliminary CD4527B Types

COS/MOS BCD Rate Multiplier

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4527 is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527 devices may be cascaded in two different modes: the Add mode and the Multiply mode. See Figs. 2 and 3. In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate})\left[0.1\ BCD_1 + 0.01\ BCD_2 + 0.001\ BCD_3 + \cdots\right]$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \text{ or 36 output}$$

pulses for every 100 clock input pulses.

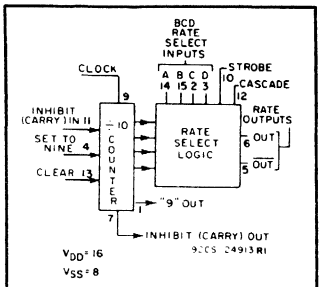
The CD4527B types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Numerical control**
- **Instrumentation**
- **Digital filtering**
- **Frequency synthesis**
- **For further application information, see ICAN-6739 "COS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions".**

Features:

- **Cascadable in multiples of 4-bits**
- **Set to "9" input and "9" detect output**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**



CD4527 Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPES E, Y	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal):	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

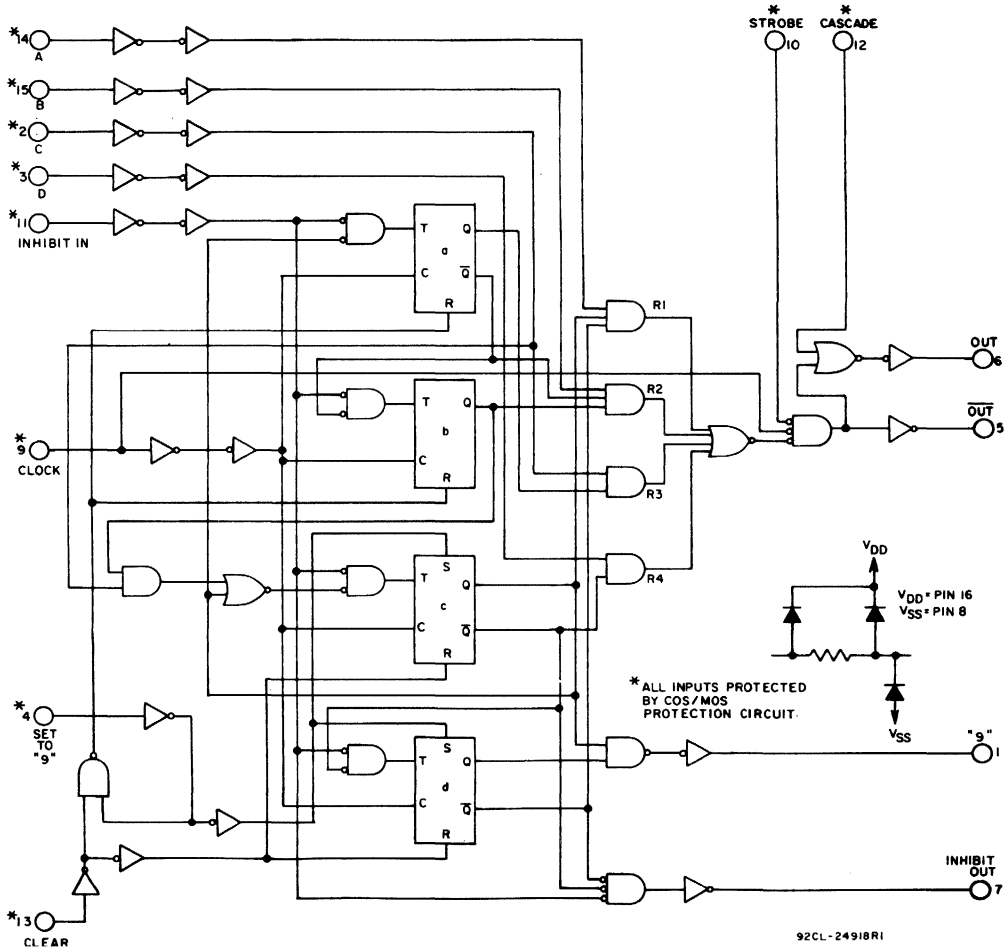


Fig. 1 – Logic diagram.

Preliminary CD4527B Types

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Clock Rise or Fall Time, t_rC_L or t_fCL:	5,10,15	—	15	μs

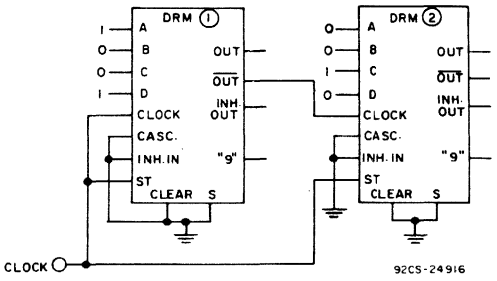


Fig.2 – Two CD4527's cascaded in the "Multiply" mode with a preset number of 36 $\left(\frac{9}{10} \times \frac{4}{10} = \frac{36}{100}\right)$

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic		Conditions			TYP. VALUES	Units
		V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current,	I_L	—	—	5	0.02	μA
		—	—	10	0.02	
		—	—	15	0.02	
		—	—	20	0.04	
Output Voltage: Low-Level,	V_{OL}	—	0,5	5	0	V
		—	0,10	10	0	
		—	0,15	15	0	
High Level,	V_{OH}	—	0,5	5	5	
		—	0,10	10	10	
		—	0,15	15	15	
Noise Immunity: Inputs Low,	V_{NL}	4.2	—	5	2.25	V
		9	—	10	4.5	
		13.5	—	15	6.75	
Inputs High,	V_{NH}	0.8	—	5	2.25	
		1	—	10	4.5	
		1.5	—	15	6.75	
Noise Margin: Inputs Low,	V_{NML}	4.5	—	5	1 Min.	V
		9	—	10	1 Min.	
		13.5	—	15	1 Min.	
Inputs High,	V_{NMH}	0.5	—	5	1 Min.	
		1	—	10	1 Min.	
		1.5	—	15	1 Min.	
Output Drive Current: N-Channel (Sink),	I_DN	0.4	—	5	0.8	mA
		0.5	—	10	1.8	
		1.5	—	15	6	
P-Channel (Source),	I_DP	4.6	—	5	−0.8	
		2.5	—	5	−3.2	
		9.5	—	10	−1.8	
		13.5	—	15	−6	
Input Leakage Current,	I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

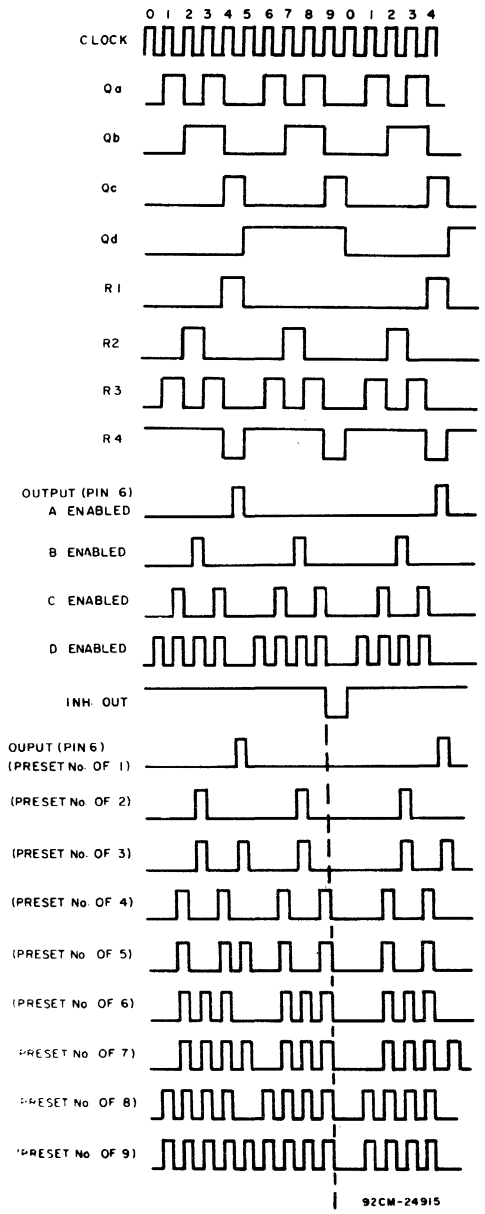


Fig.3 – Timing diagram (See Logic Diagram).

Preliminary CD4527B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Clock to "Out", t_{PHL}, t_{PLH}	5	180	ns
	10	90	
	15	65	
Clock to "Inhibit Out" t_{PHL}, t_{PLH}	5	260	
	10	130	
	15	100	
Transition Time t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Maximum Clock Input Frequency, $f_{CL(Max.)}$	5	2	MHz
	10	4.5	
	15	5.5	

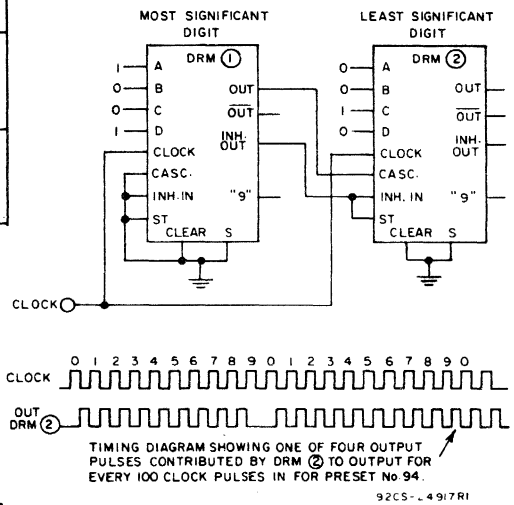


Fig.4 – Two CD4527's cascaded in the "Add" mode with a preset number

$$\text{of } 94\left(\frac{9}{10}+\frac{4}{100}=\frac{94}{100}\right).$$

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

CD4532B Types

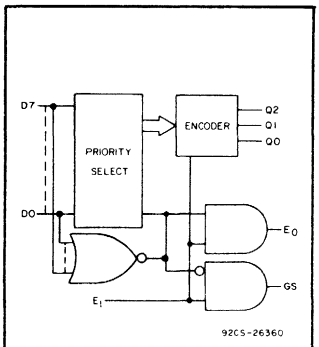
COS/MOS 8-Bit Priority Encoder

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4532 consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority; D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_I is low. When E_I is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_O) is high when no priority inputs are present. If any one input is high, E_O is low and all cascaded lower-order stages are disabled.

The CD4532B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

This device is similar to type MC14532.



CD4532 Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range (for T_A= Full Package Temp. Range)	3	18	V

Features:

- Converts from 1 of 8 to binary
- Provides cascading feature to handle any number of inputs
- Group select indicates one or more priority inputs
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications

- Priority encoder
- Binary or BCD encoder (keyboard encoding)
- Floating point arithmetic

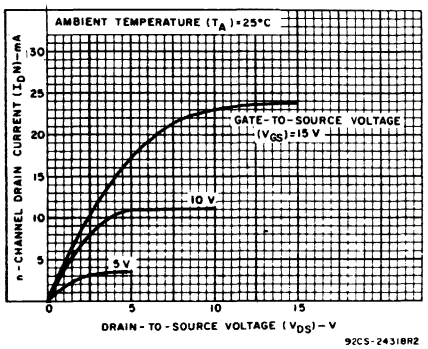


Fig.1 – Typical output-N-channel drain characteristics.

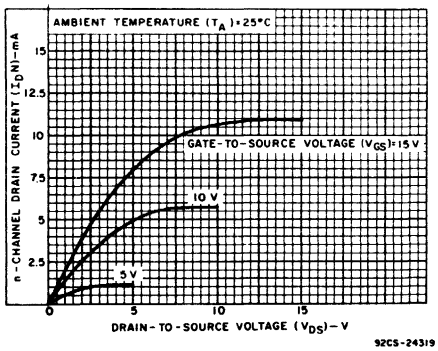


Fig.2 – Minimum output-N-channel drain characteristics.

CD4532B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C) *Values at −55,+25,+125 Apply to D,K,F,H Packages* *Values at −40,+25,+85 Apply to E,Y Packages*							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Voltage: Low-Level, V_{OL} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High Level, V_{OH} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source), I_DP Min.	4.6	–	5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	2.5	–	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	–	10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
	13.5	–	15	−3.3	−3.2	−2.5	−2.2	−3	−6	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

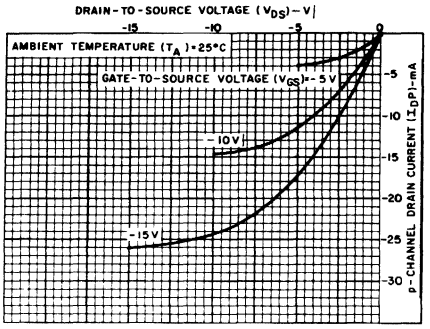


Fig.3 – Typical output-P-channel drain characteristics.

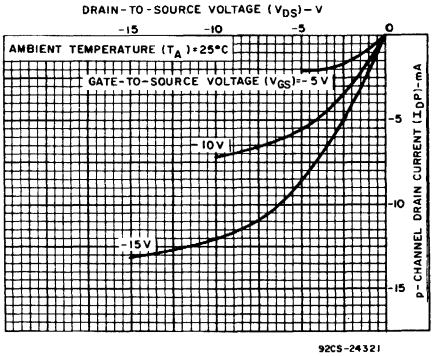


Fig.4 – Minimum output-P-channel drain characteristics.

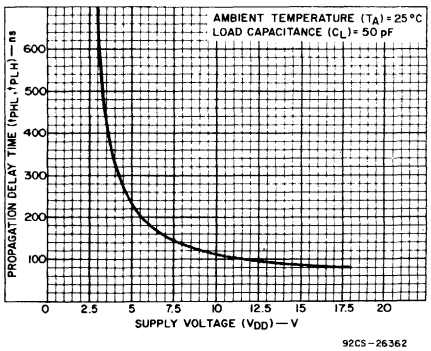


Fig.5 – Typical propagation delay (Dn to Qm) vs. supply voltage

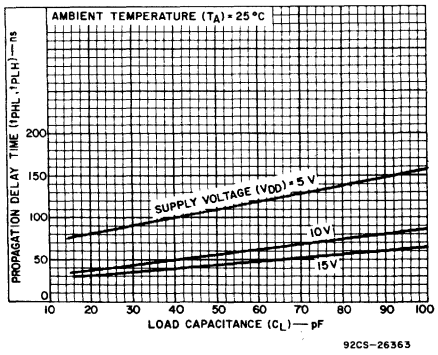


Fig.6 – Typical propagation delay (E_I to GS, E_I to E_O) vs. load capacitance.

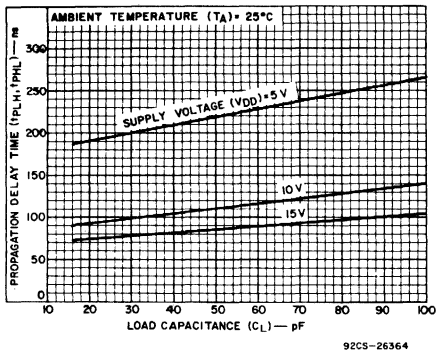


Fig.7 – Typical propagation delay (Dn to Qm) vs. load capacitance.

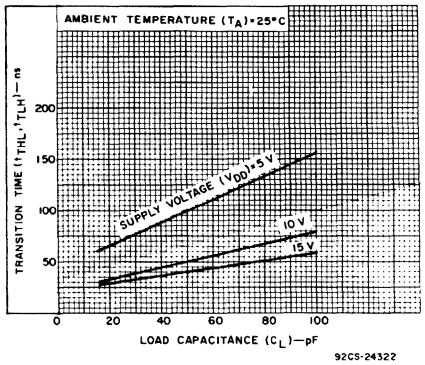


Fig.8 – Typical transition time vs. load capacitance.

CD4532B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; C_L=50 pF, Input t_r,t_f= 20 ns, R_L=200 KΩ

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} VOLTS	LIMITS ALL TYPES TYP.	LIMITS ALL TYPES MAX.	UNITS
Propagation Delay Time: E_I to E_O, E_I to GS *See Fig.8*	t_{PHL}, t_{PLH}	5	110	220	ns
		10	55	110	
		15	45	85	
E_I to Qm, Dn to GS		5	170	340	
		10	85	170	
		15	65	125	
Dn to Q_M *See Figs. 5,7*		5	220	440	
		10	110	220	
		15	85	160	
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Average Input Capacitance	C_I	Any Input	5	–	pF

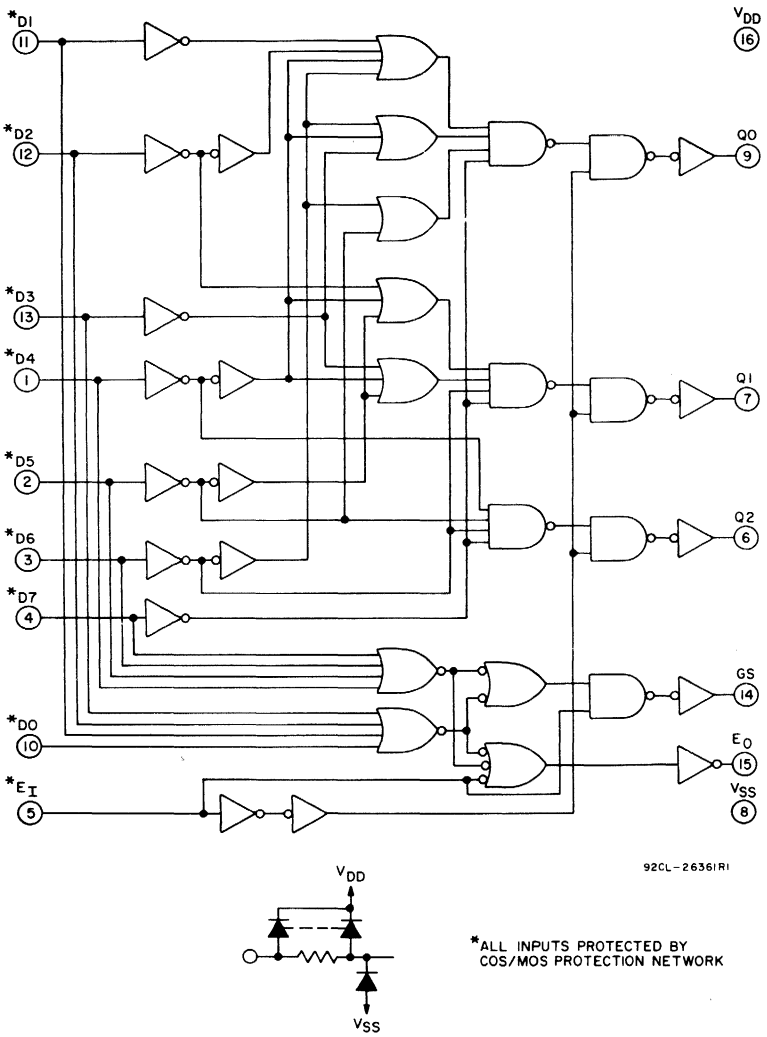


Fig.9 – CD4532 logic diagram.

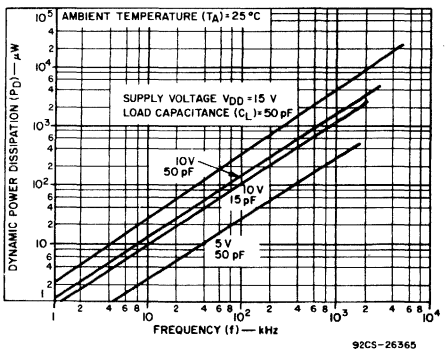


Fig.10 – Typical dynamic power dissipation vs. frequency.

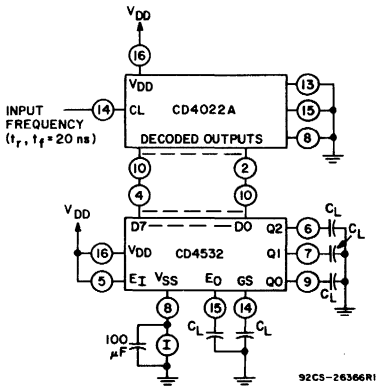


Fig.11 – Dynamic power dissipation test circuit.

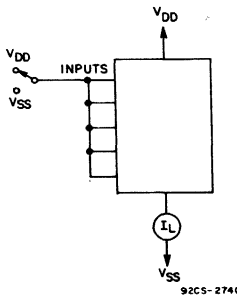


Fig.12 – Quiescent device current test circuit.

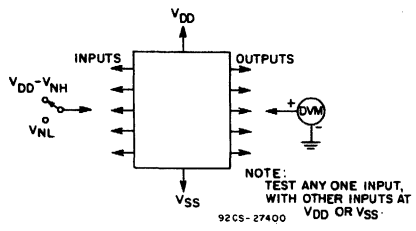


Fig.13 – Noise immunity test circuit.

CD4532B Types

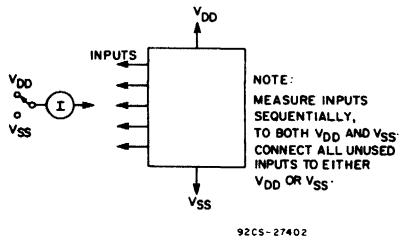


Fig. 14 – Input leakage current test circuit.

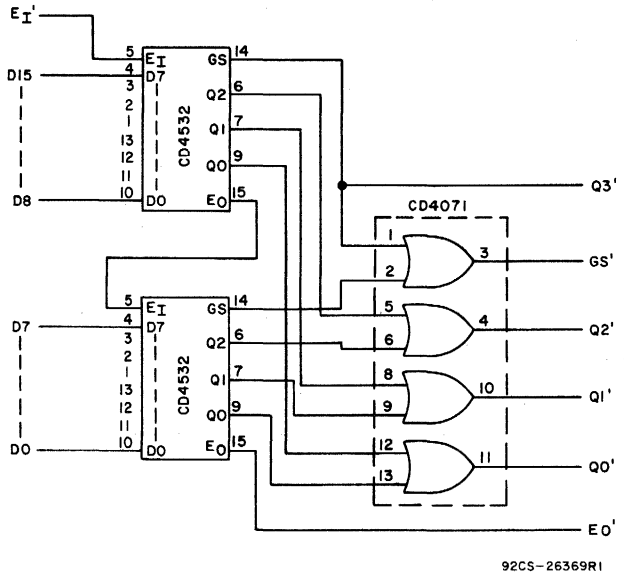
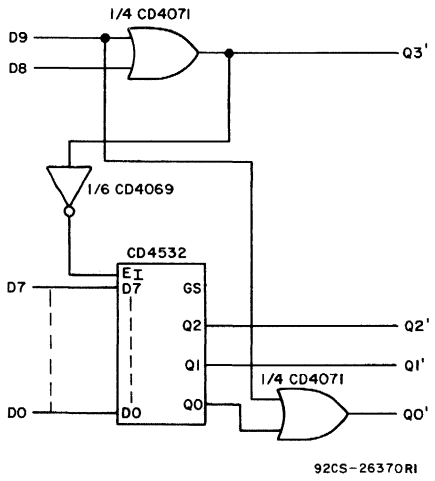


Fig. 15 – 16-level priority encoder.



TRUTH TABLE

Input										Output				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

Fig. 16 – 0-to-9 keyboard encoder.

CD4555B, CD4556B Types

COS/MOS Dual Binary to 1 of 4 Decoder/Demultiplexers

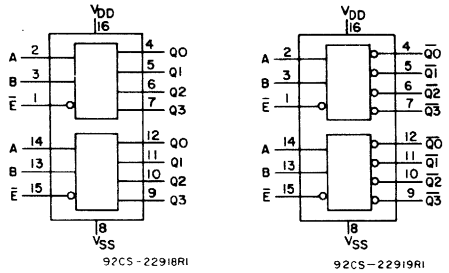
CD4555B: Outputs High on Select
CD4556B: Outputs Low on Select

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD4555B and CD4556B are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the CD4555B the outputs are high on select; on the CD4556B the outputs are low on select.

When the Enable input is high, the outputs of the CD4555B remain low and the outputs of the CD4556B remain high regardless of the state of the select inputs A and B. The CD4555B and CD4556B are similar to types MC14555 and MC14556, respectively.

The CD4555B and CD4556B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4555B CD4556B

FUNCTIONAL DIAGRAMS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (For T_A = Full Package Temp. Range)	–	3	18	V

Features:

- **Expandable with multiple packages**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Decoding**
- **Code conversion**
- **Demultiplexing (using Enable input as a data input)**
- **Memory chip-enable selection**
- **Function selection**

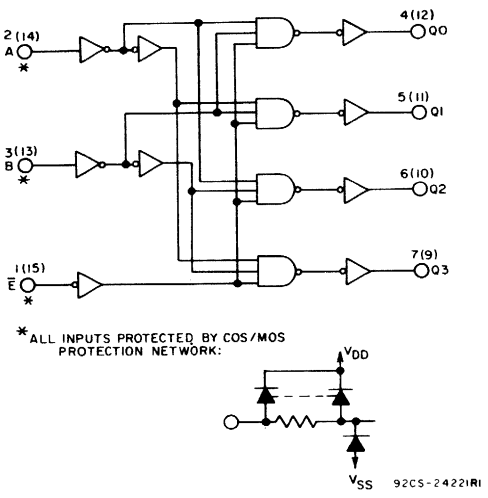


Fig. 1 – CD4555B logic diagram (1 of 2 identical circuits).

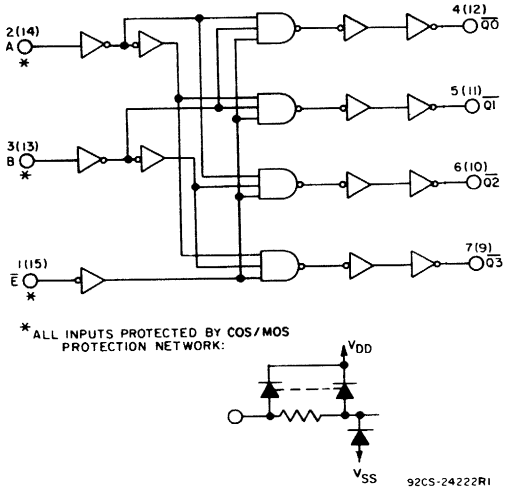


Fig. 2 – CD4556B logic diagram (1 of 2 identical circuits).

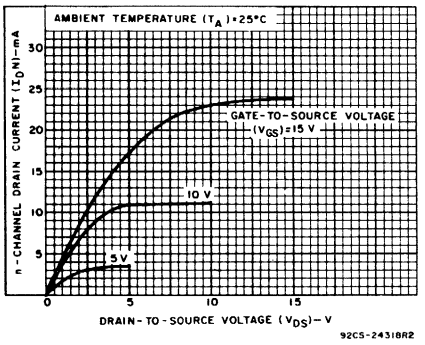


Fig. 3 – Typical output-N-channel drain characteristics.

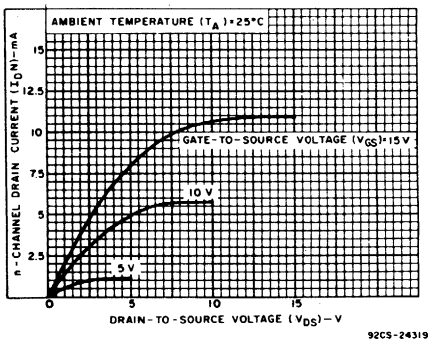


Fig. 4 – Minimum output-N-channel drain characteristics.

CD4555B, CD4556B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, K, F, H Packages Values at -40, +25, +85 Apply to E, Y Packages							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, I_L Max.	–	–	5	5	5	50	100	–	0.02	5	μA
	–	–	10	10	10	100	200	–	0.02	10	
	–	–	15	20	20	200	400	–	0.02	20	
	–	–	20	100	100	1000	2000	–	0.04	100	
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	5	0.5	0.45	0.36	0.3	0.4	0.8	–	mA
	0.5	–	10	1.1	1	0.75	0.65	0.9	1.8	–	
	1.5	–	15	3.3	3.2	2.5	2.2	3	6	–	
P-Channel (Source) I_DP Min.	4.6	–	5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	2.5	–	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	–	10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
	13.5	–	15	-3.3	-3.2	-2.5	-2.2	-3	-6	–	
Output Voltage: Low-Level, V_{OH} Max.	–	0, 5	5	0.05				–	0	0.05	V
	–	0, 10	10	0.05				–	0	0.05	
	–	0, 15	15	0.05				–	0	0.05	
High-Level V_{OL} Min.	–	0, 5	5	4.95				4.95	5	–	
	–	0, 10	10	9.95				9.95	10	–	
	–	0, 15	15	14.95				14.95	15	–	
Noise Immunity: Inputs Low, V_{NL} Min.	4.2	–	5	1.5				1.5	2.25	–	V
	9	–	10	3				3	4.5	–	
	13.5	–	15	4.5				4.5	6.75	–	
Inputs High, V_{NH} Min.	0.8	–	5	1.5				1.5	2.25	–	
	1	–	10	3				3	4.5	–	
	1.5	–	15	4.5				4.5	6.75	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5	–	5	1				1	–	–	V
	9	–	10	1				1	–	–	
	13.5	–	15	1				1	–	–	
Inputs High, V_{NMH} Min.	0.5	–	5	1				1	–	–	
	1	–	10	1				1	–	–	
	1.5	–	15	1				1	–	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		20	±1				–	$\pm 10^{-5}$	±1	μA

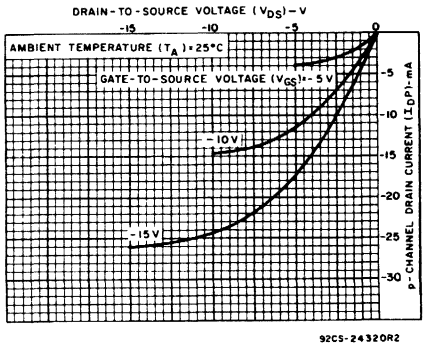


Fig. 5 – Typical output-P-channel drain characteristics.

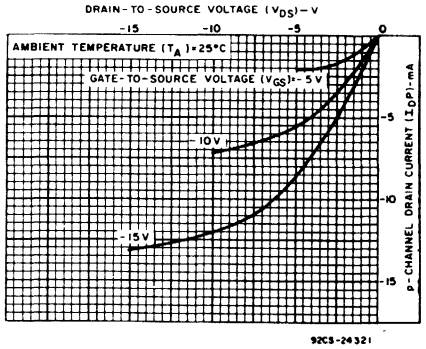


Fig. 6 – Minimum output-P-channel drain characteristics.

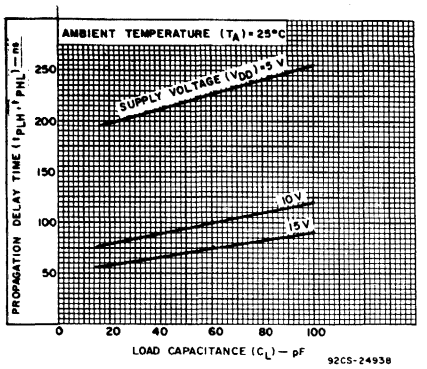


Fig. 7 – Typical propagation delay time vs. load capacitance (A or B input to any output).

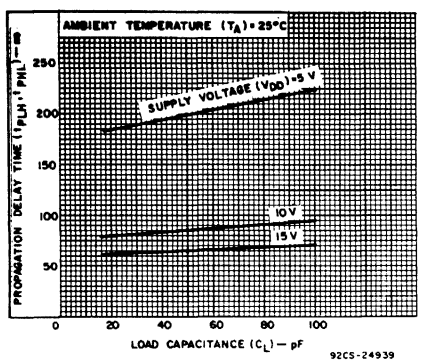


Fig. 8 – Typical propagation delay time vs. load capacitance ($\overline{E}$ input to any output).

TRUTH TABLE

INPUTS ENABLE	INPUTS SELECT		OUTPUTS CD4555B				OUTPUTS CD4556B			
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

CD4555B, CD4556B Types

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
	V_{DD} Volts	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, A or B Input to t_{PHL}, t_{PLH} Any Output t_{PLH}	5	220	440	ns
	10	95	190	
	15	70	140	
$\overline{E}$ Input to Any Output	5	200	400	ns
	10	85	170	
	15	65	130	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Average Input Capacitance, C_L	Any Input	5	—	pF

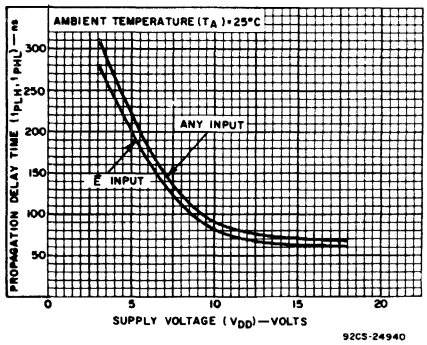


Fig. 9 – Typical propagation delay time vs. supply voltage.

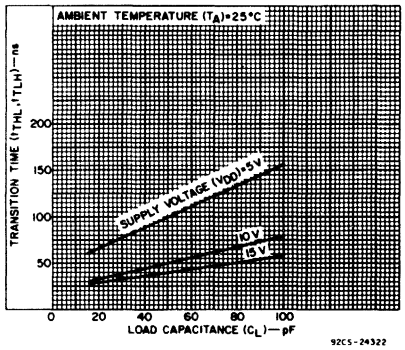
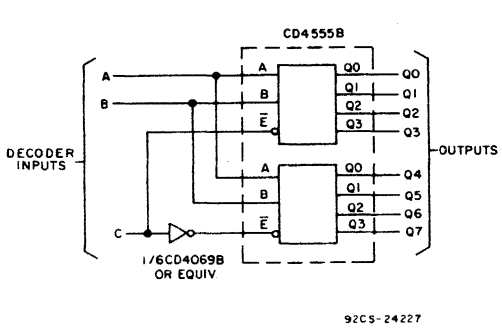


Fig. 10 – Typical transition time vs. load capacitance.



TRUTH TABLE

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 11 – 1-of-8 decoder using CD4555B.

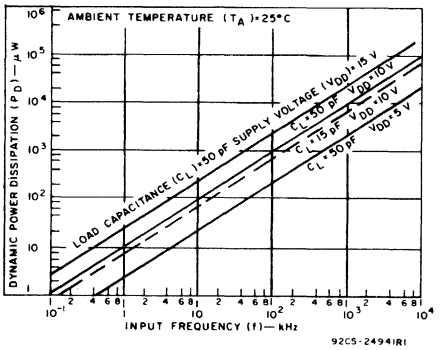
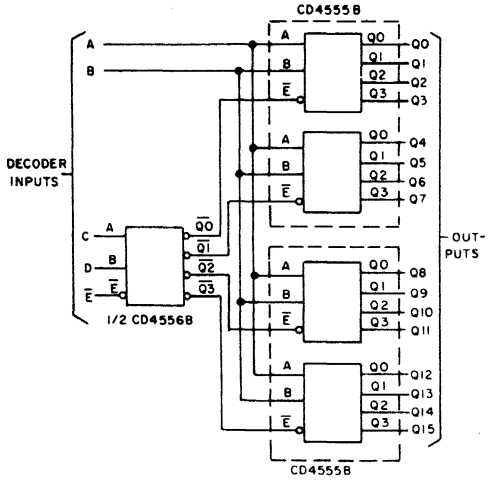


Fig. 12 – Typical dynamic power dissipation vs. frequency.



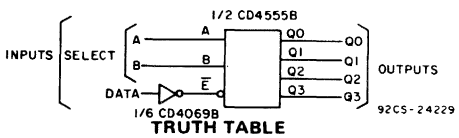
TRUTH TABLE

INPUTS					Q OUTPUTS															
Ē	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

X = don't care

Fig. 13 – 1-of-16 decoder using CD4555B and CD4556B.

APPLICATIONS



TRUTH TABLE

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

Fig. 14 – 1-of-4 line data demultiplexer using CD4555B.

CD4555B, CD4556B Types

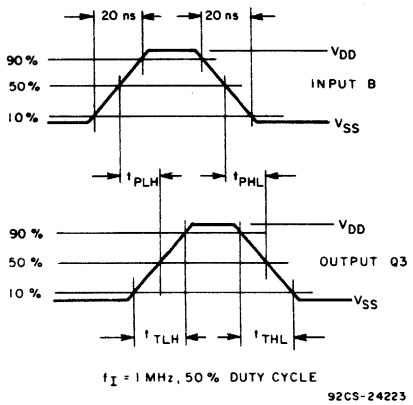


Fig. 15 – CD4555B B input to Q3 output dynamic signal waveforms.

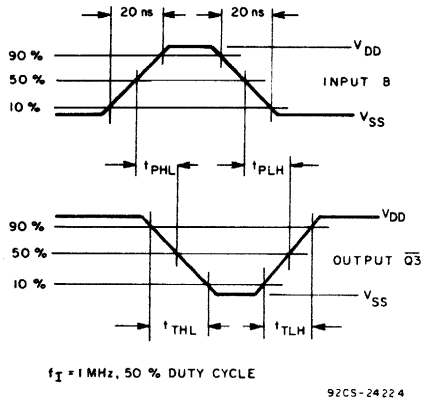


Fig. 16 – CD4556B B input to $\overline{Q3}$ output dynamic signal waveforms.

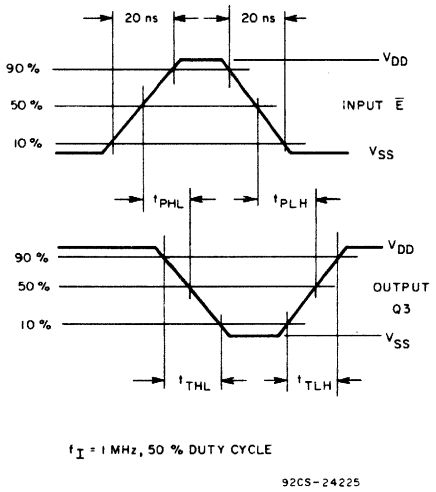


Fig. 17 – CD4555B $\overline{E}$ input to Q3 output dynamic signal waveforms.

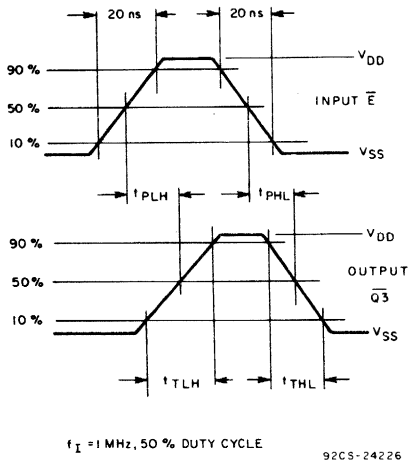


Fig. 18 – CD4556B $\overline{E}$ input to $\overline{Q}_3$ output dynamic signal waveforms.

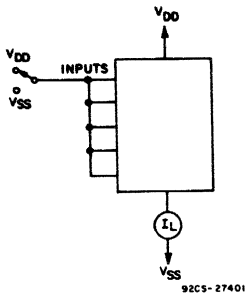


Fig. 19 – Quiescent device current.

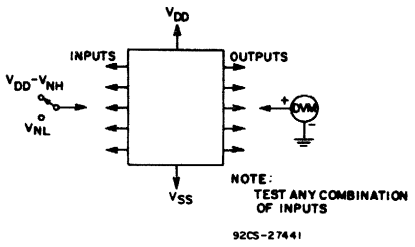


Fig. 20 – Noise immunity.

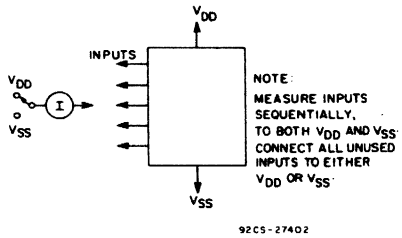


Fig. 21 – Input leakage current.

Preliminary CD40100B Types

COS/MOS 32-Stage Static Left/Right Shift Register

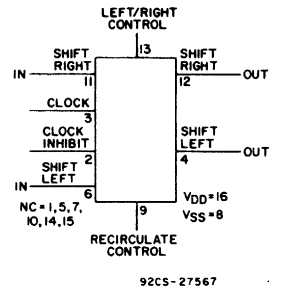
High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD40100B is a 32-stage shift register containing 32 D-type master-slave flip-flops.

The data present at the shift-right input is transferred into the first register stage synchronously with the positive clock edge, provided the left/right control is at a low level, the recirculate control is at a high level, and the clock inhibit is low. If the left/right control is at a high level and the recirculate control is also high, data at the shift-left input is transferred into the 32nd register stage synchronously with the positive clock transition, provided the clock inhibit is low.

Data is shifted one stage left or one stage right depending on the state of the left/right control, synchronously with the positive clock edge. Data clocked into the first or 32nd register stages is available at the appropriate output on the next negative clock transition. No shifting occurs on the positive clock edge if the clock inhibit line is at a high level. With the recirculate control low, data in the 32nd stage is shifted into the first stage when the left/right control is low and from the 1st stage to the 32nd stage when the left/right control is high.

The CD40100B types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD40100B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPES E, Y	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = -40 to +60° C (PACKAGE TYPES E, Y)	500 mW
FOR T_A = +60 to +85° C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125° C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

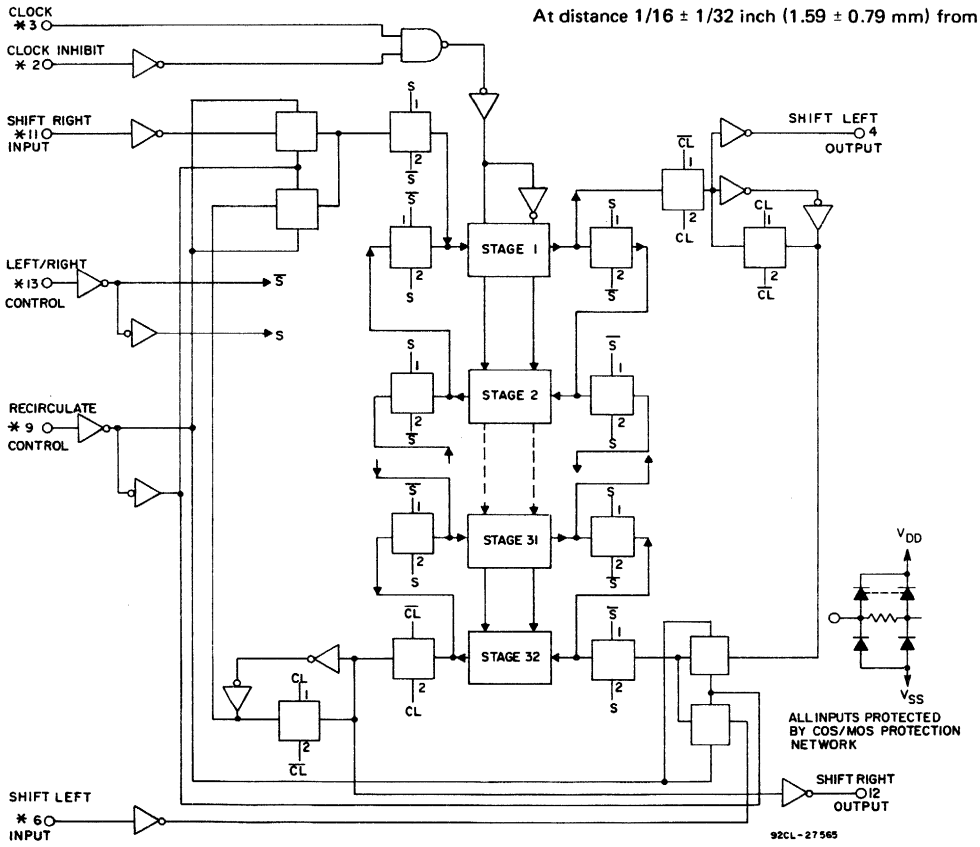


Fig. 1 – Logic diagram.

Features:

- Fully static operation
- Shift left/Shift right capability
- Multiple package cascading
- Recirculate capability
- LIFO or FIFO capability
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Serial shift registers
- Time delay circuits
- Expandable N-bit data storage stack (LIFO operation)

Preliminary CD40100B Types

RECOMMENDED OPERATING CONDITIONS

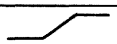
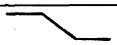
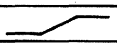
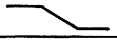
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°$ C; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Clock to Shift Left/Right Output, t_{PLH}, t_{PHL}	5	100	ns
	10	50	
	15	40	
Transition Time, t_{TLH}, t_{THL}	5	100	ns
	10	50	
	15	40	
Minimum Data Setup Time, t_S	5	50	ns
	10	30	
	15	20	
Maximum Clock Input Frequency, f_{CL}	5	2.5	MHz
	10	5	
	15	6	
Minimum Clock Pulse Width, t_W	5	200	ns
	10	100	
	15	80	
Average Input Capacitance, C_I	Any Input	5	pF

INTERNAL STAGE TRUTH TABLE #

CLOCK▲	CLOCK INHIBIT	DATA (D_N)	D_{N+1} (SHIFT RIGHT) D_{N-1} (SHIFT LEFT)
	0	0	0
	0	0	No change
	0	1	1
	0	1	No change
X	1	X	No change

CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift left	Shift left input
1	0	0	Shift left	Stage 1
0	0	1	Shift right	Shift right input
0	0	0	Shift right	Stage 32
X	1	X	No shift	—

0 = Low level
1 = High level
X = Don't care
▲ = Level change
- New data appears at the outputs on negative clock transitions.

Preliminary CD40100B Types

STATIC ELECTRICAL CHARACTERISTICS *at* $T_A = 25°C$

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.	V
	9	–	10	1 Min.	
	13.5	–	15	1 Min.	
Inputs High, V_{NMH}	0.5	–	5	1 Min.	
	1	–	10	1 Min.	
	1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink), I_{DN}	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_{DP}	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

Preliminary CD40101B Types

COS/MOS 9-Bit Parity Generator/Checker

High-Voltage Types (3-to-20-Volt Rating)

Features:

- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

The RCA-CD40101 is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking.

When used as a parity generator a parity bit is supplied along with the data to generate an even or odd parity output.

When used as a parity checker the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

Word length capability is expandable by cascading. The CD40101 is also provided with an inhibit control. If the inhibit control is set at logical "1" the even and odd outputs go to a logical "0".

The CD40101B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

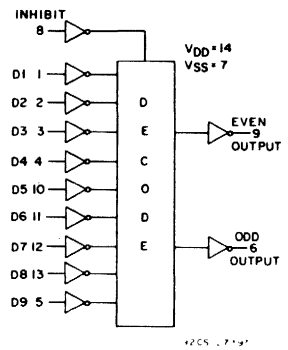


Fig. 1 – CD40101 functional diagram.

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

Truth Table

Inputs		Outputs	
D1-D9	Inhibit	Even	Odd
Σ1's=Even	0	1	0
Σ1's=Odd	0	0	1
X	1	0	0

X = Don't Care
Logic 1 = High
Logic 0 = Low

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES	UNITS
	V_O (V)	V_{DD} (V)		
Quiescent Device Current, I_L Max.	–	5	0.02	μA
	–	10	0.02	
	–	15	0.02	
	–	20	0.04	
Output Drive Current:				mA
N-Channel (Sink),	0.4	5	0.8	
I_DN Min.	0.5	10	1.8	
	1.5	15	6	
P-Channel (Source),	4.6	5	–0.8	
	2.5	5	–3.2	
I_DP Min.	9.5	10	–1.8	
	13.5	15	–6	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES	UNITS
		V_{DD} V		
Data Propagation Delay Time:		5	450	ns
High-to-Low, t_{PHL}		10	160	
		15	125	
Low-to-High, t_{PLH}		5	450	
		10	160	
		15	125	
Inhibit-to-Output Propagation Delay Time:		5	160	
		10	80	
High-to-Low, t_{PHL}		15	50	
Low-to-High, t_{PLH}		5	160	
		10	80	
		15	50	
Transition Time:		5	100	ns
High-to-Low, t_{THL}		10	50	
		15	40	
Low-to-High, t_{TLH}		5	100	
		10	50	
		15	40	
Average Input Capacitance, C_I	Any Input	–	5	pF

Preliminary CD40102B, CD40103B Types

COS/MOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (3-to-20-Volt Rating)
CD40102 — 2-Decade BCD Type
CD40103 — 8-Bit Binary Type

Features:

- Synchronous or asynchronous preset
- Medium-speed operation : f_{CL} = 3.5 MHz (typ.) @ V_{DD} = 10 V
- Cascadable
- Quiescent current specified to 20 V
- Maximum input leakage of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

The RCA-CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102 is configured as two cascaded 4-bit BCD stages, while the CD40103 contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/CLOCK ENABLE (CI/CE) input is high. The CARRY-OUT/ZERO-DETECT (CO/ZD) output goes low when the count reaches zero if the CI/CE input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the CI/CE input. When the ASYNCHRONOUS PRESET-ENABLE (APE) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the SPE, CI/CE, or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102 and a single 8-bit binary word for the CD40103. When the CLEAR (CLR) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102 and 255_{10} for the CD40103) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

The CD40102 and CD40103 may be cascaded using the CI/CE input and the CO/ZD output, in either a synchronous or ripple mode.

The CD40102B and CD40103B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Divide-by-"N" counters
- Programmable timers
- Interrupt timers

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Conditions			Typical Values	Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	—	—	5	0.02	μA
	—	—	10	0.02	
	—	—	15	0.02	
	—	—	20	0.04	
Output Voltage: Low-Level, V_{OL}	—	0,5	5	0	V
	—	0,10	10	0	
	—	0,15	15	0	
High Level, V_{OH}	—	0,5	5	5	
	—	0,10	10	10	
	—	0,15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	—	5	2.25	V
	9	—	10	4.5	
	13.5	—	15	6.75	
Inputs High, V_{NH}	0.8	—	5	2.25	
	1	—	10	4.5	
	1.5	—	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	—	5	1 Min.	V
	9	—	10	1 Min.	
	13.5	—	15	1 Min.	
Inputs High, V_{NMH}	0.5	—	5	1 Min.	
	1	—	10	1 Min.	
	1.5	—	15	1 Min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	—	5	0.8	mA
	0.5	—	10	1.8	
	1.5	—	15	6	
P-Channel (Source), I_DP	4.6	—	5	-0.8	
	2.5	—	5	-3.2	
	9.5	—	10	-1.8	
	13.5	—	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

Preliminary CD40102B, CD40103B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPES E,Y . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E,Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALVES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} CLOCK to CARRY-OUT/ZERO DETECT	5	275	ns
	10	125	
	15	90	
CARRY-IN/CLOCK ENABLE to CARRY-OUT/ZERO DETECT	5	200	ns
	10	90	
	15	65	
Transition Time, t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Setup Time: t_S SYNCHRONOUS PRESET ENABLE,	5	130	ns
	10	60	
	15	45	
JAM Inputs (Synchronous Mode)	5	75	ns
	10	40	
	15	30	
Minimum Pulse Width: t_W CLOCK or ASYNCHRONOUS PRESET ENABLE	5	225	ns
	10	95	
	15	60	
CLEAR	5	150	ns
	10	60	
	15	45	
Maximum Clock Frequency, f_{CL}	5	1.4	MHz
	10	3.5	
	15	4.8	
Input Capacitance, C_I (Any Input)	–	5	pF

TRUTH TABLE

CONTROL INPUTS				MODE	ACTION
CLR	APE	SPE	CI/CE		
1	1	1	1	Synchronous	Inhibit clock
1	1	1	0		Count down
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

Notes:
1. 0 = Low level; 1 = High level; X = Don't care
2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40103 BCD ; MSB = J7, LSB = J0; CD40102 Binary ; MSD = J7, J6, J5, J4; LSD = J3, J2, J1, J0

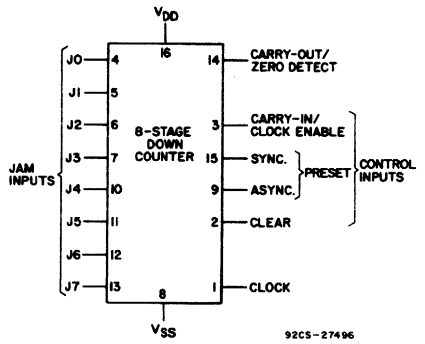


Fig. 1 – CD40102B, CD40103B functional diagram.

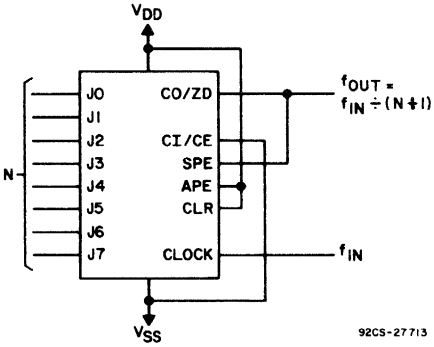


Fig. 2 – Divide-by-"N" counter.

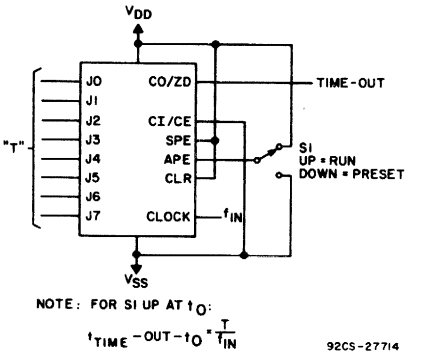


Fig. 3 – Programmable timer.

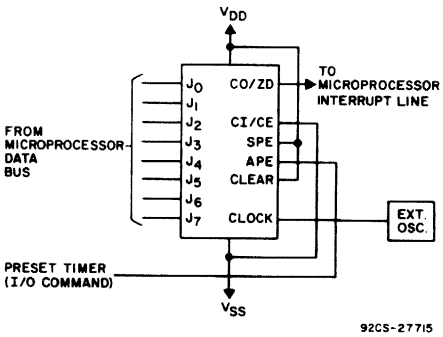


Fig. 4 – Microprocessor interrupt timer.

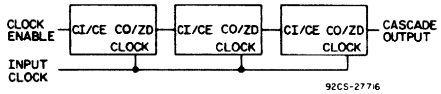


Fig. 5 – Synchronous cascading.

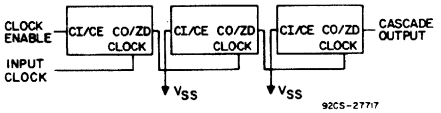


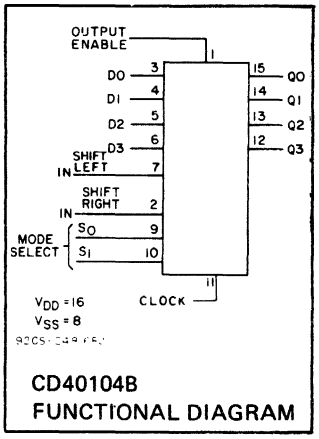
Fig. 6 – Ripple cascading.

Preliminary CD40104B Types

COS/MOS 4-Bit Bidirectional Universal Register

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.



CD40104B
FUNCTIONAL DIAGRAM

CONTROL TRUTH TABLE

CLOCK▲	MODE S_0	SELECT S_1	OUTPUT ENABLE	ACTION
⎍	0	0	1	Reset
⎍	1	0	1	Shift right (Q_0 toward Q_3)
⎍	0	1	1	Shift left (Q_3 toward Q_0)
⎍	1	1	1	Parallel load
X	X	X	0	Outputs assume high impedance

1 = High level
0 = Low level
X = Don't care
▲ = Level change

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°$ C; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Clock to Q t_{PHL}, t_{PLH}	5 10 15	375 150 110	ns
3-State Output 1 or 0 to High Impedance (Note) t_{PHZ}, t_{PLZ}	5 10 15	120 50 40	ns
3-State Output High Impedance to 1 or 0 (Note) t_{PZH}, t_{PZL}	5 10 15	150 60 45	ns
Output Transition Time t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Minimum Setup Time: D0, D3, Shift-Right In, Shift-Left In, to Clock t_S	5 10 15	60 25 20	ns
Select 0, Select 1 to Clock t_S	5 10 15	170 70 50	ns
Minimum Hold Time: D0, D3, Shift-Right In, Shift-Left In, Select 0, Select 1 to Clock t_H	5 10 15	0 0 0	ns
Minimum Clock Pulse Width t_W	5 10 15	85 35 25	ns
Maximum Clock Input Frequency f_{CL}	5 10 15	4 9 12	MHz
Average Input Capacitance C_I	Any Input	5	pF

NOTE: Measured at the point of 10% change in output with an output load of 50 pF, R_L = 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1 kΩ to V_{SS} for t_{PZH}, t_{PHZ}.

Features:

- **Medium speed operation—f_{CL} = 9 MHz (typ.) at V_{DD} = 10 V**
- **Fully static operation**
- **Synchronous parallel or serial operation**
- **Three-state outputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20-V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **Standard symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**

The RCA-CD40104B is a universal register featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems.

In the parallel-load mode, data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right and shift-left serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. The mode controls should be changed only when the clock input is low. When the output enable input is low, all outputs assume the high impedance state.

The CD40109B types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Preliminary CD40104B Types

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C.*

CHARACTERISTIC	CONDITIONS			TYP. VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 min.	V
	9	–	10	1 min.	
	13.5	–	15	1 min.	
Inputs High, V_{NMH}	0.5	–	5	1 min.	
	1	–	10	1 min.	
	1.5	–	15	1 min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current I_{OL}, I_{OH}	Forced (Output Disabled)				
	0, 20	–	20	$\pm 10^{-4}$	μA

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V

Applications:

- **Arithmetic unit bus registers**
- **Serial/parallel conversions**
- **General-purpose register for bus-organized systems**

Preliminary CD40105B Types

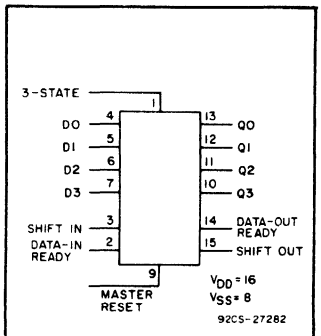
COS/MOS FIFO Register

4-Bit Wide X 16-Bit Long

High-Voltage Types (3-to-20-Volt Rating)

Features:

- **Independent asynchronous inputs and outputs**
- **3-state outputs** ■ **Expandable in either direction**
- **Status indicators on input and output** ■ **Reset capability**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**



CD40105
Functional Diagram

The RCA-CD40105 is a low-power 4-bit-wide-by-16-bit-long first-in-first-out (FIFO) register whose 4 X 16 data register is under constant control of a logic network. Each word position in the array is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse, transferring data from the preceding four data latches into its own four data latches and resetting the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data — Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a high level on the SHIFT-IN (SI) input. This input must go low momentarily before the next nibble (4-bits) of data is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Unloading Data — As soon as the first data have rippled to the output, DATA-OUT READY (DOR) goes high, and data can be removed by a falling edge on the SI input. This falling edge causes the DOR signal to go low while the word on the output is dumped and the next word moves to the output. As long as valid data are available in the FIFO, the DOR signal will go high again signifying that the next nibble of data is ready at the output. When the FIFO is empty, DOR will remain low, and any further commands will be ignored until a "1" marker ripples down to the last control register, when DOR goes high. Unloading of data is inhibited while the 3-state control input is high.

Cascading — The CD40105 can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. For words wider than 4 bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (See Figs. 2 and 3).

3-State Outputs — In order to facilitate data busing, 3-state outputs are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output.

Master Reset — A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first nibble of data is loaded.

Applications:

- **Bit rate smoothing**
- **CPU/terminal buffering**
- **Data communications**
- **Peripheral buffering**
- **Line printer input buffers**
- **Auto dialers**
- **CRT buffer memories**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPES E, Y ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): ..... −0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	70	–	ns
	10	35	–	
	15	25	–	
Shift-In or Shift-Out Rate	5	dc	1.5	MHz
	10	dc	3	
	15	dc	4	
Shift-In or Shift-Out Pulse Width, t_W	5	200	–	ns
	10	80	–	
	15	60	–	
Master Reset Pulse Width, t_W	5	160	–	ns
	10	80	–	
	15	60	–	
Shift-In or Shift-Out Rise or Fall Time, t_r or t_f:	5,10,15	–	15	μs

Preliminary CD40105B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{DD} (V)	Typ. Values	Units
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2		5	2.25	V
	9		10	4.5	
	13.5		15	6.75	
Inputs High, V_{NH}	0.8		5	2.25	
	1		10	4.5	
	1.5		15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5		5	1 min.	V
	9		10	1 min.	
	13.5		15	1 min.	
Inputs High, V_{NMH}	0.5		5	1 min.	
	1		10	1 min.	
	1.5		15	1 min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	−0.8	
	2.5	–	5	−3.2	
	9.5	–	10	−1.8	
	13.5	–	15	−6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current I_{OL}, I_{OH}	Forced (Output Disabled) 0, 20	–	20	$\pm 10^{-4}$	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{DD} Volts	ALL TYPES TYPICAL VALUES	UNITS
Transition Time	T_{TLH}, T_{THL}	5	100	ns
		10	50	
		15	50	
Ripple-Through Delay, Input to Output		5	2	μs
		10	1	
		15	0.7	
Max. Shift-In or Shift-Out Rate		5	3	MHz
		10	6	
		15	8	
Minimum Data Setup Time	t_s	5	35	ns
		10	20	
		15	15	
Min. Shift-Out or Shift-In Pulse Width		5	100	ns
		10	40	
		15	30	
Max. Shift-Out or Shift-In Rise and Fall Time		5	15	μs
		10	15	
		15	15	
Propagation Delay Time: Reset-to-Output Ready	T_{PHL}	5	90	ns
		10	45	
		15	35	
Shift-In-to-Input Ready	T_{PHL}	5	240	ns
		10	120	
		15	90	
Shift-Out-to-Output Ready	T_{PHL}	5	120	ns
		10	60	
		15	45	
3-State-to-Data Out (Turn-on)		5	100	ns
		10	50	
		15	40	
Min. Master Reset Pulse Width	t_W	5	80	ns
		10	40	
		15	30	
Input Capacitance	C_I	Any Input	5	pF

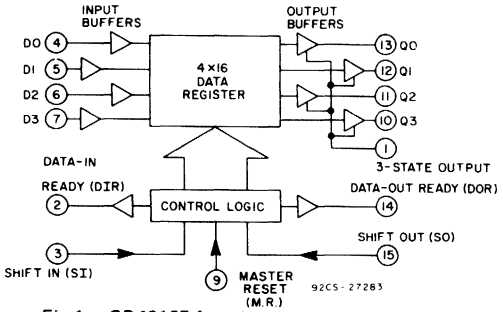


Fig.1 – CD40105 functional block diagram.

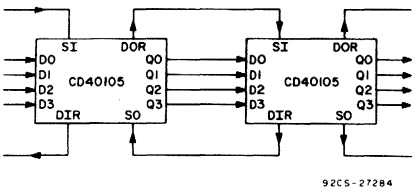


Fig.2 – Expansion, 4-bits-wide-by-N-bits long.

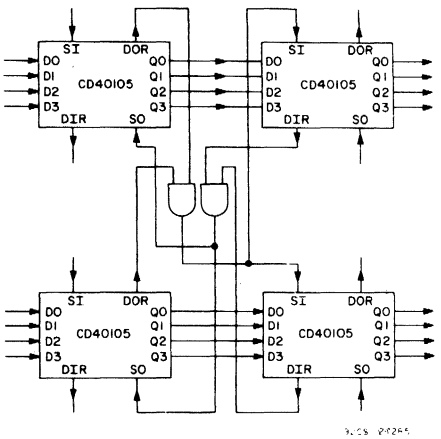


Fig.3 – Expansion, 8-bits-wide-by-N-bits long.

Preliminary CD40107B Types

COS/MOS Dual 2-Input NAND Buffer/Driver

For Use In Relay, Lamp, Light-Emitting Diode, Or Line Driver Applications

High-Voltage Type (3-to-20-Volt Rating)

The RCA-CD40107BE is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (120 mA typ. at V_{DD} = 10 V, V_{DS} = 1 V). The CD40107BE is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package.

Truth Table

A	B	C*, F*
0	0	1
1	0	1
0	1	1
1	1	0

*Requires external pull-up resistor (R_L) to V_{DD}.

Features:

- **32 times standard B-Series output current drive sinking capability — 120 mA typ. @ V_{DD} = 10 V, V_{DS} = 1 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20 V (full-package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{STG}) . . . −65 to +125°C

OPERATING-TEMPERATURE RANGE (T_A) . . . −40 to +85°C

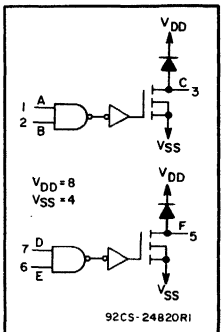
DC SUPPLY-VOLTAGE RANGE (V_{DD})
(Voltages referenced to V_{SS} terminal): . . . . −0.5 to 20 V

POWER DISSIPATION PER PACKAGE:
For T_A = −40 to +60°C . . . . . 500 mW
For T_A = +60 to +85°C derate linearly at 12 mW/°C to 200 mW

POWER DISSIPATION PER OUTPUT BUFFER:
For T_A = −40 to +60°C . . . . . 250 mW
For T_A = +60 to +85°C . derate linearly at 6 mW/°C to 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. . . . . +265°C



Functional Diagram

OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	Min.	Max.	Units
Supply Voltage Range: (T_A=Full Package Temp. Range)	3	18	V

STATIC CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS V_O Volts	TEST CONDITIONS V_{DD} Volts	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L	–	5	0.01	μA
	–	10	0.01	
	–	15	0.01	
	–	20	0.02	
Output Drive Current:	0.4	5	28	mA
	1	5	60	
N-Channel (Sink), I_DN	0.5	10	64	
	1	10	120	
	0.5	15	88	
P-Channel (Source), I_DP	No Internal Pull-Up Device			

DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, C_L = 50 pF, Input t_r, t_f = 20 ns

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	TYPICAL VALUES	UNITS
Propagation Delay: High-to-Low t_{PHL}	R_L=120Ω	5	100	ns
		10	40	
		15	30	
Low-to-High t_{PLH}	R_L=120Ω	5	100	ns
		10	60	
		15	50	
Transition Time: High-to-Low t_{THL}	R_L=120Ω	5	40	ns
		10	20	
		15	10	
Low-to-High t_{TLH}	R_L=120Ω	5	40	ns
		10	35	
		15	20	
Average Input Capacitance C_I	Any Input		5	pF

Special Considerations

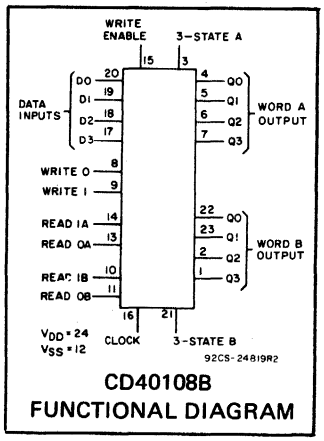
1. Limiting capacitive currents for CL > 500 pF, V_{DD} > 15 V.
   For V_{DD} > 15 V, and load capacitance (C_L) from output to ground > 500 pF, an external 25 Ω series limiting resistor should be inserted between the output terminal and C_L. No external resistor is necessary if C_L < 500 pF or V_{DD} < 15 V.
2. Forward biasing of output diodes.
   Diodes from output to V_{DD} are constructed for electrostatic protection only. To prevent excessive diode current flow in applications where these diodes may become forward biased (i.e. turning off inductive loads), these diodes must be shunted with a switching diode with low dynamic resistance, capable of conducting ⩾ 10 mA at V_F = 1 V, such as the 1N4154.

Preliminary CD40108B Types

COS/MOS 4x4 Multiport Register

The RCA-CD40108B is a 4X4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.



CD40108B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, K, H . . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60° C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85° C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100° C (PACKAGE TYPES D, K) . . . . . 500 mW

FOR T_A = +100 to +125° C (PACKAGE TYPES D, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

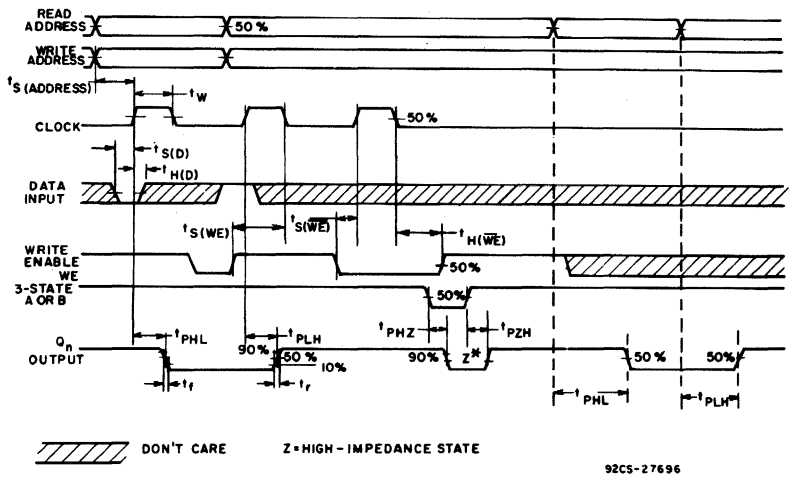
LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	STATE A	STATE B	D_n 1	Q_{nA} 1	Q_{nB} 1
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
⎍⎍	1	S1	S2	S1	S2	S1	S2	1	1	X	Z	Z
X	X	X	X	X	X	X	X	0	0			
⎍⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
⎍⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out

1 = HIGH LEVEL; 0 = LOW LEVEL; X = DON'T CARE; Z= HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0



* For measurement of 3-state propagation delay of HIGH IMPEDANCE to 1 or 0, connect R_L = 1 kΩ to V_{DD} or V_{SS} respectively.

Fig. 1 — Timing diagram.

Features:

- **Four 4-bit registers**
- **One input and two output buses**
- **Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers**
- **Three-state outputs**
- **Unlimited expansion in bit and word directions**
- **Data lines have latched inputs**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **Standard symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Scratch-pad memories**
- **Arithmetic units**
- **Data storage**

Preliminary CD40108B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25°$ C; Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ KΩ*

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Read Address or Clock to Q	5	375	ns
	10	150	
	15	110	
3-State Propagation Delay Time:* High Impedance to 1 or 0 t_{PZH}, t_{PZL}	5	150	ns
	10	60	
	15	45	
1 or 0 to High Impedance t_{PHZ}, t_{PLZ}	5	150	ns
	10	60	
	15	45	
Output Transition Time: t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Minimum Setup Time: Write Enable to $\overline{\text{Clock}}$ $t_{S(WE)}$	5	125	ns
	10	50	
	15	35	
$\overline{\text{Write Enable}}$ to Clock $t_{S(\overline{WE})}$	5	0	ns
	10	0	
	15	0	
Address to Clock $t_{S(ADDR)}$	5	125	ns
	10	50	
	15	35	
Data to Clock $t_{S(D)}$	5	0	ns
	10	0	
	15	0	
Minimum Hold Time: Data to Clock $t_{H(D)}$	5	100	ns
	10	40	
	15	30	
$\overline{\text{Clock}}$ to $\overline{\text{Write Enable}}$ $t_{H(\overline{WE})}$	5	-50	ns
	10	-20	
	15	-15	
Maximum Clock Input Frequency, f_{CL}	5	3	MHz
	10	7	
	15	9	
Minimum Clock Pulse Width, t_W	5	150	ns
	10	60	
	15	45	
Average Input Capacitance, (Any Input) C_I	–	5	pF

* Measured at the point of 10% change at the output with $R_L = 1$ kΩ to V_{DD} for t_{PLZ}, t_{PZL}, and $R_L = 1$ kΩ to V_{SS} for t_{PHZ}, t_{PZH}.

Preliminary CD40108B Types

STATIC ELECTRICAL CHARACTERISTICS *at* $T_A = 25°$ C

CHARACTERISTICS	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 min.	V
	9	–	10	1 min.	
	13.5	–	15	1 min.	
Inputs High, V_{NMH}	0.5	–	5	1 min.	
	1	–	10	1 min.	
	1.5	–	15	1 min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	15	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current, I_{OL}, I_{OH}	0, 20	Forced (Output Disabled) –	20	$\pm 10^{-4}$	μA

Preliminary CD40109B Types
COS/MOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}.

The RCA-CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

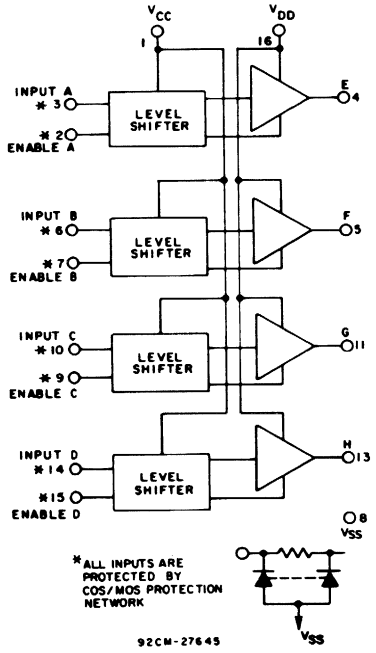
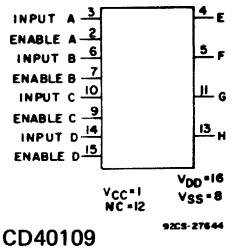


Fig. 1 – Functional block diagram for CD40109.



CD40109
FUNCTIONAL DIAGRAM

Features:

- **Independence of power supply sequence V_{CC} can exceed V_{DD}, input signals can exceed both V_{CC} and V_{DD}**
- **Up and down level-shifting capability**
- **Three-state outputs with separate enable controls**
- **Quiescent current specified to 20 V**
- **Maximum input leakage current of 1 μA at 20 V (full-package-temperature range)**
- **Standard symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Low quiescent power dissipation**

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C*

CHARACTERISTIC	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{CC}, V_{DD} (V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L	–	–	5	0.01	μA
	–	–	10	0.01	
	–	–	15	0.01	
	–	–	20	0.02	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source) I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current I_{OL}, I_{OH}	Forced (Output Disabled)		20	$\pm 10^{-4}$	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

Preliminary CD40109B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . .Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . .Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to +20 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Data Propagation Delay Time: High-to-Low Level, t_{PHL}	5	10	300	ns
	5	15	240	
	10	15	200	
Low-to-High Level, t_{PLH}	5	10	115	ns
	5	15	100	
	10	15	70	
Output Enable Propagation Delay Times: Output High to High Impedance, t_{PHZ}	5	10	60	ns
	5	15	50	
	10	15	40	
Output Low to High Impedance, t_{PLZ}	5	10	375	ns
	5	15	275	
	10	15	240	
High Impedance to Output High, t_{PZH}	5	10	325	ns
	5	15	225	
	10	15	185	
High Impedance to Output Low, t_{PZL}	5	10	110	ns
	5	15	90	
	10	15	50	
Transition Times, t_{THL}, t_{TLH}	5	10	50	ns
	5	15	40	
	10	15	40	
Average Input Capacitance, C_I	Any Input		5	pF

TRUTH TABLE

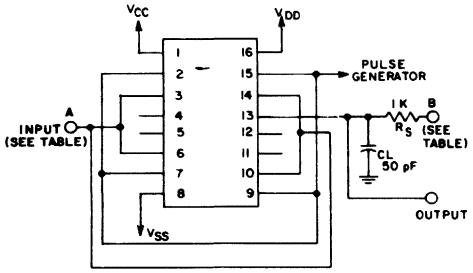
MODE	INPUTS A, B, C, D	INPUTS ENABLE A, B, C, D	OUTPUTS E, F, G, H
Low-to-high level shift	0	1	0
	1	1	1
	X	0	Z

LOGIC 0 = LOW(V_{SS}) X = DON'T CARE Z = HIGH IMPEDANCE

LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

Applications:

- **High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing**
- **Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations**



CHAR.	TEST VOLTAGE AT A	TEST VOLTAGE AT B
t_{PHZ}	V_{CC}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{CC}	V_{SS}

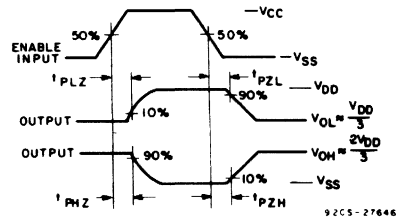


Fig. 2 – Output enable delay times test circuit and waveforms.

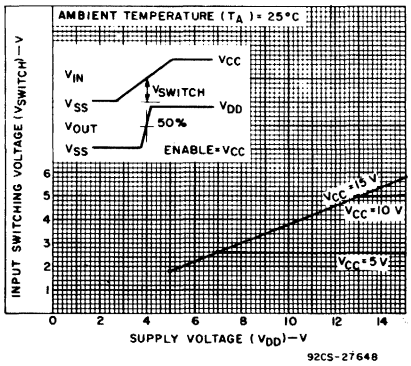


Fig. 3 – Input switching voltage vs. high-level supply voltage.

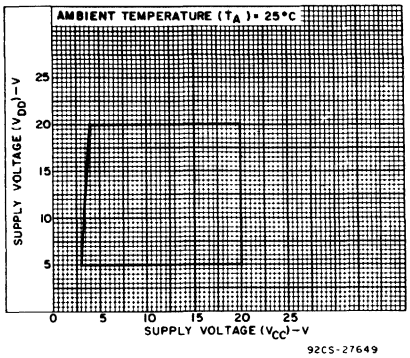


Fig. 4 – High-level supply voltage vs. low-level supply voltage.

Preliminary CD40181B Types

COS/MOS 4-Bit Arithmetic Logic Unit

High-Voltage Types (3-to-20-Volt Rating)

For **MAXIMUM RATINGS** see "Ratings and Characteristics" at the beginning of the COS/MOS section.

The RCA-CD40181B is a low-power four-bit parallel arithmetic logic unit (ALU) capable of providing 16 binary arithmetic operations on two four-bit words and 16 logical functions of two Boolean variables. The mode control input M selects logical (M = High) or arithmetic (M = Low) operation. The four select inputs (S0, S1, S2, and S3) select the desired logical or arithmetic functions, which include AND, OR, NAND, NOR, and exclusive–OR and–NOR in the logic mode, and addition, subtraction, decrement, left-shift and straight transfer in the arithmetic mode, according to the truth table. The CD40181B operation may be interpreted with either active-low or active-high data at the A and B word inputs and the function outputs F, by using the appropriate truth table.

The CD40181B contains logic for full look-ahead carry operation for fast carry generation using the carry-generate and carry-propagate outputs $\overline{G}$ and $\overline{P}$ for the four bits of the CD40181B. Use of the CD40182B look-ahead carry generator in conjunction with multiple CD40181B'S permits high-speed arithmetic operations on long words. A ripple carry output C_{n+4} is available for use in systems where speed is not of primary importance.

Also included in the CD40181B is a comparator output A = B, which assumes a high level whenever the two four-bit input words A and B are equal and the device is in the subtract mode. In addition, relative magnitude information may be derived from the carry-in input C_n and ripple carry-out output C_{n+4} by placing the unit in the subtract mode and externally decoding using the information in Figure 5.

The CD40181B types are supplied in hermetic ceramic 24-lead dual-in-line packages (D suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40181B is similar to industry type MC14581.

Features:

- **Full look-ahead carry for high-speed operations on long words**
- **Generates 16 logic functions of two Boolean variables**
- **Generates 16 arithmetic functions of two 4-bit binary words**
- **A = B comparator output available**
- **Ripple-carry input and output available**
- **Typical addition time: 200 ns @ V_{DD} = 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Parallel arithmetic units**
- **Process controllers**
- **Low-power minicomputers**

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

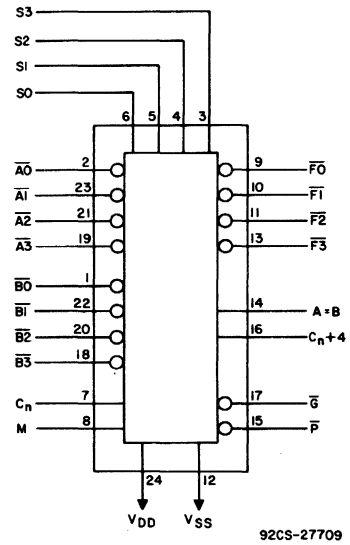


Fig. 2 – Block diagram (active-low data)

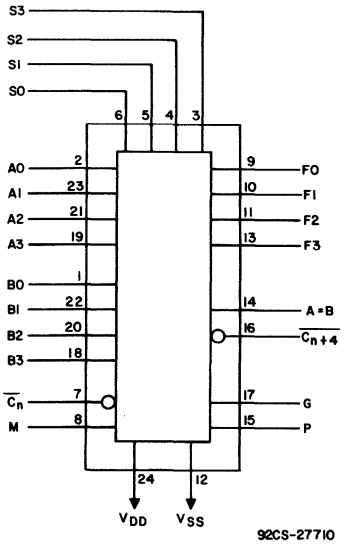


Fig. 3 – Block diagram (active-high data)

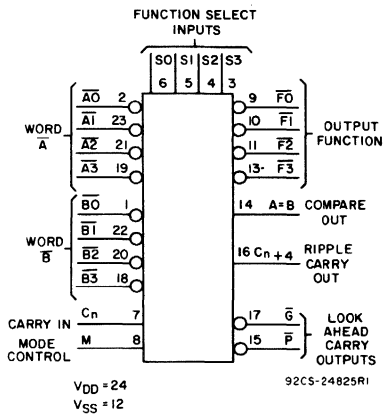


Fig. 1 – Functional block diagram (active-low data)

Preliminary CD40181B Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0,5	5	0	V
	–	0,10	10	0	
	–	0,15	15	0	
High-Level, V_{OH}	–	0,5	5	5	
	–	0,10	10	10	
	–	0,15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.	V
	9	–	10	1 Min.	
	13.5	–	15	1 Min.	
Inputs High, V_{NMH}	0.5	–	5	1 Min.	
	1	–	10	1 Min.	
	1.5	–	15	1 Min.	
Output Drive: Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

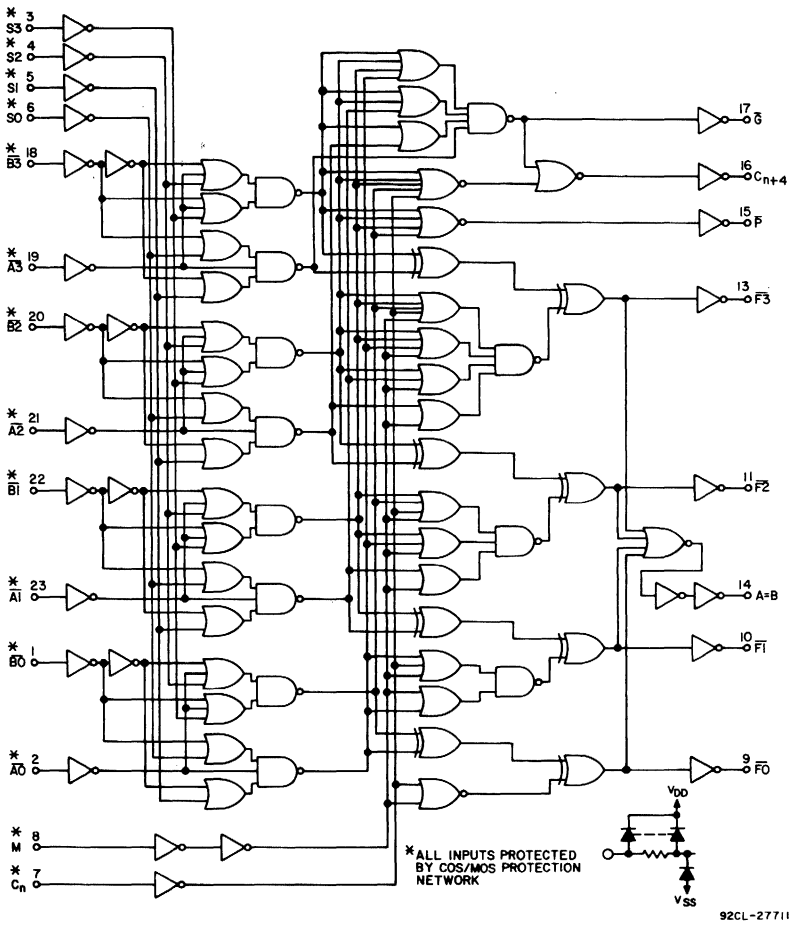


Fig. 4 – CD40181B logic diagram (active-low data)

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;

Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} A or B to F, $\overline{G}$ or $\overline{P}$	5	450	ns
	10	175	
	15	140	
A or B to C_{n+4} or A=B; A or B to F (logic mode),	5	550	ns
	10	220	
	15	170	
C_n to F or C_{n+4},	5	250	ns
	10	100	
	15	80	
Transition Time: t_{THL}, t_{TLH}	5	100	
	10	50	
	15	40	
Average Input Capacitance, C_I (Any Input)	–	5	pF

Preliminary CD40181B Types

TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION (M = H)	ARITHMETIC* FUNCTION (M = L, C_n = L)	LOGIC FUNCTION (M = H)	ARITHMETIC* FUNCTION (M = L, $\overline{C_n}$ = H)
S3	S2	S1	S0				
0	0	0	0	$\overline{A}$	A minus 1	$\overline{A}$	A
0	0	0	1	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
0	0	1	0	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{A}B$	$A+\overline{B}$
0	0	1	1	Logic 1	minus 1	Logic 0	minus 1
0	1	0	0	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
0	1	0	1	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
0	1	1	0	$A \oplus B$	A minus B minus 1	$A \oplus B$	A minus B minus 1
0	1	1	1	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
1	0	0	0	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
1	0	0	1	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
1	0	1	0	B	$A\overline{B}$ plus (A + B)	B	$(A+\overline{B})$ plus AB
1	0	1	1	A + B	A + B	AB	$A\overline{B}$ minus 1
1	1	0	0	Logic 0	A plus A	Logic 1	A plus A
1	1	0	1	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
1	1	1	0	AB	$A\overline{B}$ plus A	A + B	$(A+\overline{B})$ plus A
1	1	1	1	A	A	A	A minus 1

* Expressed as two's complement

1 = HIGH LEVEL
0 = LOW LEVEL

ACTIVE – HIGH DATA				ACTIVE – LOW DATA		
INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE		INPUT C_n	OUTPUT C_{n+4}	MAGNITUDE
1	1	$A \leqslant B$		0	0	$A \leqslant B$
0	1	$A < B$		1	0	$A < B$
1	0	$A > B$		0	1	$A > B$
0	0	$A \geqslant B$		1	1	$A \geqslant B$

1 = HIGH LEVEL
0 = LOW LEVEL

Fig. 5 – Use of C_n and C_{n+4} for magnitude comparison.

Preliminary CD40182B Types

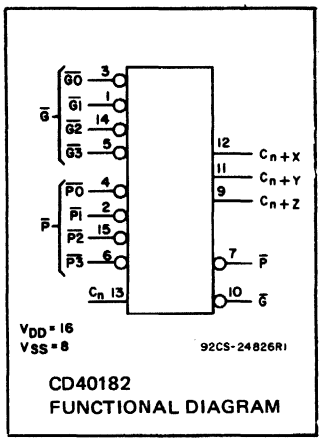
COS/MOS Look-Ahead Carry Generator

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD40182B is a high-speed look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The CD40182 is cascadable to perform full look-ahead across n-bit adders. Carry, propagate-carry, and generate-carry functions are provided as enumerated in the terminal designation table.

The CD40182, when used in conjunction with the CD40181 arithmetic logic unit (ALU), provides full high-speed look-ahead carry capability for up to n-bit words. Each CD40182 generates the look-ahead (anticipated carry) across a group of four ALU's. In addition, other CD40182's may be employed to anticipate the carry across sections of four look-ahead blocks up to n-bits. Carry inputs and outputs of the CD40181 are active-high logic, and carry-generate (G) and carry-propagate (P) outputs are active-low. Therefore the inputs and outputs of the CD40182 are compatible.

The CD40182B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD40182
FUNCTIONAL DIAGRAM

The CD40182B is similar to industry type MC14582.

Features:

- **Generates high-speeed carry across four adders or adder groups**
- **High-speed operation:**
  $t_{PHL} = t_{PLH}$ = 120 ns (typ.) @ V_{DD} = 10 V
- **Cascadable for fast carries over N bits**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **High-speed parallel arithmetic units**
- **Multi-level look-ahead carry generation for long word lengths**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H. . . . . -55 to +125°C

PACKAGE TYPES E, Y . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K). . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES). . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS
At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} P, G In to P, G Out and Carry Outs	5	300	ns
	10	120	
	15	90	
C_n to Carry Outs	5	400	ns
	10	160	
	15	125	
Transition Time: t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Input Capacitance, C_I (Any Input)	—	5	pF

TERMINAL DESIGNATIONS

DESIGNATION	TERM.	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3, 1, 14, 5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4, 2, 15, 6	Active-Low Carry-Propagate Inputs
C_n	13	Active-High Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Active-High Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

Preliminary CD40182B Types

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C.*

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 min.	V
	9	–	10	1 min.	
	13.5	–	15	1 min.	
Inputs High, V_{NMH}	0.5	–	5	1 min.	
	1	–	10	1 min.	
	1.5	–	15	1 min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

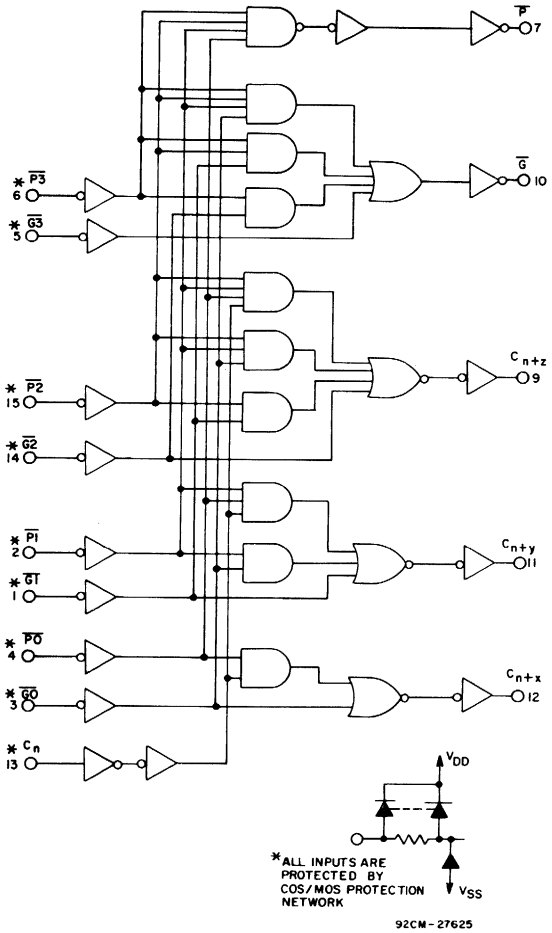


Fig. 1 – CD40182 logic diagram.

CD40182 Logic Equations:

$$C_{n+x} = G0 + P0 \cdot C_n$$

$$C_{n+y} = G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C_n$$

$$C_{n+z} = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C_n$$

$$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

$$\overline{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$$

Preliminary CD40192B, CD40193B Types

COS/MOS Presettable Up/Down Counters (Dual Clock with Reset)

High-Voltage Types (3-to-20-Volt Rating)
CD40192 – BCD Type CD40193 – Binary Type

The RCA-CD40192B Presettable BCD Up/Down Counter and the CD40193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as counters. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN inputs and a master RESET. Four buffered Q signal outputs as well as CARRY and BORROW outputs for multiple-stage counting schemes are provided.

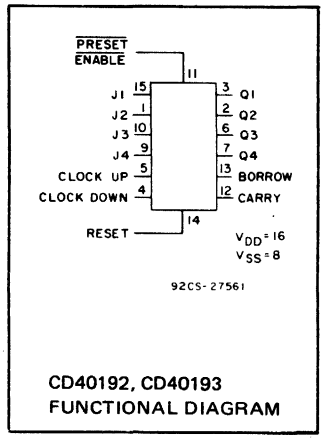
The counter can be cleared so that all outputs are in a low state by a high on the RESET line. A RESET can be accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

Both the CARRY and BORROW signals are normally high. The CARRY signal goes low when the counter reaches its maximum count in the count-up mode. The BORROW signal goes low when the counter reaches its minimum count in the count-down mode.

Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the BORROW and CARRY outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD40192, CD40193
FUNCTIONAL DIAGRAM

Features:

- **Individual clock lines for counting up or counting down**
- **Synchronous high-speed carry and borrow propagation delays for cascading**
- **Reset and Preset capability**
- **Medium-speed operation—f_{CL} = 7 MHz (typ.) @ 10 V**
- **Quiescent current specified to 20 V**
- **Maximum input leakage of 1 μA at 20 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**
- **5-V, 10-V, and 15-V parametric ratings**

Applications:

- **Up/down difference counting**
- **Multistage ripple counting**
- **Synchronous frequency dividers**
- **A/D and D/A conversion**
- **Programmable binary or BCD counting**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
  PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
  FOR T_A = -40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
⌐	1	1	0	COUNT UP
¬	1	1	0	NO COUNT
1	⌐	1	0	COUNT DOWN
1	¬	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE

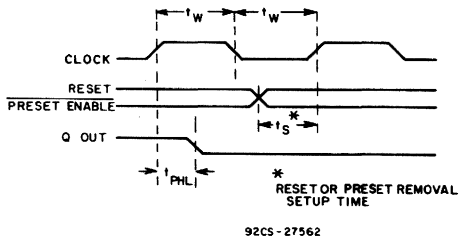


Fig. 1 – Timing diagram.

Preliminary CD40192B, CD40193B Types

RECOMMENDED OPERATING CONDITIONS *For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C*

CHARACTERISTIC	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.	V
	9	–	10	1 Min.	
	13.5	–	15	1 Min.	
Inputs High, V_{NMH}	0.5	–	5	1 Min.	
	1	–	10	1 Min.	
	1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink), I_DN	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_DP	4.6	–	5	–0.8	
	2.5	–	5	–3.2	
	9.5	–	10	–1.8	
	13.5	–	15	–6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200KΩ*

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUE	UNIT
Transition Time; t_{THL}, t_{TLH}	5	100	ns
	10	50	
	15	40	
Propagation Delay Time:	5	200	ns
t_{PHL}, t_{PLH}	10	100	
CLOCK UP or CLOCK DOWN to Q	15	80	
CLOCK UP or CLOCK DOWN	5	150	ns
to	10	75	
BORROW or CARRY	15	60	
	5	200	ns
RESET or $\overline{\text{PRESET}}$ to Q	10	100	
	15	80	
RESET or PRESET	5	280	ns
to	10	140	
BORROW or CARRY	15	110	
Minimum RESET,	5	175	ns
$\overline{\text{PRESET}}$, or CLOCK	10	70	
Pulse Width, t_W	15	60	
Maximum CLOCK	5	3	MHz
Input Frequency, f_{CL}	10	7	
	15	8	
Minimum RESET or $\overline{\text{PRESET}}$	5	150	ns
$\overline{\text{ENABLE}}$ Removal	10	80	
Setup Time*, t_S	15	60	
Input Capacitance, C_I (Any Input)	–	5	pF

* The time required for RESET or $\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$ control to be removed before clocking.

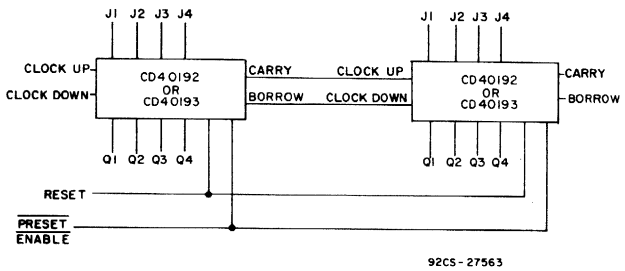


Fig. 2 – Cascaded counter packages.

Preliminary CD40194B Types

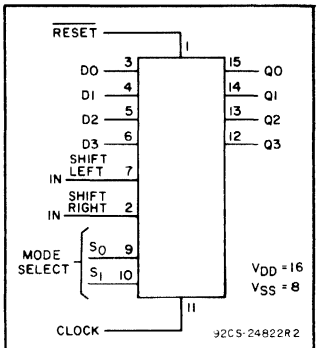
COS/MOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD40194B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. The mode controls should be changed only when the CLOCK input is low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low.

The CD40194B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40194 is similar to industry type 340194.



CD40194B
FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ*

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: t_{PLH}, t_{PHL} Clock to Q	5	375	ns
	10	150	
	15	110	
$\overline{\text{RESET}}$ to Q, t_{PHL}	5	375	ns
	10	150	
	15	110	
Output Transition Time t_{TLH}, t_{THL}	5	100	ns
	10	50	
	15	40	
Minimum Setup Time: t_S D0, D1, D2, D3, SR, SL to Clock	5	60	ns
	10	25	
	15	20	
S0, S1 to Clock	5	170	ns
	10	70	
	15	50	
Minimum Hold Time: t_H D0, D1, D2, D3, SR, SL, S0, S1 to Clock	5	0	ns
	10	0	
	15	0	
Minimum Pulse Width: t_W Clock	5	85	ns
	10	35	
	15	25	
$\overline{\text{RESET}}$	5	160	ns
	10	65	
	15	45	
Maximum Clock Input Frequency, f_{CL}	5	4	MHz
	10	9	
	15	12	
Average Input Capacitance, C_I (Any Input)	–	5	pF

Features:

- Medium-speed operation: f_{CL} = 9 MHz (typ.) @ V_{DD} = 10 V
- Fully static operation
- Synchronous parallel or serial operation
- Asynchronous master reset
- Quiescent current specified to 20 V
- Maximum input leakage current of 1 μA at 20 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-V, 10-V, and 15-V parametric ratings

Applications:

- Arithmetic unit registers
- Serial/parallel conversions
- General-purpose registers

TRUTH TABLE

CL	S0	S1	$\overline{\text{RESET}}$	ACTION
X	0	0	1	Do-Nothing
⎍	1	0	1	Shift Right (Q0 toward Q3)
⎍	0	1	1	Shift Left (Q3 toward Q0)
⎍	1	1	1	Parallel Load
X	X	X	0	Reset

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE

Preliminary CD40194B Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPES E, Y . . . . . -40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60° C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85° C (PACKAGE TYPES E, Y) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 25°C*

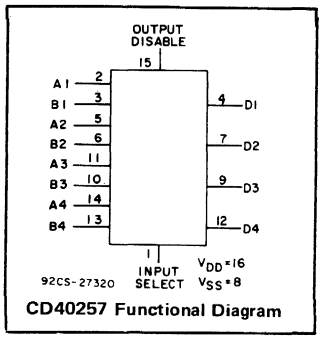
CHARACTERISTIC	CONDITIONS			TYPICAL VALUES	UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current, I_L	–	–	5	0.02	μA
	–	–	10	0.02	
	–	–	15	0.02	
	–	–	20	0.04	
Output Voltage: Low-Level V_{OL}	–	0, 5	5	0	V
	–	0, 10	10	0	
	–	0, 15	15	0	
High-Level, V_{OH}	–	0, 5	5	5	
	–	0, 10	10	10	
	–	0, 15	15	15	
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2.25	V
	9	–	10	4.5	
	13.5	–	15	6.75	
Inputs High, V_{NH}	0.8	–	5	2.25	
	1	–	10	4.5	
	1.5	–	15	6.75	
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.	V
	9	–	10	1 Min.	
	13.5	–	15	1 Min.	
Inputs High, V_{NMH}	0.5	–	5	1 Min.	
	1	–	10	1 Min.	
	1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink), I_{DN}	0.4	–	5	0.8	mA
	0.5	–	10	1.8	
	1.5	–	15	6	
P-Channel (Source), I_{DP}	4.6	–	5	-0.8	
	2.5	–	5	-3.2	
	9.5	–	10	-1.8	
	13.5	–	15	-6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA

Preliminary CD40257B Types
COS/MOS Quad 2-Line-to-1-Line Data Selector/Multiplexer

High-Voltage Types (3-to-20-Volt Rating)

The RCA-CD40257B is a Data Selector/Multiplexer featuring three-state outputs which can interface directly with and drive data lines of bus-oriented systems.

The CD40257B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, and Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD40257 Functional Diagram

Features:

- 3-State outputs
- Quiescent current specified to 20 V
- Maximum input leakage current of 1 μA at 20 V (full-package-temperature range)
- 1 V noise margin (full package-temperature range)
- 5-V, 10-V and 15-V parametric ratings

Applications:

- Digital Multiplexing
- Shift-right/shift-left registers
- True/complement selection

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPES E, Y . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = −40 to +60°C (PACKAGE TYPES E, Y) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPES E, Y) . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER QUTPUT TRANSISTOR
FOR T_A = FULL-PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package - Temperature Range)	3	18	V

TRUTH TABLE

INPUTS				OUTPUT
3-STATE OUTPUT DISABLE	SELECT	A	B	D
1	X	X	X	Z
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

X = DON'T CARE LOGIC 1 = HIGH
LOGIC 0 = LOW Z = HIGH IMPEDANCE

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time: Data Input to Output, t_{PHL}, t_{PLH}		5	130	ns
		10	60	
		15	40	
Select to Output, t_{PHL}, t_{PLH}		5	160	ns
		10	70	
		15	50	
Output Disable to Output, t_{PHL}, t_{PLH}		5	95	ns
		10	45	
		15	35	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	35	
Input Capacitance, C_I	Any Input	—	5	pF

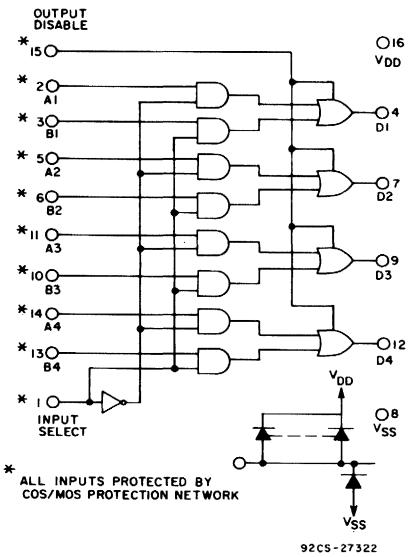


Fig. 1 – Logic diagram for CD40257B.

Preliminary CD40257B Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic		Conditions			TYP. VALUES	Units
		V_O (V)	V_{IN} (V)	V_{DD} (V)		
Quiescent Device Current:	I_L	–	–	5	0.02	μA
		–	–	10	0.02	
		–	–	15	0.02	
		–	–	20	0.04	
Output Voltage: Low-Level,	V_{OL}	–	0,5	5	0	V
		–	0,10	10	0	
		–	0,15	15	0	
High Level,	V_{OH}	–	0,5	5	5	
		–	0,10	10	10	
		–	0,15	15	15	
Noise Immunity: Inputs Low,	V_{NL}	4.2	–	5	2.25	V
		9	–	10	4.5	
		13.5	–	15	6.75	
Inputs High,	V_{NH}	0.8	–	5	2.25	
		1	–	10	4.5	
		1.5	–	15	6.75	
Noise Margin: Inputs Low,	V_{NML}	4.5	–	5	1 Min.	V
		9	–	10	1 Min.	
		13.5	–	15	1 Min.	
Inputs High,	V_{NMH}	0.5	–	5	1 Min.	
		1	–	10	1 Min.	
		1.5	–	15	1 Min.	
Output Drive Current: N-Channel (Sink),	I_DN	0.4	–	5	0.8	mA
		0.5	–	10	1.8	
		1.5	–	15	6	
P-Channel (Source),	I_DP	4.6	–	5	–0.8	
		2.5	–	5	–3.2	
		9.5	–	10	–1.8	
		13.5	–	15	–6	
Input Leakage Current,	I_{IL}, I_{IH}	Any Input		20	$\pm 10^{-5}$	μA
3-State Output Leakage Current:	I_{OL}, I_{OH}	Forced (Output Disabled)				μA
		0,20	–	20	$\pm 10^{-4}$	

Memory Integrated Circuits

Classification Charts

Type No.	Organization	Operation	No. of Pins	Access Time (ns-max)	Power Supply (V)	Operating Power (mW-typ)	Comments
CMOS Memories							
CD4036AD	4 x 8	static	24	400	10	6	CMOS I/O, decoded
CD4036AK	4 x 8	static	24	400	10	6	
CD4039AD	4 x 8	static	24	400	10	6	CMOS I/O, direct address
CD4039AK	4 x 8	static	24	400	10	6	
CD4061AD	256 x 1	static	16	380	10	40	CMOS input, 3-state output
CD4061AH	256 x 1	static	—	380	10	40	
■CD40024D	32 x 8	static	18				
■CD40032D	512 x 8	ROM	24	400 typ	10	20	mask-programmable
■CD40032E	512 x 8	ROM	24	400 typ	10	20	
CD40061E	256 x 1	static	16	300 typ	5	25	CMOS input, 3-state output
CD40061AD	256 x 1	static	16	150 typ	10	100	
CD40061AE	256 x 1	static	16	150 typ	10	100	
NMOS Memories							
MW4050D	4096 x 1	dynamic	18	300	12, −5	420	
MW4050DV1	4096 x 1	dynamic	18	250	12, −5	420	open-drain output
MW4050DV2	4096 x 1	dynamic	18	200	12, −5	420	
■MW4051D	4096 x 1	dynamic	18	300	12, −5	460	
■MW4051DV1	4096 x 1	dynamic	18	250	12, −5	460	TTL clock, open-drain output
■MW4051DV2	4096 x 1	dynamic	18	200	12, −5	460	
MW4060D	4096 x 1	dynamic	22	300	12, ±5	400	
MW4060DV1	4096 x 1	dynamic	22	250	12, ±5	400	3-state output, chip select
MW4060DV2	4096 x 1	dynamic	22	200	12, ±5	400	
■MW4101D	256 x 4	static	22	400	5	125	
■MW4101DV1	256 x 4	static	22	300	5	125	
■MW4101DV2	256 x 4	static	22	250	5	125	
■MW4104D	4096 x 1	dynamic	16	350	12, ±5	380	
■MW4104DV1	4096 x 1	dynamic	16	300	12, ±5	380	
■MW4104DV2	4096 x 1	dynamic	16	250	12, ±5	380	
■MW4111D	256 x 4	static	18	400	5	125	
■MW4111DV1	256 x 4	static	18	300	5	125	
■MW4111DV2	256 x 4	static	18	250	5	125	
■MW4112D	256 x 4	static	16	400	5	125	
■MW4112DV1	256 x 4	static	16	300	5	125	
■MW4112DV2	256 x 4	static	16	250	5	125	
MW7001ID	1024 x 1	static	22	60	15, 8, −3	360	differential output, charge pump
SOS Memories							
MWS5001D	1024 x 1	static	16	150 typ	5	4	3-state output
■MWS5001AD	1024 x 1	static	16	80 typ	5	6	
MWS5040D	256 x 4	static	22	150 typ	5	4	3-state output
■MWS5040AD	256 x 4	static	22	80 typ	5	6	
■MWS5080D	128 x 8	static	24	150 typ	5	4	
■MWS5114D	1024 x 4	static	18	175 typ	5	25	
MWS5501D	1024 x 1	static	16	90 typ	10	20	3-state output
MWS5540D	256 x 4	static	22	90 typ	10	20	3-state output

■To be announced

Replacement Guide

Industry Type No.	RCA Direct Replacement	RCA Pin-Compatible Types
Advanced Micro Devices		
AM2101	■MW4101	MWS5040, MWS5540
AM9050	MW4050	
AM9060	MW4060	
AM9101	■MW4101	MWS5040, MWS5540
AM9111	■MW4111	
AM9112	■MW4112	
American Microsystems, Inc.		
S4021	MW4060	
S4096	■MW4104	
S5101		MWS5040, MWS5540, MW4101■
S6810		MWS5080■
Advanced Memory Systems		
AMS5001		MWS5001
AMS7001I	MW7001I	
AMS7101	■MW4101	MWS5040, MWS5540
AMS7111	■MW4111	
AMS7112	■MW4112	
AMS7280	MW4060	
Cambridge Memories		
3701		MW7001I
Fairchild Semiconductor		
34720		CD4061, CD40061
93415		MWS5001, MWS5501
93425		MWS5001, MWS5501
Harris Electronics		
HM7640		CD40032■
Intersil		
IM6508		MWS5001, MWS5501
Intel		
2101	■MW4101	MWS5040, MWS5540
2104	■MW4104	
2107	MW4060	
2111	■MW4111	
2112	■MW4112	
2115		MWS5001, MWS5501
2125		MWS5001, MWS5501
2704		CD40032■
3604		CD40032■
5101		MW4101■, MWS5040, MWS5540

■To be announced

Industry Type No.	RCA Direct Replacement	RCA Pin-Compatible Types
Monolithic Memories, Inc.		
6340		CD40032■
Mostek		
MK4027	■MW4104	
MK4096		MW4104■
Motorola		
MCM6604	■MW4104	
MCM6810		MWS5080■
MCM7001I	MW7001I	
National Semiconductor		
MM2101	■MW4101	MWS5040, MWS5540
MM2111	■MW4111	
MM2112	■MW4112	
MM5280	MW4060	
Nippon Electric Co.		
μPB2205		MWS5001, MWS5501
μPD411	MW4060	
Nortek		
7001I	MW7001I	
Signetics		
2604	MW4060	
93415		MWS5001, MWS5501
82S08		MWS5001, MWS5501
82S11		MWS5001, MWS5501
Solitron		
CM4036	CD4036	
CM4039	CD4039	
Synertek		
SY2101	■MW4101	MWS5040, MWS5540
SY2111	■MW4111	
SY2112	■MW4112	
SY5101		MW4101■, MWS5040, MWS5540
SY5280	MW4060	
Texas Instruments		
TMS2101	■MW4101	MWS5040, MWS5540
TMS4050	MW4050	MW4051■
TMS4051	■MW4051	MW4050
TMS4060	MW4060	
TMS7001I	MW7001I	
Toshiba		
TC4061	CD4061	CD40061

CD4036A, CD4039A Types

COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

Binary Addressing — CD4036AD, CD4036AK
Direct Word-Line Addressing — CD4039AD, CD4039AK

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (See Fig.15). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (See Fig.4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-Oring multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig.5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

Special Features:

- **COS/MOS logic compatibility at all input and output terminals**
- **Memory bit expansion**
- **Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines**
- **Memory bypass capability for all bits**
- **Buffering on all outputs**
- **CD4036A- on-chip binary address decoding, separate READ INHIBIT and WRITE controls**
- **Access Time—200 ns(Typ) at V_{DD}=10 V**
- **CD4039A-Direct word-line addressing**

Applications:

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- **Channel Preset Memory in digital frequency-synthesizer circuits**
- **General-purpose and scratch-pad memory in COS/MOS and other low-power systems.**

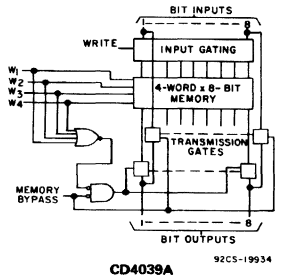
MAXIMUM RATINGS, *Absolute-Maximum Values:*

Storage Temperature Range	−65 to +150	°C
Operating Temperature Range	−55 to +125	°C
DC Supply Voltage Range (V_{DD} − V_{SS})	−0.5 to +15	V
Device Dissipation (Per Pkg.)	200	mW
All Inputs	$V_{SS} \leq V_I \leq V_{DD}$	
Recommended DC Supply Voltage (V_{DD} − V_{SS})	3 to 15	V
Lead Temperature (During soldering) At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	265	°C

STATIC ELECTRICAL CHARACTERISTICS (All inputs $V_{SS} \leq V_I \leq V_{DD}$)
(Recommended DC Supply Voltage (V_{DD} − V_{SS}) 3 to 15 V)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK									UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS Fig. No.
			V_O Volts	V_{DD} Volts	−55°C Min.	−55°C Typ.	−55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Typ.	125°C Max.		
Quiescent Device Current	I_L			5	–	–	5	–	0.5	5	–	–	300	μA	11, 12
				10	–	–	10	–	1	10	–	–	600		
Quiescent Device Dissipation/Package	P_D			5	–	–	25	–	2.5	25	–	–	1500	μW	–
				10	–	–	100	–	10	100	–	–	6000		
Output Voltage: Low-Level	V_{OL}			5	–	–	0.01	–	0	0.01	–	-	0.05	V	–
				10	–	–	0.01	–	0	0.01	–	–	0.05		
High-Level	V_{OH}			5	4.99	–	–	4.99	5	–	4.95	–	–	V	–
				10	9.99	–	–	9.99	10	–	9.95	–	–		
Noise Immunity (All inputs except bit inputs when in memory by-pass mode.)	V_{NL}		0.8	5	1.5	–	–	1.5	2.25	–	1.4	–	–	V	13
			1.0	10	3	–	–	3	4.5	–	2.9	–	–		
	V_{NH}		4.2	5	1.4	–	–	1.5	2.25	–	1.5	–	–		
			9.0	10	2.9	–	–	3	4.5	–	3	–	–		
Output Drive Current: N-Channel	I_{DN}	Normal Read Modes	0.5	5	0.12	–	–	0.10	0.20	–	0.07	–	–	mA	6
			0.5	10	0.30	–	–	0.25	0.50	–	0.17	–	–		
P-Channel	I_{DP}		4.5	5	−0.12	–	–	−0.10	−0.20	–	−0.07	–	–	mA	7
			9.5	10	−0.30	–	–	−0.25	−0.50	–	−0.17	–	–		
Output Drive Current: N-Channel	I_{DN}	Memory Bypass Mode +	0.5	5	0.04	–	–	0.03	0.06	–	0.02	–	–	mA	–
			0.5	10	0.09	–	–	0.075	0.15	–	0.05	–	–		
P-Channel	I_{DP}		4.5	5	−0.04	–	–	−0.03	−0.06	–	−0.02	–	–	mA	–
			9.5	10	−0.09	–	–	−0.075	−0.15	–	−0.05	–	–		
Input Current	I_I		–	–	–	–	–	–	10	–	–	–	–	pA	–

+Bit inputs driven from low-impedance driver.



CD4039A

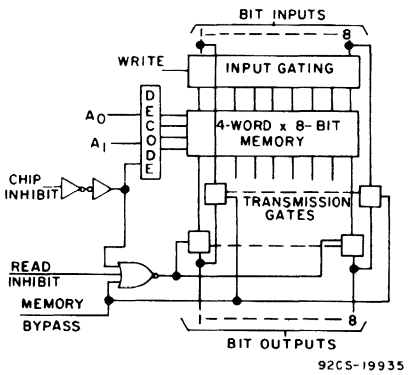


Fig.1 – CD4036A – Logic block diagram.

Write (Pin 2)	Read Inhibit (Pin 21)	Memory Bypass (Pin 11)	Chip Inhibit (Pin 22)	Operating Mode
X	X	L	H	Chip Inhibited (Outputs float)
X	X	H	H	Input/Output Shunted to output; No Reading from Memory;
L	X	H	L	Information in Memory Undisturbed
H	X	H	L	Input/Output Shunted to output; No Reading from Memory; Write Data into Addressed Word
L	L	L	L	Read Data from Addressed Word Write Deactivated
L	H	L	L	Read/Write Deactivated (Outputs float)
H	L	L	L	Read from Memory while Writing Data into Addressed Word
H	H	L	L	Write Data into Addressed Word Read Deactivated (outputs float)

Fig.2 – Operating-mode truth table.

A1 Pin 1	A0 Pin 23	Addressed Word
L	L	Word 1
L	H	Word 2
H	L	Word 3
H	H	Word 4

L = Low-Level Voltage,
H = High-Level Voltage

Fig.3 – Address truth table.

CD4036A, CD4039A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CD4036AD, CD4036AK CD4039AD, CD4039AK				UNITS	CHARACTERISTIC CURVES & TEST CIRCUITS
			V_{DD} Volts	Min.	Typ.	Max.		
Read Delay Time: (Access time) Read Inhibit (RI)	t_{rd}	OUTPUT TIED THROUGH 100 kΩ TO V_{SS} FOR DATA OUTPUT "HIGH" AND TO V_{DD} FOR DATA OUTPUT "LOW"	5	–	375	750	ns	4,5
			10	–	150	300	Note 4	
Chip Inhibit (CI)			5	–	500	1000	ns	4,5
			10	–	200	400	Note 4	
Memory Bypass (MB)			5	–	375	750	ns	4.5
			10	–	150	300		
Address[1] (ADD)			5	–	500	1000	ns	4,5,8
			10	–	200	400		
Write Set-up Time[2]	t_{WS}		5	250	125	–	ns	4,5
			10	100	50	–		
Write Removal Time[3]	t_{WR}		5	0	0	–	ns	4,5
			10	0	0	–		
Write Pulse Duration	t_W		5	150	75	–	ns	4,5
			10	60	30	–		
Data Set-up Time[5]	t_{DS}		5	–	0	0*	ns	4,5
			10	–	0	0*		
Data Overlap Time[6]	t_{DO}		5	100●	50	–	ns	4,5
			10	40●	20	–		
Output Transition Time	t_{THL}, t_{TLH}		5	–	200	400	ns	9
			10	–	100	200		
Input Capacitance	C_I	Any Input		–	5	–	pF	–

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice-versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD & 4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
   * Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.
6. The time that DATA signal must remain present after the WHITE pulse removal.
   ● Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

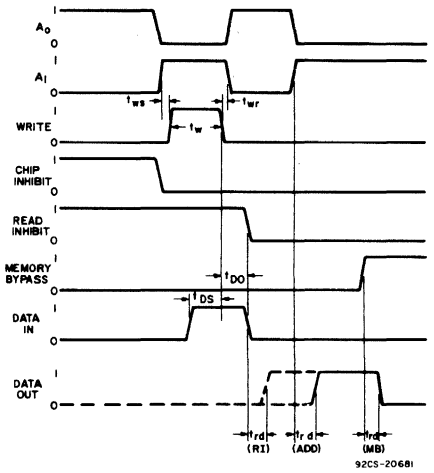


Fig.4—CD4036A Timing Diagram.

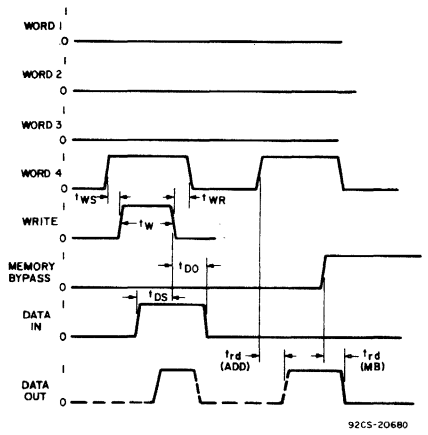


Fig.5—CD4039A Timing Diagram.

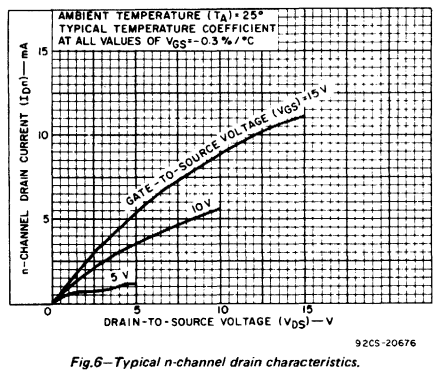


Fig.6—Typical n-channel drain characteristics.

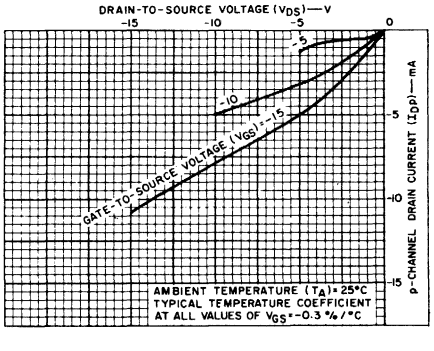


Fig.7—Typical p-channel drain characteristics.

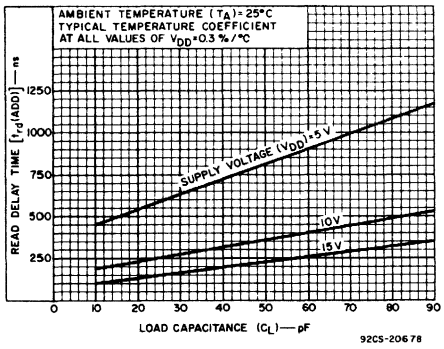


Fig.8—Typical read delay time vs. C_L.

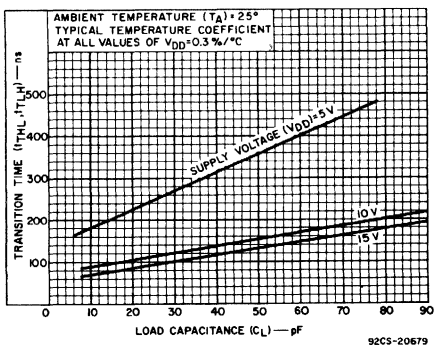


Fig.9—Typical transition time vs. C_L.

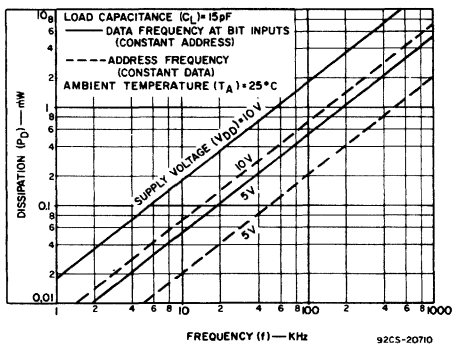


Fig.10—Typical power dissipation vs. frequency.

TEST CIRCUITS

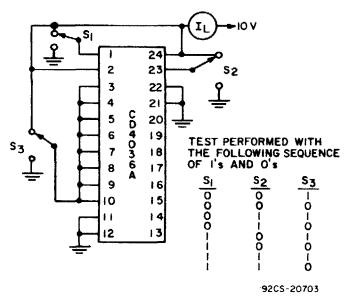


Fig.11—Quiescent current (CD4036A).

CD4036A, CD4039A Types

TEST CIRCUITS (Cont'd)

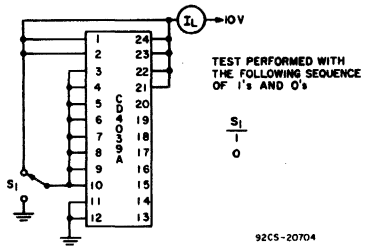


Fig.12–Quiescent current (CD4039A).

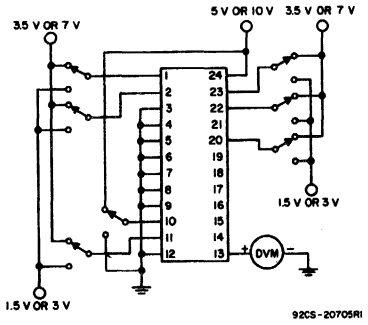
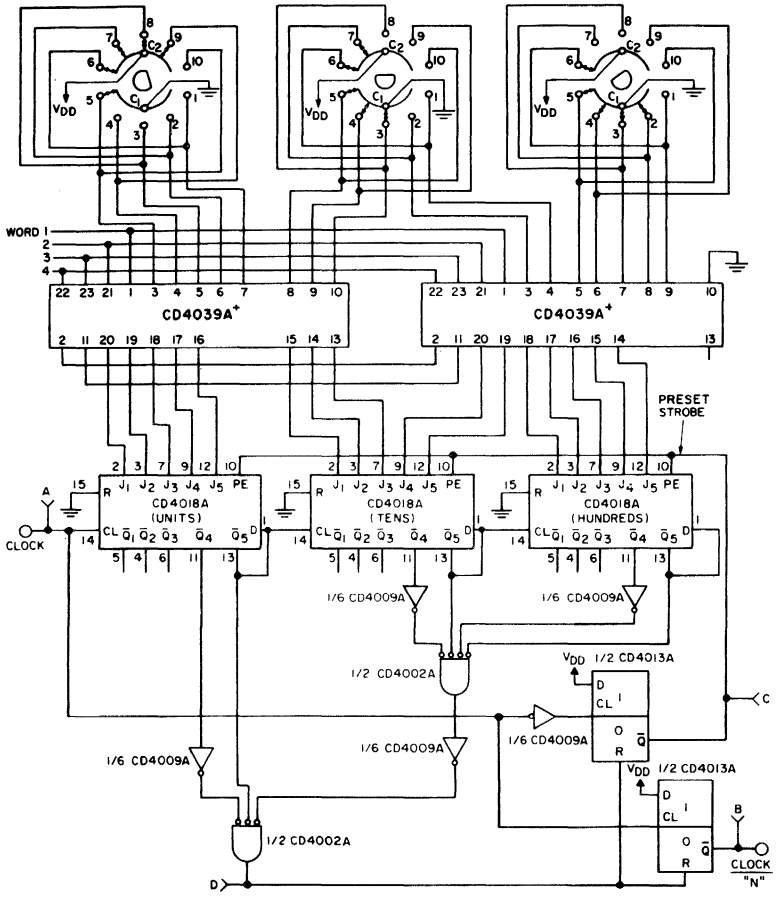


Fig.13–Noise immunity.



Switches shown are GRAYHILL 2-pole switches 50CY23133, CENTRALAB PA160, or equivalent can also be used.

Switches (left to right) read 5-3-2. The equivalent value of "N" for these switch positions (from the Table below) is 3-1-0 or N = 13.

N Value (Front panel notation)	Switch Positions
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	9
8	10
9	1

+ The CD4039A CAN BE UTILIZED IN A SIMILAR FASHION.

SEE APP. NOTE ICAN-6498 – "DESIGN OF FIXED AND PROGRAMMABLE COUNTERS USING THE RCA CD4018A COS/MOS PRESETTABLE DIVIDE-BY-'N' COUNTER" AND ICAN-6716, "LOW POWER DIGITAL FREQUENCY SYNTHESIZERS UTILIZING COS/MOS IC'S".

Fig.14–Three-decade programmable ÷ N counter with 4-channel preset memory settings for frequency synthesizers.

The divide-by-N counter system shown in Fig.14 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be read into each CD4018A by simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.

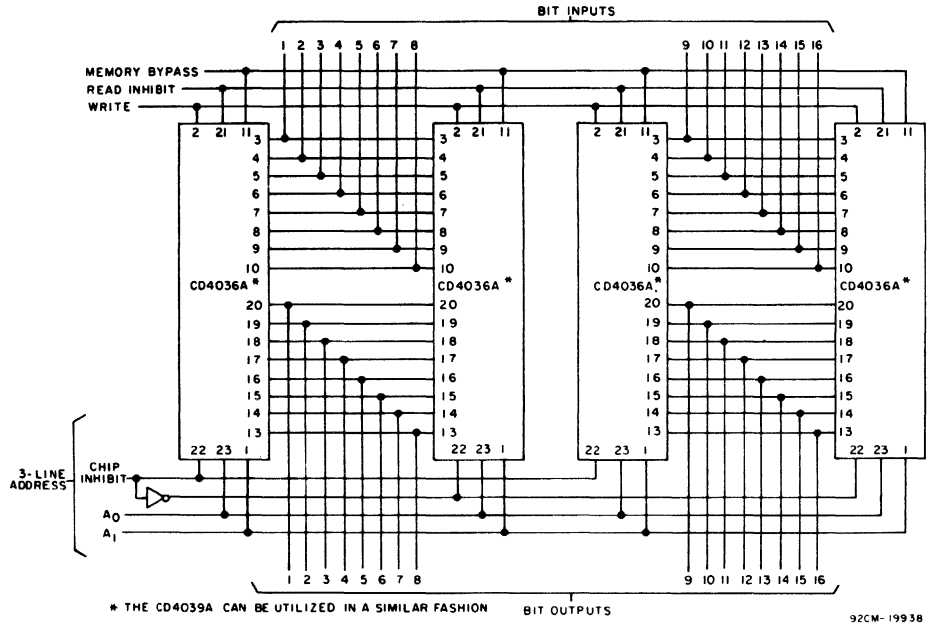


Fig.15–General-purpose memory storage – 8 words x 16 bits (RAM or ROM).

CD4061A Types

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

The RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0-A_7) to select one of 256 storage locations. Additional connections are provided for a READ/WRITE command CHIP SELECT DATA IN, and DATA OUT and DATA OUT lines.

To perform READ and WRITE operations the CHIP-SELECT signal must be low. When the CHIP-SELECT signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-SELECT signal must be returned to a high level, regardless of the logic level of the READ/WRITE input. In a multiple package application, the CHIP-SELECT signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP SELECT and READ/WRITE signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

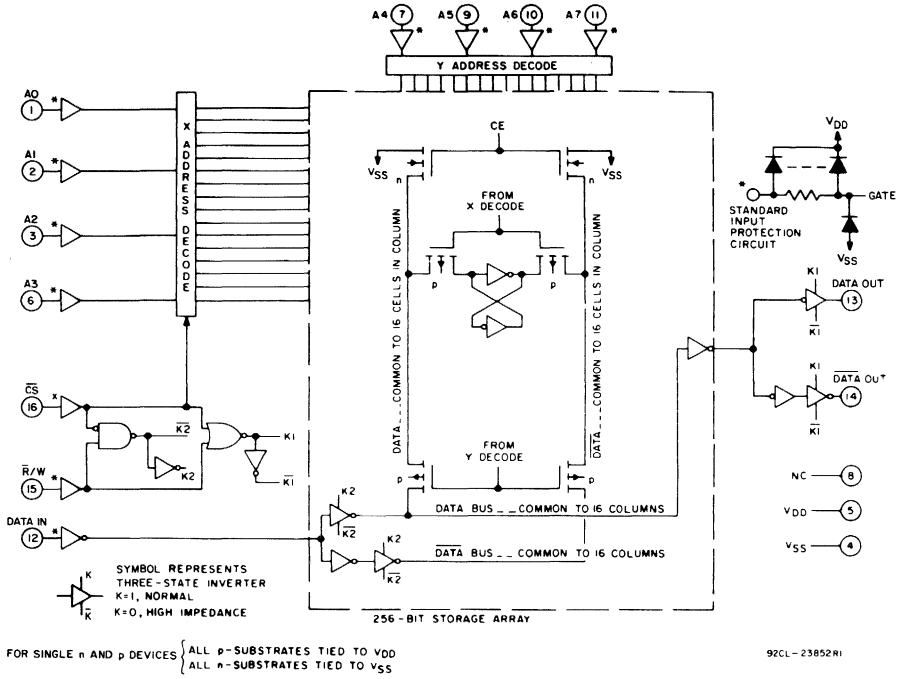


Fig. 1 – CD4061A logic diagram.

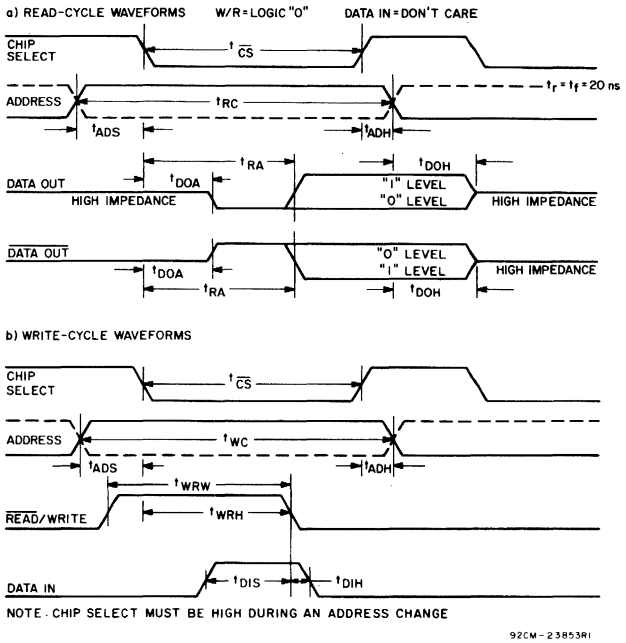


Fig. 2 – Typical write-read waveforms.

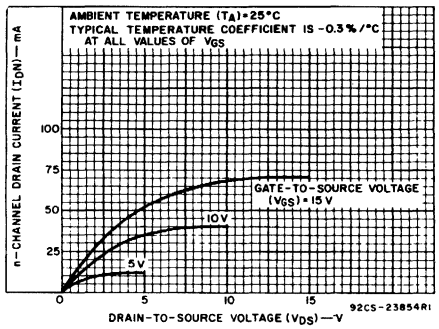


Fig. 3 – Typical n-channel drain characteristics.

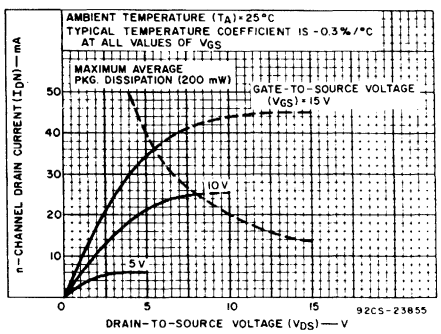


Fig. 4 – Minimum n-channel drain characteristics.

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE . . . . . –65 to +150°C

OPERATING-TEMPERATURE RANGE . . . . . –55 to +125°C

DC SUPPLY-VOLTAGE RANGE:

V_{DD} . . . . . –0.5 to +15 V

DEVICE DISSIPATION (PER PACKAGE) . . . . . 200 mW

ALL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

RECOMMENDED DC SUPPLY VOLTAGE (V_{DD}-V_{SS}) . . . . . 3 to 15 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

Features:

- **Low standby power: 10 nW/bit (typ @ V_{DD} = 10 V**
- **Access time: 380 ns (max.) @ V_{DD} = 10 V**
- **Single 3-to-15 V power supply**
- **COS/MOS input/output logic compatibility**
- **TTL output drive capability**
- **Three-state data outputs for bus-oriented systems**
- **1101-type pin designations**
- **Separate data output and data input lines**
- **Noise immunity: 45% of V_{DD} (typ.**
- **Fully decoded addressing**
- **Single write/read control line**

CD4061A Types

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	$\overline{\text{CHIP-SELECT}}$	$\overline{\text{READ/WRITE}}$	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read Modify Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

*For a READ MODIFY WRITE operation, $\overline{\text{CHIP SELECT}}$ may be held to logic 0 for the whole operation.

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25°C$, $V_{SS} = 0$ V, $C_L = 50$ pF, and t_r, $t_f = 20$ ns

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
READ CYCLE TIME						
Read Cycle	t_{RC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	ns
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	ns
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	ns
		10	200	–	–	
Read Access	t_{RA}	5	–	450	750	ns
		10	–	250	380	
Data Out Hold	t_{DOH}	5	110	170	230	ns
		10	130	160	190	
Data Out Active	t_{DOA}	5	80	120	160	ns
		10	40	70	100	
Output Transition	t_{TLH}	5	–	60	100	ns
		10	–	50	75	
	t_{THL}	5	–	35	60	
		10	–	25	40	
Chip-Select Input Rise and Fall Time,	t_{rCE}, t_{fCE}	5	–	–	15	μs
		10	–	–	5	
		15	–	–	1	
WRITE CYCLE TIME						
Write Cycle	t_{WC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	
		10	200	–	–	
Write Hold	t_{WRH}	5	150	100	–	
		10	100	70	–	
Write	t_{WRW}	5	150	100	–	
		10	100	70	–	
Data-In Setup	t_{DIS}	5	140	80	–	
		10	80	35	–	
Data-In Hold	t_{DIH}	5	25	10	–	
		10	20	10	–	

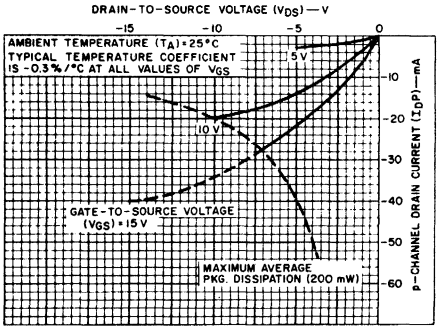


Fig. 5 – Typical p-channel drain characteristics.

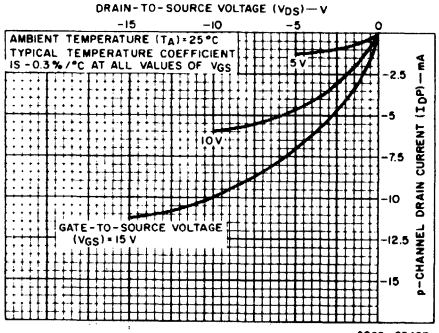


Fig. 6 – Minimum p-channel drain characteristics.

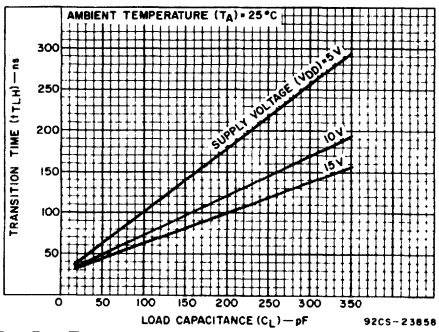


Fig. 7 – Typical low-to-high transition time (t_{TLH}) vs. C_L.

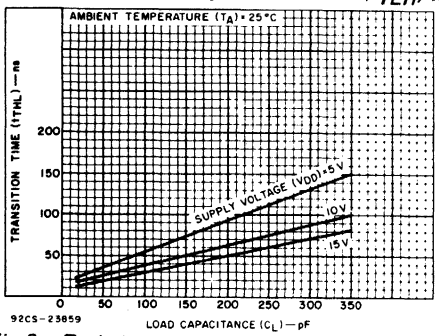


Fig. 8 – Typical high-to-low transition time (t_{THL}) vs. C_L.

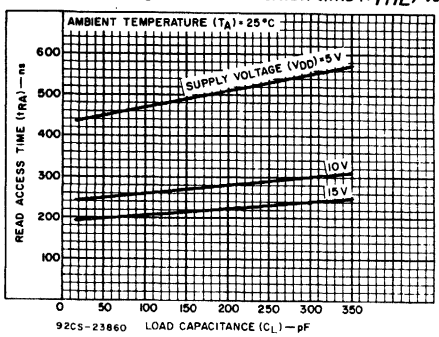


Fig. 9 – Typical read access time (t_{RA}) vs. C_L.

CD4061A Types

STATIC ELECTRICAL CHARACTERISTICS

(All inputs . . . $V_{SS} \leq V_I \leq V_{DD}$)

(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$) . . . 3 to 15 V)

CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNIT
Quiescent Device Current, I_L *See Fig. 14*		5	–	5	–	0.12	5	–	150	μA
		10	–	10	–	0.25	10	–	300	
Quiescent Device Dissipation/Package, P_D		5	–	–	–	0.6	25	–	750	μW
		10	–	–	–	2.5	100	–	3000	
Output Voltage Low-Level, V_{OL}		5	–	0.01	–	0	0.01	–	0.05	V
		10	–	0.01	–	0	0.01	–	0.05	
High-Level, V_{OH}		5	4.99	–	4.99	5	–	4.95	–	
		10	9.99	–	9.99	10	–	9.95	–	
Noise Immunity, (All Inputs) *See Fig. 17* V_{NL}	0.8	5	1.5	–	1.5	2.25	–	1.4	–	V
	1	10	3	–	3	4.5	–	2.9	–	
V_{NH}	4.2	5	1.4	–	1.5	2.25	–	1.5	–	
	9	10	2.9	–	3	4.5	–	3	–	
Output Drive Current: (Data Out, Data Out) N-Channel (Sink), I_DN *See Figs. 3, 4, 12*	0.4	4.5	2	–	1.6	2.5	–	1.1	–	mA
	0.5	10	4.3	–	3.5	5	–	2.4	–	
P-Channel (Source), I_DP *See Figs. 5, 6, 13*	2.5	5	-1.1	–	-0.9	-1.8	–	-0.65	–	
	4.6	5	-0.5	–	-0.4	-0.8	–	-0.3	–	
	9.5	10	-1.1	–	-0.9	-1.8	–	-0.65	–	
Output Off Resistance (High-Impedance State), R_O (Off)		5	10	–	10	–	–	10	–	MΩ
		10	10	–	10	–	–	10	–	

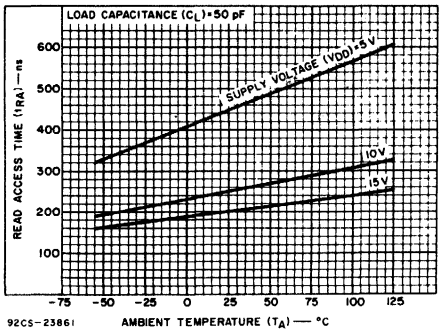


Fig. 10 – Typical read access time (t_{RA}) vs. temperature.

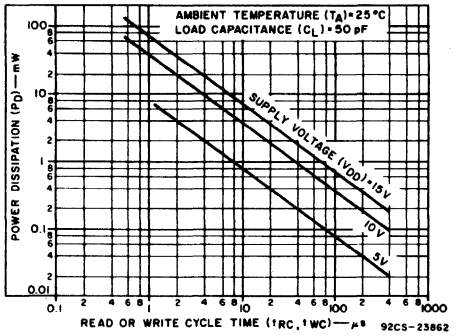
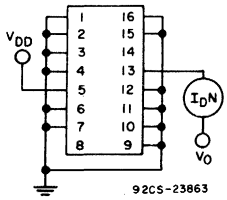


Fig. 11 – Typical power dissipation vs. cycle time.



Note: At address "0", "0" stored in memory.

Fig. 12 – N-channel drive current.

Note: At address 0, "1" stored in memory.

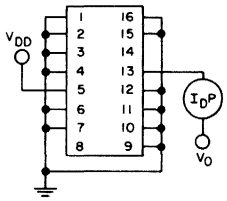


Fig. 13 – P-channel drive current.

Note for Fig. 12 and Fig. 13:
Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of t_{CE} = 400 ns.

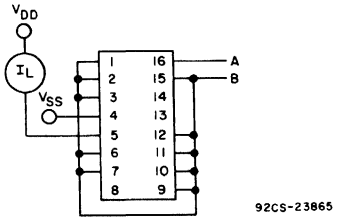


Fig. 14 – Quiescent device current.

Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

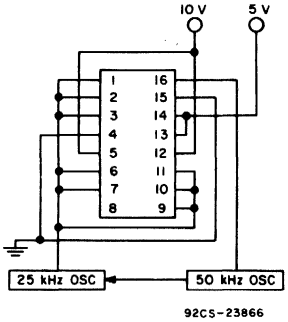
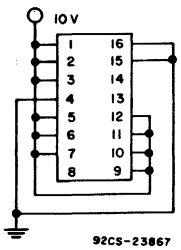


Fig. 15 – Operating life.



Description of Test:

Functional test run with random data input. All inputs toggle between 30% and 70% of V_{DD}.

Fig. 16 – Bias life.

Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.

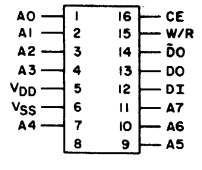


Fig. 17 – Noise immunity.

Preliminary CD40061, CD40061A Types

COS/MOS 256-Word by 1-Bit Static Random-Access Memory

The RCA-CD40061 and CD40061A are 256-word by 1-bit COS/MOS fully static random access memories. They are similar in terminal arrangement and function to the CD4061A, except that the requirement for the Chip-Select input to return to a high level between address changes in eliminated.

The CD40061AD and CD40061AE have maximum supply voltage ratings of 15 V; the CD40061E maximum rating is 7 V. These devices are fully decoded and utilize eight Address inputs (A_0-A_7) to select one of the 256 storage locations. Additional connections are provided for an active Low Chip-Select ($\overline{CS}$), a $\overline{Read}$/Write command ($\overline{R}/W$), a Data input (DATA IN), an active High 3-State Output (DATA OUT), and an active Low 3-State Output ($\overline{DATA}$ OUT). DATA OUT is the same voltage state as DATA IN.

The Chip-Select input must be low to enable the Read or Write operations. A high level both inhibits these functions and causes the outputs to exhibit a high impedance. Output voltage levels appear at the output only when both CS and $\overline{R}/W$ inputs are at low levels. These outputs interface directly with TTL devices.

Both the CD40061 and CD40061A are supplied in 16-lead dual-in-line plastic packages (E suffix) or in chip form (H suffix). The CD40061A is also supplied in a hermetically sealed 16-lead dual-in-line ceramic side-brazed package (D suffix).

Features:

- **Organization — 256-words by 1-bit**
- **COS/MOS compatible inputs and outputs**
- **Low power dissipation (typ.) @ 300 nS cycle time:**
  10 nW/Bit standby @ V_{DD} = 5 V
  0.1 mW/Bit operating @ V_{DD} = 5 V
  40 nW/Bit standby @ V_{DD} = 10 V
  0.4 mW/Bit operating @ V_{DD} = 10 V
- **Access time (typ.):**
  150 nS @ V_{DD} = 10 V; 300 nS @ V_{DD} = 5 V
- **Noise immunity (typ.): 45% of V_{DD}**
- **TTL output drive capability**
- **3-State complementary data outputs**
- **Separate data-in and data-out lines**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE:
  CERAMIC-PACKAGE TYPES ..... −55 to +125°C
  PLASTIC-PACKAGE TYPES ..... −40 to +85°C
SUPPLY VOLTAGE RANGE (V_{DD}−V_{SS}):
  CD40061E ..... 7 to −0.5 V
  CD40061AD, CD40061AE ..... 15 to −0.5 V
INPUT VOLTAGE RANGE (V_I−V_{SS}) ..... V_{DD} to −0.5 V
DEVICE DISSIPATION (per package) ..... 200 mW
RECOMMENDED DC SUPPLY VOLTAGE RANGE (V_{DD}−V_{SS}):
  CD40061E ..... 3 to 6 V
  CD40061AD, CD40061AE ..... 3 to 12 V
RECOMMENDED INPUT VOLTAGE SWING ..... V_{DD} to V_{SS}
LEAD TEMPERATURE (During soldering):
  At distance 1/16 ±1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

CD40061 and CD40061A OPERATIONAL MODES

MODE	$\overline{CHIP\text{-}SELECT}$	$\overline{READ}$/WRITE	DATA OUT	$\overline{DATA}$ OUT
Write	0	1	High Impedance	High Impedance
Read	0	0	Storage State	Complement of Storage State
Unselected	1	X	High Impedance	High Impedance

1 = High Level 0 = Low Level X = Don't Care

CAPACITANCES (V_I = 0, f = 1 MHz)

CHARACTERISTICS	Min.	Typ.	Max.	UNITS
Address Input, C_A	–	9	–	pF
Chip-Select, C_{CS}	–	9	–	pF
Read/Write Input, C_{WE}	–	5	–	pF
Data Input, C_{DI}	–	5	–	pF
Data Output, C_{DO}	–	10	–	pF

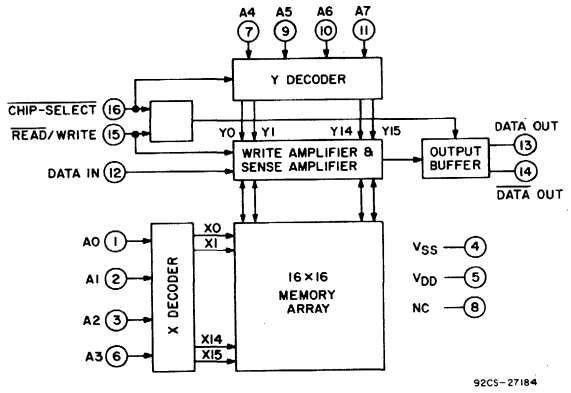


Fig. 1 — Functional block diagram for CD40061, and CD40061A.

Preliminary CD40061, CD40061A Types

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

Values shown for V_{DD} = 5 V apply to all types; values shown for V_{DD} = 10 V apply to the CD40061AD and CD40061AE only.

CHARACTERISTIC	TEST CONDITIONS V_O(V)	TEST CONDITIONS V_{DD}(V)	TYPICAL VALUES	UNITS
Quiescent Device Current, I_L		5 10	0.5 1	μA
Output Voltage, Low Level, V_{OL}		5 10	0 0	V
Output Voltage, High Level, V_{OH}		5 10	5 10	V
Output Current, Low Level, I_{OL}	0.4 0.5	5 10	1.6 3.5	mA
Output Current, High Level, I_{OH}	2.5 4.5 9	5 5 10	−0.9 −0.4 −0.9	mA
Noise Immunity, All Inputs Low, V_{NL}	0.8 1	5 10	2.25 4.5	V
Noise Immunity, All Inputs High, V_{NH}	4.2 9	5 10	2.25 4.5	V
Output Resistance, Off State, R_O(off)		5 10	10 10	MΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, and C_L = 50 pF, see Note 3.

READ CYCLE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5 10	310 180	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Read Setup,	t_{RDS}	5 10	0 0	ns
Read Hold,	t_{RDH}	5 10	0 0	ns
Data Out Hold,	t_{DOH}	5 10	40 20	ns
Data Out Active,	t_{DOA}	5 10	20 15	ns
Read Cycle, (Note 2)	t_{RC}	5 10	350 200	ns
Access,	t_{ACC}	5 10	300 150	ns

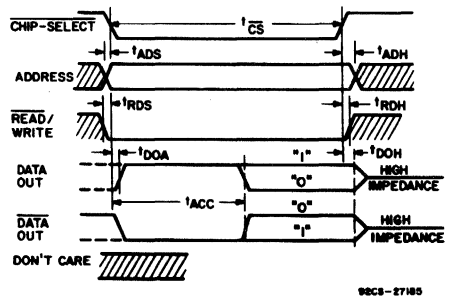


Fig. 2 – Read cycle waveforms for CD40061, CD40061A.

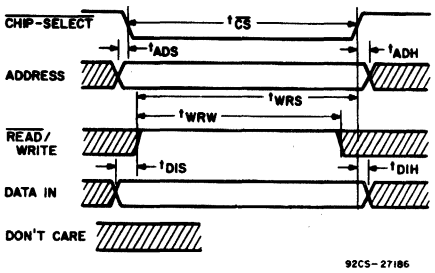


Fig. 3 – Write cycle waveforms for CD40061, CD40061A.

DYNAMIC ELECTRICAL CHARACTERISTICS (Cont'd)

WRITE CYCLE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select,	$t_{\overline{CS}}$	5 10	170 90	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Write Setup,	t_{WRS}	5 10	170 90	ns
Write Width,	t_{WRW}	5 10	170 90	ns
Data In Setup,	t_{DIS}	5 10	0 0	ns
Data In Hold,	t_{DIH}	5 10	20 10	ns
Write Cycle, (Note 2)	t_{WC}	5 10	200 110	ns

READ/MODIFY/WRITE TIMES (For waveforms, see Figs. 2, 3 and 4)

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Chip-Select, (Note 1)	$t_{\overline{CS}}$	5 10	480 270	ns
Address Setup,	t_{ADS}	5 10	20 10	ns
Address Hold,	t_{ADH}	5 10	0 0	ns
Read Setup,	t_{RDS}	5 10	0 0	ns
Data Out Active,	t_{DOA}	5 10	20 15	ns
Previous Data Hold,	t_{PDH}	5 10	40 20	ns
Access,	t_{ACC}	5 10	300 150	ns
Read Width Effective,	t_{RDW}	5 10	310 180	ns
Write Setup,	t_{WRS}	5 10	170 90	ns
Write Width	t_{WRW}	5 10	170 90	ns
Data In Setup,	t_{DIS}	5 10	0 0	ns
Data In Hold,	t_{DIH}	5 10	20 10	ns
Read/Modify/Write Cycle, (Note 2)	t_{RWC}	5 10	500 280	ns

Note 1 – The chip-select times specified provide an active output data time of 50 ns minimum.

Note 2 – Cycle time defines the shortest time in which this memory will correctly perform its desired function.

Note 3 – Address rise and fall times must be equal to or less than 1 μs under all conditions and for all modes.

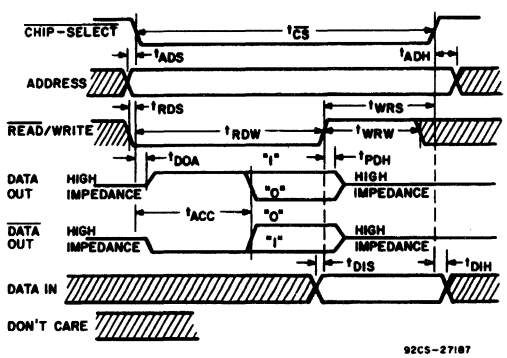


Fig. 4 – Read/modify/write cycle waveforms for CD40061, CD40061A.

Preliminary MW4050D

N-Channel 4096-Bit MOS Random-Access Memory

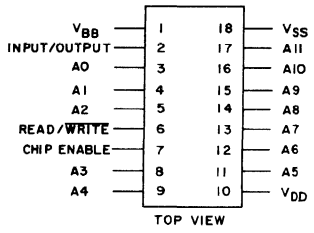
The RCA-MW4050D Series types are 4096-word by 1-bit high-speed dynamic NMOS random-access memories in the popular 18-lead package with 0.3-inch row spacing for high packing density on PC boards. The use of n-channel technology in these devices optimizes the speed, density, and power consumption. The MW4050D Series is intended for large-scale, high-performance memory systems in which low cost and high reliability are primary design objectives.

Three performance options of maximum access time are offered: 300 ns for the MW-4050D, 250 ns for the MW4050DV1, and 200 ns for the MW4050DV2. These types are direct replacements for the equivalent TMS4050, TMS4050-1, and TMS4050-2.

The Data-Input and Data-Output lines to the memory are on a common terminal. The output buffer has an open-drain configuration capable of sinking a 5-mA load current. The common I/O allows simple interfacing to the memory-system bus in Read, Write, and Read/Modify/Write modes. Read and Write are always straightforward. Data control of Read/Write is also included to avoid any conflict between Data-Out and new Data-In during Read/Modify/Write cycles. Refresh of all 64 cells on any one X address line is accomplished by executing a read cycle. In addition, when writing new data into a selected location, all the other 63 cells on this X line are automatically refreshed.

The MW4050D design uses balanced sensing to eliminate pattern sensitivity. In addition, all bit and word lines in the array are clamped to preset potentials while the memory is quiescent. The X and Y decoders use push-pull drive to virtually eliminate the effects of unwanted capacitance coupling.

The MW4050D Series is supplied in an 18-lead hermetic dual-in-line side-brazed ceramic package.



Terminal Assignment
18-Lead Dual-In-Line
White-Ceramic Package

Features:

- **Organization—4096 words by 1 bit**
- **Direct replacement for TMS4050**
- **TTL—compatible inputs (except Chip-Enable)**
- **Single low-capacitance clock**
- **Low power dissipation (typ.):**
  0.2 mW/package standby
  420 mW/package operating
- **Open drain output—common I/O**
- **On-chip address registers**
- **Data-In can be valid up to 15 ns after Read/Write low level**
- **Clamped bit lines minimize pattern sensitivity problems**
- **N-channel silicon-gate technology**
- **18-lead dual-in-line ceramic hermetic package (0.3 inch spacing)**

RCA Type No.	Access Time-ns Max.	Read or Write Cycle Time-ns Min.	Read/Modify/ Write Cycle Time-ns Min.
MW4050D	300	470	730
MW4050DV1	250	430	660
MW4050DV2	200	400	600

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC		LIMITS ALL TYPES Min.	Typ.	Max.	UNITS
Supply Voltage:					
	V_{DD}	11.4	12	12.6	V
	V_{BB}	−5.5	−5	−4.5	
	V_{SS}	−	0	−	
Input Voltage, High Level:					
Chip-Enable	V_{CEH}	V_{DD} −0.6	−	V_{DD} +1	V
All Others	V_{IH}	2.2	−	5.25	
Input Voltage, Low Level:					
Chip-Enable	V_{CEL}	−1	−	0.6	V
All Others	V_{IL}	−0.6	−	0.6	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE
..... −55 to +150°C
OPERATING TEMPERATURE RANGE
..... 0 to +70°C
SUPPLY VOLTAGE RANGES:
(V_{DD}−V_{BB}) ..... 20 to −0.3 V
(V_{SS}−V_{BB}) ..... 20 to −0.3 V
INPUT VOLTAGE RANGES:
CHIP-ENABLE INPUT (V_{CE}−V_{SS}) 20 to −0.3 V
ALL OTHER INPUTS (V_{IN}−V_{SS}) 20 to −0.3 V
OUTPUT VOLTAGE RANGE:
($V_{I/O}$ − V_{SS}) ..... 7 to −2 V
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. ..... +265°C

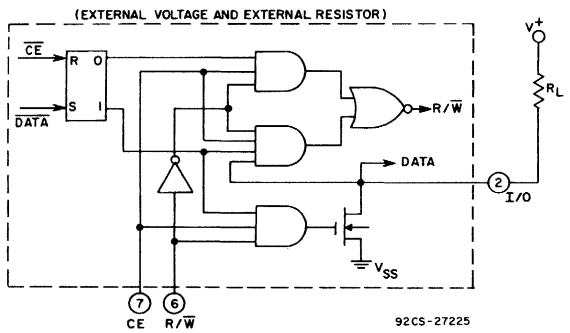


Fig. 1—Input/output logic diagram.

Preliminary MW4050D

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V, Output Load = 50 pF and one Series 74-type gate.

CHARACTERISTIC		LIMITS						UNITS
		MW4050D		MW4050DV1		MW4050DV2		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
V_{DD} Supply Current:								
During V_{CE} high level,	$I_{DD}1$	–	60	–	60	–	60	mA
Average during read or write cycle,	$I_{DD}2$	32	–	35	–	38	–	mA
Average during read/ modify/write cycle,	$I_{DD}3$	37	–	41	–	45	–	mA

CAPACITANCES at T_A = 0 to 70°C, V_{DD} = 12 V, V_{BB} = −5 V, V_I = 0 V, V_{SS} = 0 V, f = 1 MHz. V_{CE} = 0 V unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Address,	C_{AD}		–	5	7	pF
Chip-Enable,	C_{CE}	V_{CEH} = 10.8 V	–	24	28	pF
		V_{CEL} = −1 V	–	29	33	pF
Read/Write,	C_{RW}		–	5	7	pF
Data In/Out,	$C_{I/O}$		–	7	9	pF

OPERATIONAL MODES

MODE	CHIP-ENABLE	READ/$\overline{\text{WRITE}}$	CONDITION	I/O STATE	REMARKS
Read	1	1	Read stored 0	0	Output buffer enabled until CE is non-active
			Read stored 1	1	Output buffer disabled
Write	1	0	Write 0 Write 1	0 1	Output buffer disabled
Read/ Modify/ Write	1	1	Read 0 then Write 0	0	Output buffer disabled during Write; write function not executed
		then	Read 0 then Write 1	0 then 1	Output buffer disabled during Write; write function occurs as Data-In goes to high level#
		0	Read 1 then Write 0	1 then 0	Output buffer disabled; Write function occurs as R/$\overline{W}$ goes to low level
			Read 1 then Write 1	1	Output buffer disabled; Write function occurs as R/$\overline{W}$ goes to low level
Refresh	1	1		0 or 1	Same as Read cycle
Standby	0	X		1	

I/O is pulled up to high level by external network. Following read out of a low level (0), the self-timed internal Write function **cannot occur** until the new Data-In has gone to a high level (1). Thus no conflict between the previous output data state and the new data to be written can occur. No possible race hazard between R/$\overline{W}$ and Data-In exists, eliminating all possibility of false data being written in. The internal levels stored in the array depend on bit location. A data input 1 is a stored internal high level if the address state of A 5 is opposite to that of A 6. This description of the internal operation of the device is intended for user information only.

1 = High level 0 = Low level X = Don't care

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V.

CHARACTERISTIC		TEST CONDITIONS	LIMITS ALL TYPES*			UNITS
			Min.	Typ.	Max.	
Supply Current:						
For V_{DD}	I_{DDO}	V_{CEH} = 0.6 V	–	10	200	μA
For V_{BB}	I_{BBO}		–	−5	−100	
Input Current, High-Level:						
Chip-Enable	I_{CEH}	V_{CE} = 13.6 V	–	–	2	μA
All Others	I_{IH}	V_I = 5.5 V	–	–	10	
Input Current, Low-Level:						
Chip-Enable	I_{CEL}	V_{CE} = −1 V	–	–	±10	μA
All Others	I_{IL}	V_I = −0.6 V	–	–	±10	
Output Current:						
Off-State	I_{OZ}	V_O = 0 to 5.5 V	–	–	±10	μA
Output Voltage:						
High Level	V_{OH}	Open drain	•	–	–	V
Low Level	V_{OL}	I_O = 5 mA	V_{SS}	–	0.4	

* All typical values are at T_A = 25°C and nominal supply voltages.
• Output voltage determined by external pull-up resistor.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V, Output Load = 50 pF and one Series 74-gate. All input timing measured from low input level (0.8 V) or high input level (2 V) to 10% or 90% point on V_{CE} transition edges. Input/output timing measured from low output level (0.4 V) or high output level (2.4 V) to 10% or 90% point on V_{CE} transition edges. Rise time (t_r) and fall time (t_f) from 10% to 90% of V_{CE} are 20 ns. For waveforms, see Figs. 3, 4, and 5.

Read Cycle Times

CHARACTERISTIC		LIMITS						UNITS
		MW4050D		MW4050DV1		MW4050DV2		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle,	t_{RC}	470	–	430	–	400	–	ns
Chip-Enable Active,	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active,	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise,	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall,	t_{CEf}	–	40	–	40	–	40	ns
Address Setup,	t_{ADS}	0	–	0	–	0	–	ns
Address Hold,	t_{ADH}	150	–	150	–	150	–	ns
Read Setup,	t_{RDS}	0	–	0	–	0•	–	ns
Read Hold,•	t_{RDH}	40	–	40	–	40	–	ns
Access from Chip-Enable,	t_{CEA}	–	280	–	230	–	180	ns
Access from Address,	t_{ADA}	–	300	–	250	–	200	ns
Data-Out Hold,	t_{DOH}	40	–	40	–	40	–	ns

Write Cycle Times

CHARACTERISTIC		LIMITS						UNITS
		MW4050D		MW4050DV1		MW4050DV2		
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle,	t_{WC}	470	–	430	–	400	–	ns
Chip-Enable Active,	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active,	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise,	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall,	t_{CEf}	–	40	–	40	–	40	ns
Address Setup,	t_{ADS}	0	–	0	–	0	–	ns
Address Hold,	t_{ADH}	150	–	150	–	150	–	ns
Read Hold,•	t_{RDH}	–	40	–	40	–	40	ns
Write Setup,	t_{WRS}	240	–	220	–	210	–	ns
Write Width,	t_{WRW}	200	–	190	–	180	–	ns
Data-In Setup,▲	t_{DIS}	−15	–	−15	–	−15	–	ns
Data-In Hold,	t_{DIH}	40	–	40	–	40	–	ns

• Read Hold (t_{RDH}) is measured from the 10% point on the Chip-Enable input.
▲ Data-In need not be valid until 15 ns after the Read/$\overline{\text{Write}}$ input is low.

Read/Modify/Write Cycle Times

CHARACTERISTIC		LIMITS						UNITS
		MW4050D		MW4050DV1		MW4050DV2		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read/Modify/Write Cycle,	t_{RWC}	730	–	660	–	600	–	ns
Chip-Enable Active,	t_{CE}	560	4000	490	4000	430	4000	ns
Chip-Enable Non-active,	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise,	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall,	t_{CEf}	–	40	–	40	–	40	ns
Address Setup,	t_{ADS}	0	–	0	–	0	–	ns
Address Hold,	t_{ADH}	150	–	150	–	150	–	ns
Read Setup,	t_{RDS}	0	–	0	–	0	–	ns
Read Width Effective,	t_{RDW}	300	–	250	–	200	–	ns
Write Setup,	t_{WRS}	240	–	220	–	210	–	ns
Write Width,	t_{WRW}	200	–	190	–	180	–	ns
Data-In Width Effective,	t_{DIW}	225	–	205	–	195	–	ns
Data-In Hold,	t_{DIH}	40	–	40	–	40	–	ns
Access from Chip-Enable,	t_{CEA}	–	280	–	230	–	180	ns
Access from Address,	t_{ADA}	–	300	–	250	–	200	ns
Previous Data Hold,	t_{PDH}	20	–	20	–	20	–	ns

Preliminary MW4050D

DYNAMIC ELECTRICAL CHARACTERISTICS – Cont'd

Refresh Cycle Times■

CHARACTERISTIC		LIMITS						UNITS
		MW4050D		MW4050DV1		MW4050DV2		
		Min.	Max.	Min.	Max.	Min.	Max.	
Refresh Cycle,	t_{RFC}	470	–	430	–	400	–	ns
Chip-Enable Active,	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active,	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise,	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall,	t_{CEf}	–	40	–	40	–	40	ns
Address Setup,	t_{ADS}	0	–	0	–	0	–	ns
Address Hold,	t_{ADH}	150	–	150	–	150	–	ns
Read Setup,	t_{RDS}	0	–	0	–	0	–	ns
Read Hold,●	t_{RDH}	40	–	40	–	40	–	ns
Refresh Period,	t_{RFR}	–	2	–	2	–	2	ms

■ Refresh is achieved by addressing A 0 to A 5 with both Chip-Enable and Read/$\overline{\text{Write}}$ high. The output is the stored data of the decoded addresses. Refresh is not affected by the states of Addresses A 6 to A 11. Refresh is also achieved during normal operation.

● Read Hold (t_{RDH}) is measured from the 10% point on the Chip-Enable input.

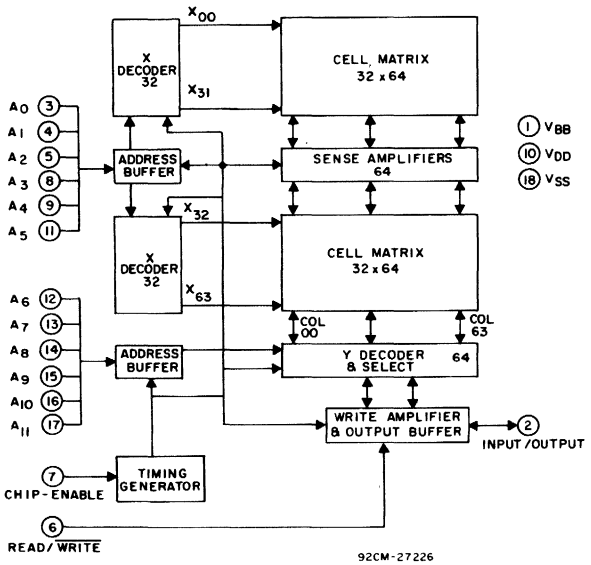


Fig. 2—Functional block diagram for MW4050D, MW4050DV1, and MW4050DV2.

Preliminary MW4060D

N-Channel 4096-Bit MOS Random-Access Memory

The RCA-MW4060D Series are 4096-word by 1-bit high-speed dynamic NMOS random-access memories. The use of N-channel silicon-gate technology in these devices optimizes the speed, density, and power consumption. The MW4060D Series is intended for large-scale high-performance memory systems in which low cost and high reliability are primary design objectives.

Three performance options of maximum access time are offered: 300 ns for the MW4060D, 250 ns for the MW4060DV1, and 200 ns for the MW4060DV2. They are direct replacements for the equivalent TMS-4060, TMS4060-1 and TMS4060-2. All inputs except the Chip-Enable are fully TTL-compatible requiring no specialized driver. One single clock (Chip-Enable) is employed for simplicity of system design. This low-capacitance input utilizes a nominal 12-V pulse.

The 3-State Data output buffer in these devices will drive two series 74- TTL gates. The Chip-Select input disables the input and output circuits for easy expansion of the memory and simple implementation of system refresh control. This input can be operated with negative set-up time relative to the Chip-Enable clock. This feature simplifies use in large memory systems where Chip-Select timing requirements may otherwise limit system performance.

The MW4060D design uses balanced sensing to eliminate pattern sensitivity. In addition, all bit and word lines in the array are clamped to preset potentials while the memory is quiescent. The X and Y decoders use push-pull drive to virtually eliminate the effects of unwanted capacitance coupling.

The MW4060D Series is supplied in a 22-lead hermetic dual-in-line ceramic side-brazed package.

Features:

- Organization — 4096 words by 1 bit
- Direct replacement for TMS4060
- TTL-compatible inputs (except Chip-Enable)
- Single low-capacitance clock
- Low power dissipation (typ.):
  0.2 mW/package standby
  400 mW/package operating
- 3-State output
- On-chip address registers
- Chip-Select simplifies memory expansion
- Chip-Select effective 30 ns after Chip-Enable
- Data-In can be valid up to 15 ns after Read/Write low level
- Separate Data-In and Data-Out circuits
- Clamped bit lines minimize pattern sensitivity problems
- N-channel silicon-gate technology
- 22-lead ceramic hermetic package

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE	−55 to +150°C
OPERATING TEMPERATURE RANGE	0 to +70°C
SUPPLY VOLTAGE RANGES:	
($V_{DD} - V_{BB}$)	20 to −0.3 V
($V_{CC} - V_{BB}$)	20 to −0.3 V
($V_{SS} - V_{BB}$)	20 to −0.3 V
INPUT VOLTAGE RANGES:	
Chip-Enable Input ($V_{CE} - V_{SS}$)	20 to −0.3 V
All Other Inputs ($V_{IN} - V_{SS}$)	20 to −0.3 V
OUTPUT VOLTAGE RANGE:	
($V_{DO} - V_{SS}$)	7 to −2 V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max..	+265°C

RCA Type No.	Access Time — ns Max.	Read or Write Cycle Time — ns Min.	Read/Modify/ Write Cycle Time — ns Min.
MW4060D	300	470	710
MW4060DV1	250	430	640
MW4060DV2	200	400	580

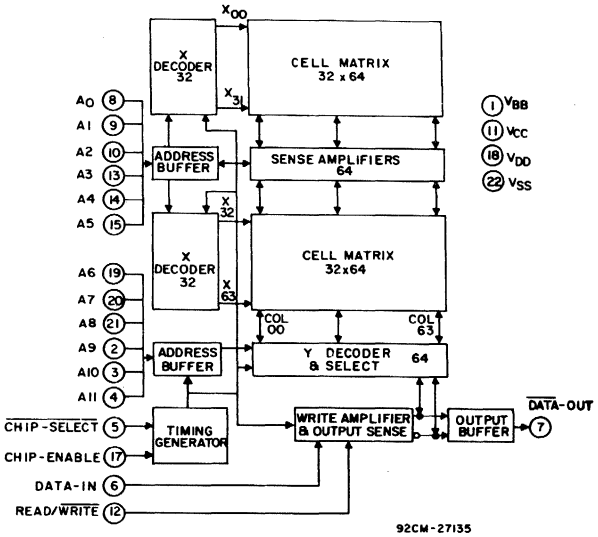


Fig. 1 — Functional block diagram for MW4060D, MW4060DV1, MW4060DV2.

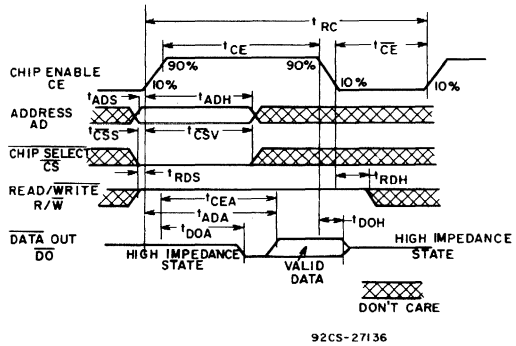


Fig. 2 — Read-cycle waveforms.

Preliminary MW4060D

OPERATIONAL MODES

MODE	CHIP-ENABLE CE	CHIP-SELECT $\overline{CS}$	READ/WRITE R/$\overline{W}$	DATA-OUT# $\overline{DO}$
Read	1	0	1	Complement of data stored
Write	1	0	0	Invalid data
Read/Modify/Write	1	0	1 then 0	Complement of data stored; then invalid data
Refresh	1	1	X	High impedance
Standby	0	X	X	High impedance

The memory inverts between Data-In and Data-Out. Actual internal levels stored in the array depend on bit location. A data input 1 is a stored internal high level if the address state of A3 is opposite to that of A6. This is transparent to the user.

1 = High level 0 = Low level X = Don't care

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC		LIMITS* ALL TYPES MIN.	TYP.	MAX.	UNITS
Supply Voltage:					
V_{DD}		11.4	12	12.6	V
V_{CC}		4.5	5	5.5	V
V_{BB}		−5.5	−5	−4.5	V
V_{SS}		–	0	–	V
Input Voltage, High-Level:					
Chip-Enable	V_{CEH}	V_{DD} − 0.6	–	V_{DD} + 1	V
All Others	V_{IH}	2.2	–	5.25	V
Input Voltage, Low-Level:					
Chip-Enable	V_{CEL}	−1	–	0.6	V
All Others	V_{IL}	−0.6	–	0.6	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{CC} = 5 V ± 10%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V

CHARACTERISTIC		TEST CONDITIONS	LIMITS*ALL TYPES Min.	Typ.	Max.	UNITS
Supply Current:						
For V_{DD}	I_{DDO}	V_{CEH} = 0.6 V	–	–	200	
For V_{CC}	I_{CCO}		–	0.2	–	μA
For V_{BB}	I_{BBO}		–	−5	−100	
Input Current, High-Level:						
Chip-Enable	I_{CEH}	V_{CE} = 13.6 V	–	–	2	μA
All Others	I_{IH}	V_I = 5.5 V	–	–	10	
Input Current, Low-Level:						
Chip-Enable	I_{CEL}	V_{CE} = −1 V	–	–	±10	μA
All Others	I_{IL}	V_I = −0.6 V	–	–	±10	
Output Current:						
Off-State	I_{OZ}	V_O = 0 to 5.5 V	–	–	±10	μA
Output Voltage:						
High Level	V_{OH}	I_O = 2 mA	2.4	–	–	V
Low Level	V_{OL}	I_O = 3.2 mA	V_{SS}	–	0.4	V

* All typical values are at T_A = 25°C and nominal supply voltages.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{CC} = 5 V ± 10%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V, Output load = 50 pF and one Series 74- gate.

CHARACTERISTIC		MW4060D Typ.	Max.	MW4060DV1 Typ.	Max.	MW4060DV2 Typ.	Max.	UNITS
V_{DD} Supply Current: At V_{CE} high level	$I_{DD}1$	–	60	–	60	–	60	mA
Average during Read or Write cycle	$I_{DD}2$	32	–	35	–	38	–	mA
Average during Read/ Modify/Write cycle	$I_{DD}3$	37	–	41	–	45	–	mA

CAPACITANCE at T_A = 0° to 70°C, V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, V_I = 0 V, V_{CE} = 0 V, f = 1 MHz, unless otherwise specified.

CHARACTERISTIC		TEST CONDITIONS	Min.	Typ.	Max.	UNITS
Address	C_{AD}		–	5	7	pF
Chip-Enable	C_{CE}	V_{CEH} = 10.8 V	–	18	22	pF
		V_{CEL} = −1 V	–	23	27	pF
Chip-Select	C_{CS}		–	4	6	pF
Data-In	C_{DI}		–	4	6	pF
Read/Write	C_{RW}		–	5	7	pF
Output	C_O		–	5	7	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0°C to 70°C, V_{DD} = 12 V ± 5%, V_{CC} = 5 V ± 10%, V_{BB} = −5 V ± 10%, V_{SS} = 0 V, Output Load = 50 pF and one Series 74- gate. All input timing measured from low input level (0.8 V) or high input level (2 V) to 10% or 90% point on V_{CE} transition edges. Output timing measured from low output level (0.4 V) or high output level (2.4 V) to 10% or 90% point on V_{CE} transition edges. Rise time (t_r) and fall time (t_f) from 10% to 90% of V_{CE} are 20 ns. For waveforms, see Figs. 2, 3, 4 and 5.

Read Cycle Times

CHARACTERISTIC		MW4060D Min.	Max.	MW4060DV1 Min.	Max.	MW4060DV2 Min.	Max.	UNITS
Read Cycle	t_{RC}	470	–	430	–	400	–	ns
Chip-Enable Active	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall	t_{CEf}	–	40	–	40	–	40	ns
Address Setup	t_{ADS}	0	–	0	–	0	–	ns
Address Hold	t_{ADH}	150	–	150	–	150	–	ns
Chip-Select Setup*	$t_{\overline{CS}S}$	−30	–	−30	–	−30	–	ns
Chip-Select Valid●	$t_{\overline{CS}V}$	150	–	150	–	150	–	ns
Read Setup	t_{RDS}	0	–	0	–	0	–	ns
Read Hold●	t_{RDH}	40	–	40	–	40	–	ns
Access from Chip-Enable	t_{CEA}	–	280	–	230	–	180	ns
Access from Address	t_{ADA}	–	300	–	250	–	200	ns
Data-Out Active	t_{DOA}	–	250	–	200	–	150	ns
Data-Out Hold	t_{DOH}	30	–	30	–	30	–	ns

Write Cycle Times

CHARACTERISTIC		MW4060D Min.	Max.	MW4060DV1 Min.	Max.	MW4060DV2 Min.	Max.	UNITS
Write Cycle	t_{WC}	470	–	430	–	400	–	ns
Chip-Enable Active	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall	t_{CEf}	–	40	–	40	–	40	ns
Address Setup	t_{ADS}	0	–	0	–	0	–	ns
Address Hold	t_{ADH}	150	–	150	–	150	–	ns
Chip-Select Setup*	$t_{\overline{CS}S}$	−30	–	−30	–	−30	–	ns
Chip-Select Valid●	$t_{\overline{CS}V}$	150	–	150	–	150	–	ns
Write Setup	t_{WRS}	240	–	220	–	210	–	ns
Write Width	t_{WRW}	200	–	190	–	180	–	ns
Data-In Setup△	t_{DIS}	−15	–	−15	–	−15	–	ns
Data-In Hold	t_{DIH}	40	–	40	–	40	–	ns

Read/Modify/Write Cycle Times

CHARACTERISTIC		MW4060D Min.	Max.	MW4060DV1 Min.	Max.	MW4060DV2 Min.	Max.	UNITS
Read/Modify/Write Cycle	t_{RWC}	710	–	640	–	580	–	ns
Chip-Enable Active	t_{CE}	540	4000	470	4000	410	4000	ns
Chip-Enable Non-active	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall	t_{CEf}	–	40	–	40	–	40	ns
Address Setup	t_{ADS}	0	–	0	–	0	–	ns
Address Hold	t_{ADH}	150	–	150	–	150	–	ns
Chip-Select Setup*	$t_{\overline{CS}S}$	−30	–	−30	–	−30	–	ns
Chip-Select Valid●	$t_{\overline{CS}V}$	150	–	150	–	150	–	ns
Read Setup	t_{RDS}	0	–	0	–	0	–	ns
Read Width●	t_{RDW}	280	–	230	–	180	–	ns
Write Setup	t_{WRS}	240	–	220	–	210	–	ns
Write Width	t_{WRW}	200	–	190	–	180	–	ns
Data-In Setup△	t_{DIS}	−15	–	−15	–	−15	–	ns
Data-In Hold	t_{DIH}	40	–	40	–	40	–	ns
Access from Chip-Enable	t_{CEA}	–	280	–	230	–	180	ns
Access from Address	t_{ADA}	–	300	–	250	–	200	ns
Data-Out Active	t_{DOA}	–	250	–	200	–	150	ns
Data-Out Hold	t_{DOH}	30	–	30	–	30	–	ns
Previous Data Hold	t_{PDH}	30	–	30	–	30	–	ns

* $\overline{\text{Chip-Select}}$ input is allowed to occur 30 ns after the Chip-Enable input is present.

△ New Data-In need not be valid until 15 ns after the Read/$\overline{\text{Write}}$ input is low.

● $\overline{\text{Chip-Select}}$ Valid ($t_{\overline{CS}V}$) and Read Hold (t_{RDH}) are measured from 10% points on the Chip-Enable input.

Preliminary MW4060D

Refresh Cycle Times■

CHARACTERISTIC		LIMITS						UNITS
		MW4060D		MW4060DV1		MW4060DV2		
		Min.	Max.	Min.	Max.	Min.	Max.	
Refresh Cycle	t_{RFC}	470	–	430	–	400	–	ns
Chip-Enable Active	t_{CE}	300	4000	260	4000	230	4000	ns
Chip-Enable Non-active	$t_{\overline{CE}}$	130	–	130	–	130	–	ns
Chip-Enable Rise	t_{CEr}	–	40	–	40	–	40	ns
Chip-Enable Fall	t_{CEf}	–	40	–	40	–	40	ns
Address Setup	t_{ADS}	0	–	0	–	0	–	ns
Address Hold	t_{ADH}	150	–	150	–	150	–	ns
Chip-Select Setup*	$t_{\overline{CS}S}$	−30	–	−30	–	−30	–	ns
Chip-Select Valid●	$t_{\overline{CS}V}$	150	–	150	–	150	–	ns
Refresh Period	t_{RFR}	–	2	–	2	–	2	ms

* $\overline{\text{Chip-Select}}$ input is allowed to occur 30 ns after the Chip-Enable input is present.

Δ New Data-In need not be valid until 15 ns after the Read/$\overline{\text{Write}}$ input is low.

● $\overline{\text{Chip-Select}}$ Valid ($t_{\overline{CS}V}$) and Read Width (t_{RDW}) are measured from 10% point on the Chip-Enable input.

■ Refresh is achieved by addressing A_0 to A_5 with both $\overline{\text{Chip-Select}}$ and Chip-Enable high. A high-impedance state exists at the output and refresh is not affected by the states of Read/ $\overline{\text{Write}}$ or Addresses A_6 to A_{11}. Refresh is also achieved during normal operation.

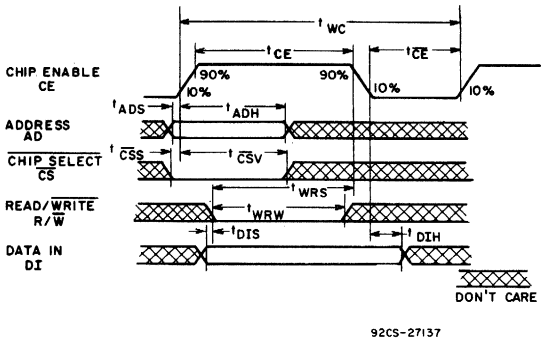


Fig.3 – Write-cycle waveforms.

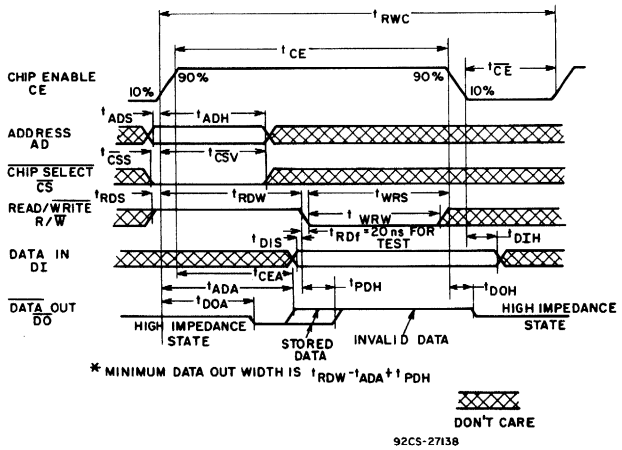


Fig.4 – Read/modify/write-cycle waveforms.

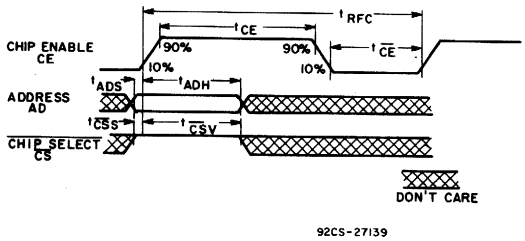


Fig.5 – Refresh cycle waveforms.

MW7001ID

N-Channel 1024-Word by 1-Bit LSI Static Random-Access Memory

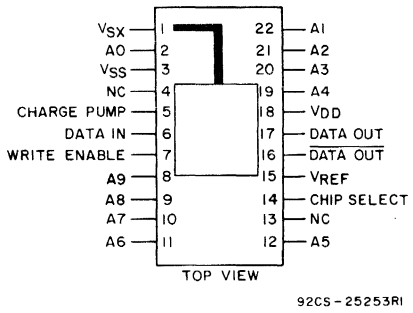
The RCA-MW7001ID is a 1024-word by 1-bit static random access memory fabricated with industry-proven high-yield n-channel metal-gate MOS technology. A novel refresh mechanism utilizing internal charge pumps enables static operation without the need for periodic refresh cycles. It is designed for high performance, low cost, and large bit-storage applications.

The MW7001ID has on-chip Address input latches and requires only a low-level voltage swing (TTL levels) at all inputs, except Chip Select. TTL voltage levels greatly simplify over-all system design, and minimize the cost of memory systems of all sizes built with the MW7001ID. Additional economies can be realized from the low standby power consumption of this device.

The low output capacitance allows OR-typing of ten[1] MW7001ID's with no noticeable degradation in speed. A separate Chip Select lead allows easy selection of an individual device when output are OR-tied.

The RCA-7001ID is packaged in 22-lead hermetic ceramic dual-in-line package.

[1] Increases access 4 ns



Terminal Assignment

Features

- **Organization – 1024 words by 1 bit**
- **TTL-compatible inputs (except chip select)**
- **Static memory – no refresh period**
- **Low power dissipation: 510 μW/Bit max. operating 15 μW/Bit max. standby**
- **Access time – 60 ns max.**
- **Cycle time – 180 ns max.**
- **On-chip address input latches**
- **Differential output sink current**
- **Chip select – simplifies memory expansion**
- **OR-tie capability**
- **Standard 22-pin ceramic hermetic package**
- **Direct replacement for AMS7001I, MCM7001I**

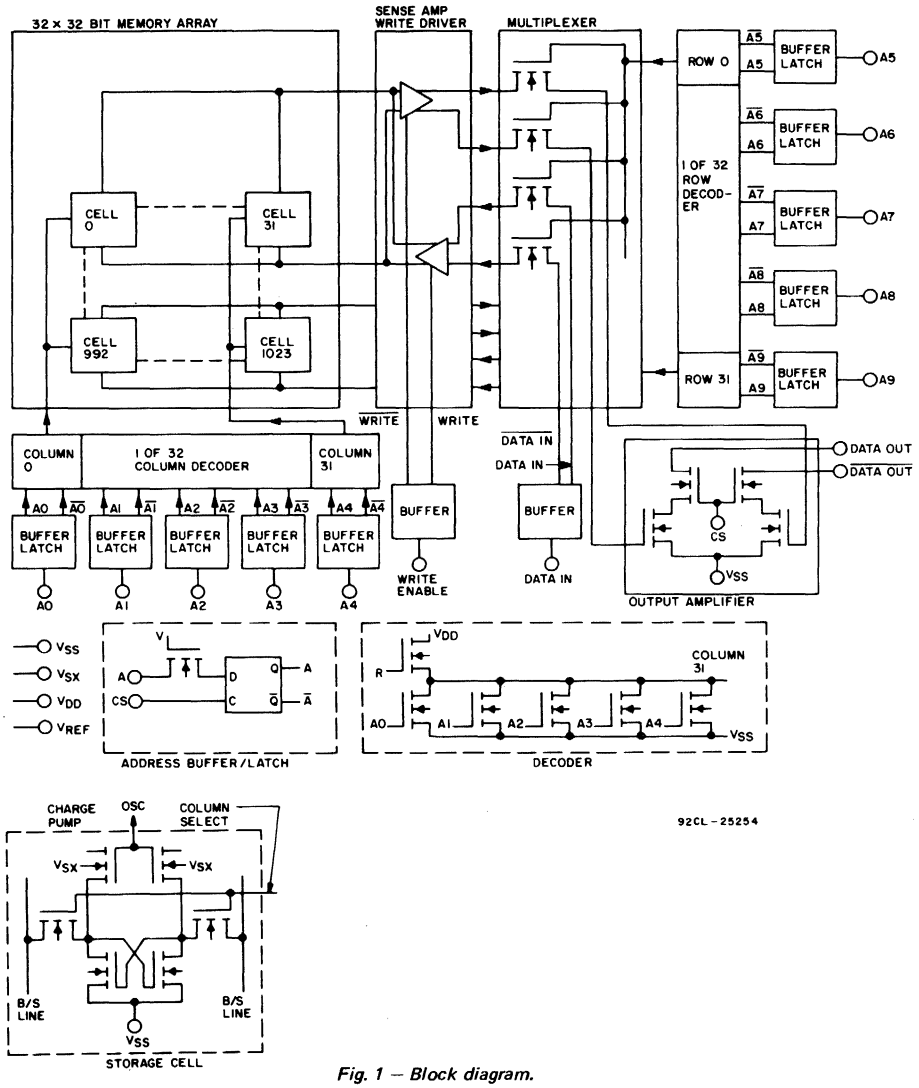


Fig. 1 – Block diagram.

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE TEMPERATURE
RANGE ..... −55 to +125°C
OPERATING TEMPERATURE
RANGE* ..... 0 to +70°C
SUPPLY VOLTAGE RANGES
($V_{DD} - V_{SS}$)
($V_{REF} - V_{SS}$) ..... +25 to −0.5 V
($V_{SX} - V_{SS}$) ..... −10 to +0.5 V
($V_{DD} - V_{SX}$), ($V_{REF} - V_{SX}$) +30 to −0.5 V
($V_{REF} - V_{DD}$) ..... −25 to +0.5 V
INPUT VOLTAGE RANGE
($V_I - V_{SS}$) ..... +30 to −0.5 V
OUTPUT VOLTAGE RANGE
($V_O - V_{SS}$) ..... +30 to −0.5 V
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 in.
(1.59 ±0.79 mm) from case for
10 s max. ..... +265°C

*200 linear feet/minute airflow.

MW7001ID

STATIC ELECTRICAL CHARACTERISTICS

T_A=0°C to 70°C, V_{SS}=0 V, V_{SX}= −3V ±10%, V_{DD}= +15V ±5%, V_{REF} = +7.5 V ±5%

CHARACTERISTIC	TEST CONDITIONS	Min.	Typ.[1]	Max.	UNITS
Supply Current:	STANDBY				
For V_{SX} (I_{SX})		–	–	150	μA
For V_{DD} (I_{DD})		–	1.2	300	μA
For V_{REF} (I_{REF})	(Chip Select = V_{SS})	–	–	100	μA
For V_{SS} (I_{SS})		–	400	1000	μA
Input Current High-Level Chip-Select ($I_{\overline{CS}}H$)	$V_{CS}H = V_{DD}$	–	–	20	mA
All Others (Selected) (I_IH)	V_{IH}=4V, Chip Select = V_{SS}	–	0.2	20	μA
Change Pump ($I_{QP}L$)	$V_{QP}H = V_{DD}$	–	–	±20	μA
Input Current Low-Level: Chip Select ($I_{CS}L$)	Address = High $V_{CS}L = V_{SS}$	–	–	±50	μA
All Others (Selected (I_IL)	$V_{IL} = V_{CS}L = V_{SS}$	–	−0.2	±20	μA
Charge Pump ($I_{QP}L$)	$V_{QP}L = V_{SX}$ = 5V	–	–	±20	μA
Differential Output Current (Sink) (I_O)	Flowing into Data Out terminal when reading a stored high	0.1	1	–	mA
Output Leakage Current (I_{OL})	$V_O = V_{REF}$ Chip Select = V_{SS}	–	–	2	μA
Input Voltage: High Level (V_IH)		2.4	–	V_{REF}	V
Low Level (V_IL)		V_{SS}−0.5	–	V_{SS}+0.8	V
Chip Select Voltage: High-Level ($V_{CS}H$)		V_{DD}−1	–	V_{DD}+1	V
Low-Level ($V_{CS}L$)		V_{SS}−0.5	–	V_{SS}+1	V
Charge Pump Input Voltage High-Level ($V_{QP}H$)		V_{REF}+2	–	12	V
Charge Pump Input Voltage Low-Level ($V_{QP}L$)		V_{SX}−5	–	V_{SX}−2	V

1 Typical currents are at 25°C. 2 Operating supply currents are maximum at 0°C.

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{SS} = 0 V, V_{SX} = −3 V ± 10%, V_{DD} = +15 V ±5, V_{REF} = +7.5 V ±5%

Rise Time (t_r) And Fall Time (t_f) From 10% to 90% Are 4 ns Minimum, 20 ns Maximum

CHARACTERISTIC	SYMBOL	Min.	Typ.[1]	Max.	UNITS
Average Operating Currents (Supply Currents are Maximum at T_A=0°C, Duty Cycle Time=180 ns)					
Supply Current:					
For V_{SX}	I_{SXO}	–	–	±175	μA
For V_{DD}	I_{DDO}	–	24	40	mA
For V_{REF}	I_{REFO}	–	–	10	mA
For V_{SS}	I_{SSO}	–	−45	−65	mA
Read Cycle Times					
Chip Select	t_{CS}	80	–	500	ns
Unselected	$t_{\overline{CS}}$	100	–	–	ns
Address Set Up	t_{ASU}	0	–	–	ns
Address Hold	t_{AH}	40	–	–	ns
Write Enable Set Up	t_{WS}	0	–	–	ns
Write Enable Hold	t_{WHR}	0	–	–	ns
Access Time (t_r (CS) = 10 ns)	t_{ACC}	–	45	60	ns
Read Cycle	t_{RC}	180	–	–	ns
Write Cycle Times					
Chip Select	t_{CS}	80	–	500	ns
Unselected	$t_{\overline{CS}}$	100	–	–	ns
Address Set Up	t_{ASU}	0	–	–	ns
Address Hold	t_{AH}	40	–	–	ns
Write Enable	t_{WW}	0	–	–	ns
Write Enable Hold	t_{WHW}	0	–	–	ns
Input Data Set Up	t_{DSU}	0	–	–	ns
Input Data Hold	t_{DHO}	0	–	–	ns
Write Cycle	t_{WC}	180	–	–	ns
Charge Pump Input Pulse					
Frequency	f_p	–	–	4	MHz
Duty Cycle	–	25	–	75	%
Rise Time	t_r	100	–	250	ns
Fall Time	t_f	100	–	250	ns
Capacitance (V_I = V_{SS}, f = 1 MHz Unless Otherwise Specified)					
Address	C_{AD}	–	–	6	pF
Chip-Select	C_{CS}	–	–	60	pF
Write-Enable	C_{WE}	–	–	6	pF
Data Input	C_{DI}	–	–	6	pF
Data Output	C_{DO}	–	–	6	pF
Change Pump (V_{CP} = V_{SS})	C_{QP}	–	–	70	pF
Change Pump (V_{CP} = V_{SX})*	C_{QP}	–	–	100	pF

*Device not under power

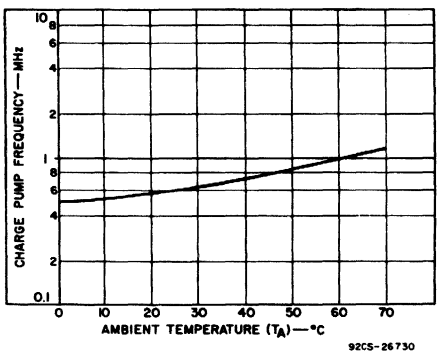


Fig. 2 — Minimum charge pump frequency vs. ambient temperature.

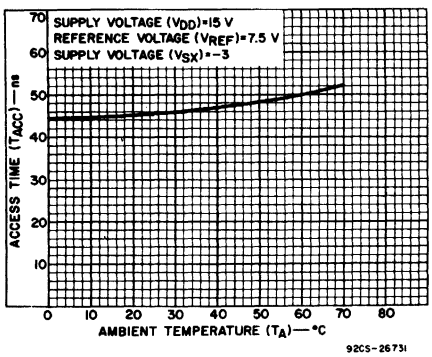


Fig. 3 — Access time vs. ambient temperature.

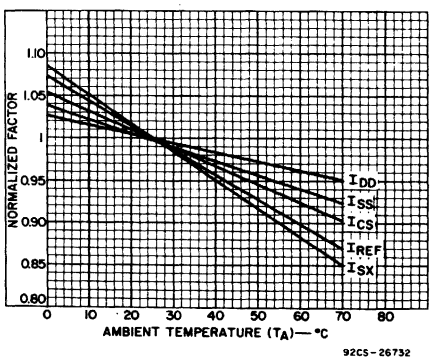


Fig. 4 — Normalized current vs. ambient temperature.

MW7001ID

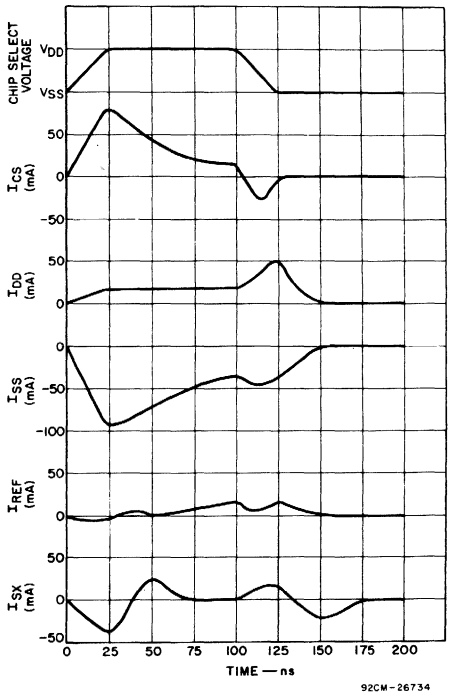
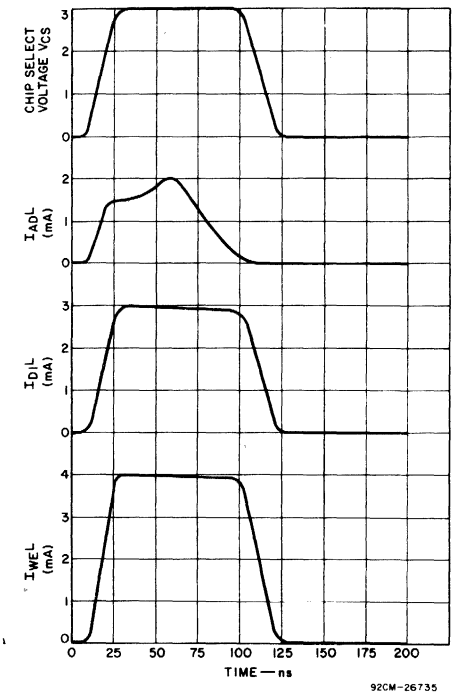
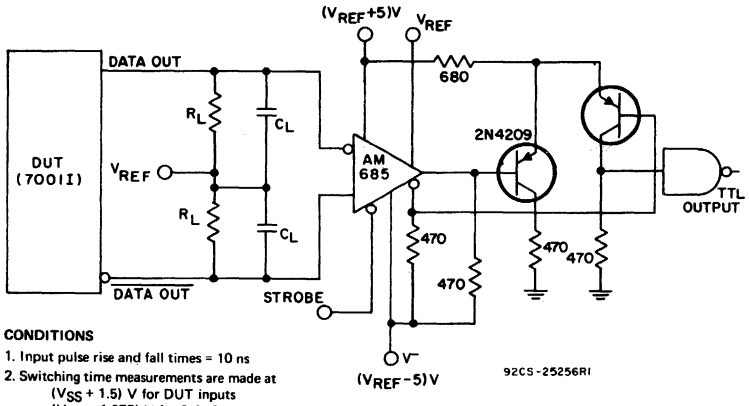


Fig. 5a — Typical supply circuit waveforms during selection period.



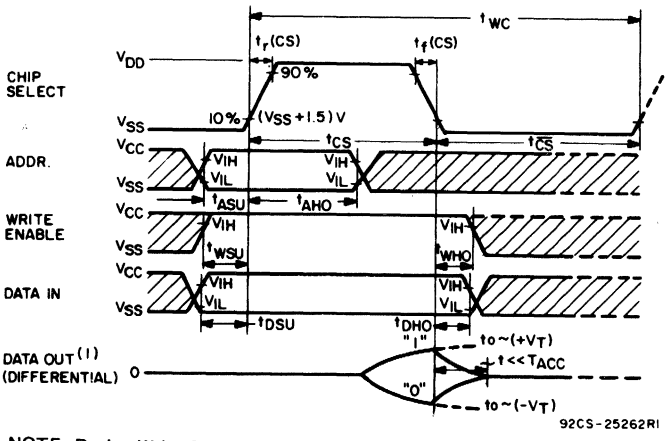
b — Typical current waveforms during selection period.



CONDITIONS

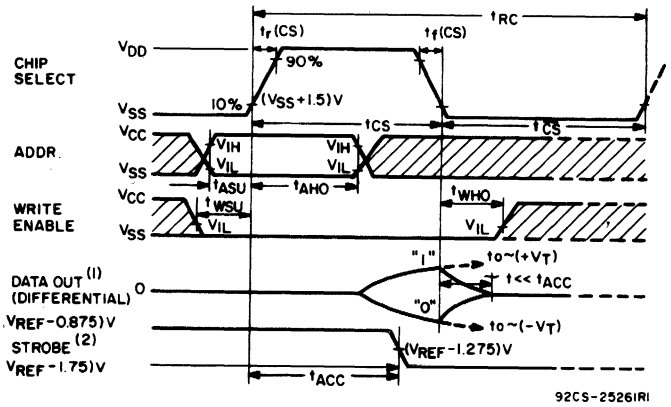
1. Input pulse rise and fall times = 10 ns
2. Switching time measurements are made at
   (V_{SS} + 1.5) V for DUT inputs
   (V_{CC} −1.275) V for S.A. Strobe Input
3. Output Loading is
   R_L = 100 Ω
   C_L = (30 pF Includes device and jig capacitance)

Fig.6 — Test load.



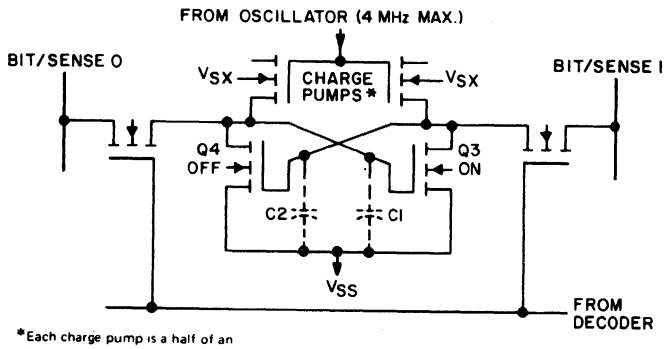
NOTE: During Write Cycle Data Out reflects Data In.

Fig. 8b. — Write cycle waveforms.



NOTES 1: Voltage at Data Out Terminal with respect to Data Out.
2: Strobe signal at Strobe Input of Sense Amplifier Latch.

Fig. 8a. — Read cycle waveforms.



*Each charge pump is a half of an MOS Transistor that acts as a current source to replenish the charge lost in C1 and C2.

Fig. 7 — Memory cell configuration.

Preliminary MWS5001D

SOS 1024-Bit COS/MOS LSI Static Random Access Memory

Features:

- **Organization—1024 words by 1 bit**
- **Fully static operation—no external clocks required**
- **Access time—150 ns (typ.) @ V_{DD} = 5 V**
- **Cycle time—160 ns (typ.) @ V_{DD} = 5 V**
- **Low power dissipation:**
  - **0.1 μW/Bit (typ.) standby @ V_{DD} = 5 V**
  - **4 μW/Bit (typ.) operating @ V_{DD} = 5 V**
- **Operation from a single power supply—V_{DD} = 4.5 to 6 V**
- **High noise immunity—30% of V_{DD} (typ.)**
- **TTL output drive capability**
- **Three-state data output for bus-oriented systems**

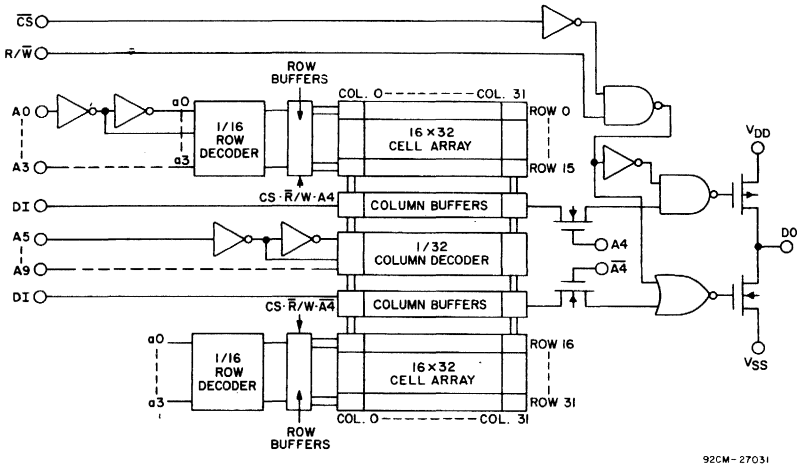


Fig. 1—Functional block diagram.

The RCA-MWS5001D is a 1024-word by 1-bit static random access memory designed for use in memory systems where high speed, low power, and ease of use are primary design requirements. These characteristics are obtained primarily from the use of self-aligned silicon-gate COS/MOS SOS technology.

The output state of the MWS5001D is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip select input or any other input terminal for fully static operation, therefore the chip select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$=1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The MWS5001 is supplied in a hermetically sealed 16-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

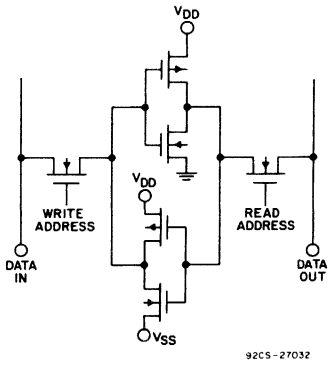


Fig. 2—Memory cell configuration.

TRUTH TABLE

INPUTS		OUTPUT
READ/ WRITE R/$\overline{W}$	CHIP-SELECT $\overline{CS}$	DATA OUTPUT DO
X	1	High Impedance
0	X	High Impedance
1	0	Contents of Addressed Cell

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE ..... −65 to +150°C
OPERATING TEMPERATURE RANGE ..... −20 to +85°C
DC SUPPLY VOLTAGE RANGE (V_{DD}−V_{SS}) ..... −0.5 to +6 V
ALL INPUTS ..... $V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE (V_{DD}−V_{SS}) ..... 4.5 to 6 V
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V ± 5%

CHARACTERISTIC		TEST CONDITIONS		TYPICAL VALUES	UNITS
			V_O (V)		
Quiescent Device Current*	I_L			20	μA
Quiescent Device Dissipation*	P_D			100	μW
Output Voltage:					
Low Level	V_{OL}			0.01	V
High Level	V_{OH}			4.99	V
Noise Immunity	V_{NL}	All Inputs	3.6	1.5	V
	V_{NH}	All Inputs	1.4	1.5	V
Output Drive Current:					
N-Channel (Sink)	I_{DN}	Data Output (Sink)	0.4	2	mA
P-Channel (Source)	I_{DP}	Data Output (Source)	4.6	1	mA
Data Output Off-Resistance	R_O(Off)	Data Output High Impedance State		5	MΩ
Input Current	I_I	Any Input		1	nA

* Standby current is independent of any input state.

Preliminary MWS5001D

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V ± 5%, Input t_r,t_f = 20 ns, and C_L = 30 pF

CHARACTERISTIC		TYPICAL VALUES	UNITS
Read Cycle Times:			
Read Access	t_{RA}	150	ns
Read Cycle	t_{RC}	160	ns
Output Enable	t_{EN}	60	ns
Read/Write Hold	t_{WH}	50	ns
Read/Write Set-Up	t_{WS}	50	ns
Output Disable	t_{DIS}	20	ns
Write Cycle Times:			
Write Cycle	t_{WC}	160	ns
Read/Write Hold	t_{WH}	50	ns
Read/Write Pulse Width	t_W	60	ns
Read/Write Set-Up	t_{WS}	50	ns
Input Data Set-Up	t_{DS}	30	ns
Input Data Hold	t_{DH}	30	ns
Read/Modify/Write Cycle Times:			
Read/Modify/Write Cycle	t_{MC}	270	ns
Read Hold	t_{RH}	160	ns
Read Access	t_{RA}	150	ns
Output Enable	t_{EN}	60	ns
Read/Write Pulse Width	t_W	60	ns
Read/Write Set-Up	t_{WS}	50	ns
Input Data Set-Up	t_{DS}	30	ns
Input Data Hold	t_{DH}	30	ns
Output Disable	t_{DIS}	20	ns

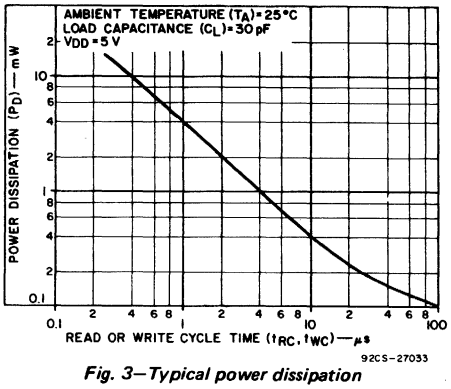


Fig. 3—Typical power dissipation vs. cycle time.

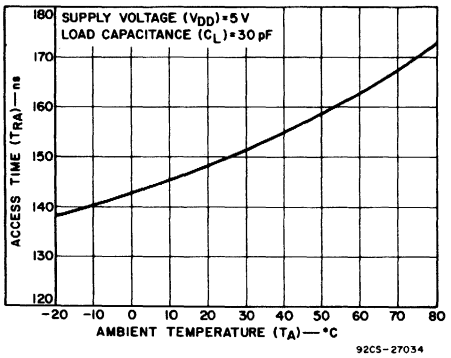
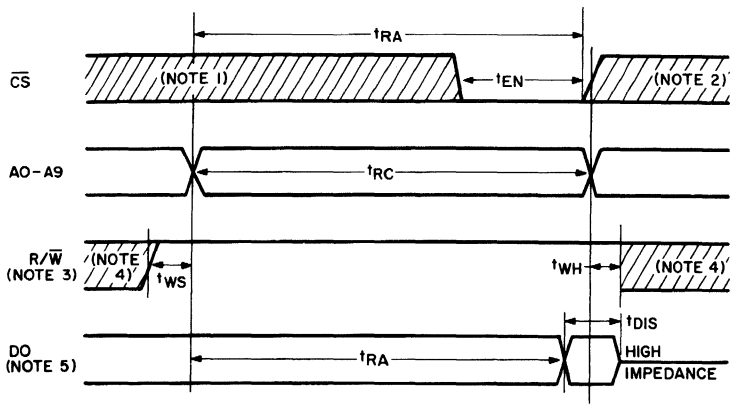
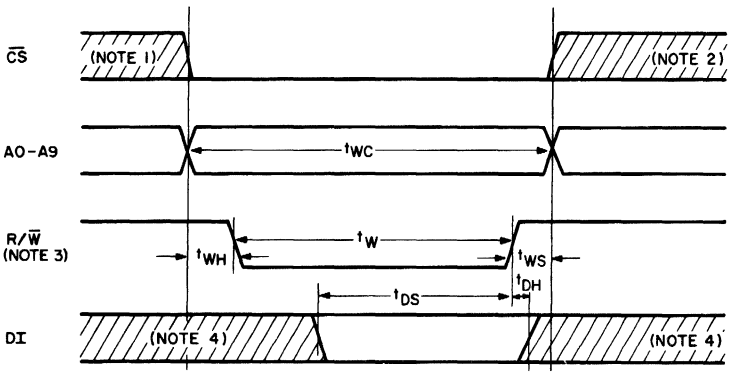


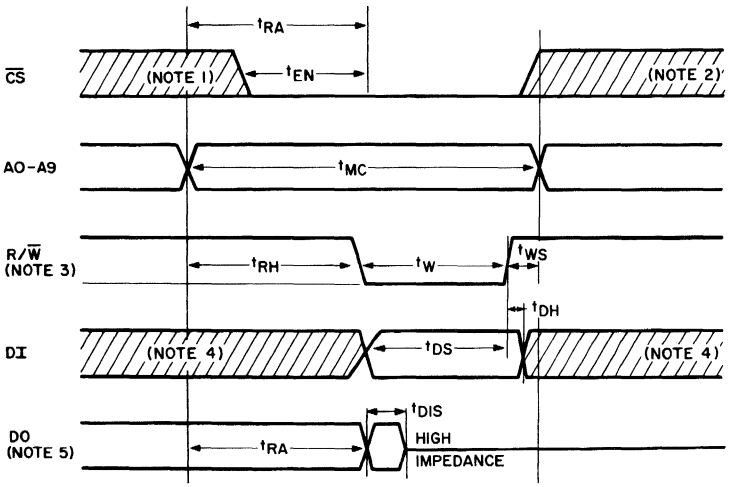
Fig. 4—Typical access time vs. ambient temperature.



READ-CYCLE WAVEFORMS.



WRITE-CYCLE WAVEFORMS.



READ/MODIFY/WRITE-CYCLE WAVEFORMS.

92CL-27035

Fig. 5—Read cycle, write cycle, and read/modify/write cycle waveforms.

Note 1. Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
Note 2. Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
Note 3. Read/Write (R/$\overline{W}$) must be at a high level during all address transitions.
Note 4. Don't care.
Note 5. Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/$\overline{W}$ or the rising edge of $\overline{CS}$.

Preliminary MWS5040D

SOS 256-Word by 4-Bit COS/MOS LSI Static Random-Access Memory

The RCA-MWS5040D is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, low power, and simplicity in use are desirable. The design of this device utilizes self-aligned silicon-gate technology. The MWS5040D has separate data inputs and data outputs and is operated from a single 5-volt supply. Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. After valid data appears at the output, the address inputs may be changed immediately. This output data will be valid until either the Output Disable input or the Chip-Select input is high, or the new data of the next memory cycle is applied.

The MWS5040D is supplied in a 22-lead hermetic dual-in-line side-brazed ceramic package (D suffix), and in chip form (H suffix).

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE TEMPERATURE RANGE . . . . . −65 to +150°C

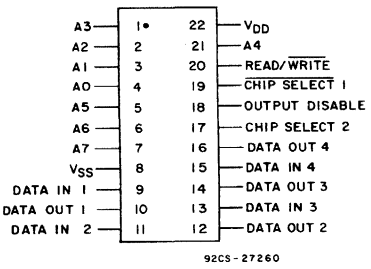
OPERATING TEMPERATURE RANGE . . . . . −20 to +85°C

DC SUPPLY VOLTAGE RANGE (V_{DD}–V_{SS}) . . . . . −0.5 to +6 V

ALL INPUTS . . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$

RECOMMENDED DC SUPPLY VOLTAGE (V_{DD}–V_{SS}) . . . . . 4.5 to 6 V

LEAD TEMPERATURE (During Soldering):
At distance 1/16±1/32 inch (1.59±0.79 mm) from case for 10 seconds max . . . 265°C



TERMINAL ASSIGNMENT

Features:

- Organization – 256 words by 4 bits
- Fully static operation – no external clocks required
- Access time – 150 ns (typ.) @ V_{DD} = 5 V
- Cycle time – 160 ns (typ.) @ V_{DD} = 5 V
- Low power dissipation:
  0.15 mW/package standby @ V_{DD} = 5V
  4 mW/package operating @ V_{DD} = 5 V
- Separate data inputs and outputs
- Two Chip-Select inputs to simplify memory system expansion
- Output Disable to allow common I/O system
- Operation from a single power supply – V_{DD} = 4.5 to 6 V
- High noise immunity – 30% of V_{DD} (typ.)
- TTL output drive capability
- Three-state data output for bus-oriented systems
- Pin-compatible with Intel 5101

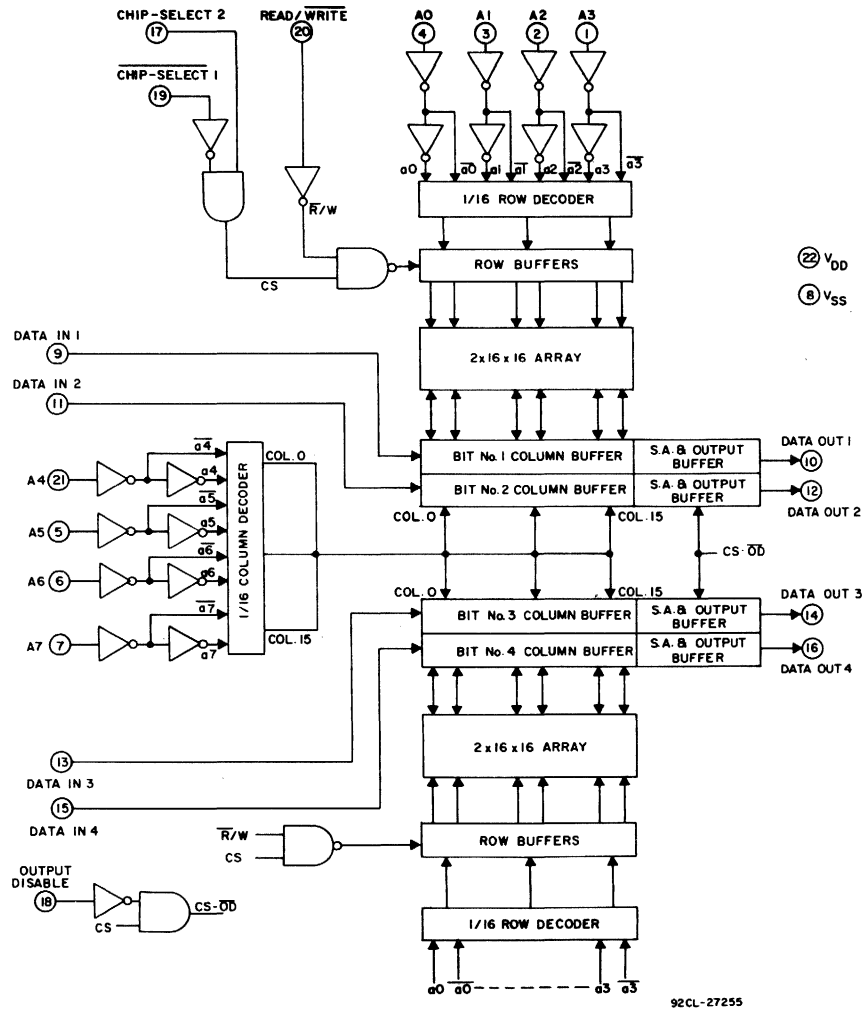


Fig. 1 – Functional block diagram for MWS5040D.

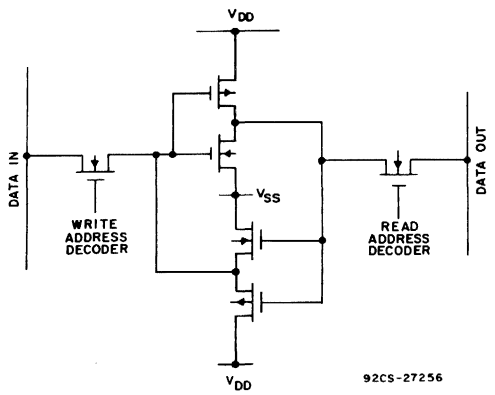


Fig. 2 – Memory cell configuration for MWS5040D.

Preliminary MWS5040D

OPERATIONAL MODES

MODE	READ/$\overline{\text{WRITE}}$ R/$\overline{W}$	$\overline{\text{CHIP SELECT 1}}$ $\overline{CS_1}$	CHIP SELECT 2 CS_2	OUTPUT DISABLE OD	DATA OUT DO
Read	1	0	1	0	Storage State of Addressed Cell
Write	0	0	1	1	High Impedance
Write	0	0	1	0	New Data In State
Standby	X	1	X	X	High Impedance
Standby	X	X	0	X	High Impedance
Output Disable	X	X	X	1	High Impedance

LOGIC 1 = HIGH LOGIC 0 = LOW X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V ± 5%

CHARACTERISTIC		TEST CONDITIONS	(V_O (V)	TYPICAL VALUES	UNITS
Quiescent Device Current*	I_L			30	μA
Quiescent Device Dissipation*	P_D			150	μW
Output Voltage:					
Low Level	V_{OL}			0.01	V
High Level	V_{OH}			4.99	V
Noise Margin▲	V_{NML}	All Inputs	0.5	1	V
	V_{NMH}	All Inputs	4.5	1	V
Output Drive Current:					
N-Channel (Sink)	I_{DN}	Data Output (Sink)	0.4	2	mA
P-Channel (Source)	I_{DP}	Data Output (Source)	4.6	1	mA
Data Output Off-Resistance	R_O(Off)	Data Output High Impedance State		5	MΩ

* Standby current is independent of any input state.

▲ Input high level = 3.5 V, input low level = 1.5 V for non-inverting inputs.

CAPACITANCES at T_A = −20 to +80°C, V_{DD} = 5 V
V_I = 0 V, V_{SS} = 0 V, f = 1 MHz

CHARACTERISTIC		TYPICAL VALUES	UNITS
Input	C_I	5	pF
Output	C_O	5	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5V ±5%,
Input t_r, t_f = 20 ns, and C_L = 30 pF. For waveforms, see Fig. 3.

Read Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Read Cycle	t_{RC}	160	ns
Access from Address	t_{ADA}	150	ns
Read Setup	t_{RDS}	50	ns
Read Hold	t_{RDH}	50	ns
Output Active from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	25	ns
Output Active from Chip-Select 2	t_{DOA2}	20	ns
Output Active from Output Disable	t_{DOA3}	20	ns
Output Hold from Chip-Select 1	t_{DOH1}	25	ns
Output Hold from Chip-Select 2	t_{DOH2}	20	ns
Output Hold from Output Disable	t_{DOH3}	20	ns

Write Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Write Cycle	t_{WC}	160	ns
$\overline{\text{Chip-Select 1}}$ Setup	$t_{\overline{CSS1}}$	70	ns
Chip-Select 2 Setup	t_{CSS2}	60	ns
Read Hold	t_{RDH}	50	ns
Write Setup	t_{WRS}	110	ns
Write Width	t_{WRW}	60	ns
Data In Width Effective	t_{DIW}	30	ns
Data In Hold	t_{DIH}	30	ns

Read/Modify/Write Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Read/Modity/Write Cycle	t_{RWC}	270	ns
Access from Address	t_{ADA}	150	ns
Read Width	t_{RDW}	160	ns
Write Setup	t_{WRS}	110	ns
Write Width	t_{WRW}	60	ns
Previous Data Hold	t_{PDH}	20	ns
Data In Width Effective	t_{DIW}	30	ns
Data In Hold	t_{DIH}	30	ns
Output Active from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	25	ns
Output Active from Chip-Select 2	t_{DOA2}	20	ns
Output Active from Output Disable	t_{DOA3}	20	ns
$\overline{\text{Chip-Select 1}}$ Hold	$t_{\overline{CSH1}}$	5	ns
Chip-Select 2 Hold	t_{CSH2}	0	ns
Output Hold from Output Disable	t_{DOH}	20	ns

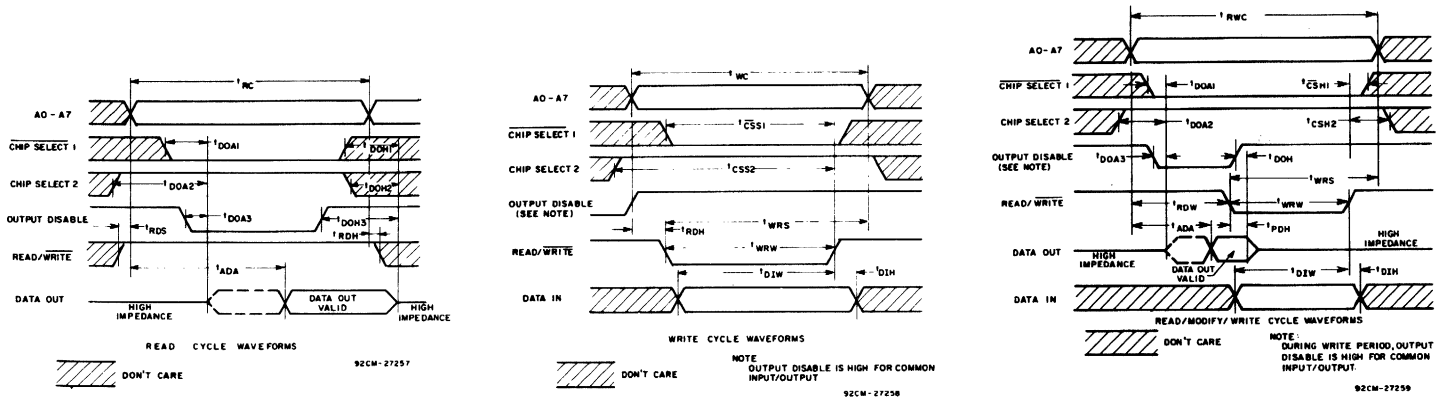


Fig. 3 — Read cycle, write cycle, and read/modify/write cycle waveforms.

Preliminary MWS5501D

SOS 1024-Bit COS/MOS LSI Static Random Access Memory

The RCA-MWS5501D is a 1024-word by 1-bit static random access memory designed for use in memory systems where high speed, low power, and ease of use are primary design requirements. These characteristics are obtained primarily from the use of self-aligned silicon-gate COS/MOS SOS technology.

The output state of the MWS5501D is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip select input or any other input terminal for fully static operation, therefore the chip select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$=1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

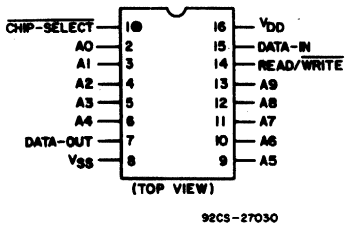
The MWS5501 is supplied in a hermetically sealed 16-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE TEMPERATURE RANGE ..... −65 to +150°C
OPERATING TEMPERATURE RANGE ..... −20 to +85°C
DC SUPPLY VOLTAGE RANGE
(V_{DD}−V_{SS}) ..... −0.5 to +11 V
ALL INPUTS ..... $V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE
(V_{DD}−V_{SS}) ..... 4.5 to 10 V
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

Features:

- **Organization—1024 words by 1 bit**
- **Fully static operation—no external clocks required**
- **Access time— 90 ns (typ.) @ V_{DD} = 10 V**
- **Cycle time—100 ns (typ.) @ V_{DD} = 10 V**
- **Low power dissipation:**
  3 μW/Bit (typ.) standby @ V_{DD} = 10 V
  20 μW/Bit (typ.) operating @ V_{DD} = 10 V
- **Operation from a single power supply—V_{DD} = 4.5 to 10 V**
- **High noise immunity—30% of V_{DD} (typ.)**
- **TTL output drive capability**
- **Three-state data output for bus-oriented systems**
- **Pin compatible with 6508 types**



Terminal Assignment

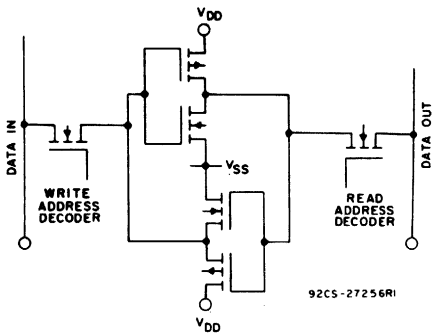


Fig. 2—Memory cell configuration.

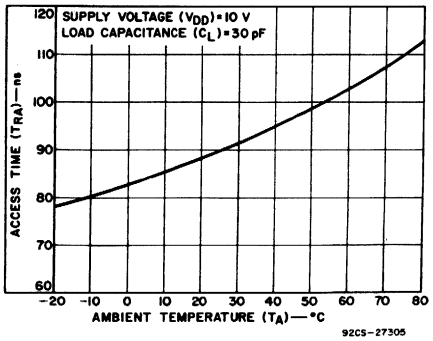


Fig. 3 — Typical access time vs. ambient temperature.

OPERATIONAL MODES

MODE	INPUTS		OUTPUT
	READ/WRITE R/$\overline{W}$	CHIP-SELECT $\overline{CS}$	DATA OUTPUT DO
Standby	X	1	High Impedance
Write	0	X	High Impedance
Read	1	0	Contents of Addressed Cell

X = DON'T CARE
LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

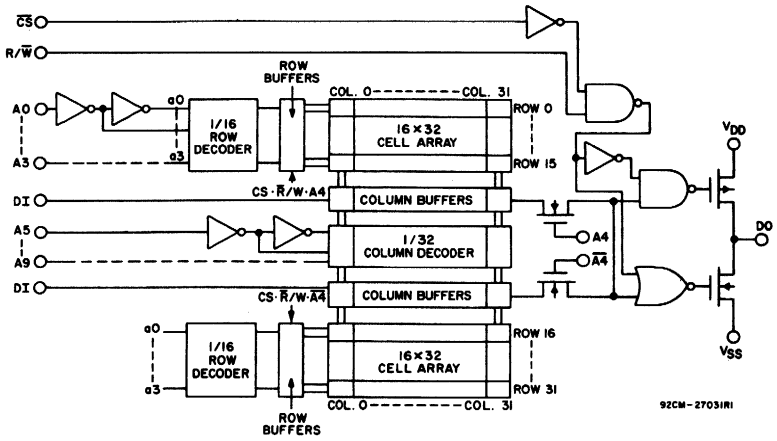


Fig. 1—Functional block diagram.

Preliminary MWS5501D

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V_{DD} = 10\ V \pm 5\%$

CHARACTERISTIC		TEST CONDITIONS		TYPICAL VALUES	UNITS
			V_O (V)		
Quiescent Device Current *	I_L			300	μA
Quiescent Device Dissipation *	P_D			3000	μW
Output Voltage:					
Low Level	V_{OL}			0.01	V
High Level	V_{OH}			9.99	V
Noise Immunity	V_{NL}	All Inputs	8.6	1.5	V
	V_{NH}	All Inputs	1.4	1.5	V
Output Drive Current:					
N-Channel (Sink)	I_{DN}	Data Output (Sink)	0.5	3.5	mA
P-Channel (Source)	I_{DP}	Data Output (Source)	9.5	1.5	mA
Data Output Off-Resistance	R_O(Off)	Data Output High Impedance State		5	MΩ
Input Leakage Current,	I_{IL}, I_{IH}	Any Input		1	μA

* Standby current is independent of any input state.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V_{DD} = 10\ V \pm 5\%$, Input $t_r, t_f = 20$ ns, and $C_L = 30$ pF

CHARACTERISTIC		TYPICAL VALUES	UNITS
Read Cycle Times:			
Read Access	t_{RA}	90	ns
Read Cycle	t_{RC}	100	ns
Output Enable	t_{EN}	30	ns
Read/Write Hold	t_{WH}	30	ns
Read/Write Set-Up	t_{WS}	30	ns
Output Disable	t_{DIS}	15	ns
Write Cycle Times:			
Write Cycle	t_{WC}	100	ns
Read/Write Hold	t_{WH}	25	ns
Read/Write Pulse Width	t_W	40	ns
Read/Write Set-Up	t_{WS}	35	ns
Input Data Set-Up	t_{DS}	20	ns
Input Data Hold	t_{DH}	15	ns
Read/Modify/Write Cycle Times:			
Read/Modify/Write Cycle	t_{MC}	175	ns
Read Hold	t_{RH}	100	ns
Read Access	t_{RA}	90	ns
Output Enable	t_{EN}	30	ns
Read/Write Pulse Width	t_W	40	ns
Read/Write Set-Up	t_{WS}	35	ns
Input Data Set-Up	t_{DS}	20	ns
Input Data Hold	t_{DH}	15	ns
Output Disable	t_{DIS}	15	ns

CAPACITANCES at $T_A = 25^oC$, $V_{DD} = 10\ V$, $V_I = 0\ V$, $V_{SS} = 0\ V$, $f = 1\ MHz$

CHARACTERISTIC		TYPICAL VALUES	UNITS
Input	C_I	5	pF
Output	C_O	5	pF

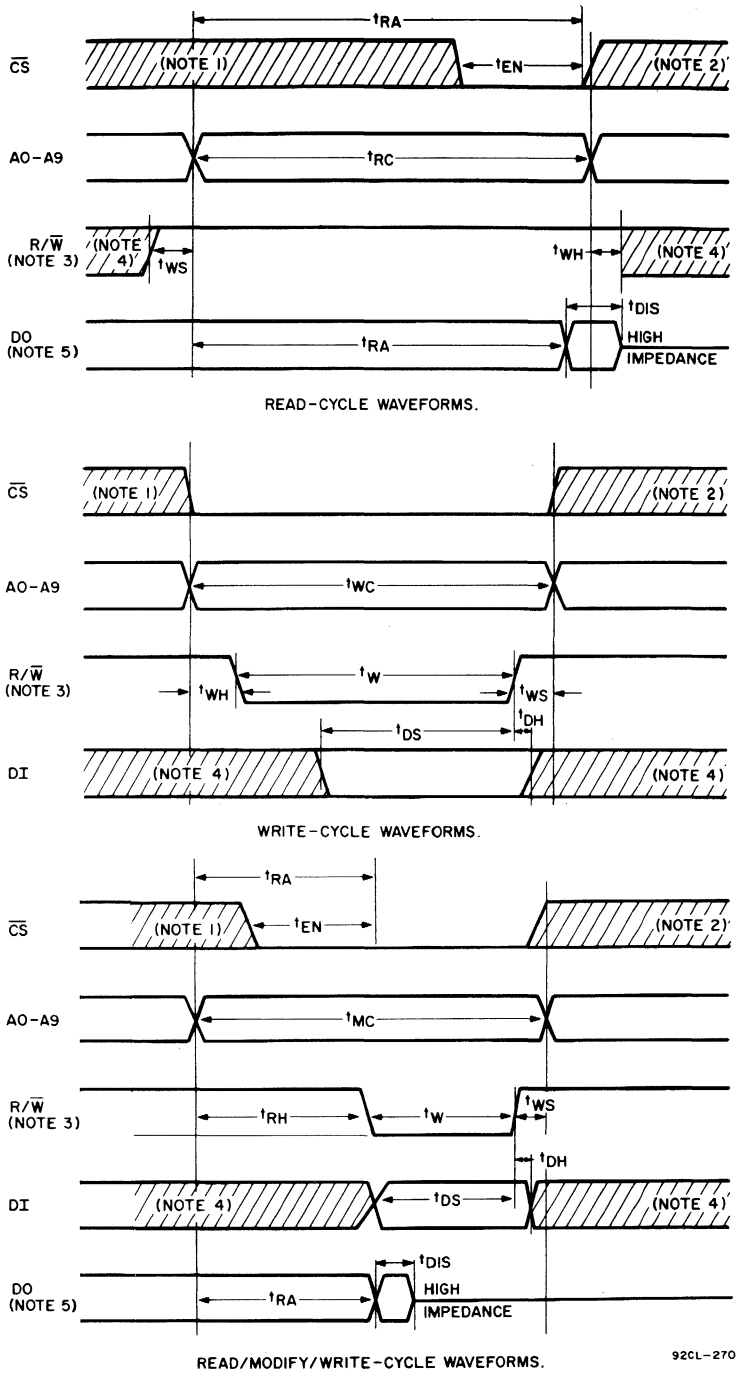


Fig. 4 — Read cycle, write cycle, and read/modify/write cycle waveforms.

Note 1. Chip-Select ($\overline{CS}$) permitted to change from high to low level or remain low on a selected device.
Note 2. Chip-Select ($\overline{CS}$) permitted to change from low to high level or remain low.
Note 3. Read/Write (R/$\overline{W}$) must be at a high level during all address transitions.
Note 4. Don't care.
Note 5. Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/$\overline{W}$ or the rising edge of $\overline{CS}$.

Preliminary MWS5540D

SOS 256-Word by 4-Bit COS/MOS LSI Static Random Access Memory

The RCA-MWS5540D is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, low power, and simplicity in use are desirable. The design of this device utilizes self-aligned silicon-gate technology. The MWS5540D has separate data inputs and data outputs and is operated from a single 10-volt supply. Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. After valid data appears at the output, the address inputs may be changed immediately. This output data will be valid until either the Output Disable input or the Chip-Select input is high, or the new data of the next memory cycle is applied.

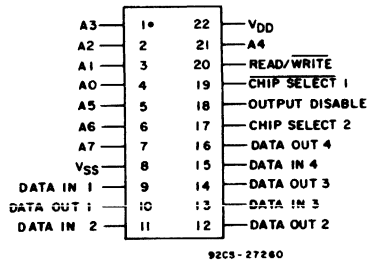
The MWS5540D is supplied in a 22-lead hermetic dual-in-line side-brazed ceramic package (D suffix), and in chip form (H suffix).

Features:

- **Organization— 256 words by 4 bits**
- **Fully static operation—no external clocks required**
- **Access time— 90 ns (typ.) @ V_{DD} = 10 V**
- **Cycle time—100 ns (typ.) @ V_{DD} = 10 V**
- **Low power dissipation:**
  3 μW/Bit (typ.) standby @ V_{DD} = 10 V
  20 μW/Bit (typ.) operating @ V_{DD} = 10 V
- **Separate data inputs and outputs**
- **Two Chip-Select inputs to simplify memory system expansion**
- **Output Disable to allow common I/O system**
- **Operation from a single power supply — V_{DD} = 4.5 to 10 V**
- **Noise immunity — 30% V_{DD}**
- **TTL output drive capability**
- **Three-state data output for bus-oriented systems**
- **Pin compatible with 5101 types**

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE TEMPERATURE RANGE . . . . . −65 to +150°C
OPERATING TEMPERATURE RANGE . . . . . −20 to +85°C
DC SUPPLY VOLTAGE RANGE
(V_{DD}−V_{SS}) . . . . . −0.5 to +11 V
ALL INPUTS. . . . . $V_{SS} \leqslant V_I \leqslant V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE
(V_{DD}−V_{SS}) . . . . . 4.5 to 10 V
LEAD TEMPERATURE (During Soldering):
At distance 1/16±1/32 inch (1.59±0.79 mm) from case for 10 seconds max. . . 265°C



Terminal Assignment

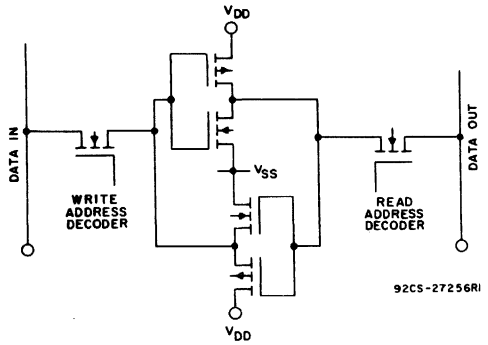


Fig. 2 — Memory cell configuration for MWS5540D.

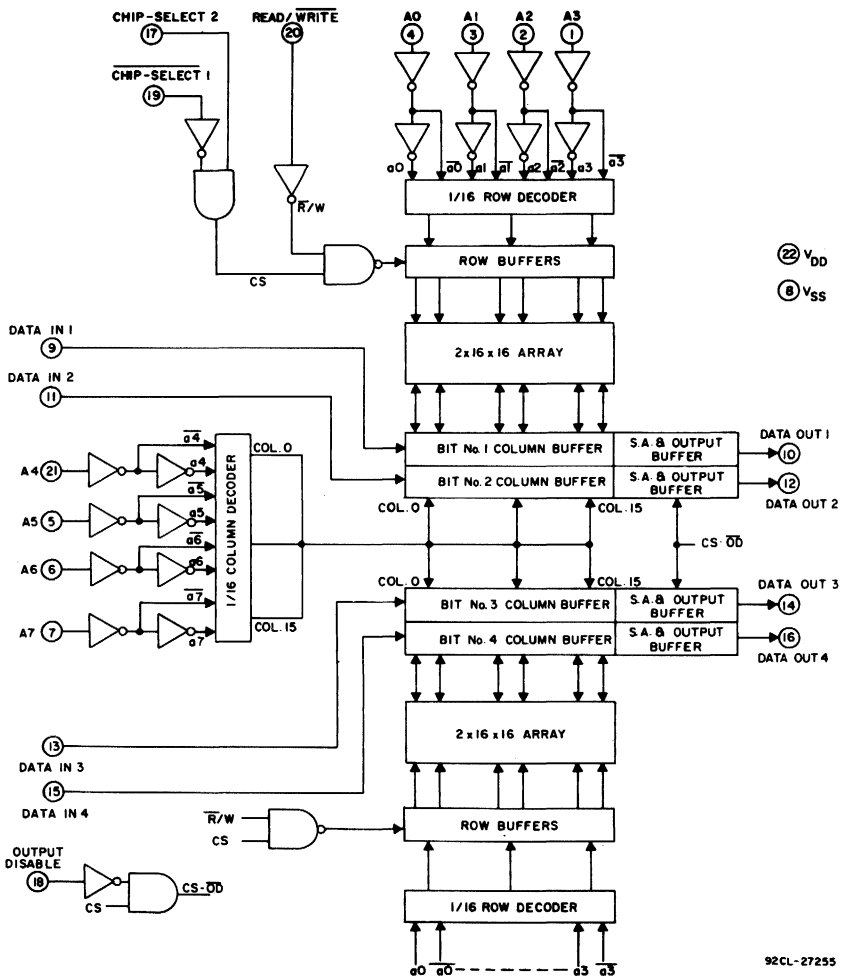


Fig. 1 — Functional block diagram for MWS5540D.

Preliminary MWS5540D

OPERATIONAL MODES

MODE	READ/WRITE R/$\overline{W}$	CHIP SELECT 1 $\overline{CS_1}$	CHIP SELECT 2 CS_2	OUTPUT DISABLE OD	DATA OUT DO
Read	1	0	1	0	Storage State of Addressed Cell
Write	0	0	1	1	High Impedance
Write	0	0	1	0	New Data In State
Standby	X	1	X	X	High Impedance
Standby	X	X	0	X	High Impedance
Output Disable	X	X	X	1	High Impedance

LOGIC 1 = HIGH LOGIC 0 = LOW X = DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 10 V ± 5%

CHARACTERISTIC		TEST CONDITIONS	V_O (V)	TYPICAL VALUES	UNITS
Quiescent Device Current *	I_L			300	μA
Quiescent Device Dissipation *	P_D			3000	μW
Output Voltage:					
Low Level	V_{OL}			0.01	V
High Level	V_{OH}			9.99	V
Noise Immunity	V_{NL}	All Inputs	8.6	1.5	V
	V_{NH}	All Inputs	1.4	1.5	V
Output Drive Current:					
N-Channel (Sink)	I_DN	Data Output (Sink)	0.5	3.5	mA
P-Channel (Source)	I_DP	Data Output (Source)	9.5	1.5	mA
Data Output Off-Resistance	R_O(Off)	Data Output High Impedance State		5	MΩ
Input Leakage Current,	I_{IL}, I_{IH}	Any Input		1	μA

*Standby current is independent of any input state.

CAPACITANCES at T_A = 25°C, V_{DD} = 10 V, V_I = 0 V, V_{SS} = 0 V, f = 1 MHz

CHARACTERISTIC		TYPICAL VALUES	UNITS
Input	C_I	5	pF
Output	C_O	5	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 10 V ±5%, Input t_r, t_f = 20 ns, and C_L = 30 pF. For waveforms, see Fig. 3.

Read Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Read Cycle	t_{RC}	90	ns
Access from Address	t_{ADA}	100	ns
Read Setup	t_{RDS}	30	ns
Read Hold	t_{RDH}	30	ns
Output Active from Chip-Select 1	t_{DOA1}	20	ns
Output Active from Chip-Select 2	t_{DOA2}	15	ns
Output Active from Output Disable	t_{DOA3}	15	ns
Output Hold from Chip-Select 1	t_{DOH1}	20	ns
Output Hold from Chip-Select 2	t_{DOH2}	15	ns
Output Hold from Output Disable	t_{DOH3}	15	ns

Write Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Write Cycle	t_{WC}	100	ns
Chip-Select 1 Setup	$t_{\overline{CS}1}$	45	ns
Chip-Select 2 Setup	t_{CS2}	40	ns
Read Hold	t_{RDH}	35	ns
Write Setup	t_{WRS}	65	ns
Write Width	t_{WRW}	40	ns
Data In Width Effective	t_{DIW}	20	ns
Data In Hold	t_{DIH}	15	ns

Read/Modify/Write Cycle Times

CHARACTERISTIC		LIMITS Typ.	UNITS
Read/Modify/Write Cycle	t_{RWC}	175	ns
Access from Address	t_{ADA}	90	ns
Read Width	t_{RDW}	100	ns
Write Setup	t_{WRS}	65	ns
Write Width	t_{WRW}	40	ns
Previous Data Hold	t_{PDH}	15	ns
Data In Width Effective	t_{DIW}	20	ns
Data In Hold	t_{DIH}	20	ns
Output Active from Chip-Select 1	t_{DOA1}	20	ns
Output Active from Chip-Select 2	t_{DOA2}	15	ns
Output Active from Output Disable	t_{DOA3}	15	ns
Chip-Select 1 Hold	$t_{\overline{CS}H1}$	5	ns
Chip-Select 2 Hold	t_{CSH2}	0	ns
Output Hold from Output Disable	t_{DOH}	15	ns

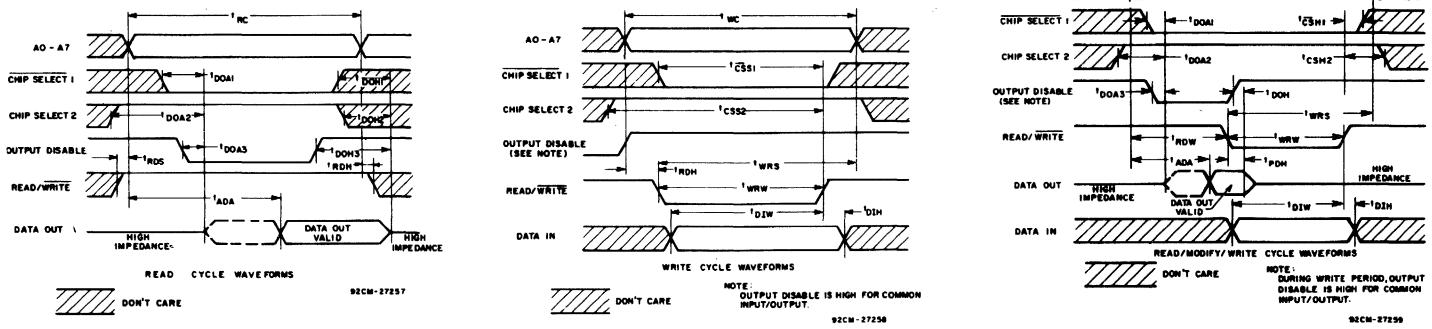


Fig. 3 – Read cycle, write cycle, and read/modify/write cycle waveforms.

Microprocessor Integrated Circuits

Selection Chart

Part Number Designations

The CDP1800 Series includes the complete family of 8-bit microprocessor CPUs featuring the COSMAC architecture, plus compatible memory and input/output interfacing support circuits. Numbers for this series are assigned in the following categories:

CDP1801-1809	CPU
CDP1821-1829	RAM
CDP1831-1839	ROM
CDP1851-1859	I/O

CPUs

CDP1802C	1 chip, 4 to 6 V
CDP1802	1 chip, 3 to 12 V
CDP1801C	2 chips, 4 to 6 V
CDP1801	2 chips, 3 to 12 V

ROMs

CDP1831C	512 x 8, 4 to 6 V
CDP1831	512 x 8, 3 to 12 V
CDP1832C	512 x 8, 4 to 6 V
CDP1832	512 x 8, 3 to 12 V

RAMs

CDP1821SC	1024 x 1, 4 to 6 V
CDP1821S	1024 x 1, 4 to 10 V
CDP1822SC	256 x 4, 4 to 6 V
CDP1822S	256 x 4, 4 to 10 V
CDP1824C	32 x 8, 4 to 6 V
CDP1824	32 x 8, 3 to 12 V

I/Os

CDP1852C	Byte I/O, 4 to 6 V
CDP1852	Byte I/O, 3 to 12 V

The CDP18S00 Series includes all the hardware and software support systems based on COSMAC microprocessors. Numbers for this series are assigned in the following categories:

CDP18S001-099	Hardware Development Systems
CDP18S101-899	PC Card Assemblies
CDP18S901-999	Software Systems

Hardware Systems

CDP18S011	Microtutor
CDP18S020	Evaluation Kit (1802)
CDP18S001	Basic COSMAC Development System
CDP18S002	Stand-Alone CDS
CDP18S004	Stand-Alone CDS with 1802 Emulator
CDP18S801	Floppy Disc

Software Systems

CDP18S900	CSDP Tape (1801)
CDP18S901	CSDP Deck (1801)
CDP18S910	CSDP II Tape (1802)
CDP18S911	CSDP II Deck (1802)

PC Cards

CDP18S101	1802 Emulator Card
CDP18S200	1K RAM Card
CDP18S201	4K RAM Card
CDP18S400	512-Byte PROM Card
CDP18S500	Monitor Card
CDP18S501	Byte I/O Card
CDP18S502	Extender Card

Support Literature

MPM-101	User Manual for the CDP1801 COSMAC Microprocessor
MPM-102	Program Development Guide for the CDP1801 COSMAC Microprocessor
MPM-109	Microtutor Instruction Manual
MPM-201	User Manual for the CDP1802 COSMAC Microprocessor
MPM-202	Program Development Guide for the CDP1802 COSMAC Microprocessor on Time-Sharing Systems
MPM-203	CDP1802 Evaluation Kit Manual
MPM-204	CSDP II Installation Manual
MPM-208	Program Development and Operator's Guide for the COSMAC Development System

CDP1801D, CDP1801CD

RCA CDP1801, CDP1801C Microprocessor (COSMAC)

CDP1801U, CDP1801CU Microprocessor Control IC
CDP1801R, CDP1801CR Microprocessor Register IC

The RCA-CDP1801 and CDP1801C Microprocessors (COSMAC) are LSI COS/MOS, 8-bit register-oriented central-processing units (CPU) designed for use as general-purpose computing or control elements in a wide range of stored-program systems or products. The CDP1801 and CDP1801C each comprise two units; the control unit designated CDP-1801U, CDP1801CU and the register unit designated CDP1801R, CDP1801CR.

The CDP1801 is functionally identical to the CDP1801C. The CDP1801 has an operating voltage range of 3 to 12 volts; the CDP1801C, an operating voltage range of 4 to 6 volts.

These microprocessors include all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The COSMAC architecture was designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The COSMAC CPU also provides a synchronous interface to memories and external controllers for I/O devices and minimizes the cost of interface controllers. Furthermore, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct-memory-access modes.

The CDP1801U and CDP1801CU control units are supplied in a 40-lead hermetic ceramic dual-in-line package (D suffix) and in chip form (H suffix). The CDP1801R and CDP1801CR register units are supplied in a 28-lead hermetic ceramic dual-in-line package (D suffix) and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C
Operating-Temperature Range (T_A) ..... −55 to +125°C
DC Supply-Voltage Range (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$:
CDP1801 ..... −0.5 to +15 V
CDP1801C ..... − 0.5 to +7 V
Power Dissipation Per Package (P_D):
For T_A = −55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW
Device Dissipation Per Output Transistor:
For T_A = −55°C to +125°C ..... 100 mW
Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS V_{CC}[1] (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1801 Min.	LIMITS CDP1801 Max.	LIMITS CDP1801C Min.	LIMITS CDP1801C Max.	UNITS
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	–	3	12	4	6	V
Recommended Input Voltage	–	–	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V
Clock Input Rise or Fall Time, t_r,t_f	3 - 15	3 - 15	–	15	–	15	μs
Instruction Time (See Fig. 4)	5	5	16	–	16	–	μs
	5 - 10	10	6	–	–	–	
Clock Input Frequency, f_{CL}	5	5	DC	1	DC	1	MHz
	5 - 10	10	DC	3	–	–	
Clock Pulse Width, t_{WL}, t_{WH}	5	5	500	–	500	–	ns
	5 - 10	10	160	–	–	–	
Clear Pulse Width	5	5	500	–	500	–	ns
	5 - 10	10	160	–	–	–	
Data Hold Time, t_{DH}	5	5	0	–	0	–	ns
	5 - 10	10	0	–	–	–	

Notes:
1. $V_{CC} \leq V_{DD}$. For CD1801C $V_{DD} = V_{CC} = 5$ volts.
2. Because a large number of nodes may be switching simultaneously, a 0.1 μF by-pass capacitor is recommended in the power supply.
3. In order to maintain proper circuit operation, the CDP1801 intra-unit wiring capacitance should be less than 25 pF.

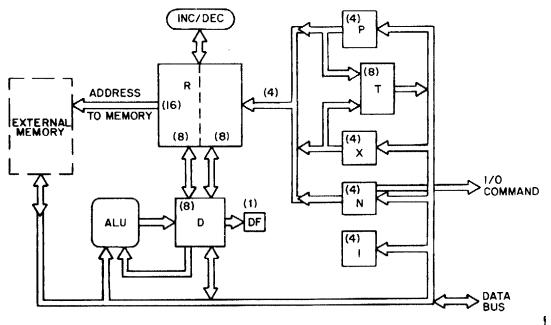
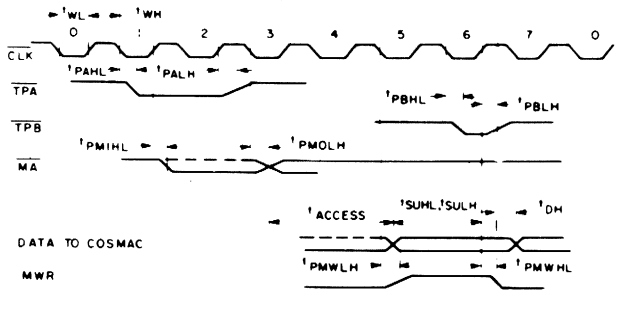


Fig. 1—CDP1801, CDP1801C Microprocessor data flow chart.

Features:

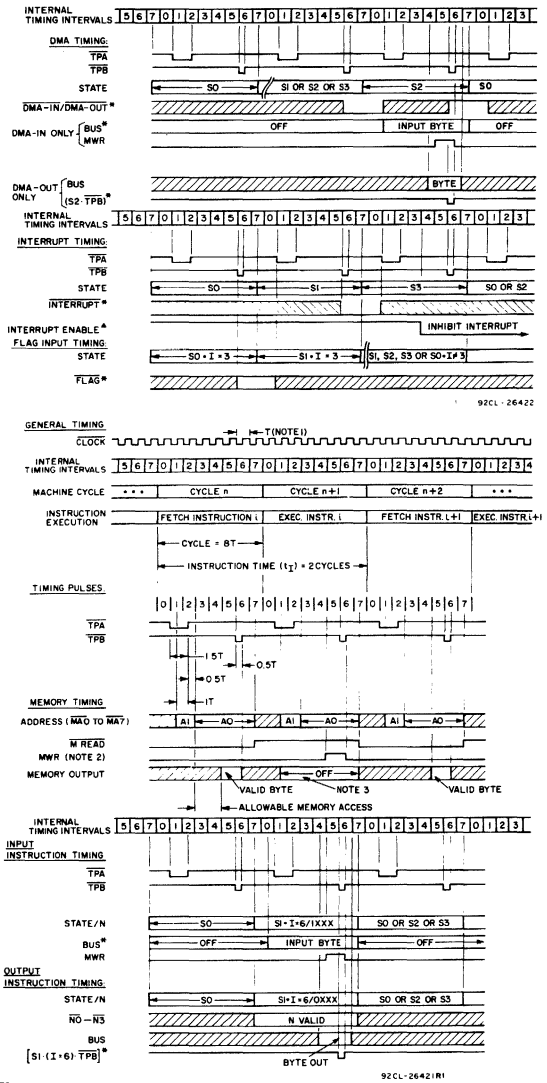
- **Static COS/MOS circuitry, no minimum clock frequency**
- **Full military temperature range**
- **High noise immunity, wide operating voltage range**
- **TTL compatibility**
- **8-bit parallel organization with bidirectional data bus**
- **Built-in program-load facility**
- **Any combination of standard RAM/ROM via common interface**
- **Memory addressing up to 65,536 bytes**
- **Flexible programmed I/O mode**
- **Program interrupt mode**
- **On-chip DMA facility**
- **Four I/O flag inputs directly testable by Branch instructions**
- **One-byte instruction format with two machine cycles for each instruction**
- **57 easy-to-use instructions**
- **16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers**



Notes 1 This timing diagram is used to show signal relationships only and does not represent any specific machine cycle
2 All measurements are referenced to 50% point of the waveforms

Fig. 2—Timing waveforms.

CDP1801D, CDP1801CD



NOTES:
1. MINIMUM T DETERMINED BY V_{DD} -- NO MAXIMUM T
2. MEMORY WRITE PULSE WIDTH (MWR) = 1.5 T
3. MEMORY OUTPUT "OFF" INDICATES HIGH-IMPEDANCE CONDITION
4. SHADING INDICATES "DON'T CARE" OR INTERNAL DELAYS DEPENDING ON V_{DD} AND THE CLOCK SPEED.

* = SIGNAL GENERATED BY USER
▲ = INTERNAL TO COSMAC

Fig. 3—CDP1801 and CDP1801C Microprocessor timing diagram.

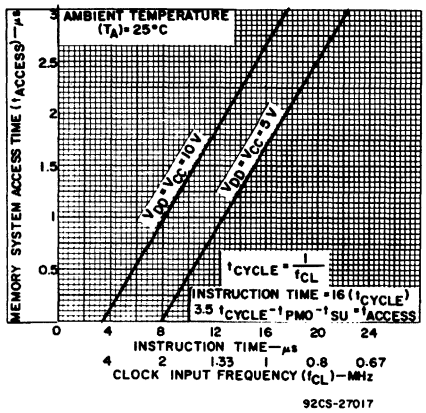


Fig. 4—Typical instruction time vs. memory system access time.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS V_O (V)	CONDITIONS V_{CC}= V_{DD} (V)	CDP1801U, CDP1801R LIMITS Min.	CDP1801U, CDP1801R LIMITS Typ.	CDP1801U, CDP1801R LIMITS Max.	CDP1801CU, CDP1801CR LIMITS Min.	CDP1801CU, CDP1801CR LIMITS Typ.	CDP1801CU, CDP1801CR LIMITS Max.	UNITS
Static									
Quiescent Device Current, I_L (See Figs. 11, 12)	–	5	–	0.01	0.1	–	0.01	0.5	mA
	–	10	–	0.01	0.5	–	–	–	
	–	15	–	0.05	1.0	–	–	–	
Output Voltage: Low-Level, V_{OL}	–	5	–	0	0.05	–	0	0.05	V
	–	10	–	0	0.05	–	–	–	
High-Level, V_{OH}	–	5	4.95	5	–	4.95	5	–	V
	–	10	9.95	10	–	–	–	–	
Noise Immunity: Inputs Low, V_{NL}	0.5	5	1.5	2.25	–	1.5	2.25	–	V
	1	10	3.0	3.45	–	–	–	–	
Inputs High, V_{NH}	4.5	5	1.5	2.25	–	1.5	2.25	–	V
	9	10	3.0	3.45	–	–	–	–	
Noise Margin: Inputs Low, V_{NML}	1	5	1	–	–	1	–	–	V
	1	10	1	–	–	–	–	–	
Inputs High, V_{NMH}	4	5	1	–	–	1	–	–	V
	9	10	1	–	–	–	–	–	
Output Drive Current●: N-Channel (Sink), I_{DN} (See Figs. 7, 8)	0.4	5	1.6	3.2	–	1.6	3.2	–	mA
	0.5	10	3.6	7.2	–	–	–	–	
P-Channel (Source), I_{DP} (See Figs. 5, 6)	2.5	5	−0.8	−1.6	–	−0.8	−1.6	–	mA
	4.6	5	−0.2	−0.4	–	−0.2	−0.4	–	
	9.5	10	−0.45	−0.9	–	–	–	–	
Input Leakage Current (Any Input), I_{IL}, I_{IH} (See Figs. 13, 14)	–	5	–	–	–	–	$\pm 10^{-5}$	±1	µA
	–	15	–	$\pm 10^{-5}$	±1	–	–	–	
Dynamic at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF									
Propagation Delay Times: (See Fig. 2) Clock to TPA t_{PAHL}	–	5	–	685	–	–	685	–	ns
	–	10	–	240	–	–	–	–	
t_{PALH}	–	5	–	720	–	–	720	–	ns
	–	10	–	250	–	–	–	–	
Clock to TPB t_{PBHL}	–	5	–	430	–	–	430	–	ns
	–	10	–	190	–	–	–	–	
t_{PBLH}	–	5	–	650	–	–	650	–	ns
	–	10	–	230	–	–	–	–	
Clock-to-Memory Address MA8 to MA15 t_{PMIHL}	–	5	–	900	–	–	900	–	ns
	–	10	–	340	–	–	–	–	
MA0 to MA7 t_{PMOLH}	–	5	–	870	–	–	870	–	ns
	–	10	–	300	–	–	–	–	
Dynamic at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF									
Data Setup Time: (See Fig. 2) t_{SULH}	–	5	–	750	–	–	750	–	ns
t_{SUHL}	–	10	–	450	–	–	–	–	
Clock-to-Memory Write Time (See Fig. 2) t_{PMWHL}	–	5	–	780	–	–	780	–	ns
t_{PMWLH}	–	10	–	270	–	–	–	–	
Device Dissipation (Total, Both Units), P_D OP CODE = 00 f_{CL} = 1.0 MHz	–	5	–	3	–	–	3	–	mW
f_{CL} = 3.0 MHz	–	10	–	32	–	–	–	–	
Transition Time●: (See Figs. 9, 10) t_{TLH}	–	5	–	170	–	–	170	–	ns
	–	10	–	100	–	–	–	–	
t_{THL}	–	5	–	30	–	–	30	–	ns
	–	10	–	20	–	–	–	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF

● Values are for signal lines going to external connections.

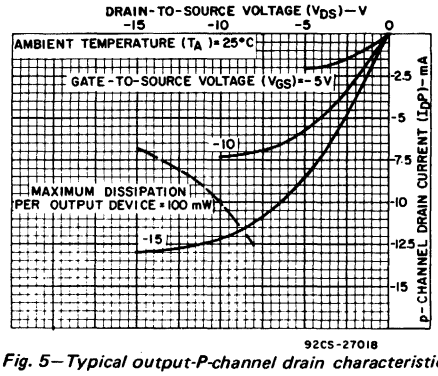


Fig. 5—Typical output-P-channel drain characteristics.

CDP1801D, CDP1801CD

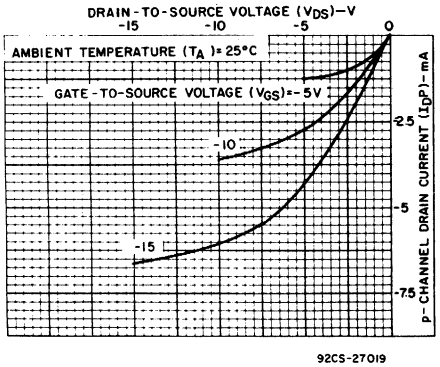


Fig. 6—Minimum output-P-channel drain characteristics.

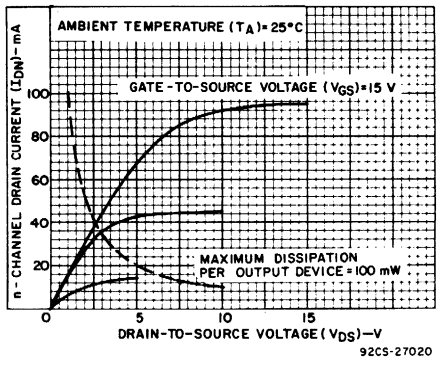


Fig. 7—Typical output-N-channel drain characteristics.

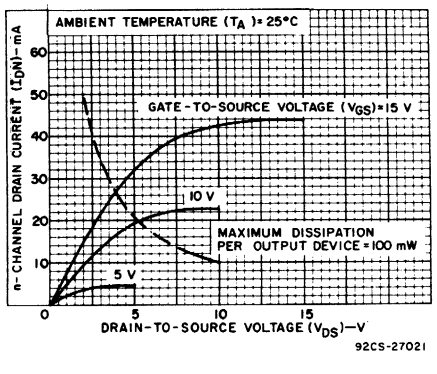


Fig. 8—Minimum output-N-channel drain characteristics.

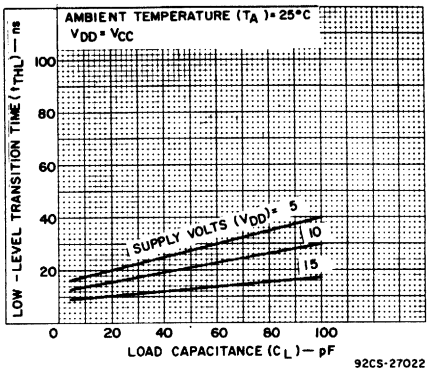


Fig. 9—Typical high-to-low level transition time vs. load capacitance.

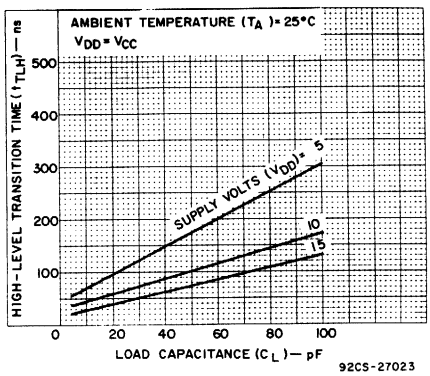


Fig. 10—Typical low-to-high level transition time vs. load capacitance.

TEST CIRCUITS

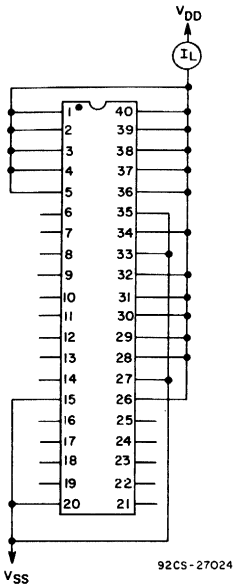


Fig. 11—CDP1801U, CDP1801CU quiescent device current.

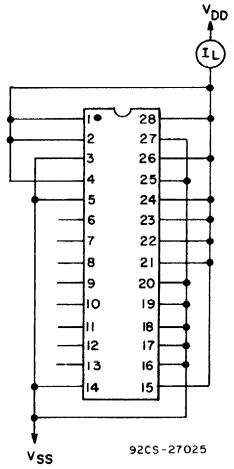


Fig. 12—CDP1801R, CDP1801CR quiescent device current.

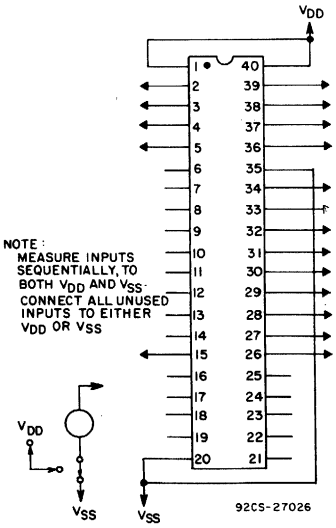


Fig. 13—CDP1801U, CDP1801CU input leakage current.

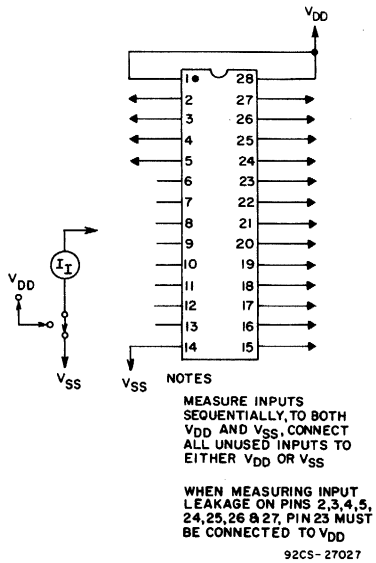


Fig. 14—CDP1801R, CDP1801CR input leakage current.

CDP1801D, CDP1801CD

Instruction Set

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes. Many of the instructions have been discussed in the Architecture section. Symbols used are:

R(W): Register designated by W, where W = N, or X, or P
R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)

Operation Notation

M(R(N)) → D;R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

Slash (/) mark in Operations Column indicates else or otherwise.

Table I – Instruction Summary

Register Operations

(Code (Note 1); Assembler Mnemonic (Note 2); Name; Operation)

I	N			
1	N	INC	INCREMENT	R(N)+1
2	N	DEC	DECREMENT	R(N)−1
8	N	GLO	GET LO	R(N).0→D
9	N	GHI	GET HI	R(N).1→D
A	N	PLO	PUT LO	D→R(N).0
B	N	PHI	PUT HI	D→R(N).1

N=0,1,2, . . .,9,A,B, . . .,E,F (Hexadecimal Notation)

Memory Reference

I	N			
4	N	LDA	LOAD ADV	M(R(N))→D;R(N)+1
5	N	STR	STORE	D→M(R(N))

ALU Operations

	I	N			
	F	0	LDX	LOAD BY X	M(R(X))→D
	F	1	OR	OR	M(R(X)) vD→D
	F	2	AND	AND	M(R(X))·D→D
	F	3	XOR	EXCL.OR	M(R(X))⊕ D→D
*	F	4	ADD	ADD	M(R(X))+D→D;C→DF
*	F	5	SD	SUBTRACT D	M(R(X))−D→D;C→DF
*	F	6	SHR	SHIFT RIGHT	SHIFT D RIGHT; LSB→DF;0→MSB
*	F	7	SM	SUBTRACT M	D−M(R(X))→D;C→DF
	F	8	LDI	LOAD IMM	M(R(P))→D;R(P)+1
	F	9	ORI	OR IMM	M(R(P)) vD→D;R(P)+1
	F	A	ANI	AND IMM	M(R(P))·D→P;R(P)+1
	F	B	XRI	EXCL.OR IMM	M(R(P))⊕ D→D; R(P)+1
*	F	C	ADI	ADD IMM	M(R(P))+D→D; C→DF;R(P)+1
*	F	D	SDI	SUBT D IMM	M(R(P))−D→D; C→DF;R(P)+1
*	F	F	SMI	SUBT M IMM	D−M(R(P))→D; C→DF;R(P)+1

*These are the only operations that modify DF. DF is set or reset by an ALU carry during add or subtract. Subtraction is by 2's complement: A−B = A+$\overline{B}$+1.

Branching

I	N			
3	0	BR	UNCOND.BR.	M(R(P))→R(P).0
3	2	BZ	BR.IF D=00	M(R(P))→R(P).0 IF D=00/R(P)+1
3	3	BDF	BR.IF DF=1	M(R(P))→R(P).0 IF DF=1/R(P)+1
3	4	B1	BR.IF EF1=1	M(R(P))→R(P).0 IF EF1=1/R(P)+1
3	5	B2	BR.IF EF2=1	M(R(P))→R(P).0 IF EF2=1/R(P)+1
3	6	B3	BR.IF EF3=1	M(R(P))→R(P).0 IF EF3=1/R(P)+1
3	7	B4	BR.IF EF4=1	M(R(P))→R(P).0 IF EF4=1/R(P)+1
3	8	SKP	SKIP	R(P)+1
3	A	BNZ	BR.IF D≠00	M(R(P))→R(P).0 IF D≠00/R(P)+1
3	B	BNF	BR.IF DF=0	M(R(P))→R(P).0 IF DF=0/R(P)+1
3	C	BN1	BR.IF EF1=0	M(R(P))→R(P).0 IF EF1=0/R(P)+1
3	D	BN2	BR.IF EF2=0	M(R(P))→R(P).0 IF EF2=0/R(P)+1
3	E	BN3	BR.IF EF3=0	M(R(P))→R(P).0 IF EF3=0/R(P)+1
3	F	BN4	BR.IF EF4=0	M(R(P))→R(P).0 IF EF4=0/R(P)+1

Control

I	N			
0	0	IDL	IDLE	WAIT FOR INTERRUPT/ DMA-IN/ DMA-OUT
D	N	SEP	SET P	N→P
E	N	SEX	SET X	N→X
7	0	RET	RETURN	M(R(X))→X, P; R(X)+1;1→IE
7	1	DIS	DISABLE	M(R(X))→X, P; R(X)+1;0→IE
7	8	SAV	SAVE	T→M(R(X))

Input-Output Byte Transfer

I	N	(Note 3)		
6	1	OUT 1	OUTPUT 1	M(R(X))→BUS; R(X)+1;N=1
6	2	OUT 2	OUTPUT 2	M(R(X))→BUS; R(X)+1;N=2
6	3	OUT 3	OUTPUT 3	M(R(X))→BUS; R(X)+1;N=3
6	4	OUT 4	OUTPUT 4	M(R(X))→BUS; R(X)+1;N=4
6	5	OUT 5	OUTPUT 5	M(R(X))→BUS; R(X)+1;N=5
6	6	OUT 6	OUTPUT 6	M(R(X))→BUS; R(X)+1;N=6
6	7	OUT 7	OUTPUT 7	M(R(X))→BUS; R(X)+1;N=7
6	9	INP 1	INPUT 1	BUS→M(R(X)); N=9
6	A	INP 2	INPUT 2	BUS→M(R(X)); N=A
6	B	INP 3	INPUT 3	BUS→M(R(X)); N=B
6	C	INP 4	INPUT 4	BUS→M(R(X)); N=C
6	D	INP 5	INPUT 5	BUS→M(R(X)); N=D
6	E	INP 6	INPUT 6	BUS→M(R(X)); N=E
6	F	INP 7	INPUT 7	BUS→M(R(X)); N=F

Note 1: The use of non-specified machine codes is not recommended.

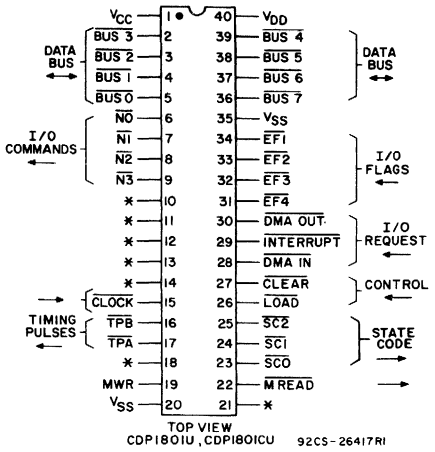
Note 2: This type of abbreviated nomenclature is used when programs are designed with the aid of the COSMAC Assembler Simulator/Debugger System, which is available on commercial timesharing systems. Refer to "Program Development Guide for the COSMAC Microprocessor", MPM-102, for details.

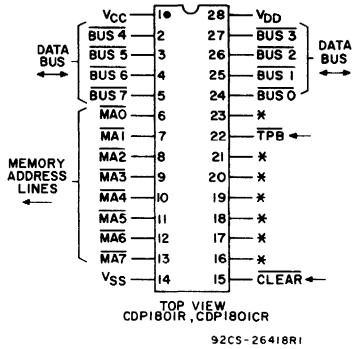
Note 3: When executing any of the 69 to 6F instructions, the contents of the D register may be altered.

Test and Branch

The Test and Branch instructions can branch unconditionally, test for D=0 or D=1, test for DF=0 or DF=1, or can test the status of the four I/O flags. A "successful" branch loads the byte following the instruction into the lower-order byte position of the current program counter, effecting a branch within the current 256-byte "page" of memory. If the test to branch is not successful, the next instruction in sequence is executed.

CDP1801D, CDP1801CD





Package Interconnections

Pin Terminals To:						*	*	*	*	*		*	*					
CDP1801U,CU	1	2	3	4	5	10	11	12	13	14	16	18	21	27	36	37	38	39	40
CDP1801R,CR	1	27	26	25	24	17	18	19	20	23	22	21	16	15	5	4	3	2	28
						*	*	*	*	*		*	*						

* These pins are for interchip connections only.

Notes:

1. Any unused input pins should be connected to V_{DD} or V_{CC}.
2. The DATA BUS lines are bi-directional and have three-state outputs. They may be individually connected to V_{CC} through external pull-up resistors (22 KΩ recommended) to prevent floating inputs.
3. All inputs have the same noise immunity and level-shifing capability. All outputs have the same drive capability whether they have three-state outputs or not.
4. For the CDP1801C, V_{CC} must be connected to V_{DD}.

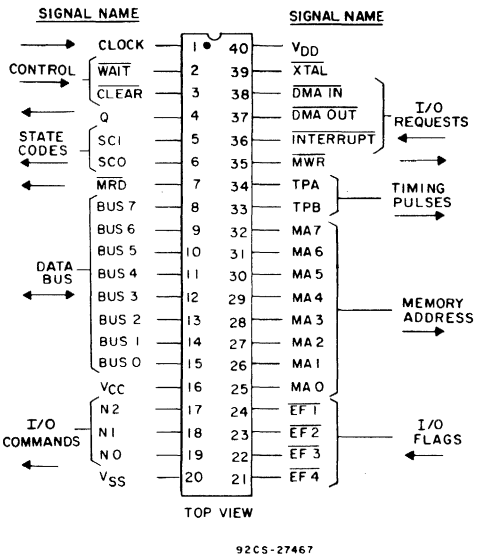
Fig. 17—Terminal assignment diagrams.

Preliminary CDP1802D, CDP1802CD
COSMAC Microprocessor

The RCA-CDP1802 is an LSI COS/MOS 8-bit register-oriented central-processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

It has the same basic COSMAC architecture as the CDP1801 microprocessor (see Fig. 5), but has an expanded instruction set, including a more powerful set of branch and ALU instructions, and enhanced hardware and performance features. The CDP1802 incorporates both the register and control chips of the CDP1801 on a single chip in a 40-lead hermetic dual-in-line ceramic package.

The CDP1802D is functionally identical to the CDP1802CD. The CDP1802D has a recommended operating voltage range of 3-12 volts; the CDP1802CD, a recommended operating voltage range of 4-6 volts.



Terminal Assignment for CDP1802

Features:

- **Static silicon-gate CMOS circuitry—CD4000 series compatible**
- **Instruction fetch-execute time of 2.5/3.75 μs at V_{DD} = 10 V**
- **Compatible with CDP1801 software**
- **Full military-temperature range (−55 to +125°C)**
- **High noise immunity, wide operating-voltage range**
- **Single voltage supply**
- **No minimum clock frequency**
- **Low power**
- **TTL compatible**
- **Single-phase clock; optional on-chip crystal-controlled oscillator**
- **Simple control of reset, start, and pause**
- **8-bit parallel organization with bidirectional data bus**
- **Any combination of standard RAM and ROM**
- **Memory addressing up to 65,536 bytes**
- **Flexible programmed I/O mode**
- **Program interrupt mode**
- **On-chip DMA**
- **Four I/O flag inputs directly tested by branch instructions**
- **Programmable output port**
- **91 easy-to-use instructions**
- **16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers**

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
$V_{CC} \leq V_{DD}$:
CDP1802D ..... −0.5 to +15 V
CDP1802CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A = −55 to +100°C ..... 500 mW
For T_A = +100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A = −55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = 25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS		TYPICAL VALUES		UNITS
	V_{CC}[1] (V)	V_{DD} (V)	CDP1802D	CDP1802CD	
Supply-Voltage Range (At T_A = Full Package-Temperature Range)	–	–	3 to 12	4 to 6	V
Recommended Input Voltage Range	–	–	V_{SS} to V_{CC}	V_{SS} to V_{CC}	V
Clock Input Rise or Fall Time, t_r or t_f	3-15	3-15	5	5	μs
Instruction Time[2] (See Fig. 1)	5	5	5	5	μs
	5	10	3.2	–	
	10	10	2.5	–	
DMA Transfer Rate	5	5	400	400	KBytes/sec
	5	10	625	–	
	10	10	800	–	
Clock Input Frequency, f_{CL}	5	5	DC - 3.2	DC - 3.2	MHz
	5	10	DC - 5.0	–	
	10	10	DC - 6.4	–	
Clock Pulse Width, t_{WL}, t_{WH}	5	5	160	160	ns
	5	10	100	–	
	10	10	80	–	
Clear Pulse Width	5	5	300	300	ns
	5	10	200	–	
	10	10	150	–	

Notes:
1. $V_{CC} \leq V_{DD}$; for CDP1802CD $V_{DD} = V_{CC} = 5$ volts.
2. Equals 2 machine cycles—one Fetch and one Execute operation for all instructions except Long Branch and Long Skip, which require 3 machine cycles—one Fetch and two Execute operations.

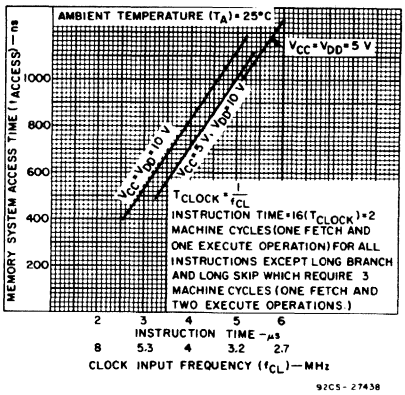


Fig. 1— Typical instruction time vs. memory system access time.

Preliminary CDP1802D, CDP1802CD

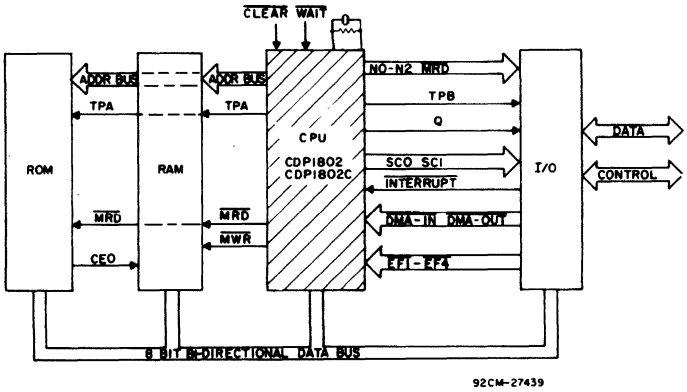


Fig. 2– Typical CDP1802 microprocessor system.

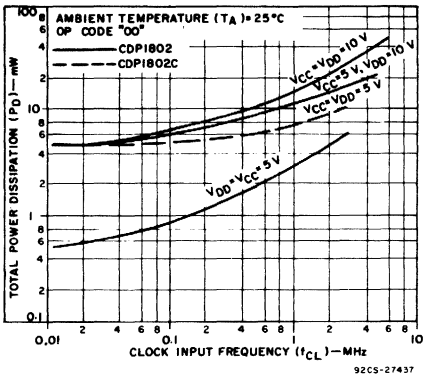


Fig. 4—Typical total power dissipation vs. clock input frequency.

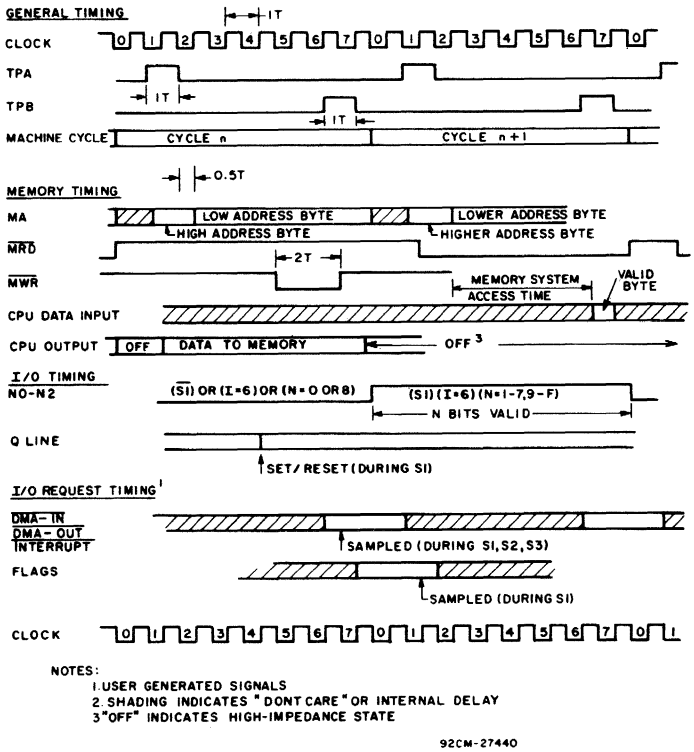


Fig. 3– Timing diagram.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC			CONDITIONS V_O (V)	CONDITIONS V_{CC}, V_{DD} (V)	CDP1802D TYPICAL VALUES	CDP1802CD TYPICAL VALUES	UNITS
Quiescent Device Current, I_L			–	5, 5	100	500	μA
			–	10, 10	500	–	
			–	15, 15	1000	–	
Total Power Dissipation: OP CODE "00" (See Fig. 4)	f = MHz	3.2	–	5, 5	6	8	mW
		5.0	–	5, 10	30	–	
		6.4	–	10, 10	40	–	
Output Voltage: Low-Level, V_{OL}			–	5, 5	0.01	0.01	V
			–	10, 10	0.01	–	
High-Level, V_{OH}			–	5, 5	5	5	
			–	10, 10	10	–	
Noise Immunity: Inputs Low, V_{NL}			0.5	5, 5	2.25	2.25	V
			–1	10, 10	3.45	–	
Inputs High, V_{NH}			4.5	5, 5	2.25	2.25	
			9	10, 10	3.45	–	
Output Drive Current: N-Channel (Sink), I_{DN}			0.4	5, 5	1.5	1.5	mA
			0.5	10, 10	3.0	–	
P-Channel (Source), I_{DP}			2.5	5, 5	–1.6	–1.6	
			4.6	5, 5	–0.4	–0.4	
			9.5	10, 10	–0.9	–	
Input Leakage Current (Any Input), I_{IL}, I_{IH}			–	5, 5	±1	±1	μA
			–	15, 15	±1	–	

ARCHITECTURE

The COSMAC block diagram is shown in Fig. 5. The principal feature of this system is a register array (R) consisting of sixteen 16-bit scratchpad registers. Individual registers in the array (R) are designated (selected) by a 4-bit binary code from one of the 4-bit registers labeled N, P, and X. The contents of any register can be directed to any one of the following three paths:

1. the external memory (multiplexed, higher-order byte first, on to 8 memory address lines);
2. the D register (either of the two bytes can be gated to D);
3. the increment/decrement circuit where it is increased or decreased by one and stored back in the selected 16-bit register.

The three paths, depending on the nature of the instruction, may operate independently or in various combinations in the same machine cycle.

With two exceptions, COSMAC instructions consist of two 8-clock-pulse machine cycles. The first cycle is the fetch cycle, and the second—and third, if necessary—are execute cycles. During the fetch cycle the four bits in the P designator select one of the 16 registers R(P) as the current program counter. The selected register R(P) contains the address of the memory location from which the instruction is to be fetched. When the instruction is read out from the memory, the higher-order 4 bits of the instruction byte are loaded into the I register and the lower-order 4 bits into the N register. The content of the program counter is automatically incremented by one so that R(P) is now "pointing" to the next byte in the memory.

Preliminary CDP1802D, CDP1802CD

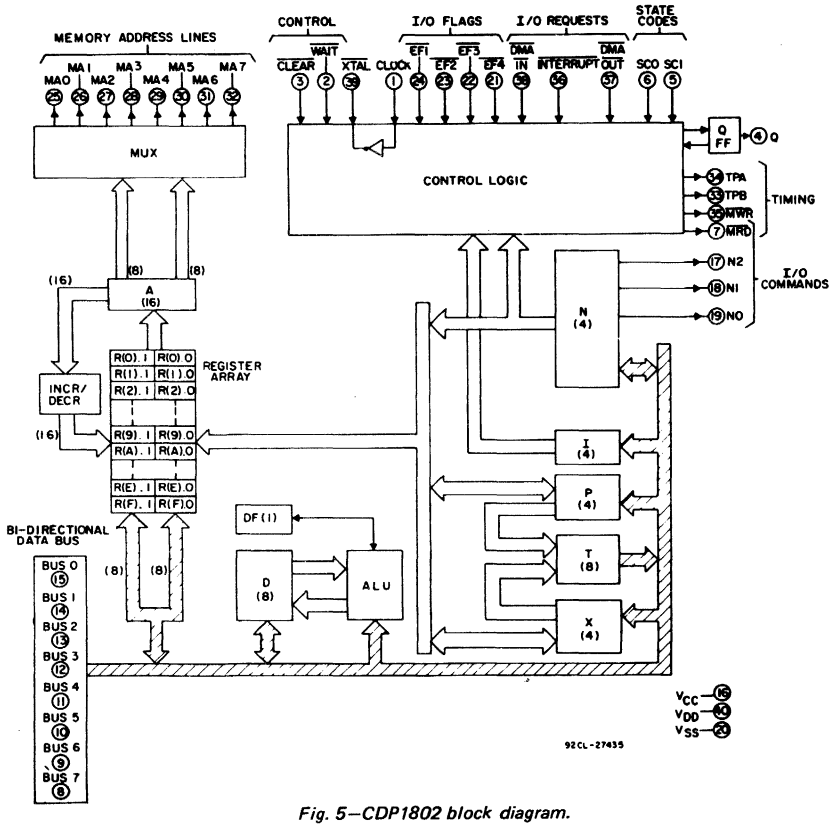


Fig. 5—CDP1802 block diagram.

The X designator selects one of the 16 registers R(X) to "point" to the memory for an operand (or data) in certain ALU or I/O operations.

The N designator can perform the following five functions depending on the type of instruction fetched:

1. designate one of the 16 registers in R to be acted upon during register operations;
2. indicate to the I/O devices a command code or device-selection code for peripherals;
3. indicate the specific operation to be executed during the ALU instructions, types of tests to be performed during the Branch instructions, or the specific operation required in a class of miscellaneous instructions (70-73 and 78-7B);
4. indicate the value to be loaded into P to designate a new register to be used as the program counter R(P);
5. indicate the value to be loaded into X to designate a new register to be used as data pointer R(X).

The registers in R can be assigned by a programmer in three different ways: as program counters, as data pointers, or as scratchpad locations (data registers) to hold two bytes of data.

Program Counters

Any register can be the main program counter; the address of the selected register is held in the P designator. Other registers in R can be used as subroutine program counters. By a single instruction the contents of the P register can be changed to effect a "call" to a subroutine. When interrupts are being serviced, register R(1) is used as the program counter for the interrupt servicing routine. At all other times the register designated as program counter is at the discretion of the user.

Data Pointers

The registers in R may be used as data pointers to indicate a location in memory. The register designated by X (i.e., R(X)) points to memory for the following instructions (see Table I):

1. ALU operations F0-F5, F7, 74, 75, 77;
2. output instructions 61 through 67;
3. input instructions 69 through 6F;
4. certain miscellaneous instructions—70-73, 78.

The register designated by N (i.e., R(N)) points to memory for the "load D from memory" instructions 0N and 4N and the "Store D" instruction 5N. The register designated by P (i.e., the program counter) is used as the data pointer for ALU instructions F8-FD, FF, 7C, 7D, 7F. During these instruction executions the operation is referred to as "data immediate".

Another important use of R as a data pointer supports the built-in Direct-Memory-Access (DMA) function. When a DMA-In or DMA-Out request is received, one machine cycle is "stolen". This operation occurs at the end of the execute machine cycle in the current instruction. Register R(0) is always used as the data pointer during the DMA operation. The data is read from (DMA-Out) or written into (DMA-In) the memory location pointed to by the R(0) register. At the end of the transfer, R(0) is incremented by one so that the processor is ready to act upon the next DMA byte transfer request. This feature in the COSMAC architecture saves a substantial amount of logic when fast exchanges of blocks of data are required, such as with magnetic discs or during CRT-display-refresh cycles.

A program load facility, using the DMA-In channel, is provided to enable users to load programs into the memory. This facility provides a simple, one-step means for initially entering programs into the microprocessor system and eliminates the requirement for specialized "bootstrap" ROM's.

Data Registers

When registers in R are used to store bytes of data, four instructions are provided which allow D to receive from or write into either the higher-order- or lower-order-byte portions of the register designated by N. By this mechanism (together with loading by data immediate) program pointer and data pointer designations are initialized. Also, this technique allows scratchpad registers in R to be used to hold general data. By employing increment or decrement instructions, such registers may be used as loop counters.

The Q Flip Flop

An internal flip flop, Q, can be set or reset by instruction and can be sensed by conditional branch instructions. The output of Q is also available as a microprocessor output.

Interrupt Servicing

Register R(1) is always used as the program counter whenever interrupt servicing is initiated. When an interrupt request comes in and the interrupt is allowed by the program (again, nothing takes place until the completion of the current instruction) the contents of the X and P registers are stored in the temporary register T, and X and P are set to new values; hex digit 2 in X and hex digit 1 in P. Interrupt enable is automatically deactivated to inhibit further interruptions. The interrupt routine is now in control; the contents of T are saved by means of a single instruction (78) in the memory location pointed to by R(X). At the conclusion of the interrupt, the routine restores the pre-interrupted values of X and P with a single instruction (70 or 71). The interrupt-enable flip-flop can be activated to permit further interrupts or can be disabled to prevent them.

Preliminary CDP1802D, CDP1802CD

TABLE I – INSTRUCTION SUMMARY

(For Notes, see below)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) −1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) −1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS◆◆			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76◆	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E◆	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		
ARITHMETIC OPERATIONS◆◆			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P) +1
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P) +1
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38◆	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33◆	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B◆	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1

INSTRUCTION SUMMARY (CONT'D)

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8◆	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	CB	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38◆	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8◆	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT; M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

◆◆NOTE: THE ARITHMETIC OPERATIONS AND THE SHIFT INSTRUCTIONS ARE THE ONLY INSTRUCTIONS THAT CAN ALTER THE DF.
AFTER AN ADD INSTRUCTION:
DF = 1 DENOTES A CARRY HAS OCCURRED
DF = 0 DENOTES A CARRY HAS NOT OCCURRED
AFTER A SUBTRACT INSTRUCTION:
DF = 1 DENOTES NO BORROW. D IS A TRUE POSITIVE NUMBER
DF = 0 DENOTES A BORROW. D IS TWO'S COMPLEMENT
THE SYNTAX "−(NOT DF)" DENOTES THE SUBTRACTION OF THE BORROW

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request ($\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, or $\overline{\text{DMA-OUT}}$) is activated. When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

◆NOTE: THIS INSTRUCTION IS ASSOCIATED WITH MORE THAN ONE MNEMONIC. EACH MNEMONIC IS INDIVIDUALLY LISTED.

Preliminary CDP1802D, CDP1802CD

1. Long-Branch, Long-Skip and No Op instructions are the only instructions that require three cycles to complete (1 fetch + 2 execute).

   Long-Branch instructions are three bytes long. The first byte specifies the condition to be tested; and the second and third byte, the branching address.

   The long-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address bytes are loaded in the high-and-low-order bytes of the current program counter, respectively. This operation effects a branch to any memory location.

   If the tested condition is not met, the branching address bytes are skipped over, and the next instruction in sequence is fetched and executed. This operation is taken for the case of unconditional no branch.

2. The short-branch instructions are two bytes long. The first byte specifies the condition to be tested, and the second specifies the branching address.

   The short-branch instructions can:
   a) Branch unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test the status (1 or 0) of the four EF flags
   f) Effect an unconditional no branch

   If the tested condition is met, then branching takes place; the branching address byte is loaded into the low-order byte position of the current program counter. This effects a branch with the current 256-byte page of the memory, i.e., the page which holds the branching address. If the tested condition is not met, the branching address byte is skipped over, and the next instruction in sequence is fetched and executed. This same action is taken in the case of unconditional no branch.

3. The skip instructions are one byte long. There is one Unconditional Short-Skip (SKP) and eight Long-Skip instructions.

   The Unconditional Short-Skip instruction takes 2 cycles to complete (1 fetch + 1 execute). Its action is to skip over the byte following it. Then the next instruction in sequence is fetched and executed. This SKP instruction is identical to the unconditional no-branch instruction (NBR) except that the skipped-over byte is not considered part of the program.

   The Long-Skip instructions take three cycles to complete (1 fetch + 2 execute).

   They can:
   a) Skip unconditionally
   b) Test for D=0 or D≠0
   c) Test for DF=0 or DF=1
   d) Test for Q=0 or Q=1
   e) Test for IE=1

   If the tested condition is met, then Long Skip takes place; the current program counter is incremented twice. Thus two bytes are skipped over and the next instruction in sequence is fetched and executed. If the tested condition is not met, then no action is taken. Execution is continued by fetching the next instruction in sequence.

COSMAC Register Summary

D	8 Bits	Data Register (Accumulator)	N	4 Bits	Holds Low-Order Instr. Digit
DF	1 Bit	Data Flag (ALU Carry)	I	4 Bits	Holds High-Order Instr. Digit
R	16 Bits	1 of 16 Scratchpad Registers	T	8 Bits	Holds old X, P after Interrupt (X is high byte)
P	4 Bits	Designates which register is Program Counter	IE	1 Bit	Interrupt Enable
X	4 Bits	Designates which register is Data Pointer	Q	1 Bit	Output Flip Flop

INSTRUCTION SET

The COSMAC instruction summary is given in Table I. Hexadecimal notation is used to refer to the 4-bit binary codes.

In all registers bits are numbered from the least significant bit (LSB) to the most significant bit (MSB) starting with 0.

R(W): Register designated by W, where W=N or X, or P

R(W).0: Lower-order byte of R(W)
R(W).1: Higher-order byte of R(W)
N0 = Least significant Bit of N Register

Operation Notation
M(R(N)) → D; R(N) + 1

This notation means: The memory byte pointed to by R(N) is loaded into D, and R(N) is incremented by 1.

SIGNAL DESCRIPTIONS

BUS 0 to BUS 7 (Data Bus)

8-bit bi-directional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

N0 to N2 (I/O Command)

Issued by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 and is indicated by the level of the MRD signal.

$\overline{MRD} = V_{CC}$: Data from I/O to CPU and Memory
$\overline{MRD} = V_{SS}$: Data from Memory to I/O

$\overline{EF1}$ to $\overline{EF4}$ (4 Flags)

These levels enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

Preliminary CDP1802D, CDP1802CD

SIGNAL DESCRIPTIONS (Cont'd)

$\overline{\text{INTERRUPT}}$, $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ (3 I/O Requests)

These signals are sampled by the CDP1802 during the interval between the leading edge of TPB and the leading edge of TPA.

Interrupt Action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed.

DMA Action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

SC0, SC1, (2 State Code Lines)

These lines indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H = V_{CC}, L = V_{SS}.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB (2 Timing Pulses)

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

MA0 to MA7 (8 Memory Address Lines)

The higher-order byte of a 16-bit COSMAC memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system are strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

$\overline{\text{MWR}}$ (Write Pulse)

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

$\overline{\text{MRD}}$ (Read Level)

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory **does** not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction:

$\overline{\text{MRD}}$ = V_{CC}: Data from I/O to CPU and Memory

$\overline{\text{MRD}}$ = V_{SS}: Data from Memory to I/O

Q

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

CLOCK

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at V_{CC} = V_{DD} = 10 volts.

The clock is counted down internally to 8 clock pulses per machine cycle.

$\overline{\text{XTAL}}$

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and $\overline{\text{XTAL}}$) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39.

ninary CDP1802D, CDP1802CD

SIGNAL DESCRIPTION (Cont'd)

$\overline{WAIT}$, $\overline{CLEAR}$ (2 Control Lines)

Provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Load

Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset

Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. Interrupt and DMA servicing are suppressed during the initialization cycle.

The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude interrupts until ready for them. Power-up reset can be realized by connecting an external RC to $\overline{CLEAR}$.

Pause

Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run

May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

V_{DD}, V_{SS}, V_{CC} (Power Levels)

The internal voltage supply V_{DD} is isolated from the Input/Output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with various external circuit technologies, including T^2L at 5 volts. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

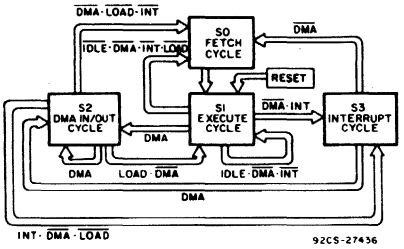


Fig. 6—CDP1802 microprocessor state transitions (Run Mode).

The CDP1802 and CDP1802C CPU state transitions when in the RUN mode are shown in Fig. 6. Each machine cycle requires the same period of time—8 clock pulses. The execution of an instruction requires either two or three machine cycles, S0 followed by a single S1 cycle or two S1 cycles. S2 is the response to a DMA request and S3 is the interrupt response.

Preliminary CDP1821SD, CDP1821SCD

1024-Word x 1-Bit Static Random-Access Memory

The RCA-CDP1821SD and CDP1821SCD are 1024-word x 1-bit COS/MOS silicon-on-sapphire (SOS), fully static, random-access memories for use in CDP1800 microprocessor systems.

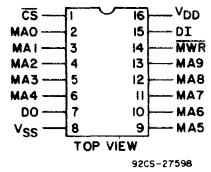
The output state of the CDP1821S is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may then be changed immediately. It is not necessary to clock the chip-select input or any other input terminal for fully static operation; therefore, the chip-select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}$=1), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The CDP1821SD is functionally identical to the CDP1821SCD. The CDP1821SD has a recommended operating voltage range of 4 to 10 volts, and the CDP1821SCD has a recommended operating voltage range of 4 to 6 volts.

The CDP1821SD and CDP1821SCD are supplied in 16-lead, hermetic, dual-in-line ceramic packages.

Features:

- Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible
- Compatible with CDP1800—series microprocessors at maximum speed
- Fast access time:
  350 ns typ. at V_{DD} = 5 V;
  200 ns typ. at V_{DD} = 10 V
- Single voltage supply
- No precharge or external clocks required
- Low quiescent and operating power
- Separate data inputs and outputs



Terminal Assignment

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −20 to +85°C

DC Supply-Voltage Range (V_{DD}-V_{SS}):

CDP1821SD ..... −0.5 to +11 V

CDP1821SCD ..... −0.5 to +7 V

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

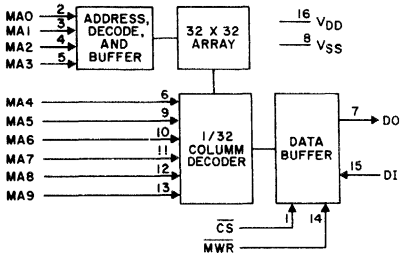
OPERATIONAL MODES

Mode	Input		Output
	$\overline{MRD}$	$\overline{CS}$	DO
Standby	X	1	High-Impedance
WRITE	0	0	High-Impedance
READ	1	0	Data

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1821SD Min.	CDP1821SD Max.	CDP1821SCD Min.	CDP1821SCD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	4	10	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	–	5	–	5	μs



Functional Diagram

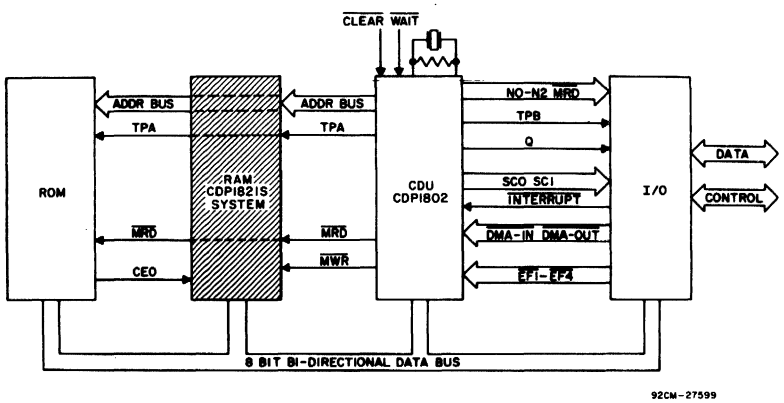
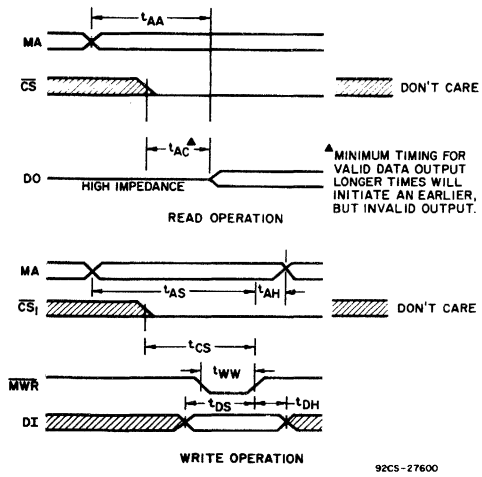


Fig. 1—Typical CDP1802 microprocessor system.



Timing Diagrams

nary CDP1821SD, CDP1821SCD

...RICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1821SD	CDP1821SCD	
		V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
Total Power Dissipation, P_D at 1 μs cycle		–	5	5	8	mW
		–	10	20	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_DN	Any Output	0.4	5	2	2	mA
		0.5	10	3.5	–	
P-Channel (Source), I_DP	Any Output	4.6	5	−1	−1	
		9.5	10	−15	–	
Data Output Off-Resistance, R_O(Off)	$\overline{CS}$ = H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA
Dynamic: t_r,t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	350	350	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	250	250	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	150	150	ns
		–	10	100	–	
Data Setup Time, t_{DS}		–	5	150	150	ns
		–	10	100	–	
Data Hold Time, t_{DH}		–	5	100	100	ns
		–	10	50	–	
Chip Select Setup Time, t_{CS}		–	5	250	250	ns
		–	10	150	–	
Address Setup Time, t_{AS}		–	5	200	200	ns
		–	10	150	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	
Capacitance						
Input/Output, C_I/C_O		–	–	5	5	pF

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1821S. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1821S is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$
$t_{AH} = 1.0\ t_c$
$t_{AS} = 4.5\ t_c$
$t_{DH} = 1.0\ t_c$ } Data transfers from
$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1821S is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary CDP1822SD, CDP1822SCD

256-Word x 4-Bit Static Random-Access Memory

The RCA-CDP1822SD and CDP1822SCD are 256-word x 4-bit COS/MOS SOS static random-access memories. These memories are compatible with the CDP1802 and will interface directly without additional components.

The CDP1822S has separate inputs and data outputs and is operated from a single voltage supply. Two Chip-Select inputs, of opposite polarity, are provided to simplify system expansion. The $\overline{MRD}$ signal (output disable control) provides WIRE-OR capability and is also useful in common input/output systems.

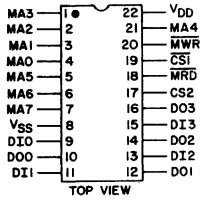
After valid data appears at the output, the address inputs may be changed immediately. This output data will be valid until either the $\overline{MRD}$ signal goes high or the device is deselected ($\overline{CS1}$=H or CS2=L).

The CDP1822SD is functionally identical to the CDP1822SCD. The CDP1822SD has a recommended operating voltage range of 4 to 10 volts, and the CDP1822SCD has a recommended operating voltage range of 4 to 6 volts.

The CDP1822SD and CDP1822SCD are supplied in 22-lead, hermetic, dual-in-line ceramic packages.

Features:

- **Static COS/MOS Silicon-On-Sapphire circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1802 microprocessor without additional components**
- **Fast access time:**
  350 ns typ. at V_{DD} = 5 V;
  100 ns typ. at V_{DD} = 10 V
- **Single voltage supply**
- **Separate data inputs and outputs**
- **Two-chip select inputs to simplify memory system expansion**
- **Output disable to allow common I/O system**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −20 to +85°C

DC Supply-Voltage Range (V_{DD})
(All voltages referenced to V_{SS} terminal)
CDP1822SD ..... −0.5 to +11 V
CDP1822SCD ..... −0.5 to +7 V

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1822SD Min.	LIMITS CDP1822SD Max.	LIMITS CDP1822SCD Min.	LIMITS CDP1822SCD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	4	10	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	–	5	–	5	μs

OPERATIONAL MODES

Function	$\overline{MWR}$	$\overline{CS1}$	CS2	$\overline{MRD}$	Data Out DO
READ	1	0	1	0	Storage State of Addressed Cell
WRITE (Output Disabled)	0	0	1	1	High-Impedance
WRITE	0	0	1	0	New Data In State
Standby	X	1	X	X	High-Impedance
	X	X	0	X	High-Impedance
	1	0	1	1	High-Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

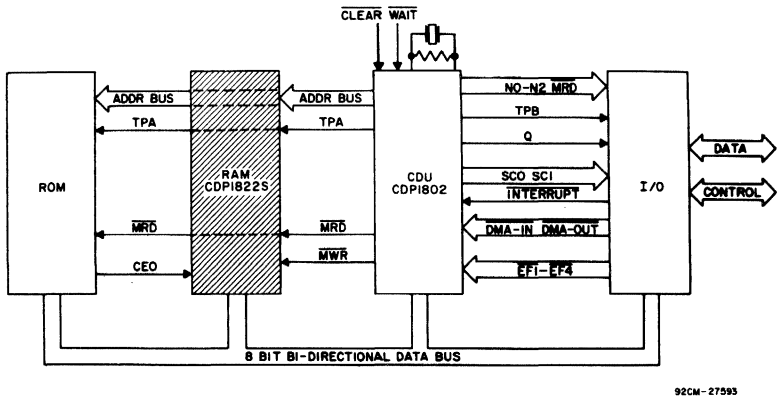
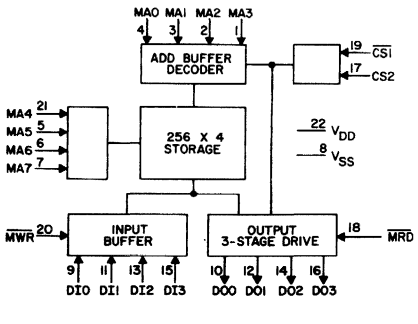


Fig. 1—Typical CDP1802 microprocessor system.

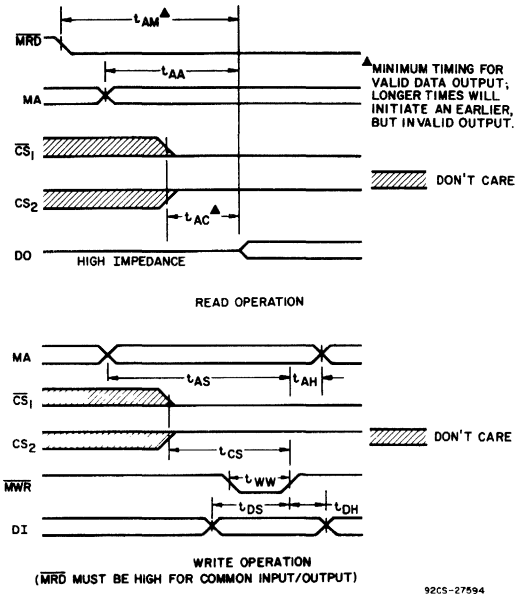


Functional Diagram

Preliminary CDP1822SD, CDP1822SCD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1822SD	CDP1822SCD	
		V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
Total Power Dissipation, P_D, at 1 μs cycle		–	5	8	10	mW
		–	10	35	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_DN	Any Output	0.4	5	0.8	0.8	mA
		0.5	10	1.8	–	
P-Channel (Source), I_DP	Any Output	4.6	5	–0.8	–0.8	
		9.5	10	–1.8	–	
Data Output Off-Resistance, R_O(Off)	$\overline{MRD}$ = H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	1	1	μA
Dynamic: t_r,t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	350	350	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	250	250	ns
		–	10	150	–	
Output Active From $\overline{MRD}$, t_{AM}		–	5	250	250	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	150	150	ns
		–	10	100	–	
Data Setup Time, t_{DS}		–	5	150	150	ns
		–	10	100	–	
Data Hold Time, t_{DH}		–	5	100	100	ns
		–	10	50	–	
Chip Select Setup Time, t_{CS}		–	5	250	250	ns
		–	10	150	–	
Address Setup Time, t_{AS}		–	5	200	200	ns
		–	10	150	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	
Capacitance						
Input/Output, C_I/C_O		–	–	5	5	pF



Timing Diagrams

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1822S. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1822S is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$ } Data transfers from

$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1822S is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary CDP1824D, CDP1824CD
32-Word x 8-Bit Static Random-Access Memory

The RCA-CDP1824D and CDP1824CD are 32-word x 8-bit fully static COS/MOS random-access memories for use in CDP1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824D is functionally identical to the CDP1824CD. The CDP1824D has a recommended operating voltage range of 3 to 12 volts, and the CDP1824CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1824D and CDP1824CD are supplied in 18-lead, hermetic, dual-in-line ceramic packages.

Features:
- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Interfaces with CDP1802 microprocessor without additional components
- Fast access time:
  400 ns typ. at V_{DD} = 5 V;
  200 ns typ. at V_{DD} = 10 V
- Single voltage supply
- No precharge or clock required
- Full military temperature range (−55°C to +125°C)
- Low quiescent and operating power

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

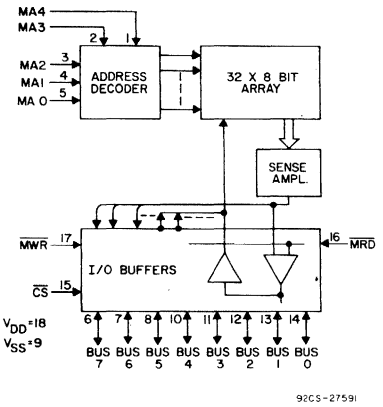
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
- CDP1824D ..... −0.5 to +15 V
- CDP1824CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
- For T_A=−55 to +100°C ..... 500 mW
- For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
- For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



Functional Diagram

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Conditions V_{DD} (V)	LIMITS CDP1824D Min.	CDP1824D Max.	CDP1824CD Min.	CDP1824CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise and Fall Time, t_r,t_f	–	–	5	–	5	μs

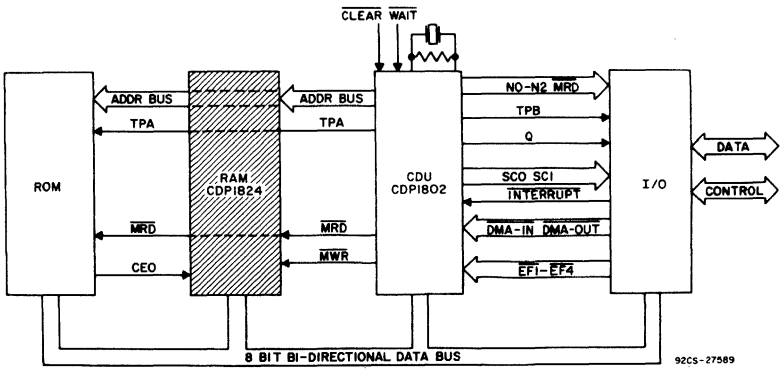


Fig. 1—Typical CDP1802 microprocessor system.

OPERATIONAL MODES

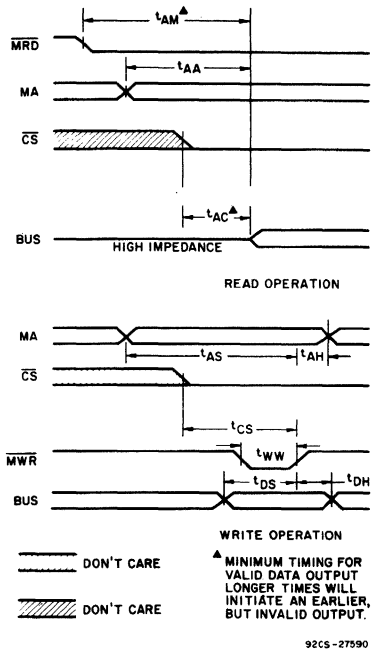
Function	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	Data Pins Status
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input, Output Disabled
Not Selected	1	X	X	Output Disabled High-Impedance State
Standby	0	1	1	

Logic 1 = High Logic 0 = Low X = Don't Care

Preliminary CDP1824D, CDP1824CD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
				CDP1824D	CDP1824CD	
		V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static						
Quiescent Device Current, I_L		–	5	100	500	μA
		–	10	500	–	
		–	15	1000	–	
Output Voltage: Low-Level, V_{OL}		–	5-10	0.01	0.01	V
High-Level, V_{OH}		–	5	4.99	4.99	
		–	10	9.99	–	
Noise Margin: V_{NML}	Any Input	0.5	5	1	1	V
		1	10	1.5	–	
V_{NMH}	Any Input	4.5	5	1	1	
		9	10	1.5	–	
Output Drive Current: N-Channel (Sink), I_{DN}	Any Output	0.4	5	1.6	1.6	mA
		0.5	10	3.6	–	
P-Channel (Source), I_{DP}	Any Output	4.6	5	−1.6	−1.6	
		9.5	10	−3.6	–	
Data Output Off-Resistance, R_O(Off)	$\overline{MRD}/\overline{CS}$=H	–	5-10	5	5	MΩ
Input Leakage, I_{IL}, I_{IH}	Any Input	–	5-10	±1	±1	μA
Dynamic: t_r,t_f=10 ns, C_L=50 pF						
Read Operation						
Access Time From Address Change, t_{AA}		–	5	400	400	ns
		–	10	200	–	
Access Time From Chip Select, t_{AC}		–	5	300	300	ns
		–	10	150	–	
Output Active From $\overline{MRD}$, t_{AM}		–	5	300	300	ns
		–	10	150	–	
Write Operation						
Write Pulse Width, t_{WW}		–	5	200	200	ns
		–	10	150	–	
Data Setup Time, t_{DS}		–	5	100	100	ns
		–	10	50	–	
Data Hold Time, t_{DH}		–	5	40	40	ns
		–	10	20	–	
Chip Select Setup Time, t_{CS}		–	5	550	550	ns
		–	10	300	–	
Address Setup Time, t_{AS}		–	5	500	500	ns
		–	10	300	–	
Address Hold Time, t_{AH}		–	5	100	100	ns
		–	10	50	–	



Timing Diagrams

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$
$t_{AH} = 1.0\ t_c$
$t_{AS} = 4.5\ t_c$
$t_{DH} = 1.0\ t_c$ } Data transfers from
$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CDP1802 clock frequency}}$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary CDP1831D, CDP1831CD

512-Word x 8-Bit Static Read-Only Memory

The RCA-CDP1831D and CDP1831CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. They will directly interface with either the CDP1801 or CDP1802 microprocessors without additional components.

The CDP1831 responds to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word byte of 64K memory space. Three Chip-Select signals—CS1, CS2, $\overline{MRD}$—are also provided.

The polarity of the clock (TPA), and CS1 and CS2 are user mask-programmable. The Chip-Enable output signal (CEO) goes "high" when the device is selected. This signal is intended for use as an output disable control for small memory systems.

The CDP1831D is functionally identical to the CDP1831CD. The CDP1831D has a recommended operating voltage range of 3 to 12 volts, and the CDP1831CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1831D and CDP1831CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

Features:
- **Static Silicon-Gate CMOS circuitry—CD4000-series compatible**
- **Compatible with CDP1800-series microprocessors at maximum speed**
- **Interfaces with CDP1801, CDP1802 microprocessors without additional components**
- **Fast access time: 400 ns typ. at V_{DD} = 10 V**
- **Single voltage supply**
- **On-chip address latch**
- **Full military temperature range (−55°C to +125°C)**
- **Optional programmable location within 64K memory space**
- **Low quiescent and operating power**

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

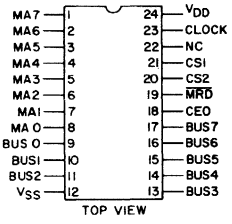
DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1831D ..... −0.5 to +15 V
CDP1831CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

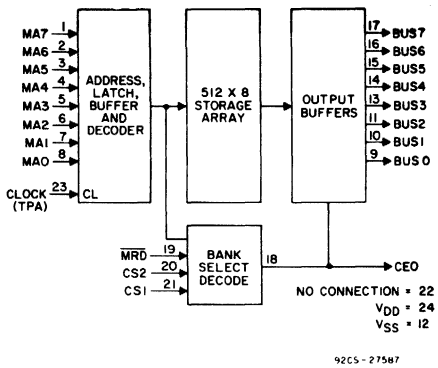
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



Terminal Assignment

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1831D Min.	CDP1831D Max.	CDP1831CD Min.	CDP1831CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Clock Pulse Width (TPA), t_{PAW}		Typical		Typical		ns
	5	100		100		
	10	50		–		
Address Setup Time, t_{AS}	5	100		100		ns
	10	50		–		
Address Hold Time, t_{AH}	5	150		150		ns
	10	75		–		



CDP1832 Functional Diagram

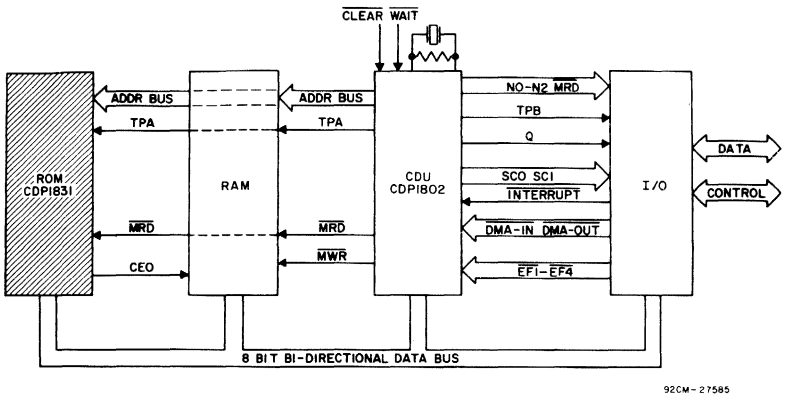
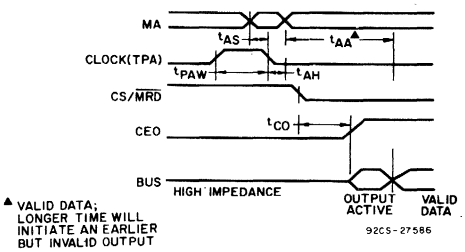


Fig. 1—Typical CDP1802 microprocessor system.



Timing Diagram

Preliminary CDP1831D, CDP1831CD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1831D	CDP1831CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	100	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	0.8	0.8	
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	–0.8	–0.8	
	9.5	10	–1.8	–	
Dynamic: t_r,t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Chip Enable Output Delay Time From CS, t_{CO}	–	5	400	400	ns
	–	10	200	–	

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with the CDP1802 microprocessor:

$t_{AH} = 0.5\ t_c$

$t_{PAW} = 1.0\ t_c$

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1831 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

Preliminary CDP1832D, CDP1832CD

512-Word x 8-Bit Static Read-Only Memory

The RCA-CDP1832D and CDP1832CD are static 4096-bit mask-programmable COS/MOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems. The CDP1832 ROM's are completely static—no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

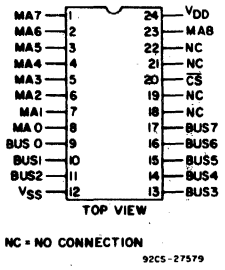
The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704/8704 Reprogrammable Read-Only Memories.

The CDP1832D is functionally identical to the CDP1832CD. The CDP1832D has a recommended operating voltage range of 3 to 12 volts, and the CDP1832CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1832D and CDP1832CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.

Features:

- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Fast access time: 400 ns typ. at V_{DD} = 10 V
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Functional replacement for industry type 8704 512 x 8 PROM
- Three-state outputs
- Low quiescent and operating power



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values*

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1832D ..... −0.5 to +15 V
CDP1832CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

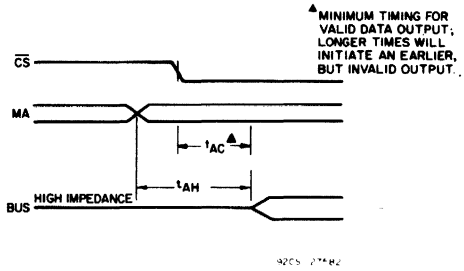
Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1832D Min.	CDP1832D Max.	CDP1832CD Min.	CDP1832CD Max.	UNITS
Static						
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V



CDP1832
Timing Diagram

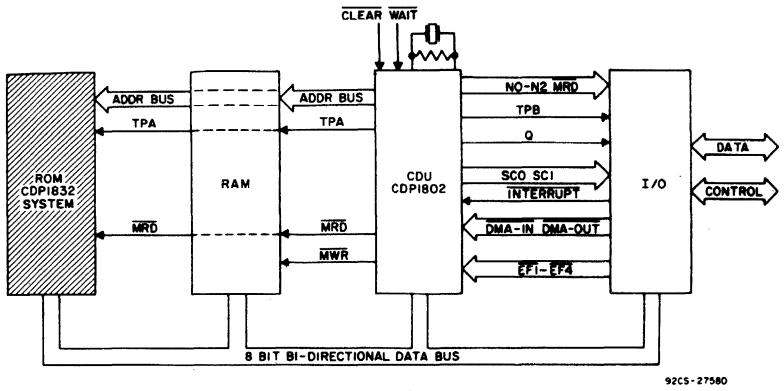
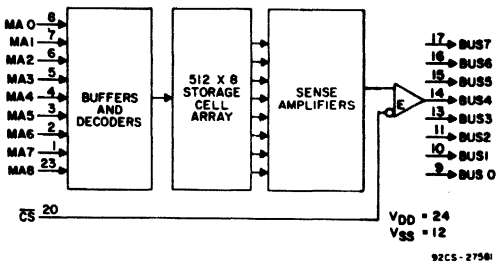


Fig. 1—Typical CDP1802 microprocessor system.



CDP1832
Functional Diagram

Preliminary CDP1832D, CDP1832CD

ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS		UNITS
			CDP1832D	CDP1832CD	
	V_O (V)	V_{DD} (V)	TYPICAL VALUES	TYPICAL VALUES	
Static					
Quiescent Device Current, I_L	–	5	100	500	μA
	–	10	500	–	
	–	15	1000	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	0.8	0.8	
	0.5	10	1.8	–	
P-Channel (Source), I_DP	4.6	5	–0.8	–0.8	
	9.5	10	–1.8	–	
Dynamic: t_r,t_f=10 ns, C_L=50 pF					
Access Time From Address Change, t_{AA}	–	5	850	850	ns
	–	10	400	–	
Access Time From Chip Select, t_{AC}	–	5	400	400	ns
	–	10	200	–	

Preliminary CDP1852D, CDP1852CD
8-Bit Input/Output Port

Features:
- Static Silicon-Gate CMOS circuitry—CD4000-series compatible
- Compatible with CDP1800-series microprocessors at maximum speed
- Interfaces with CDP1802 microprocessor without additional components
- Single voltage supply
- Full military temperature range (−55°C to +125°C)
- Parallel 8-bit data register and buffer
- Flip-flop for service request
- Asynchronous register clear
- Low quiescent and operating power

The RCA-CDP1852D and CDP1852CD are parallel, 8-bit, mode-programmable COS/MOS input/output ports designed for use in CDP-1800 series microprocessor systems. These input/output ports are compatible and will interface directly with the CDP1802 without additional components.

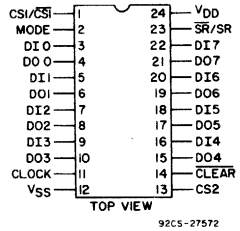
The mode control is used to program the device as an input port (mode=0) or output port (mode=1). If the CDP1852 is used as an input port (mode=0), data is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative, high-to-low transition of the clock sets the Service Request Flip-Flop ($\overline{SR}$=0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the microprocessor. When CS1·CS2=1 the three-state output drivers are enabled, the negative high-to-low transition of CS1·$\overline{CS2}$ resets the Service Request Flip-Flop, $\overline{SR}$=1.

If the CDP1852 is used as an output port (mode=1), data is strobed into the port's 8-bit register when $\overline{CS1}$·CS2·CLOCK=1. The three-state output drivers are enabled at all times when the CDP1852 is configured as an output port. The service request signal is generated at the termination of $\overline{CS1}$·CS2=1 and will be present, 1 level, until the following negative, high-to-low transition of the clock.

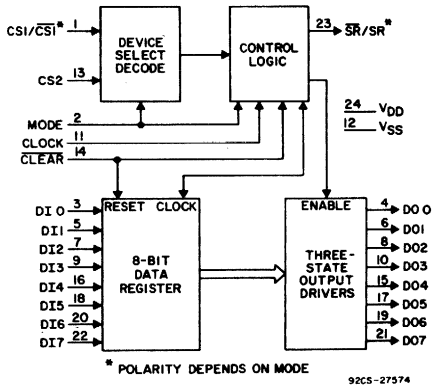
A $\overline{CLEAR}$ control is provided for resetting the port's register and service request flip-flop.

The CDP1852D is functionally identical to the CDP1852CD. The CDP1852D has a recommended operating voltage range of 3 to 12 volts, and the CDP1852CD has a recommended operating voltage range of 4 to 6 volts.

The CDP1852D and CDP1852CD are supplied in 24-lead, hermetic, dual-in-line ceramic packages.



Terminal Assignment



Functional Diagram

MAXIMUM RATINGS,
Absolute-Maximum Values

Storage-Temperature Range (T_{stg}) ..... −65 to +150°C

Operating-Temperature Range (T_A) ..... −55 to +125°C

DC Supply-Voltage Range (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1852D ..... −0.5 to +15 V
CDP1852CD ..... −0.5 to +7 V

Power Dissipation Per Package (P_D):
For T_A=−55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly to 200 mW

Device Dissipation Per Output Transistor:
For T_A=−55°C to +125°C ..... 100 mW

Input Voltage Range, All Inputs ..... −0.5 to V_{DD} +0.5 V

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1852D Min.	CDP1852D Max.	CDP1852CD Min.	CDP1852CD Max.	UNITS
Supply-Voltage Range (At T_A=Full Package-Temperature Range)	–	3	12	4	6	V
Recommended Input Voltage Range	–	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Strobe Pulse Width, t_{WS}		Typical		Typical		ns
	5	200		200		
	10	100		–		
Data Setup Time, t_{DS}	5	0		0		ns
	10	0		–		
Data Hold Time, t_{DH}	5	100		100		ns
	10	50		–		

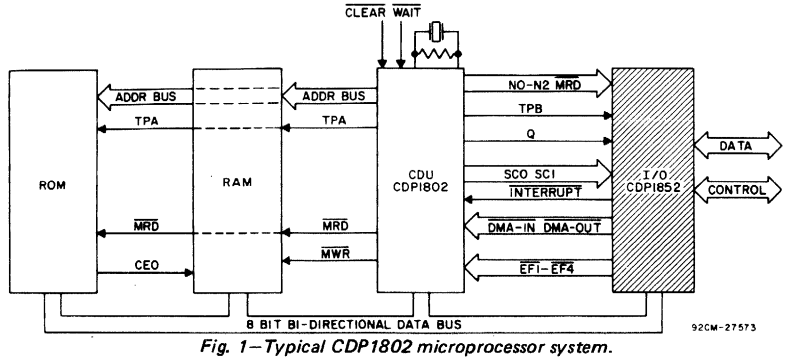
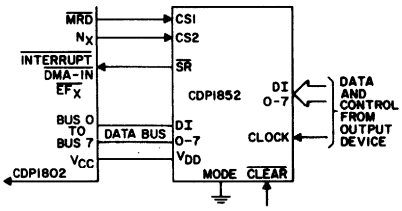


Fig. 1—Typical CDP1802 microprocessor system.

Preliminary CDP1852D, CDP1852CD

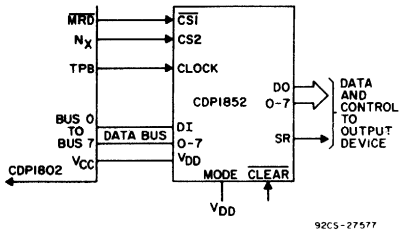
ELECTRICAL CHARACTERISTICS at T_A=25°C

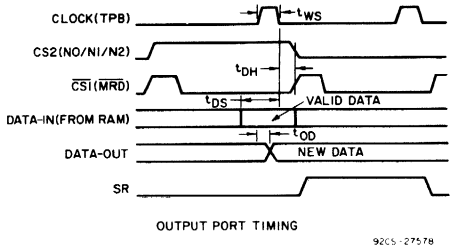
CHARACTERISTIC	TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{DD} (V)	LIMITS CDP1852D TYPICAL VALUES	LIMITS CDP1852CD TYPICAL VALUES	UNITS
Static					
Quiescent Device Current, I_L	–	5	50	100	μA
	–	10	100	–	
	–	15	500	–	
Output Drive Current:					mA
N-Channel (Sink), I_DN	0.4	5	1.6	1.6	
	0.5	10	3.6	–	
P-Channel (Source), I_DP	4.6	5	–1.6	–1.6	
	9.5	10	–3.6	–	
Dynamic: t_r,t_f=10 ns, C_L=50 pF					
Propagation Delay Times:					ns
Output from CS, t_{CA}	–	5	200	200	
	–	10	100	–	
Data to Output, t_{OD}	–	5	200	200	
	–	10	100	–	

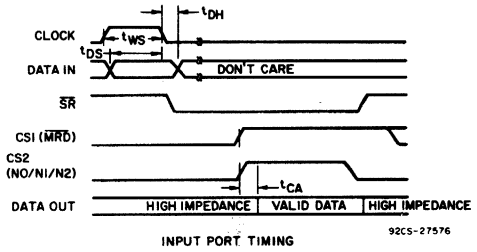


MODE = 0

CLOCK	CS1·CS2	$\overline{CLEAR}$	Data Out Equals
X	0	X	High-Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In







MODE = 1

CLOCK	$\overline{CS1}$·CS2	$\overline{CLEAR}$	Data Out Equals
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SR = 1▲	SR = 0
$\overline{CS1}$·CS2 ↘	CLOCK ↘ Or $\overline{CLEAR}$ ↘

$\overline{SR}$ = 0	$\overline{SR}$ = 1▲
CLOCK ↘	CS1·CS2 ↘ Or $\overline{CLEAR}$ ↘

Fig. 2–CDP1852 output port operation.

Fig. 3– CDP1852 input port operation.

Note:
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1852. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1852 is used as an output port with the CDP1802 microprocessor:

$$t_{WS}(TPB) = 1.0\ t_c$$

$$t_{DH} = 0.5\ t_c$$

$$t_c = \frac{1}{\text{CDP1802 clock frequency}}$$

of the port. The termination of the signal may improperly place the service request flip-flop in the "1" state. The transition used to set and reset $\overline{SR}$/SR may be positive or negative. The polarity will not affect circuit operation shown in Figs.2 and 3.

▲ The service request flip-flop is placed in the "1" state by the termination of the I/O port selection, CS1·CS2 or $\overline{CS1}$·CS2. System implementations should be avoided which cause a transient selection

High-Reliability Integrated Circuits

RCA offers high-reliability versions of a broad range of integrated circuits. These high-reliability integrated circuits include COS/MOS types, microprocessor systems, CMOS and NMOS memories, and linear types that are processed in accordance with MIL-STD-883 (Military Standard for Test Methods, Microelectronics). In addition, twenty-seven COS/MOS integrated circuits are currently being "qualified" to meet the requirements of MIL-M-38510 (Military Standard for Microelectronics or Integrated Circuits). RCA plans to qualify a number of its more than 100 standard linear integrated circuits in accordance with MIL-M-38510 in the future.

The product-classification charts shown in Tables I through IV list RCA high-reliability integrated circuits processed in accordance with MIL-STD-883 (slash-series types) and MIL-M-38510 that are currently available or that are planned for the near future. (Note: High-reliability slash-series types of any commercial RCA integrated circuit may also be obtained on a custom basis.)

RCA also offers a broad line of high-reliability integrated-circuit chips for use in hybrid circuits. Standard chips are normally inspected to MIL-STD-883, Method 2010.1, Condition B Visual. Chips subjected to the more critical Condition A Visual inspections and to SEM (scanning-electron-microscope) inspections are also available.

TABLE I — Product Classification Guide for RCA High-Reliability COS/MOS Integrated Circuits

MIL-STD-883 Slash-Series and MIL-M-38510 Series Types				
Standard Product Type No.	Descriptive Title	Availability of MIL-STD-883 Slash-Series Types	MIL-M-38510 Series Types	
			Detailed Electrical Specification No.	Availability of Parts
CD4000A	Dual 3-Input NOR Gate Plus Inverter	Now	MIL-M-38510/05201	Now
CD4001A	Quad 2-Input NOR Gate	Now	MIL-M-38510/05202	Now
CD4002A	Dual 4-Input NOR Gate	Now	MIL-M-38510/05203	Now
CD4006A	18-Stage Static Shift Register	Now	MIL-M-38510/05701	Now
CD4007A	Dual Complementary Pair Plus Inverter	Now	MIL-M-38510/05301	Now
CD4008A	4-Bit Full Adder With Parallel Carry-out	Now	MIL-M-38510/05401	Now
CD4009A	Hex Buffer/Converter (Inverting Type)	Now	MIL-M-38510/05501	Now
CD4010A	Hex Buffer/Converter (Non-Inverting Type)	Now	MIL-M-38510/05502	Now
CD4011A	Quad 2-Input NAND Gate	Now	MIL-M-38510/05001	Now
CD4012A	Dual 4-Input NAND Gate	Now	MIL-M-38510/05002	Now
CD4013A	Dual "D" Type Flip-Flop With Set/Reset Capability	Now	MIL-M-38510/05101	Now
CD4014A	8-Stage Static Shift Register (Synchronous)	Now	MIL-M-38510/05702	Now
CD4015A	Dual 4-Stage Static Shift Register	Now	MIL-M-38510/05703	Now
CD4016A	Quad Bilateral Switch	Now	MIL-M-38510/05801	Now
CD4017A	Decade Counter/Divider	Now	MIL-M-38510/05601	Now
CD4018A	Presettable Divide-By-"N" Counter	Now	MIL-M-38510/05602	Now
CD4019A	Quad AND-OR Select Gate	Now	MIL-M-38510/05302	Now
CD4020A	14-Stage Ripple-Carry Binary Counter/Divider	Now	MIL-M-38510/05603	Now
CD4021A	8-Stage Static Shift Register (Asynchronous)	Now	MIL-M-38510/05704	Now
CD4022A	Divide-By-8 Counter/Divider With 8 Decoded Outputs	Now	MIL-M-38510/05604	Now
CD4023A	Triple 3-Input NAND Gate	Now	MIL-M-38510/05003	Now
CD4024A	7-Stage Binary Ripple Counter	Now	MIL-M-38510/05605	Now
CD4025A	Triple 3-Input NOR Gate	Now	MIL-M-38510/05204	Now
CD4026A	Decade Counter/Divider	Now		Note 1
CD4027A	Dual J-K Master-Slave Flip-Flop With Set/Reset Capability	Now	MIL-M-38510/05102	Now
CD4028A	BCD-TO-Decimal Decoder	Now	MIL-M-38510/05901	Note 2
CD4029A	Presettable Up/Down Counter	Now	MIL-M-38510/05606	Note 2
CD4030A	Quad Exclusive-OR Gate	Now	MIL-M-38510/05303	Note 2
CD4031A	64-Stage Static Shift Register	Now	MIL-M-38510/05705	Now
CD4033A	Decade Counter/Divider	Now		Note 1
CD4034A	8-Stage Parallel-In/Parallel-Out Bidirectional Static Shift Register	Now	MIL-M-38510/05706	Note 2
CD4035A	4-Stage Parallel-In/Parallel-Out Shift Register	Now	MIL-M-38510/05707	Note 2
CD4036A	4-Word X 8-Bit RAM (Binary Addressing)	Now		Note 1
CD4039A	4-Word X 8-Bit RAM (Direct Word-Line Addressing)	Now		Note 1
CD4040A	12-Stage Binary/Ripple Counter	Now	MIL-M-38510/05607	Note 2
CD4041A	Quad True/Complement Buffer	Now	MIL-M-38510/05505	Note 2
CD4042A	Quad Clocked "D" Latch	Now	MIL-M-38510/05103	Note 2
CD4043A	Quad 3-State NOR R/S Latch	Now		Note 1
CD4044A	Quad 3-State NAND R/S Latch	Now		Note 1
CD4045A	21-Stage Clock-Timer Counter	Now		Note 1
CD4046A	Micropower Phase-Locked Loop	Now		Note 1
CD4047A	Low-Power Monostable/Astable Multivibrator	Now	MIL-M-38510/05014	Note 2
CD4048A	Multi-Function Expandable 8-Input Gate	Now		Note 1
CD4049A	Hex Buffer/Converter (Inverting Type)	Now	MIL-M-38510/05503	Now
CD4050A	Hex Buffer /Converter (Non-Inverting Type)	Now	MIL-M-38510/05504	Now
CD4051A	Single 8-Channel Analog Multiplexer	Now	MIL-M-38510/05803	Note 2
CD4052A	Differential 4-Channel Anglog Multiplexer	Now		Note 1
CD4053A	Triple 2-Channel Analog Mutliplexer	Now		Note 1
CD4057A	LSI 4-Bit Arithmetic Array	Now	MIL-M-38510/05903	Note 2

TABLE I – Product Classification Guide for RCA High-Reliability COS/MOS Integrated Circuits (Continued)

MIL-STD-883 Slash-Series and MIL-M-38510 Series Types				
Standard Product Type No.	Descriptive Title	Availability of MIL-STD-883 Slash-Series Types	MIL-M-38510 Series Types	
			Detailed Electrical Specification No.	Availability of Parts
CD4059A	Divide-by-N Counter (Programmable)	2nd Q 1976		Note 1
CD4060A	14-Stage Binary Counter and Oscillator	Now		Note 1
CD4061A	256-Bit Static Random-Access Memory	Now	MIL-M-38510/05902	Note 2
CD4062A	200-Stage Dynamic Shift Register	Now		Note 1
CD4063B	4-Bit Magnitude Comparator	Now		Note 1
CD4066A	Quad Bilateral Switch	Now	MIL-M-38510/05802	Note 2
CD4067B	Single 16-Channel Multiplexer/ Demultiplexer	1st Q 1976		Note 1
CD4068B	8-Input NAND Gate	Now		Note 1
CD4069B	Hex Inverter	Now		Note 1
CD4070B	Quad Exclusive-OR Gate	1st Q 1976		Note 1
CD4071B	Quad 2-Input OR Gate	Now		Note 1
CD4072B	Dual 4-Input OR Gate	Now		Note 1
CD4073B	Triple 3-Input AND Gate	Now		Note 1
CD4075B	Triple 3-Input OR Gate	Now		Note 1
CD4076B	3-State 4-Bit "D" Type Register	1st Q 1976		Note 1
CD4077B	Quad Exclusive-NOR Gate	1st Q 1976		Note 1
CD4078B	8-Input NOR Gate	Now		Note 1
CD4081B	Quad 2-Input AND Gate	Now		Note 1
CD4082B	Dual 4-Input AND Gate	Now		Note 1
CD4085B	Dual 2-Wide 2-Input AND-OR-Invert Gate	Now		Note 1
CD4086B	Expandable 4-Wide 2-Input AND-OR-Invert Gate	Now		Note 1
CD4089B	Binary Rate Multiplier	1st Q 1976		Note 1
CD4093B	Quad 2-Input NAND Schmitt Trigger	1st Q 1976		Note 1
CD4094B	8-Bit Bus Register With Shift and Store	1st Q 1976		Note 1
CD4095B	Gated JK Flip-Flop (Non-Inverting J and K Inputs)	1st Q 1976		Note 1
CD4096B	Gated JK Flip-Flop (Inverting and Non-Inverting J and K Inputs)	1st Q 1976		Note 1
CD4097B	Differential 8-Channel Multiplexer/ Demultiplexer	1st Q 1976		Note 1
CD4098B	Dual Retiggerable/Resettable Monostable Multivibrator	1st Q 1976		Note 1
CD4099B	8-Bit Addressable Latch	1st, 2nd Q 1976		Note 1
CD4502B	Strobed Hex Inverter/Buffer	2nd Q 1976		Note 1
CD4508B	Dual 4-Bit Latch	2nd Q 1976		Note 1
CD4510B	4-Bit BCD Up/Down Counter	1st Q 1976		Note 1
CD4511B	BCD-to-Seven-Segment Latch Decoder Driver	1st Q 1976		Note 1
CD4514B	4-Bit Latch/4-to-16 Line Decoder (Outputs High)	Now		Note 1
CD4515B	4 Bit Latch/4-to-16 Line Decoder (Outputs Low)	Now		Note 1
CD4516B	4-Bit Binary Up/Down Counter	1st Q 1976		Note 1
CD4518B	Dual BCD Up Counter	Now		Note 1
CD4520B	Dual Binary Up Counter	Now		Note 1
CD4527B	BCD Rate Multiplier	3rd Q 1976		Note 1
CD4532B	8-Input Priority Encoder	1st Q 1976		Note 1
CD4555B	Dual 1-of-4 Decoder/Demultiplexer (Outputs High)	1st Q 1976		Note 1
CD4556B	Dual 1-of-4 Decoder/Demultiplexer (Ouputs Low)	1st Q 1976		Note 1
CD40100	32-Bit Left/Right Shift Register	3rd Q 1976		Note 1
CD40101	Parity Generator/Checker	3rd Q 1976		Note 1
CD40102	Presettable 8-Bit BCD Down Counter	3rd Q 1976		Note 1
CD40103	Presettable 8-Bit Binary Down Counter	3rd Q 1976		Note 1
CD40104	3-State, 4-Bit Left/Right Shift Register	3rd Q 1976		Note 1
CD40105	FIFO Buffer Register	3rd Q 1976		Note 1
CD40107	Dual 2-Input NAND Buffer/Driver	3rd Q 1976		Note 1
CD40108	4 X 4 Multiport Register	3rd Q 1976		Note 1

Table 1 – Product Classification Guide for RCA High-Reliability COS/MOS Integrated Circuits (Continued)

MIL-STD-883 Slash-Series and MIL-M-38510 Series Types				
Standard Product Type No.	Descriptive Title	Availability of MIL-STD-883 Slash-Series Types	MIL-M-38510 Series Types	
			Detailed Electrical Specification No.	Availability of Parts
CD40109	Quad Low-to-High Voltage Level Shifter	3rd Q 1976		Note 1
CD40181	4-Bit Arithmetic Logic Unit	3rd Q 1976		Note 1
CD40182	Look-Ahead-Carry Block Arithmetic Logic Unit	3rd Q 1976		Note 1
CD40192	Synchronous 4-Bit Up/Down 3 BCD Counter	3rd Q 1976		Note 1
CD40193	Synchronous 4-Bit Up/Down Binary Counter	3rd Q 1976		Note 1
CD40194	4-Bit Left/Right Shift Register	3rd Q 1976		Note 1
CD40257	Quad 2-line-to-1-line Data Selector Multiplexer	3rd Q 1976		Note 1

Notes:
1. No MIL-M-38510 detailed electrical specifications have been defined as yet. RCA plans to add additional types to the MIL-M-38510 series on a continuing basis.
2. MIL-M-38510 nomenclature has been assigned for these circuits. Proposed detailed electrical specifications have been developed and are under review by governmental agencies. RCA will take custom orders for these circuits, processed and tested to the proposed specifications, starting about mid-1976.

Table II – Product Classification Guide for RCA High-Reliability Microprocessors

CDP1801 System		
MIL-STD-883 Slash-Series Types		
Product Type #	Description	Availability to MIL-STD-883 RCA Slash Series
	Microprocessor (COSMAC)	
CDP1801D	Two-Chip Set	Mid 1976
CDP1801UD	Processor Chip	
CDP1801RD	Register Chip	
	I/O Circuit	
CD4000 Series COS/MOS		Now
	Memory	
CD4061A	256-Bit RAM	Now
	CDP1802 System	
MIL-STD-883 Slash-Series Type		
Product Type #	Description	Availability to MIL-STD-883 RCA Slash Series
	Microprocessor	
CDP1802D	Complete Processor	Early 1977
	Memory	
CDP1821SD	1024 x 1 RAM	1977
CDP1822SD	256 x 4 RAM	1977
CDP1824D	32 x 8 RAM	1977
CDP1831D	512 x 8 ROM (COSMAC Compatible)	1977
CDP1832D	512 x 8 ROM (Intel PROM Compatible)	1977
	I/O Circuits	
CDP1852D	BYTE I/O	1977
CDP1853D	1-of-8 Latch Decoder	1977
CDP1854D	UART	1977
CDP1855D	Multiply/Divide Chip	1977

Table III – Product Classification Guide for RCA High-Reliability CMOS and NMOS Integrated-Circuit Memories

Product Type #	Description	Technology	Availability to MIL-STD-883 RCA Slash Series
CD4061AD	256X1 Bit RAM	Std. COS/MOS	Now
MSW5501D	1024X1 Bit (10V)	SOS/CMOS	2nd Half 1976
MWS5540D	256X4 Bit (10V)	SOS/CMOS	Early 1977
MW4050D	4096X1 Bit/18 Pin	NMOS	Mid 1976
MW4060D	4096X1 Bit/22 Pin	NMOS	Mid 1976

Table IV – Product Classification Guide for RCA High-Reliability Linear Integrated Circuits

MIL-STD-883 Slash-Series Types		
Standard Product Type No.	Descriptive Title	Availability of MIL-STD-883 Slash-Series Types
CA101AT	Operational Amplifier, General-Purpose	Now 1975
CA101T	Operational Amplifier, General-Purpose	Now 1975
CA107T	Operational Amplifier, General-Purpose	Now 1975
CA108AT	Operational Amplifier, Precision	Now 1975
CA108T	Operational Amplifier, Precision	Now 1975
CA111T	Voltage Comparator	Now 1975
CA723T	Voltage Regulator	Now 1975
CA741CT	Operational Amplifier, General-Purpose	Use CA741T
CA741T	Operational Amplifier, General-Purpose	Now
CA747CT	Operational Amplifier, General-Purpose	Use CA747T
CA747T	Operational Amplifier, General-Purpose	Now
CA748CT	Operational Amplifier, General-Purpose	Use CA748T
CA748T	Operational Amplifier, General-Purpose	Now
CA1458T	Operational Amplifier, General-Purpose	Use CA1558T
CA1541D	Dual-Input Memory Sense Amplifier	Custom Basis Only
CA1558T	Operational Amplifier, General-Purpose	Now
CA3000	DC Amplifier	Now
CA3001	Video and Wide-Band Amplifier	Now
CA3002	IF Amplifier	Now
CA3004	RF Amplifier	Now
CA3005	RF Amplifier	Use CA3006
CA3006	RF Amplifier	Now
CA3010	Operational Amplifier	Use CA3015, CA3015A
CA3010A	Operational Amplifier	Use CA3015, CA3015A
CA3011	FM IF Amplifier	Use CA3014
CA3012	FM IF Amplifier	Use CA3014
CA3013	Wide-Band Amplifier/Limiter/FM Detector	Use CA3014
CA3014	Wide-Band Amplifier/Limiter/FM Detector	Custom Basis Only
CA3015	Operational Amplifier	Now
CA3015A	Operational Amplifier	Now
CA3018	General-Purpose Transistor Array	Use CA3018A
CA3018A	General-Purpose Transistor Array	Now
CA3019	Diode Array (Quad and Two Individual Diodes)	Now
CA3020	Multipurpose Wide-Band Power Amplifier	Use CA3020A
CA3020A	Multipurpose Wide-Band Power Amplifier	Now
CA3026	Dual Independent Differential Amplifier	Now
CA3028A	Differential/Cascode Amplifier	Use CA3028B
CA3028B	Differential/Cascode Amplifier	Now
CA3036	Dual Darlington Array	Custom Basis Only
CA3037	Operational Amplifier	Use CA3038, CA3038A
CA3037A	Operational Amplifier	Use CA3038, CA3038A
CA3038	Operational Amplifier	Custom Basis Only
CA3038A	Operational Amplifier	Custom Basis Only
CA3039	Diode Array (Six Matched Diodes)	Now
CA3043	FM IF Subsystem	Custom Basis Only
CA3045	General-Purpose Transistor Array	Now
CA3046	General-Purpose Transistor Array	Use CA3045
CA3049T	Dual Independent Differential RF/IF Amplifier	Now
CA3053	Differential/Cascode Amplifier	Use CA3028B
CA3058	Zero-Voltage Switch	Now
CA3060AD	Triple Operational Transconductance Amplifier Array	Custom Basis Only
CA3060BD	Triple Operational Transconductance Amplifier Array	Custom Basis Only
CA3060D	Triple Operational Transconductance Amplifier Array	Use CA3060AD

Table IV – Product Classification Guide for RCA High-Reliability Linear Integrated Circuits (Continued)

MIL-STD-883 Slash-Series Types		
Standard Product Type No.	**Descriptive Title**	**Availability of MIL-STD-883 Slash-Series Types**
CA3076	High-Gain Wide-Band IF Amplifier-Limiter	Custom Basis Only
CA3078AT	Micropower Operational Amplifier	Now
CA3078T	Micropower Operational Amplifier	Now
CA3080	Operational Transconductance Amplifier	Now
CA3080A	Operational Transconductance Amplifier	Now
CA3085	Positive Voltage Regulator	Now
CA3085A	Positive Voltage Regulator	Now
CA3085B	Positive Voltage Regulator	Now
CA3086	General-Purpose N-P-N Transistor Array	Use CA3045
CA3091D	Four-Quadrant Multiplier	Custom Basis Only
CA3094AT	Programmable Power Switch/Amplifier	Now
CA3094BT	Programmable Power Switch/Amplifier	Now
CA3094T	Programmable Power Switch/Amplifier	Now
CA3100T	Wide-Band Operational Amplifier	Now
CA3118AT	High-Voltage Transistor Array	Now
CA3118T	High-Voltage Transistor Array	Now
CA3130T	COS/MOS Operational Amplifier	Now
CA3130AT	COS/MOS Operational Amplifier	Now
CA3130BT	COS/MOS Operational Amplifier	Now
HR3N187	Dual-Gate FET	Now
HR3N200	Dual-Gate FET	Now

MIL-M-38510 Series Types			
Standard Product Type No.	**Descriptive Title**	**MIL-M-38510/100 Series Type**	
		Detailed Electrical Specification No.	**Projected Availability**
CA101A	Operational Amplifier	MIL-M-38510/10103	Mid 1976
CA108A	Operational Amplifier	MIL-M-38510/10104	Late 1976
CA741	Operational Amplifier	MIL-M-38510/10101	Early 1976
CA747	Operational Amplifier	MIL-M-38510/10102	Mid 1976
CA723	Voltage Regulator	MIL-M-38510/10201	Mid 1976
CA111	Voltage Comparator	MIL-M-38510/10304	Mid 1976
CA3018A CA3045	Transistor Arrays	In Process	Early 1976

MIL-STD-883 Requirements

RCA Solid State Division offers a broad range of COS/MOS and linear integrated circuits processed and screened in accordance with MIL-STD-883, Method 5004.3, Class A, B, or C requirements.

The product-flow chart for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883 is shown in Fig. 1. After wafer processing, special visual inspections are performed to MIL-STD-883, Method 2010.2, Condition B or A at both chip and pre-seal inspections to assure a packaged chip of high reliability. In the case of Class A product (RCA levels /1 and /2), parts are tested functionally, and then receive a dc parameter test; significant parameters are recorded.

A 240-hour burn-in at 125°C is performed on all parts. All readings are repeated, and delta shifts calculated. The customer is provided with print-outs of these parameters identified by the serial number on the part. The parts then go through 100-per-cent high- and low-temperature testing under functional and dc operating conditions. Next, 100-per-cent ac testing is accomplished followed by Group A sampling of all test conditions. The Class A product is branded, visually inspected, and retested both functionally and to dc parameters prior to packaging and shipment to the customer. The screening tests for Class B (RCA level /3) and Class C (RCA level /4) devices are reduced as shown in Table V in which X designates that a test is performed 100 percent and S indicates that the test is a screen. For Class-B devices, the main difference is that burn-in is for 160 hours with GO-NO/GO parameter readings made before and after burn-in. Temperature testing is done on a sampling basis, and visual inspection prior to sealing is not as critical. Class-C devices are tested similarly to Class-B devices less the burn-in, temperature, and ac tests.

MIL-M-38510 Requirements for High-Reliability COS/MOS Integrated Circuits

MIL-M-38510 is the general specification for integrated circuits and the top document for MIL-STD-883. This general specification, introduced a year after MIL-STD-883 was in existence, adds a number of quality constraints not included in MIL-STD-883, which is a specification of test methods, procedures, and screening tests. Parts are provided to MIL-M-38510 under a series of /050 numbers of which nine are in existence. These nine numbers cover twenty-seven COS/MOS types. Parts meet requirements similar to those of Classes A, B, and C of MIL-STD-883. Method 5004 screening, except that additional requirements, including more test conditions and tightened limits, are imposed. The additional criteria for each class of product are designated by an X in Table VI. Also provided in MIL-M-38510 tests are PDA's (Per-Cent Defective Allowed) of 10 per cent for the three burn-in operations performed on Class-A product, and 10 per cent for the one burn-in of Class-B product. Table VII provides a list of the COS/MOS devices for which MIL-M-38510 /050-number specification sheets have been written.

Fig. 2 shows a product-flow diagram for RCA COS/MOS integrated circuits processed in accordance with MIL-M-38510.

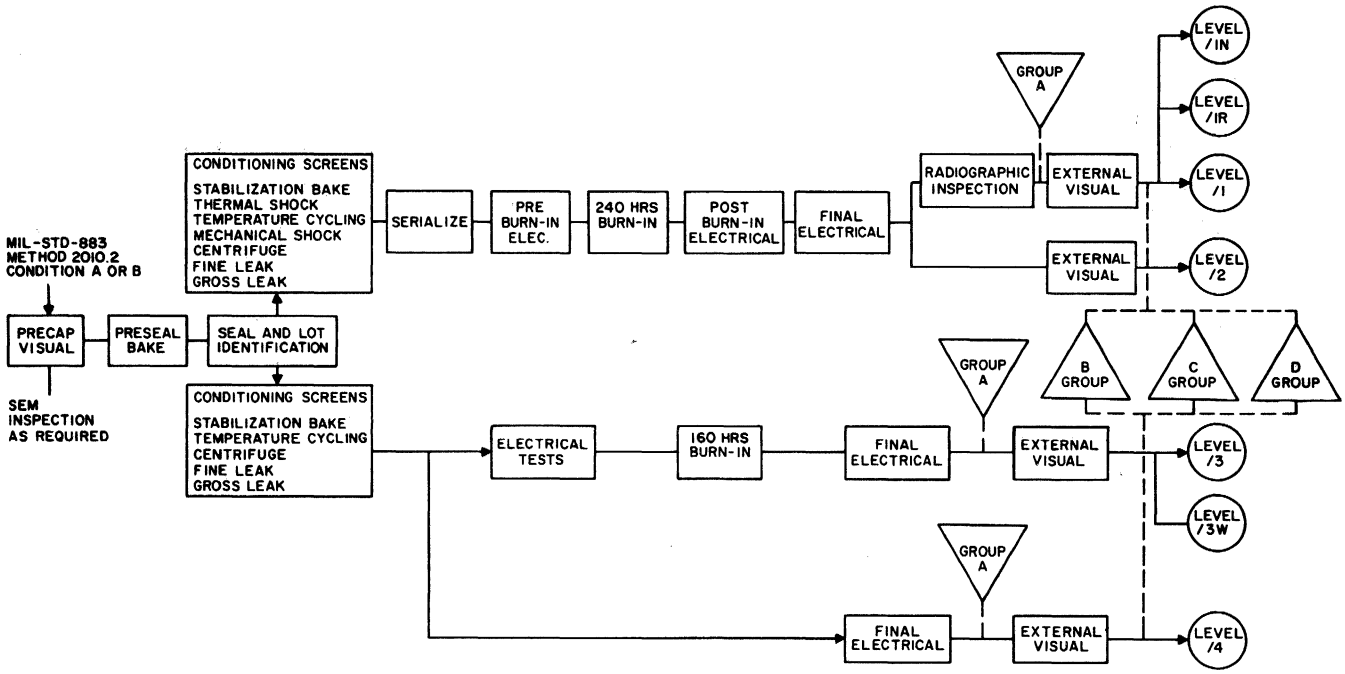


Fig. 1 – Product-flow diagram for RCA high-reliability integrated circuits processed in accordance with MIL-STD-883, Methods 5004.3 and 5005.3.

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Table V – Description of Total Lot Screening per MIL-STD-883, Method 5004.3

Test	Conditions	MIL-STD-883		Screening Levels						
		Method	Conditions	/1N	/1R	/1	/2	/3	/3W	/4
SEM Inspection	–	2018	–	X	X	–	–	–	–	
Precap Visual	–	2010.2	A	X	–		–	–	–	–
Precap Visual	–	2010.2	B	–	X	X	X	X	X	X
Preseal Bake	2 Hrs. min. at 200°C	–	–	X	X	X	X	X	X	X
Seal & Lot Identification	–	–	–	X	X	X	X	X	X	X
Stabilization Bake	48 hrs. at 150°C	1008	C	X	X	X	X	X	X	X
Temperature Cycling	10 cycles	1010	C	X	X	X	X	X	X	X
Centrifuge	Y_2, Y_1 direction,	2001	E	X	X	X	X	–	–	–
	Y_1 direction only	2001	E	–	–	–	–	X	X	X
Fine Leak	–	1014	A	X	X	X	X	X	X	X
Gross Leak	–	1014	C	X	X	X	X	X	X	X
Electrical Tests	–	–	–	X	X	X	X	X	X	–
Serialize	–	–	–	X	X	X	X	–	–	–
Pre Burn-in Electrical	see Table IX	–	–	X	X	X	X	–	–	–
Burn-in	240 hours (see Note 1)	1015	B, D, E, or F	X	X	X	X	–	–	–
	160 hours (see Note 1)	1015	B, D, E, or F	–	–	–	–	X	X	–
Post Burn-in Electrical	Delta Requirements (See Table IX)	–	–	X	X	X	X	–	–	–
Final Electrical										
a) 25°C	see Table VII	–	–	X	X	X	X	X	X	X
b) -55 and +125°C DC and 25°C AC	see Table VII	–	–	X	X	X	X	X	–	S
Radiographic Inspection	1 view	2012	–	X	X	X	–	–	–	–
External Visual	–	2009	–	X	X	X	X	X	X	X

Note 1: RCA may substitute method 1015 Condition F, which provides variable burn-in time and temperature options.

Table VI – MIL-M-38510 requirements in addition to those of MIL-STD-883

Requirements	Class A	Class B	Class C
Product assurance plan	X	X	X
Manufacturing Certification	X	X	X
Line certification	X		
SEM inspection	X		
Radiographic NHB5300.4(3E)	X		
Two bias burn-in 24 hrs.	X		
Tighter DC electrical	X	X	X
Tighter AC electrical	X	X	X

Table VII – COS/MOS devices for which specification sheets have been written

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/050	
01	CD4011A
02	CD4012A
03	CD4023A
MIL-M-38510/051	
01	CD4013A
02	CD4027A
MIL-M-38510/052	
01	CD4000A
02	CD4001A
03	CD4002A
04	CD4025A
MIL-M-38510/053	
01	CD4007A
02	CD4019A
MIL-M-38510/054	
01	CD4008A
No other detailed electrical specifications have been defined by NASA or military agencies at this time. RCA plans to qualify most of the COS/MOS product line in the future.	

Detailed Electrical Specification, MIL-M-38510	Device Covered
MIL-M-38510/055	
01	CD4009A
02	CD4010A
03	CD4049A
04	CD4050A
MIL-M-38510/056	
01	CD4017A
02	CD4018A
03	CD4020A
04	CD4022A
05	CD4024A
MIL-M-38510/057	
01	CD4006A
02	CD4014A
03	CD4015A
04	CD4021A
05	CD4031A
MIL-M-38510/058	
01	CD4016A

MIL-M-38510 Wafer Lot Acceptance, Screening Procedures, Qualification and Conformance Testing per MIL-STD-883 Methods 5007, 2018, 2010.2, 5004.3 and 5005.3

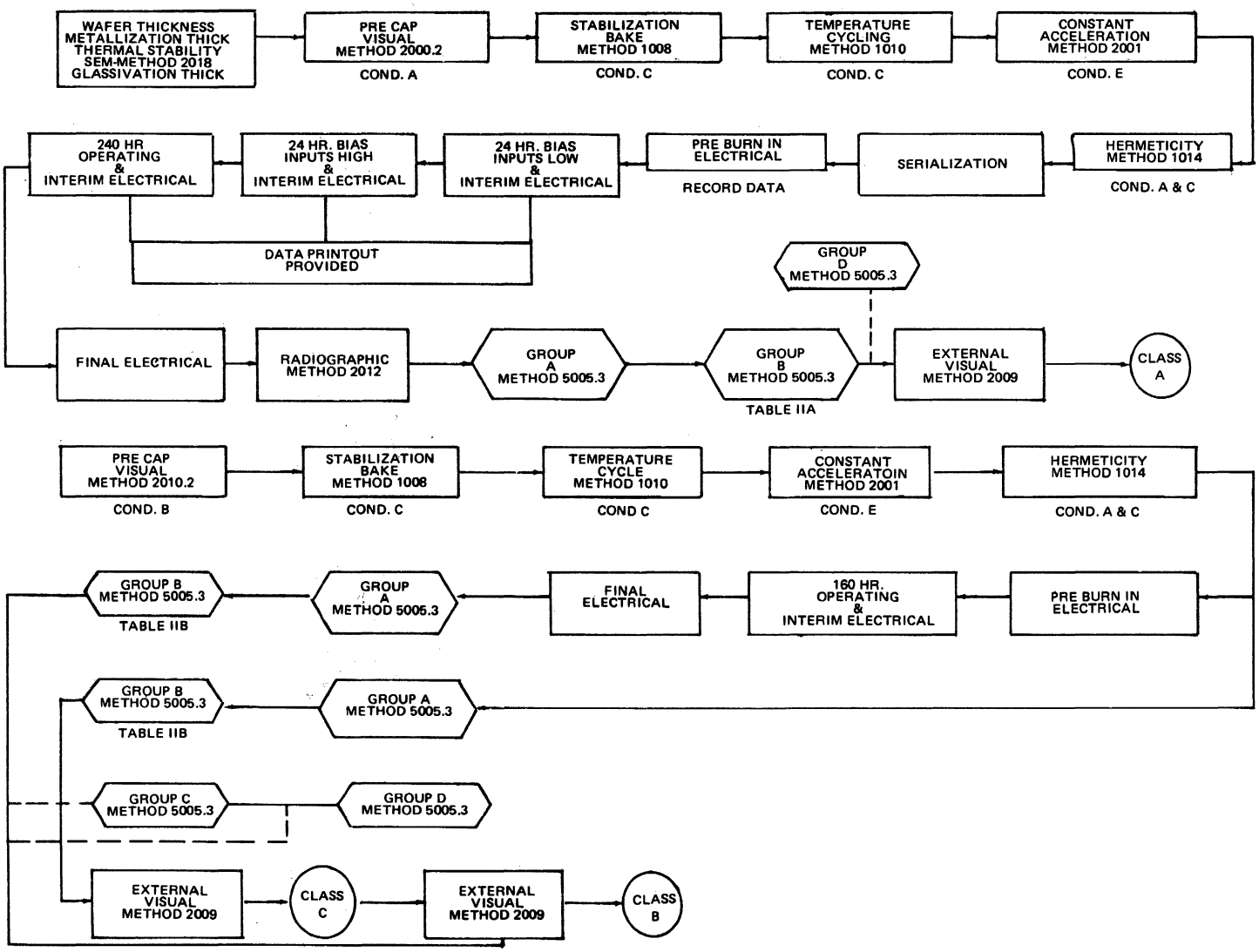


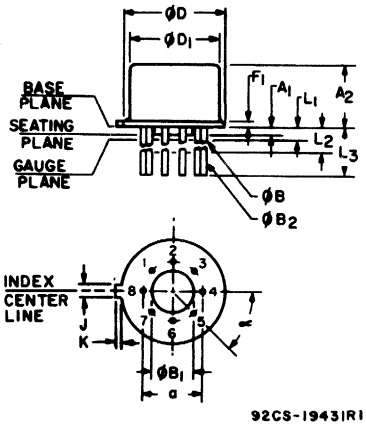
Fig. 2 – PRODUCT FLOW CHART for RCA Class A High Reliability Integrated Circuits Processed in Accordance with MIL-M-38510.

Appendix

Dimensional Outlines

DIMENSIONAL OUTLINES FOR LINEAR INTEGRATED CIRCUITS AND MOS/FET DEVICES

(T) Suffix JEDEC MO-002-AL 8-Lead TO-5 Style

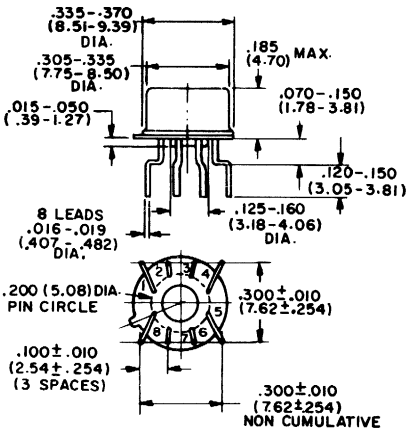


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

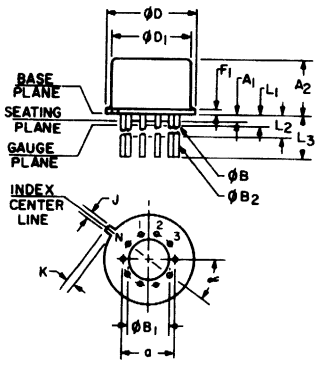
NOTES

1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

(S) Suffix 8-Lead TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)



(T) Suffix JEDEC MO-006-AF 10-Lead TO-5 Style



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

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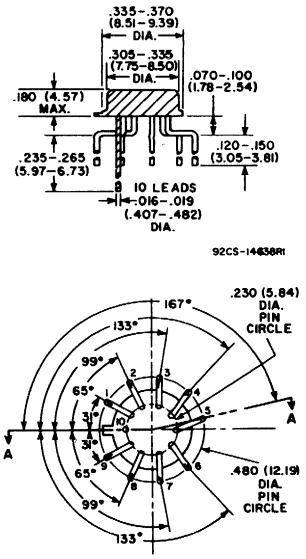
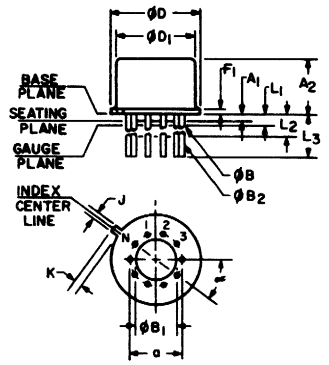
(V) Suffix 10 Formed Leads Radially Arranged TO-5 Type



Dimensional Outlines (Cont'd)

(T) Suffix JEDEC MO-006-AG 12-Lead TO-5 Style



SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
ϕB	0.016	0.019	3	0.407	0.482
ϕB_1	0	0		0	0
ϕB_2	0.016	0.021	3	0.407	0.533
ϕD	0.335	0.370		8.51	9.39
ϕD_1	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	30° TP			30° TP	
N	12		6	12	
N_1	1		5	1	

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. ϕD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

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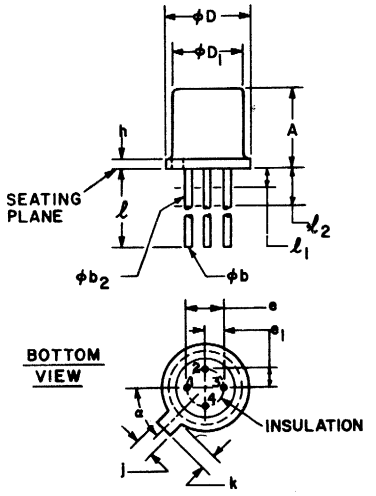


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		4
e_1	0.050 T.P.		1.27 T.P.		4
h		0.030		0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500		12.70		2
l_1		0.050		1.27	2
l_2	0.250		6.35		2
α	45° T.P.		45° T.P.		4, 6

Note 1: (Four leads). Maximum number leads omitted in this outline, "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.

Note 2: (All leads) ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and .500" (12.70 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond .500" (12.70 mm) from seating plane.

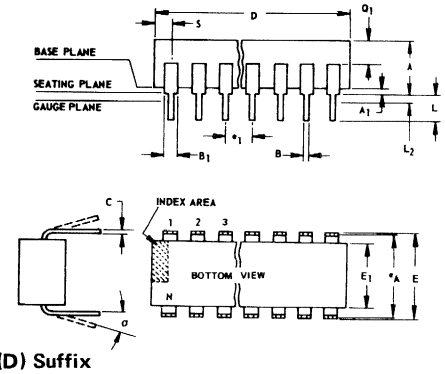
Note 3: Measured from maximum diameter of the product.

Note 4: Leads having maximum diameter .019" (.483 mm) measured in gaging plane .054" (1.37 mm) + .001" (.025 mm) – .000" (.000 mm) below the seating plane of the product shall be within .007" (.178 mm) of their true position relative to a maximum width tab.

Note 5: The product may be measured by direct methods or by gage.

Note 6: Tab centerline.

White Ceramic Dual-In-Line Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix JEDEC MO-001-AD 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.065	0.090		1.66	2.28

92SS-441IRI

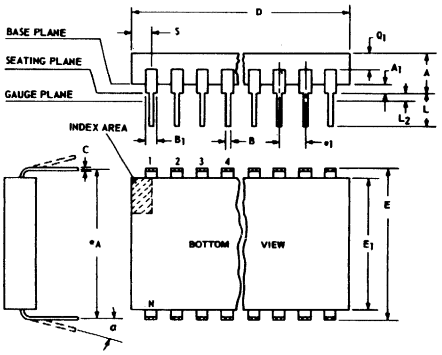
(D) Suffix JEDEC MO-001-AE 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.160		3.05	4.06
A_1	0.020	0.065		0.51	1.65
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.050	0.085		1.27	2.15
S	0.015	0.060		0.39	1.52

92SS-4286R4

Dimensional Outlines (Cont'd)

CERAMIC DUAL-IN-LINE PACKAGES (Cont'd)



NOTES:

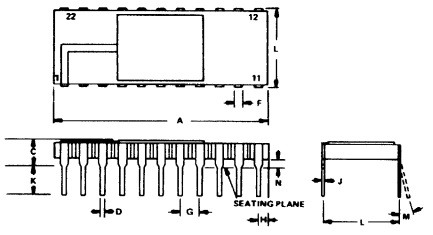
Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix
JEDEC MO-015-AG
24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.090	0.150		2.29	3.81
A_1	0.020	0.065	2	0.51	1.65
B	0.015	0.020		0.381	0.508
B_1	0.045	0.055		1.143	1.397
C	0.008	0.012	1	0.204	0.304
D	1.15	1.22		29.21	30.98
E	0.600	0.625		15.24	15.87
E_1	0.480	0.520		12.20	13.20
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.180		2.54	4.57
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.020	0.080		0.51	2.03
S	0.020	0.060		0.51	1.52

92CS-19948



92CS-25186

NOTES

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAXIMUM LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013" (0.33 mm).

(D) Suffix
JEDEC MO-015-AH
28-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.100	.200	2.6	5.0	2
A_1	.000	.070	0	1.77	
B	.015	.020	.381	.508	
B_1	.015	.055	.39	1.39	
C	.008	.012	.204	.304	
D	1.380	1.420	35.06	36.06	
E	.600	.625	15.24	15.87	
E_1	.485	.515	12.32	13.08	
e_1	.100 TP		2.54 TP		3
e_A	.600 TP		15.24 TP		3
L	.100	.200	2.6	5.0	
L_2	.000	.030	0	.76	
α	0	15	0°	15°	4
N	28		28		5
N_1	0		0		6
Q_1	.020	.070	.51	1.77	
S	.040	.070	1.02	1.77	
See Note	1				

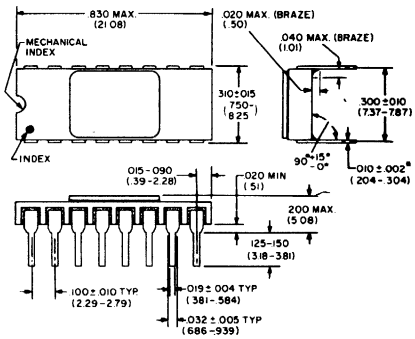
92CM-20250

(D) Suffix
22-Lead Dual-In-Line Side-Brazed

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	27.05	27.94	1.065	1.100
C	2.16	3.68	0.085	0.145
D	0.43	0.56	0.017	0.023
F	1.02 REF.		0.040 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	9.65	10.67	0.380	0.420
M	–	7°	–	7°
N	0.64	1.27	0.025	0.050

White Ceramic Side-Brazed Packages

(D) Suffix
16-Lead Dual-In-Line Side-Brazed

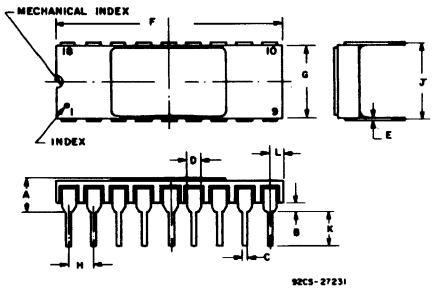


* WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAX. LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED .0013 (.033mm)

NOTE: DIMENSIONS IN PARENTHESES ARE IN MILLIMETERS AND ARE DERIVED FROM THE BASIC INCH DIMENSIONS

92CS-21219

(D) Suffix
18-Lead Dual-In-Line Side-Brazed



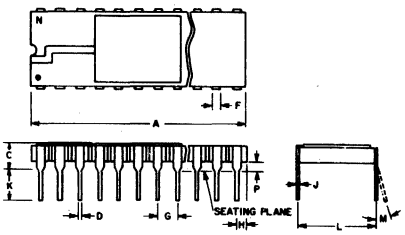
92CS-27231

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	–	0.200	–	5.08	
B	0.020	0.045	0.51	1.14	
C	0.015	0.021	0.381	0.533	
D	0.54		1.37		
E	0.008	0.012	0.204	0.304	1
F	0.890	0.915	22.61	23.24	
G	0.280	0.300	7.12	7.62	
H	0.100		2.54		2
J	0.300		7.62		2, 3
K	0.125	0.150	3.18	3.81	
L	0.035	0.065	0.89	1.65	

NOTES:

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.13 mm) radius of true position at maximum material condition.
3. Lead spacing (center to center) when formed parallel.

Dimensional Outlines (Cont'd)



(D) Suffix
28-Lead Dual-In-Line Side-Brazed

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	35.06	36.06	1.380	1.420
C	2.16	3.68	0.085	0.145
D	0.43	0.56	0.017	0.023
F	1.27 REF.		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050
N	28		28	

92CM-26419

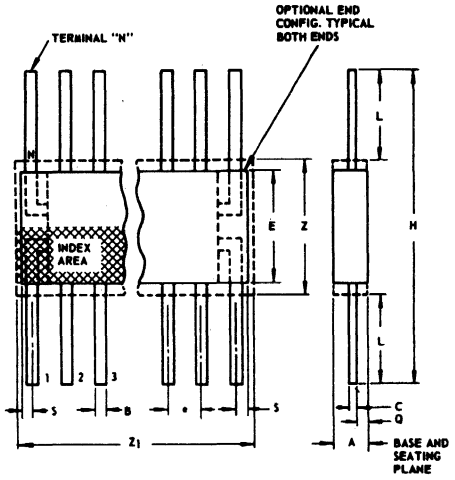
NOTES:
1. Leads within 0.13 mm (0.005) radius of true position at maximum material condition.
2. Dimension "L" to center of leads when formed parallel.
3. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).

(D) Suffix
40-Lead Dual-In-Line Side-Brazed

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	50.30	51.30	1.980	2.020
C	2.42	3.93	0.095	0.155
D	0.43	0.56	0.017	0.023
F	1.27 REF.		0.050 REF.	
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	4.45	0.125	0.175
L	14.74	15.74	0.580	0.620
M	–	7°	–	7°
P	0.64	1.27	0.025	0.050
N	40		40	

92CM-27029

Ceramic Flat Packs



NOTES:
1. Refer to JEDEC Publication No. 13 for Rules for Dimensioning Peripheral Lead Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(K) Suffix
JEDEC MO-004-AF 14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	14		3	14	
Q	0.005	0.050		0.13	1.27
S	0.000	0.050		0.00	1.27
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92SS-4300RI

(K) Suffix
JEDEC MO-004-AG 16-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.008	0.100		0.21	2.54
B	0.015	0.019	1	0.381	0.482
C	0.003	0.006	1	0.077	0.152
e	0.050 TP		2	1.27 TP	
E	0.200	0.300		5.1	7.6
H	0.600	1.000		15.3	25.4
L	0.150	0.350		3.9	8.8
N	16		3	16	
Q	0.005	0.050		0.13	1.27
S	0.000	0.025		0.00	0.63
Z	0.300		4	7.62	
Z_1	0.400		4	10.16	

92CS-17271RI

(K) Suffix
24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	24		3	24	
Q	0.035	0.070		0.89	1.77
S	0.060	0.110	1	1.53	2.79
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-19949

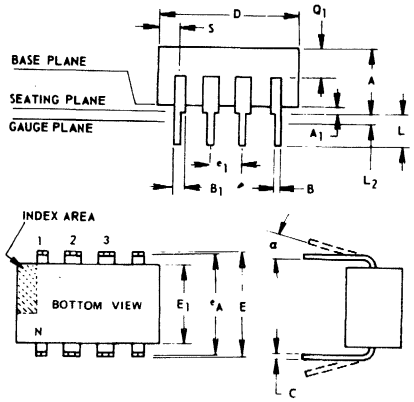
(K) Suffix
28-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.075	0.120		1.91	3.04
B	0.018	0.022	1	0.458	0.558
C	0.004	0.007	1	0.102	0.177
e	0.050 TP		2	1.27 TP	
E	0.600	0.700		15.24	17.78
H	1.150	1.350		29.21	34.29
L	0.225	0.325		5.72	8.25
N	28		3	28	
Q	0.035	0.070		0.89	1.77
S	0	0.060	1	0	1.53
Z	0.700		4	17.78	
Z_1	0.750		4	19.05	

92CS-20972

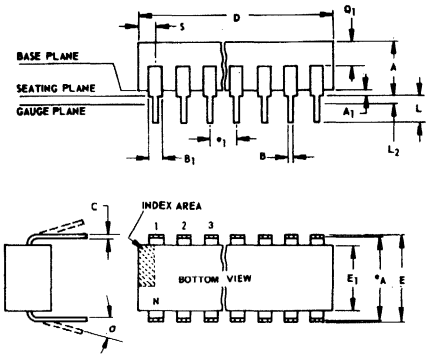
Dimensional Outlines (Cont'd)

DUAL-IN-LINE PLASTIC AND FRIT-SEAL CERAMIC PACKAGES



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.



(E), (F) and (G) Suffixes
JEDEC MO-001-AB
14-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

92SS-4296R2

(F) Suffix
8-Lead Frit-Seal Ceramic

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.203	0.304
D	0.376	0.396		9.55	10.05
E	0.315	0.345		8.00	8.76
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.100	0.150		2.54	3.81
L_2	0.000	0.030		0.000	0.762
α	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.020	0.060		0.508	1.52

92CM-20827

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(E) and (F) Suffixes
JEDEC MO-001-AC
16-Lead
(except types CD4026AF, CD4029AF, CD4031AF, CD4033AF)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.89	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.785		18.93	19.93
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.39	1.52

92CM-15967R3

(E) and (G) Suffixes
8-Lead Plastic (Mini-Dip)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.508	1.27
B	0.014	0.020		0.356	0.508
B_1	0.035	0.065		0.889	1.65
C	0.008	0.012	1	0.203	0.304
D	0.370	0.400		9.40	10.16
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.762
α	0°	15°	4	0°	15°
N	8		5	8	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.015	0.060		0.381	1.52

92CS-24026

(E) and (F) Suffixes
JEDEC MO-001-AG
16-Lead
(Types CD4026AF, CD4029AF, CD4031AF, CD4033AF)

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	*0.165*	*0.210*		*4.20*	*5.33*
A_1	*0.015*	*0.045*		*0.381*	*1.14*
B	*0.015*	0.020		*0.381*	0.508
B_1	*0.045*	*0.070*	7	*1.15*	*1.77*
C	*0.009*	**0.011*		*0.229*	*0.279*
D	*0.750*	*0.795*		*19.05*	*20.19*
E	*0.295*	0.325		*7.50*	8.25
E_1	*0.245*	*0.300*		*6.23*	*7.62*
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	*0.120*	*0.160*		*3.05*	*4.06*
L_2	0.000	0.030		0.000	0.76
α	*2°*	15°	4	*2°*	15°
N	16		5	16	
N_1	0		6	0	
Q_1	*0.050*	*0.080*		*1.27*	*2.03*
S	*0.010*	0.060		*0.254*	1.52

92CM-22284

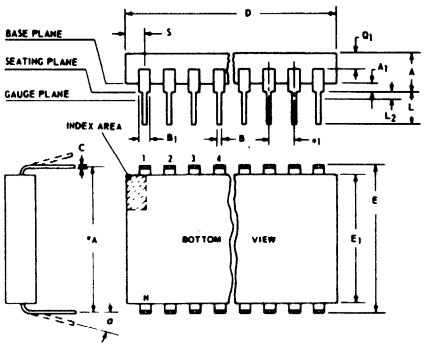
NOTES

1. Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines.
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.
7. B_1 applies to all leads except the four end leads which have one-half the normal width (B_1 min. = 0.025 in.)

This outline differs from the standard 16-Lead frit-seal ceramic package MO-001-AC as indicated by the values in italics shown in the chart above.

Dimensional Outlines (Cont'd)

DUAL-IN-LINE PLASTIC PACKAGES



NOTES:
Refer to JEDEC Publication No. 13 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).
2. When base of body is to be attached to heat sink, terminal lead standoffs are not required and $A_1 = 0$. When $A_1 = 0$, the leads emerge from the body with the B_1 dimension and reduce to the B dimension above the seating plane.
3. e_1 and e_A apply in zone L_2 when unit is installed. Leads within 0.005 " (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

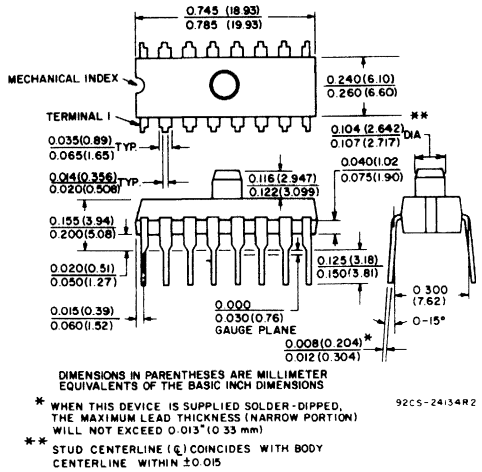
(E) Suffix
JEDEC MO-015-AA 24-Lead

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.120	0.250		3.10	6.30
A_1	0.020	0.070	2	0.51	1.77
B	0.016	0.020		0.407	0.508
B_1	0.028	0.070		0.72	1.77
C	0.008	0.012	1	0.204	0.304
D	1.20	1.29		30.48	32.76
E	0.600	0.625		15.24	15.87
E_1	0.515	0.580		13.09	14.73
e_1	0.100 TP		3	2.54 TP	
e_A	0.600 TP		3	15.24 TP	
L	0.100	0.200		2.54	5.00
L_2	0.000	0.030	3	0.00	0.76
α	0°	15°	4	0°	15°
N	24		5	24	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.040	0.100		1.02	2.54

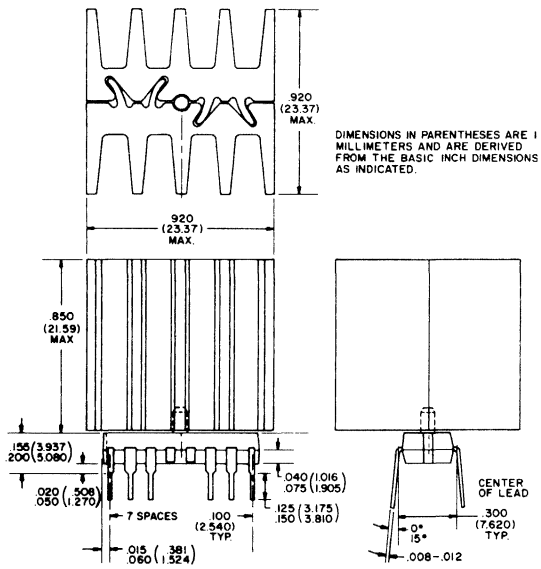
92CS-26938

DUAL-IN-LINE PLASTIC PACKAGES (Power Stud and Heat-Sink Types)

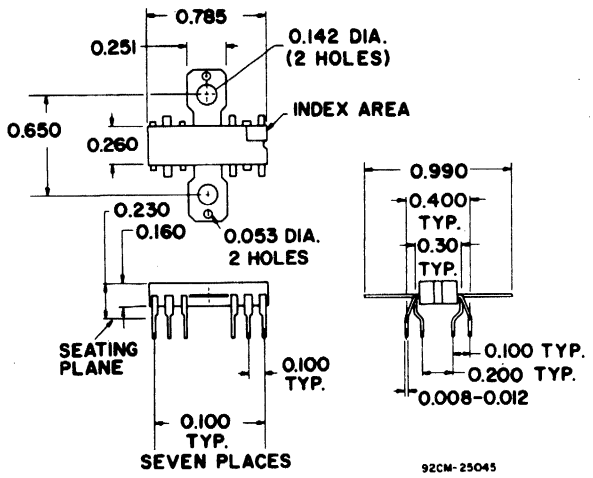
(E) Suffix
16-Lead "Power-Stud" Package



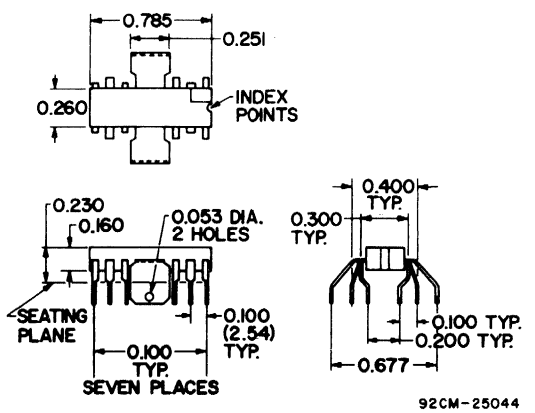
(EM) Suffix
Modified 16-Lead with Integral Heat Sink



(QM) Suffix
Modified 16-Lead with Integral Flat Wing-Tab Heat Sink



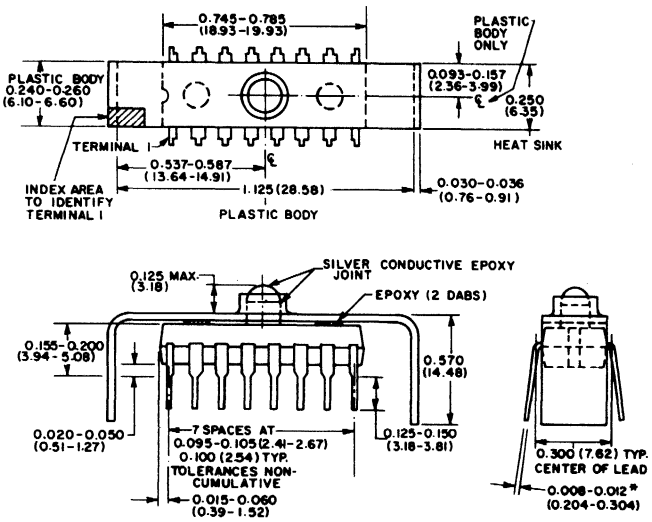
(Q) Suffix
Modified 16-Lead with Integral Bent Down Wing-Tab Heat Sink



Dimensional Outlines (Cont'd)

DUAL-IN-LINE and QUAD-IN-LINE PLASTIC PACKAGES
(Power Stud and Heat-Sink Types)

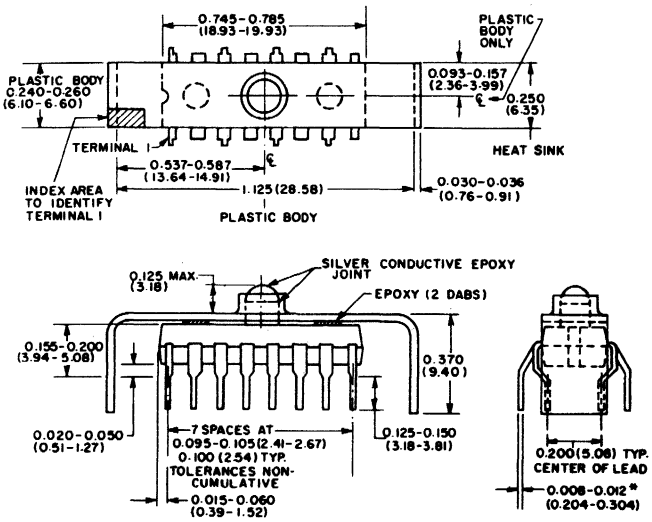
(EM) Suffix
16-Lead with Integral Strap Heat Sink



* WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAXIMUM LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013" (0.33 mm)

92CM-25649RI

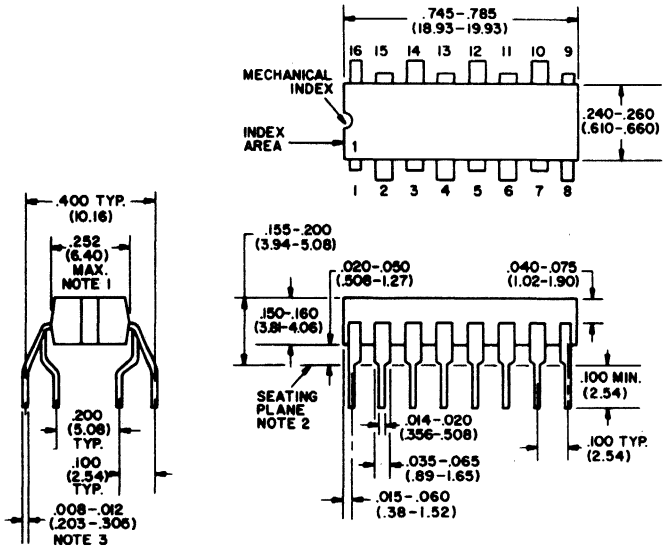
(QM) Suffix
16-Lead with Integral Strap Heat Sink



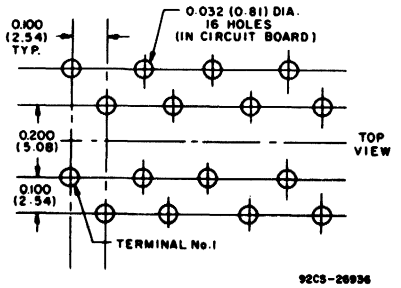
* WHEN THIS DEVICE IS SUPPLIED SOLDER-DIPPED, THE MAXIMUM LEAD THICKNESS (NARROW PORTION) WILL NOT EXCEED 0.013" (0.33 mm)

92CM-26671RI

(W) Suffix
16-Lead Staggered



Recommended Mounting – Hole Dimensions and Spacing



92CS-26936

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.
3. When this device is supplied solder dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).

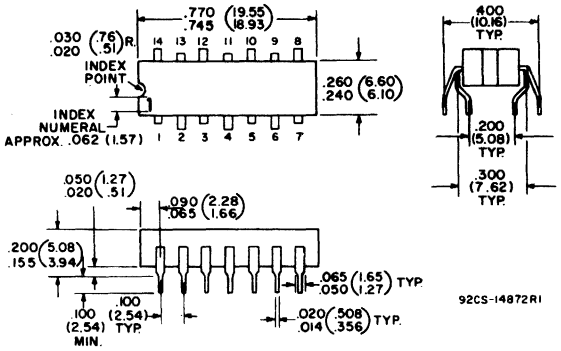
92CM-26937

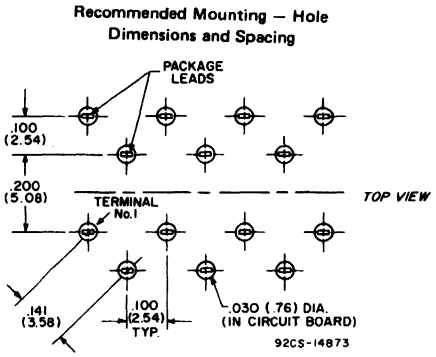
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

Dimensional Outlines (Cont'd)

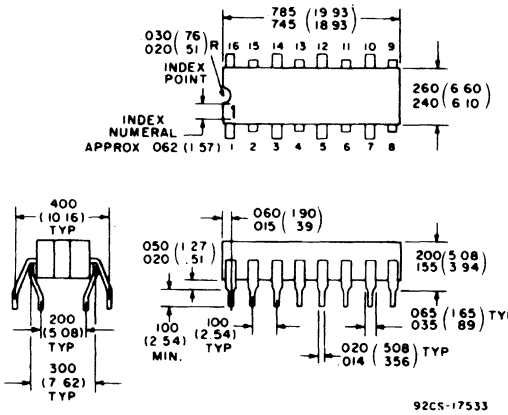
QUAD-IN-LINE PLASTIC PACKAGES

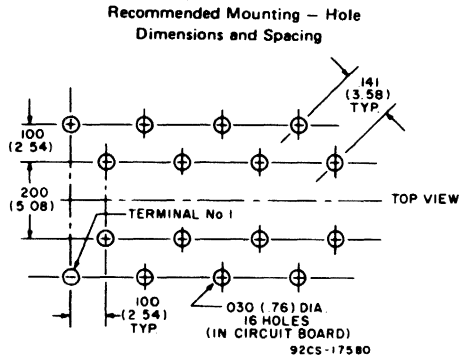
(Q) Suffix 14-Lead



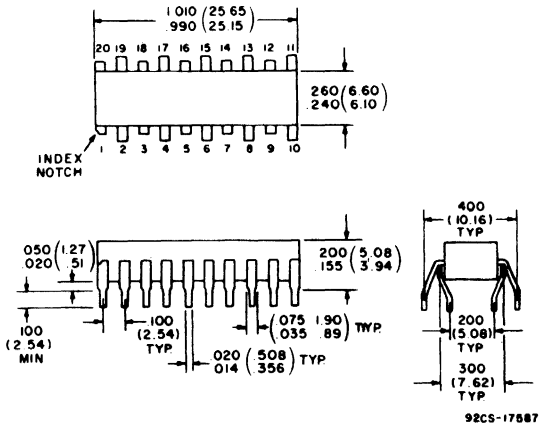


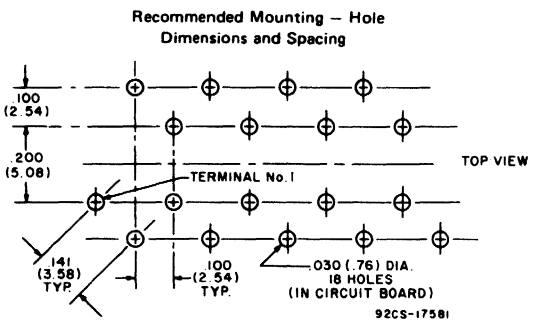
(Q) Suffix 16-Lead





(Q) Suffix 20-Lead





Application Note Abstracts

LINEAR INTEGRATED CIRCUITS

ICAN-4072 . . . . . 8 pages
Applications of the RCA-CA3048 Integrated-Circuit Amplifier Array

The RCA-CA3048 integrated circuit, an array of four identical amplifiers, each with independent inputs and outputs, all on a single monollthic silicon chip, has an operating and storage temperature range of −25°C to +85°C. Each amplifier in the low-noise array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The gain-frequency response, stability, output swing versus supply voltage, and noise of the device are discussed. Circuit applications include Hartley and Colpitts Oscillators, astable multivibrators, a 4-channel linear mixer, a driver for a 600-ohm balanced line, and a gain-controlled amplifier.

ICAN-5015 . . . . . 15 pages
Application of the RCA-CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

This Note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the CA3008 and CA3010 operational amplifiers. These amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from ±3 volts to ±6 volts). The power dissipation in the amplifiers ranges from 7.0 milliwatts to 92 milliwatts depending upon the supply-voltage level and the desired output-power level. The amplifiers are primarily intended to operate with externally applied negative feedback; however, they may also be operated successfully under open-loop conditions.

ICAN-5022 . . . . . 26 pages
Application of the RCA-CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

The CA3004, CA3005, and CA3006 rf amplifiers are discussed. These silicon-epitaxial monolithic integrated circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from −55°C to +125°C, and at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide wide- or narrow-band amplification, mixing, limiting, product detection, frequency generation, and generation of pulse or digital waveforms. The CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration. The CA3005 and CA3006 rf amplifiers are well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

ICAN-5030 . . . . . 11 pages
Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

This Note describes the RCA-CA3000 dc amplifier, a stabilized and compensated differential amplifier that has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils. The CA3000 can be used as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter, and can handle input signals up to about 80 millivolts rms before significant cross-modulation or intermodulation products are generated.

ICAN-5036 . . . . . 9 pages
Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

The RCA-CA3002 integrated-circuit if amplifier described in this Note is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits. It features all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from −55 to 125°C, and contains a built-in temperature-compensating network for stabilization of gain and dc operating points over this operating-temperature range.

ICAN-5037 . . . . . 4 pages
Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

This Application Note describes the RCA-CA3007 audio driver, a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from −55 to 125°C. Because of its circuit configuration (a balanced differential pair fed by a constant-current transistor), the CA3007 is an excellent controlled-gain audio driver for systems requiring audio squelching. This circuit is also usable as a servo driver.

ICAN-5038 . . . . . 8 pages
Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from −55 to 125°C, balanced differential-amplifier configuration with low-impedance double-ended input, and a built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from −55 to 125°C.

ICAN-5213 . . . . . 6 pages
Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

The integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from ±12-volt supplies as well as from ±6 volt or ±3 volt supplies. This Note describes the operating characteristics of the CA3015 and CA3016 at ±12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages: a 50-dB amplifier; a 10-dB, 42-MHz amplifier; a twin-T bandpass amplifier; a 20-dB, 10-MHz bandpass amplifier; and a voltage-follower.

ICAN-5269 . . . . . 7 pages
Integrated Circuits for FM Broadcast Receivers

This Note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

ICAN-5296 . . . . . 5 pages
Application of the RCA-CA3018 Integrated-Circuit Transistor Array

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers. Because the CA3018 has the feature of device balance, it is useful in special applications of the differential amplifier, and can be used to advantage in circuits that require temperature compensation of base-to-emitter voltage.

ICAN-5299 . . . . . 6 pages
Application of the RCA-CA3019 Integrated-Circuit Diode Array

The CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits. Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations. Consequently, the CA3019 is particularly useful in circuit configurations that require either a balanced diode bridge or identical diodes.

ICAN-5337 . . . . . 10 pages
Application of the RCA-CA3028A and CA-3028B Integrated-Circuit RD Amplifiers in the HF and VHF Ranges

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in rf amplifiers, autodyne converters, if amplifiers, and limiters. The CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers. The CA3028B, which features tight control of operating current, input offset voltage, and input bias and offset current, is recommended for those applications in which balance and operating conditions are important.

ICAN-5338 . . . . . 14 pages
Application of the RCA-CA3021, CA3022, and CA3023 Integrated-Circuit, Wideband Amplifiers

The CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM

Application Note Abstracts (Cont'd)

if stages in single-power-supply systems. Specifically, they can be used in video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired. Typical power dissipation with a 6-volt supply is 3 milliwatts for the CA3021, 12 milliwatts for the CA3022, and 36 milliwatts for the CA3023. Wider bandwidths can be achieved with the CA3023, intermediate bandwidths with the CA3022, and narrower bandwidths with the CA3021.

ICAN-5380 . . . . . 7 pages
Integrated - Circuit Frequency - Modulation if Amplifiers

The discussion in this Note shows that the simplest approach to the use of the CA3012 and CA3028 integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

ICAN-5641 . . . . . 8 pages
Application of RCA-CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers

The CA3033 and CA3033A high performance operational amplifiers are capable of delivering power outputs in excess of 250 milliwatts into a 500-ohm load resistance with harmonic distortion of less than 0.2 per cent and have a typical input impedance of one megohm with voltage gain of at least 90 dB. Offset voltage is less than 5 millivolts and offset current is typically 9 nanoamperes. Input bias current is typically 100 nanoamperes. These features make these amplifiers especially suitable for systems in which an operational amplifier and power amplifier or driver were formerly required. Specific applications discussed in this Note include astable multivibrator, linear staircase generator, comparator, monostable multivibrator, and the bistable multivibrator.

ICAN-5766 . . . . . 8 pages
Application of the RCA-CA3020 and CA3020A Integrated-Circuit Multipurpose Wideband Power Amplifiers

The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo-control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz. Applications covered include audio, wideband, and driver amplifiers.

ICAN-5831 . . . . . 5 pages
Application of the RCA-CA3044 and CA3044VI Integrated Circuits in Automatic-Fine-Tuning Systems

This Note describes the use of the CA3044 and CA3044VI integrated circuits as automatic fine-tuning (AFT) system components and discusses the advantages of integrated circuits in this application. The CA3044VI is electrically identical to the CA3044, but is supplied with formed leads for easier printed-circuit-board mounting. The construction and performance of a typical automatic-fine-tuning system for a color television system are examined.

ICAN-5841 . . . . . 4 pages
Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

ICAN-5977 . . . . . 11 pages
Principal Features and Applications of the RCA-CA3040 Integrated-Circuit Wideband Amplifier

This Note describes the operation of the CA3040, its electrical characteristics and ratings, and its primary application as a wideband amplifier. The CA3040 is a monolithic integrated circuit designed for use in wideband video and intermediate-frequency amplifier applications to frequencies as high as 100 MHz. The device, offered in a 12-pin TO-5 package, features a balanced differential voltage gain of 37 dB with less than 1 dB of imbalance and provides a typical 3-dB bandwidth of 55 MHz. Useful voltage gain is well beyond the 3-dB frequency roll-off point which, in some applications, extends to frequencies up to 200 MHz. Additional features of the CA3040 include temperature compensation for gain and voltage over the −55 to 125°C temperature range, a choice of zero or 180-degree phase shift from input to output terminals, and high input and low output impedance characteristics over a broad bandwidth.

ICAN-6022 . . . . . 4 pages
An IC for AM Radio Applications

The RCA-CA3088E is designed for use in high-quality AM superheterodyne receivers. It provides the basic functions of signal conversion, if amplification, detection, and audio preamplification sufficient to drive a separate power amplifier. Auxiliary functions supplied are: a supply-voltage regulator, internal agc for the first if amplifier, agc voltage for an optional external rf stage, and an amplified signal to drive a tuning-meter output. While the circuit design is intended for use in commercial AM broadcast receivers, it is equally suited for use in most AM receiver applications up to a frequency of 30 MHz. In addition, since most functions are externally accessible, this device is also a general-purpose amplifier array.

ICAN-6048 . . . . . 12 pages
Some Applications of A Programmable Power Switch/Amplifier

The CA3094 monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094 and illustrates its use in class A instrumentations and power amplifiers, a class A driver-amplifier for complementary power transistors, wide-frequency-range power multivibrators, current- or voltage-controlled oscillators, comparators (threshold detectors), voltage regulators, analog timers (long time delays), alarm systems, motor-speed controllers, thyristor-firing circuits, battery-charger regulator circuits, and ground-fault-interrupter circuits.

ICAN-6080 . . . . . 6 pages
Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC

COS/MOS integrated circuits have demonstrated outstanding performance in a wide variety of digital applications. Simplified circuitry, design flexibility, low power consumption, moderate speed, and the high noise immunity of these devices can complement the high transconductance of bipolar IC's in an extension to linear signal processing applications. This Note demonstrates the use of the CD4007A COS/MOS dual complementary pair plus inverter as the digital-to-analog (D/A) switch; the op-amp output stage for a digital-to-analog converter (DAC) uses COS/MOS and bipolar transistor-array IC's.

ICAN-6157 . . . . . 10 pages
Applications of the CA3085-Series Monolithic IC Voltage Regulators

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting. A circuit in which the CA3085 is used as a general-purpose amplifier is also shown. The RCA-CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100 milliamperes over the temperature range from −55° to +125°C.

ICAN-6182 . . . . . 28 pages
Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. These integrated-circuit switches operate from an ac input voltage of 24, 120, 208 to 230, or 277 volts at 50, 60, or 400 Hz. Zero-voltage switches (ZVS) trigger the thyristors at zero-voltage points in the supply-voltage cycle. Consequently, transient load-current surges and radio-frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches reduces the rate of change of on-state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These circuits have been used to provide transient-free temperature control in self-cleaning ovens, to control gun-muzzle temperature in low-temperature environments, to provide sequential switching of heating elements in warm-air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different ac power-control functions.

ICAN-6222 . . . . . 9 pages
Designing With an IC Transistor Array Containing Matched Super-Beta Transistors

The super-beta transistor array, CA3095, is discussed in terms of operation and typical applications. Super-beta transistors are similar to conventional bipolar transistors except that they have betas in the range of 1000 to 5000; the beta range of a conventional bipolar transistor ranges from 50 to 400. These applications include a high-input-resistance low-noise amplifier, a low-noise amplifier, a long-delay monostable multivibrator, a low-input-bias current comparator, an analog timer for long delay, various preamplifier applications, and a high-input-impedance dc-voltmeter circuit.

Application Note Abstracts (Cont'd)

ICAN-6259 . . . . . 9 pages
Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability while at the same time substantially reducing the number of external components and adjustments. As contrasted with prior state-of-the-art IC designs, sample-and-hold techniques are used in the phase detectors for the AFPC and the ACC-killer loops of the CA3162Q. The improved signal-to-dc unbalance attained thereby makes it possible to eliminate the adjustments conventionally used in those circuits. The only set-up adjustment is a trimmer capacitator to tune the crystal filter.

ICAN-6257 . . . . . 9 pages
Application of the CA3089E FM-IF Subsystem

The CA3089E is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC. This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

ICAN-6289 . . . . . 10 pages
Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator

The CA3090AQ integrated-circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment, which reduces to a minimum the manual effort during assembly; the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of the required external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art of stereo decoder designs.

ICAN-6294 . . . . . 11 pages
Features and Applications of RCA-CD2500E-Series MSI BCD-to-7-Segment Decoder-Drivers

The BCD-to-7-segment decoder-drivers, types CD2500E, CD2501E, CD2502E, and CD2503E, are medium-scale-integration (MSI) monolithic circuits designed to accept four inputs in BCD 8-4-2-1 code and provide decoded outputs that represent a decimal number from 0 to 9 on a 7-segment incandescent display device. The operating temperature range is from 0°C to +75°C. The CD2500E and CD2501E are 30-milliampere-per-line drivers intended for use with 7-segment incandescent display devices. The CD2502E and CD2503E are 80-milliampere-per-line drivers intended for use with high-current lamps and relays and may also be used for multiplex operation of RCA Numitrons. The CD2500E and CD2502E include a decimal-point driver, and the CD2501E and CD2503E have a special terminal that may be used for ripple blanking and/or intensity control. Applications discussed include a floating-decimal-point circuit and a typical multiplexing system.

ICAN-6302 . . . . . 9 pages
Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor

The CA3120E is a 16-pin, dual-in-line-monolithic-silicon integrated circuit that processes a video signal and provides the following outputs: non-inverted video output; noise-processed, inverted video output; dual-polarity, composite synchronization signals; and automatic gain-control signals (agc). The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimum TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

ICAN-6303 . . . . . 17 pages
A Single IC for the Complete PIX-IF-System in TV Receivers

The CA3068 linear integrated circuit is a PIX-IF-subsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-if-system for a TV receiver. This Note describes the receiver functions performed by the CA3068 and its application to color and monochrome TV receivers. A detailed description of circuit functions within the integrated circuit is given together with examples of the use of the CA3068 in PIX-IF amplifier PC-boards for color and monochrome TV.

ICAN-6538 . . . . . 6 pages
Applications of the RCA-CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits

The CA3062 is a monolithic silicon integrated circuit consisting of a photosensitive detector and a switching amplifier with a pair of high-current output transistors. This Note describes how the CA3062 with only 3 resistors outboarded can provide a light-activated switch that will drive a variety of practical loads such as solenoids, relays, triacs, SCR's, etc. "Normally ON" and "Normally OFF" outputs are available simultaneously.

ICAN-6668 . . . . . 16 pages
Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

The CA3080 and CA3080A operational amplifiers not only include the usual differential input terminals, but also an additional control terminal than enhances the device's flexibility. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. The amplifier's output-current is proportional to the voltage difference at its differential input terminals. This Note describes the operation of the OTA and features various circuits using the OTA; for example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micro-power comparators. In addition, circuits have been included to show the operation of the OTA in conjunction with COS/MOS devices as post-amplifiers.

ICAN-6724 . . . . . 8 pages
A Flexible Integrated-Circuit Color Demodulator for Color Television

This Note describes the circuit operation and application of the CA3067 in a color television receiver. The CA3067, which is supplied in a quad-in-line 16-lead plastic package, provides the following color-demodulator circuit functions: amplification, balanced chroma demodulation, dc-operated tint (phase) control, and zener-diode voltage regulation.

ICAN-6732 . . . . . 8 pages
Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

Burst or "popcorn" noise in LIC's exhibits itself as a random, abrupt change in the output voltage, the duration of which can last from 1/2 millisecond to several seconds. These noise voltages are not regular in their occurrence and can often be absent when measuring spot frequency noise. Thus it was necessary to evolve an entirely different measurement system to ensure the selection of a very-high-gain device that is free from "popcorn" noise. This Note discusses test configuration and conditions, pass-fail criteria, burst-noise test system circuits, and spurious noise sources and their suppression.

MOS FIELD-EFFECT DEVICES

AN-3193 . . . . . 9 pages
Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor

This Note describes applications and vhf circuit considerations for a high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

AN-3341 . . . . . 3 pages
VHF Mixer Design Using the RCA-3N128 MOS Transistor

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

AN-3452 . . . . . 7 pages
Chopper Circuits Using RCA MOS Field-Effect Transistors

Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but that eliminate their inherent offset-voltage and leakage-current problems.

AN-3453 . . . . . 6 pages
An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

AN-3535 . . . . . 6 pages
An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response, dynamic range, noise immunity, gain, and feed-through capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer. A conversion gain

Application Note Abstracts (Cont'd)

of 17.5 dB was obtained to provide an over-all tuner gain of approximately 30 dB. RF and mixer circuit considerations pertinent to the design are discussed.

AN-4018 . . . . . 5 pages
Design of Gate-Protected MOS Field-Effect Transistors

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential buildup across the gate insulation.

AN-4125 . . . . . 7 pages
MOS/FET Biasing Techniques

Field-effect transistors are applied in rf amplifiers and mixers, if and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits. The dual-gate MOS/FET appears to be particularly useful in rf stages because of low feedback capacitance, high transconductance, and superior cross modulation with automatic-gain-control capability. The rules for biasing FET's vary slightly depending on type. However, most possibilities are covered in this Note through examination of the biasing of a single-gate, a junction-gate, and a dual-gate transistor. Substrate biasing and biasing to compensate for temperature variations are also discussed.

AN-4431 . . . . . 7 pages
RF Applications of the Dual-Gate MOS/FET up to 500 MHz

The RCA dual-gate protected, metal-oxide silicon, field-effect transistor (MOS/FET) is especially useful for high-frequency applications in rf amplifier circuits. The dual-gate feature permits the design of simple agc circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS/FET in RF applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

AN-4590 . . . . . 16 pages
Using MOS/FET Integrated Circuits in Linear Circuit Applications

A brief review of MOS/FET IC device theory is given, and some linear circuit applications are surveyed. Theory discussed includes gate protection and electrical requirements. Applications include choppers, attenuators, constant-current sources, general-purpose amplifier circuits, and rf amplifiers, oscillators, and mixers.

COS/MOS DIGITAL INTEGRATED CIRCUITS

ICAN-6000 . . . . . 6 pages
Handling and Operating Considerations for MOS Integrated Circuits

Manual and automated methods for handling, mounting, and storing unmounted chips and packaged devices and for handling and storing devices mounted on boards are discussed. Operating voltage conditions, interfacing, protection circuits, and electrical failure modes to be avoided are also presented.

ICAN-6080 . . . . . 6 pages
Digital-to-Analog Conversion Using the RCA-CD-4007A COS/MOS IC

The use of the RCA-CD4007A COS/MOS dual complementary pair plus inverter as a digital-to-analog (D/A) switch is demonstrated. The op-amp output stage for the digital-to-analog converter (DAC) uses COS/MOS and bipolar transistor-array IC's. Resistance networks for DAC's, the design of a voltage-follower amplifier for single supply operation, and a 9-bit COS/MOS DAC are described.

ICAN-6086 . . . . . 12 pages
Timekeeping Advances Through COS/MOS Technology

Most COS/MOS timing circuits consist of an oscillator, some digital processing logic, and logic-circuit drivers. This Note discusses oscillator design (including crystal characteristics and feedback circuit and oscillator-amplifier configurations), practical COS/MOS oscillator circuits, frequency dividers, and COS/MOS timing-circuit applications in wristwatches, wall clocks, and automobile clocks.

ICAN-6101 . . . . . 8 pages
The RCA COS/MOS Phase-Locked-Loop — A Versatile Building Block for Micro-Power Digital and Analog Applications

The phase-locked-loop described in this Note is the COS/MOS CD4046A, which consumes only 600 microwatts of power at 10 kHz, a power consumption 160 times *less* than the 100 milliwatts required by similar monolithic bipolar PLL's. The Note discusses the fundamentals of phase-locked-loops and presents a detailed technical description of the COS/MOS PLL as well as its application in FM demodulators, frequency synthesizers, split-phase data synchronization and decoding, and phase-locked-loop lock detection.

ICAN-6166 . . . . . 16 pages
COS/MOS MSI Counter and Register Design and Applications

Logic and schematic diagrams for counter and register types CD4006A, CD4014A, CD4015A, CD4018A, CD4020A, CD4021A, CD4022A, and CD4024A are presented; circuit designs are outlined and device-design trade-off's are discussed. Performance criteria are summarized and applications by type are outlined by means of logic or subsystems diagrams and waveforms photographs.

ICAN-6176 . . . . . 8 pages
Noise Immunity of COS/MOS Integrated-Circuit Logic Gates

The types of noise usually encountered in a logic system are discussed and the noise immunity of a COS/MOS integrated-circuit logic-gate test circuit in relation to system variables is evaluated. The evaluation is performed on a circuit that includes a CD4000A dual 3-input gate plus inverter and a CD4001A quad 2-input gate connected in cascade to drive a CD4013A flip-flop. Measurement of the voltage required at various gate leads to switch the flip-flop defines the noise immunity threshold of the gate circuits.

ICAN-6210 . . . . . 11 pages
A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts

This Note is developed in terms of a typical system for process controls. The flexibility of system design and common data-bus architecture made possible by the three-state outputs and bidirectional input/outputs incorporated in many COS/MOS circuits are stressed, as is the ease of system design for data handling in increments of 4 bits made possible by the CD4000A family. The implementation of the system is shown in terms of the COS/MOS standard parts that can be used to perform the desired system functions. Attention is focused on the multiplicity of applications and the scope of information processing that can be covered by standard parts.

ICAN-6218 . . . . . 2 pages
Gate Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits

A protection circuit developed by RCA to reduce the problem of gate-oxide failure in COS/MOS integrated circuits is presented. The circuit has been shown to be effective in minimizing occurrences of gate-oxide failure and, when used in conjunction with the handling guidance contained in ICAN-6000, "Handling Considerations for MOS Integrated Circuits," in eliminating the problem entirely.

ICAN-6224 . . . . . 2 pages
Radiation Resistance of the COS/MOS CD4000A Series

Two types of radiation resistance, permanent and temporary, are discussed, and the radiation resistance of CD4000 and CD4000A series devices are compared. The use of shielding to increase resistance is examined.

ICAN-6230 . . . . . 13 pages
Using the CD4047A in COS/MOS Timing Applications

This Note compares the theoretical and actual performance of oscillator circuits with that of the CD4047A. The device functions as either an oscillator or one-shot and meets the power dissipation, stability, and speed requirements of most COS/MOS systems. Applications discussed include a noise discriminator, a frequency discriminator, a low-pass filter, a band-pass filter, an envelope detector and a pulse generator. Four appendixes amplify test material.

ICAN-6267 . . . . . 8 pages
Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits

This Note describes several techniques that may be used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. The circuits shown can be formed by use of COS/MOS inverters and NAND or NOR gates connected in an inverter configuration. The Note also describes various applications for COS/MOS multivibrator circuits (e.g.: voltage-controlled oscillators, voltage-controlled pulse-width circuits, phase-locked voltage-controlled oscillators, frequency multipliers, and modulator/demodulators (envelope detectors). Specific data relate to use of "A" series gates.

ICAN-6289 . . . . . 12 pages
A COS/MOS PCM Telemetry and Remote Data Acquisition Design

Descriptive background material on telemetry systems is given along with systems for both immediate and remote data conversion and transmission. Parts from the CD4000 family are used to show how various sections of the system may be realized in the general case. The exact configuration of any specific system will, of course, depend on the unique requirements of the application.

ICAN-6304 . . . . . 5 pages
Power Supplies for COS/MOS

Examples of various COS/MOS power-supply circuits and their relative costs are given along with factors important in their design. Design examples include low-frequency systems, mixed systems of 2-MHz and 50-kHz circuits, a COS/MOS system powered by a 5-volt TTL supply, and battery-powered systems. Design considerations discussed include operating frequency, noise immunity, power dissipation, and regulation.

Application Note Abstracts (Cont'd)

ICAN-6315 . . . . . 7 pages
COS/MOS Interfacing Simplified
Examples of practical circuits for a wide variety of interfacing situations are given in this Note; design constraints are included in each case. Interfaces discussed are COS/MOS to: TTL, HNIL, DTL, 10k ECL, NMOS, PMOS, industrial power-control circuits, op-amps, and LCD, LED, and gas-discharge displays.

ICAN-6346 . . . . . 6 pages
Application of the RCA-CD4093B COS/MOS Schmitt Trigger
This Note describes the characteristics and some typical applications of the CD4093B COS/MOS quad two-input NAND Schmitt Trigger. The CD4093B may be used in all applications in which the logical NAND function is required and, in addition, in a whole range of timing, waveshaping, and interfacing applications in which Schmitt Trigger action on the inputs is used.

ICAN-6362 . . . . . 10 pages
Using the CD4520B to Design Dividers with Symmetrical Outputs
The general-purpose COS/MOS dual up-counter, the CD4520B, a counter that may be used in various counting and dividing applications is discussed. Dividers of the form $N=2^i \pm 1$ and $N=2^i \pm 1$ and described. Applications of symmetrical dividers are also discussed.

ICAN-6374 . . . . . 8 pages
The COS/MOS CD4059A Programmable Divide-by-N Counter in FM and Citizens-Band-Transceiver Tuners
The frequency synthesis capability of the CD4059A programmable divide-by-N counter is demonstrated in applications in an FM digital tuner and in the digital tuner for a citizens-band tranceiver. The digital approach described in the paper allows desired frequencies to be selected by depressing numbered buttons on a keyboard. By using the appropriate basic circuitry along with a phase-locked-loop circuit, the local oscillator of the receiver is adjusted and locked to the proper frequency, thus assuring proper station selection. Alternate methods of station selection that enhance the flexibility of the system are described.

ICAN-6498 . . . . . 6 pages
Design of Fixed and Programmable Counters Using the RCA CD4018A COS/MOS Presettable Divide-by-N Counter
The use of the CD4018A single-decade and multidecade fixed and programmable divide-by-N counters are described. System considerations such as switch simplifications, components minimization, and speed are also discussed.

ICAN-6576 . . . . . 6 pages
Power-Supply Considerations for COS/MOS Devices
This Note describes those features of COS/MOS devices that permit them to operate from a wide range of power sources. The Note also provides the system designer with the information he needs to design an economical power supply for his COS/MOS system. Features discussed are quiescent device dissipation, switching characteristics, and ac dissipation and performance characteristics. The calculation of system power, regulation and filtering requirements, and high-dc sources are also discussed along with a battery standby system.

ICAN-6600 . . . . . 6 pages
Arithmetic Arrays Using Standard COS/MOS Building Blocks
The design of a COS/MOS arithmetic unit capable of adding, subtracting, multiplying, and dividing is described. The device is also able to perform the logical functions of OR, AND and the Exclusive OR of two 4-bit words. Three 4-bit registers are provided that permit either of two words to perform a desired operation with a third word. The system is configured with standard, commercially available COS/MOS devices, which include registers, AND-OR select gates, a full adder, and NOR and NAND gates.

ICAN-6601 . . . . . 12 pages
Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch
The CD4016A quad bilateral switch is the ideal semiconductor switch for use in switching applications; it can be used for the transmission of analog or digital signals with low distortion. The Note discusses features of the device; operation of the COS/MOS switch; switch and logic applications, including switch and logic functions; multiplexing/demultiplexing; digital control of signal gain, frequency, and impedance, including resistor networks, and variable frequency control; digital-to-analog conversion, including weighted resistor networks for the D/A converter, and an R-2R resistor ladder D/A converter; sample-and-hold applications; and squelch control (level detection).

ICAN-6602 . . . . . 12 pages
Interfacing COS/MOS with Other Logic Families
The RCA CD4000A COS/MOS series circuits operate from power-supplies of 3 to 15 volts. Thus, they can drive and be driven by a number of logic families, including all DTL and TTL families, within certain conditions and limitations. This Note describes the conditions of interface.

ICAN-6716 . . . . . 15 pages
Low-Power Digital Frequency Synthesizers Utilizing COS/MOS IC's
A digital frequency synthesizer that employs a digital phase-locked loop and other COS/MOS circuits is described. Following a reveiw of phase-locked-loop fundamentals, the use of COS/MOS devices in FM receiver systhesizers is discussed.

ICAN-6733 . . . . . 16 pages
Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decode Counters — 7 Segment Output Types
This Note describes the CD4033A and CD4026A and their use with various 7-segment display units presently available. Interface packages and methods are discussed to help the the designer select the best system to meet his demands. Also included are battery-operated systems for digital clocks and watches.

ICAN-6739 . . . . . 12 pages
COS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions
COS/MOS rate multipliers, the CD4527B and CD4089B, can be used as building blocks to generate a range of digital functions in low-power systems where minimum package count is desirable. The circuits may be employed in numerical control, instrumentation, digital filtering, and frequency synthesis. When used with an up/down counter and control logic, they can be used to perform such operations as multiplication, addition, subtraction, generation of algebraic equations and differential equations, integration, and to raise numbers to various powers. Symmetric rate multiplication, the problem of eliminating round-off error in a direct frequency-synthesis application in a common-carrier multiplex system is also covered.

MEMORY INTEGRATED CIRCUITS

ICAN-6401 . . . . . 5 pages
Applications Information for the RCA MW-7001ID RAM
The RCA MW 7001 ID, a 1024-word by 1-bit n-channel random-access memory uses an internal charge-pump refresh mechanism to automatically refresh all memory cells. The charge-pump mechanism eliminates the need for the periodic refresh cycles normally required in dynamic access memories. It also allows the MW 7001 ID to operate as a static memory while retaining the low power dissipation and high speed characteristics of dynamic memories. The MW 7001 ID requires TTL logic levels at all inputs except chip select. The latching circuitry in the input address lines allows address input signals to be removed after 40 nanoseconds, measured from the 1.5-volt point of the rising edge of the chip-select pulse. This Note discusses input loading of the device, recommended interface circuits, and the operation of the internal charge-pump.

ICAN-6445 . . . . . 8 pages
Memory-System Characteristics and Applications of the CD4061A
The CD4061A 256-word by 1-bit RAM is a versatile building block in medium-scale memory systems. This Note describes circuit and system applications concepts of the device and includes design, timing, performance and testing details for a practical memory-system.

MICROPROCESSOR INTEGRATED CIRCUITS

ICAN-6416 . . . . . 8 pages
An Introduction to Microprocessors and the RCA COSMAC COS/MOS Microprocessor
A microprocessor, in addition to performing arithmetic and logical functions, can address memory, input, output, and store data, and make program branch decisions. This Note is an introduction to the fundamentals of microprocessors and to the specific capabilities of the RCA COSMAC microprocessor.

Index to Devices

Index to Devices

This index does not include package designation suffix letters for individual type numbers; the various packages available are shown in the data section. However, notations are included to show the availability of chip versions (■) and beam-lead versions (◆); detailed information on these versions is available in the following publications:

Beam-Lead Linear ICs: Data Bulletin File No. 515
Linear IC Chips: Data Bulletin File No. 516
Other Chip Versions: Individual Data Bulletins

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